Description (continued)

The device is available in a 32-lead QFN (package ET), with an exposed thermal pad. It is lead (Pb) free with 100% matte tin leadframe plating.

Applications include the following:

- Display backlighting
- Monocolor, multicolor, or full-color LED display
- Monocolor, multicolor, LED Signboard
- Multicolor LED lighting

Selection Guide

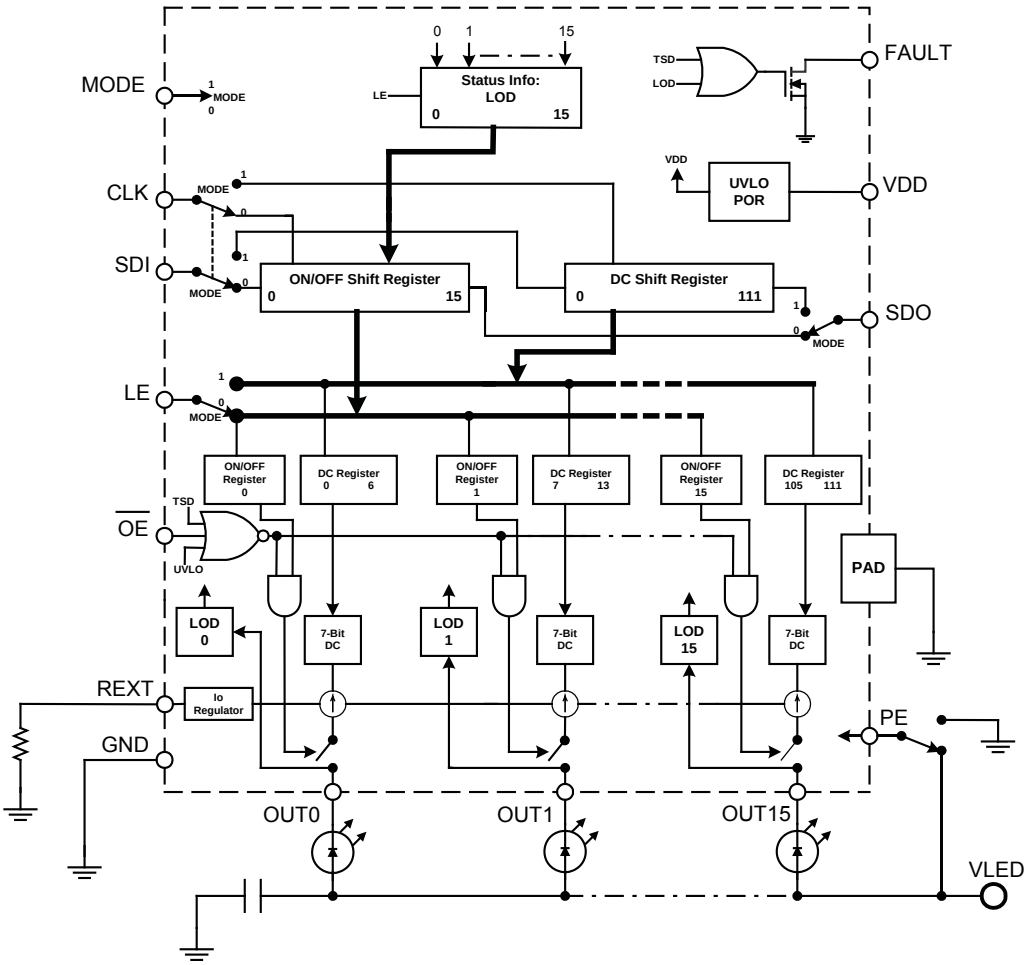
Part Number	Package	Packing (estimated)
A6285EETTR-T	5×5 mm QFN, 32 pin, exposed thermal pad	1500 pieces per 7-in reel

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Min.	Max.	Unit
Supply Voltage*	V_{DD}		–0.3	5.5	V
OUTx Current (any single output)	I_O		–	90	mA
Input Voltage Range*	V_I	V_{OE}, V_{LE}, V_{CLK}, V_{SDI}, V_{MODE}	–0.3	V_{DD} + 0.3	V
LED Load Supply Range*	V_{LED}		–0.3	13.2	V
ESD Rating		HBM (JEDEC JESD22-A114, Human Body Model)	–	1.5	kV
		CDM (JEDEC JESD22-C101, Charged Device Model)	–	1.0	kV
Operating Temperature Range (E)	T_A		–40	85	°C
Junction Temperature	T_J(max)		–	150	°C
Storage Temperature Range	T_{stg}		–55	150	°C

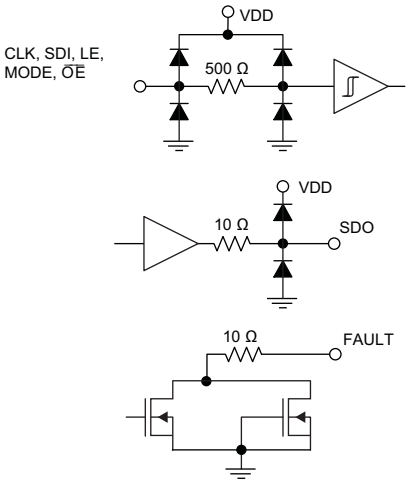
*With respect to ground (GND, PGND).

Functional Block Diagram



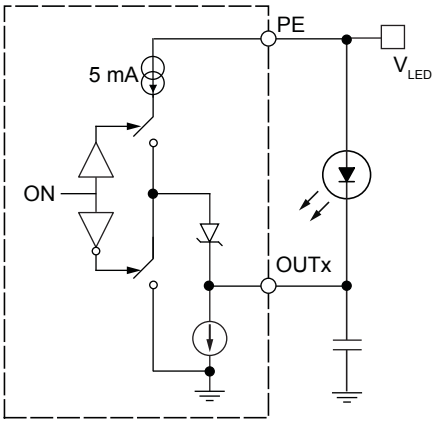
Inputs and Outputs Equivalent Circuits

(Note: Resistor values are equivalent resistance and not tested.)

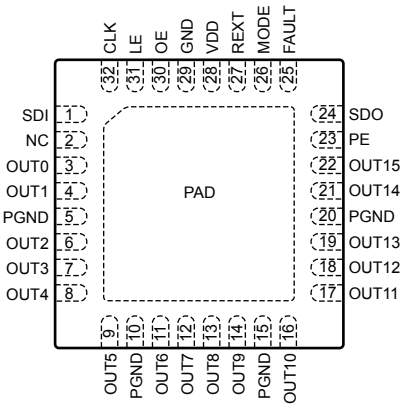


Active Pull-up Cell

(1 of 16 Outputs)



Pin-out Diagram



Terminal List Table

Name	Number	Description
$\overline{OE}$	30	Output Enable input. Active low. When $\overline{OE}$ = High, all OUTx outputs are forced OFF. When $\overline{OE}$ = Low, ON/OFF of OUTx outputs are controlled by input data.
GND	29	Logic supply ground.
PE	23	Active Pull-up Enable. When connected to LED Load Supply (V_{LED}) = enabled, when connected to PGND = disabled.
REXT	27	Reference current input/output terminal.
MODE	26	Logic input, Mode select. When MODE = Low, then SDI, SDO, CLK, LE are connected to ON/OFF control logic. When MODE = High, SDI, SDO, CLK, LE are connected to dot-correction logic.
NC	2	No connection. Not internally connected.
OUT0	3	Constant current outputs.
OUT1	4	
OUT2	6	
OUT3	7	
OUT4	8	
OUT5	9	
OUT6	11	
OUT7	12	
OUT8	13	
OUT9	14	
OUT10	16	
OUT11	17	
OUT12	18	
OUT13	19	
OUT14	21	
OUT15	22	
PGND	5, 10, 15, 20	Power ground.
CLK	32	Data shift clock input. Note that the internal connections are switched by input at MODE pin. At CLK↑, the shift-registers selected by MODE shift the data.
SDI	1	Serial Data In. Data input of serial data interface.
SDO	24	Serial Data Out. Data output of serial data interface.
VDD	28	Logic Supply.
FAULT	25	Error output. FAULT is open drain terminal. FAULT goes low when LOD or TSD detected.
LE	31	Latch Enable input. Note that the internal connections are switched by input at the MODE pin. At LE↑, the latches selected by MODE get new data.
PAD	–	Exposed pad for enhanced thermal dissipation; not connected internally, connect to power ground plane.

Operating Characteristics

ELECTRICAL CHARACTERISTICS at T_A[1] = 25°C, V_{DD} = 3.0 to 5.5 V, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
Logic Supply Voltage Range	V_{DD}	Operating	3.0	5.0	5.5	V
LED Load Supply Output Voltage	V_{LED}	Operating	–	–	12.0	V
Undervoltage Lockout	$V_{DD(UV)}$	V_{DD} 0 → 5.0 V	2.5	2.7	2.95	V
		V_{DD} 5 → 0.0 V	2.3	2.5	2.75	V
Output Current	I_O	V_{DS} = 1 V, R_{EXT} = 600 Ω	70	80	90	mA
		V_{DS} = 1 V, R_{EXT} = 1.2 kΩ	35	40	45	mA
Output to Output Matching Error[4]	Err	1 V = $V_{DS(x)}$, R_{EXT} = 600 Ω; All outputs on	–	±1.0	±4.4	%
		1 V = $V_{DS(x)}$, R_{EXT} = 1.2 kΩ; All outputs on	–	±1.0	±4.4	%
Load Regulation	ΔI_{Oreg}	$V_{DS(X)}$ = 1 to 3 V, R_{EXT} = 600 Ω; All outputs on	–	–	±6.0	%
Output Leakage Current	I_{DSS}	V_{OH} = 12 V	–	–	0.5	µA
Logic Input Voltage	V_{IH}		0.8×V_{DD}	–	V_{DD}	V
	V_{IL}		GND	–	0.2×V_{DD}	V
Logic Input Voltage Hysteresis	V_{Ihys}	All digital inputs	250	–	900	mV
Logic Input Current	I_I	All digital inputs	–1	–	1	µA
SDO Voltage	V_{OL}	I_{OL} = 1 mA	–	–	0.5	V
	V_{OH}	I_{OH} = –1 mA	V_{DD}–0.5	–	–	V
Supply Current[3]	$I_{DD(OFF)}$	R_{EXT} = 9.6 kΩ, V_{OE} = 5 V	–	–	6	mA
		R_{EXT} = 1.2 kΩ, V_{OE} = 5 V	–	–	17	mA
	$I_{DD(ON)}$	All outputs on, R_{EXT} = 1.2 kΩ, V_O = 1 V, data transfer 30 MHz	–	–	25	mA
		All outputs on, R_{EXT} = 600 Ω, V_O = 1 V, data transfer 30 MHz	–	26	40	mA
FAULT Output	$V_{OUT(0)}$	I_{OUT} = 5 mA; faults asserted	–	–	0.4	V
	$I_{OUT(1)}$	V_{OUT} = 5.5 V, open drain; faults negated	–	–	1	µA
Active Pull-up	$I_{OUT(0)}$	V_{LED} = 1 V, all outputs off	–	2.8	–	mA
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	$T_{JTSDhys}$		–	15	–	°C
Open LED Detection Threshold	V_{LOD}		–	0.30	0.40	V
Reference Voltage at R_{EXT}	V_{EXT}	R_{EXT} = 600 Ω	1.19	1.23	1.28	V

[1]Tested at 25°C. Specifications are assured by design and characterization over the operating temperature range of –40°C to 85°C.
[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
[3]Recommended operating range: V_O = 1.0 to 3.0 V.
[4]Err = (I_O(min or max) – I_O(av)) / I_O(av).

SWITCHING CHARACTERISTICS at T_A[1] = 25°C, V_{DD} = V_{IH} = 3.0 to 5.5 V, V_{DS} = 1 V, V_{IL} = 0 V, R_{EXT} = 1.2 kΩ, I_O = 40 mA, V_L = 3 V, R_L = 51 Ω, C_L = 15 pF (see table 9)

Characteristic	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Unit
Clock Frequency	f_{CLK}	CLK	–	–	30	MHz
Clock Pulse Duration	t_{wh0}/t_{wl0}	CLK = High/Low	16	–	–	ns
Clock Frequency (cascaded)	f_{CLKC}	CLK	–	–	25	MHz
LE Pulse Duration	t_{wh1}	LE = High	20	–	–	ns
Setup Time	t_{su0}	SDI to CLK↑	10	–	–	ns
	t_{su1}	CLK↑ to LE↑	10	–	–	ns
	t_{su2}	MODE↑↓ to CLK↑	10	–	–	ns
	t_{su3}	MODE↑↓ to LE↑	10	–	–	ns
Hold Time	t_{h0}	CLK↑ to SDI	10	–	–	ns
	t_{h1}	LE↓ to CLK↑	10	–	–	ns
	t_{h2}	CLK↑ to MODE↑↓	10	–	–	ns
	t_{h3}	LE↓ to MODE↑↓	10	–	–	ns
Rise Time	t_{r0}	SDO, 10/90% points (see figure 1)	–	–	16	ns
	t_{r1}	OUTx, V_{DD} = 5 V, DC = 127, 10/90% points (see figure 2)	–	10	30	ns
Fall Time	t_{f0}	SDO, 10/90% points (see figure 1)	–	–	16	ns
	t_{f1}	OUTx, V_{DD} = 5 V, DC = 127, 10/90% points (see figure 2)	–	10	30	ns
Propagation Delay Time	t_{pd0}	CLK↑ to SDO↑↓ (see figure 1)	–	–	30	ns
	t_{pd1}	MODE↑↓ to SDO↑↓ (see figure 1)	–	–	30	ns
	t_{pd2}	$\overline{OE}$↓ to OUT0↑↓ (see figure 2)	–	–	60	ns
	t_{pd3}	LE↑ to OUT0↑↓ (see figure 2)	–	–	60	ns
	t_{pd4}	OUTx↑↓ to FAULT↑↓ (see figures 2 and 3)	–	–	1000	ns
	t_{pd5}	LE↑ to I_{OUT} (DC) (see figure 2)	–	–	200	ns
LOD Sample and Read Time	t_{LOD}	LE_1↑ to LE_2↑	1660	–	–	ns
Output Delay Time	t_d	OUTx↑↓ to OUT(x+1)↑↓ (see figure 2)	10	20	40	ns

[1]Tested at 25°C. Specifications are assured by design and characterization over the operating temperature range of –40°C to 85°C.
[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits d maximum and minimum limits.

Parameter Measurement Information

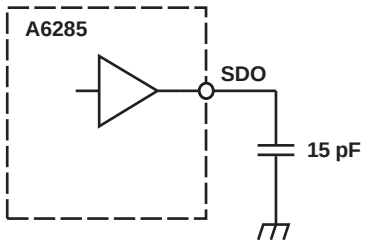


Figure 1. Test circuit for t_{r0}, t_{f0}, t_{d0}, and t_{d1}

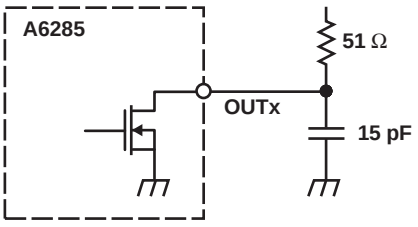


Figure 2. Test circuit for t_{r1}, t_{f1}, t_{pd2}, t_{pd3}, t_{pd5}, and t_{pd6}

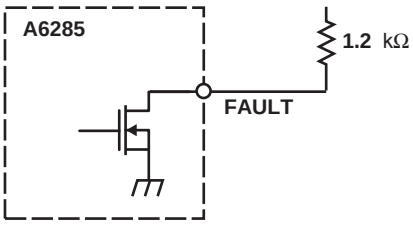


Figure 3. Test circuit for t_{pd4}

Operating Characteristics

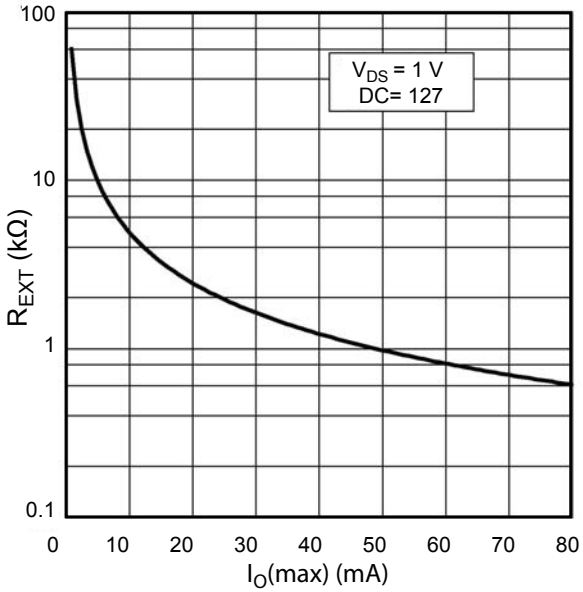


Figure 4. Value of external reference resistor, REXT, versus channel Constant Output Current

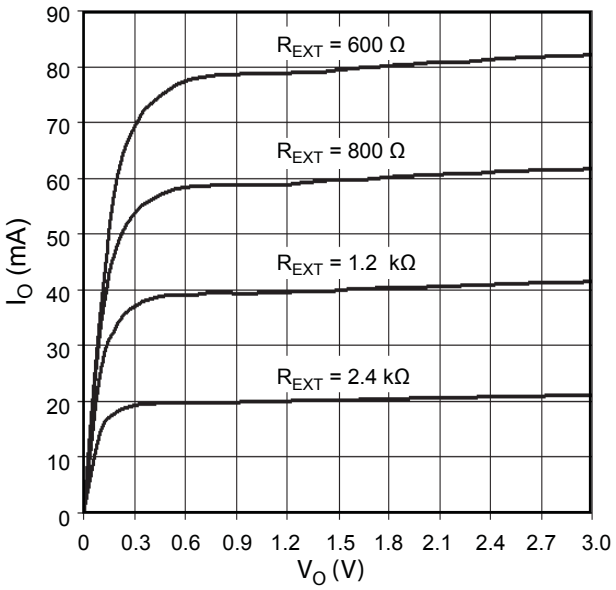


Figure 5. Output Voltage versus Output Current at various levels of R_{EXT}

Thermal Characteristics

Characteristic	Symbol	Test Conditions[1]	Value[2]	Units
Package Power Dissipation	P_D	Continuous, T_A = 25°C	3.9	W
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	32	°C/W

[1]Additional thermal information available on Allegro website.
[2]Actual performance significantly affected by application.

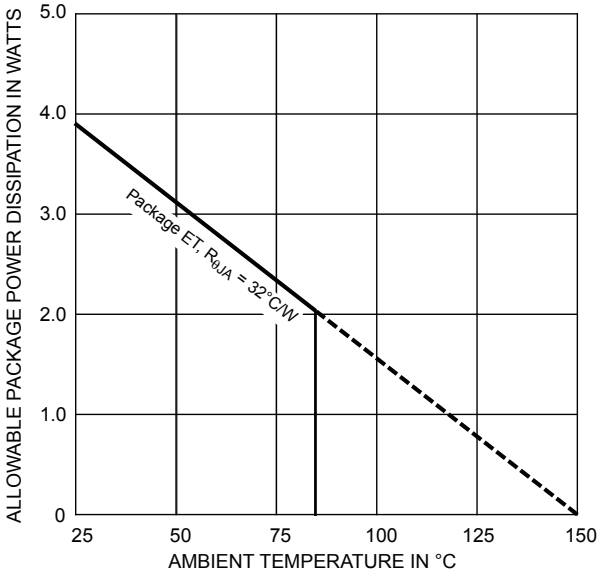


Figure 6. Power Dissipation versus temperature

Functional Description

Setting Maximum Channel Current The maximum output current per channel is set by a single external resistor, REXT, which is placed between the REXT pin and PGND. The voltage on REXT, V_{EXT}, is set by an internal band gap. The maximum channel current is equivalent to the current flowing through REXT multiplied by 38.4. The maximum channel output current can be calculated as:

$$I_O(\text{max}) = \frac{V_{EXT}}{R_{EXT}} \times 38.4 \quad , \qquad (1)$$

where:

V_{EXT} is 1.25 V typical, and

R_{EXT} is the value of the user-selected external resistor, which should not be less than 600 Ω, corresponding to 80 mA.

Figure 4 shows the maximum per channel constant output current, I_O(max), of OUT0 to OUT15, versus R_{EXT}, the value of the resistor between REXT terminal and ground.

Dot Correction The A6285 can independently fine-adjust the current of each output channel, a feature referred to as *dot correction*. This feature is used to compensate for the brightness deviations of the LEDs connected to the output channels, OUT0 through OUT15.

Each of the 16 channels can be programmed with a 7-bit word. The channel output can be adjusted in 128 steps from 0% to 100% of the maximum programmable per channel output current, I_O(max). Equation 2 determines the output current for each OUT*x*:

$$I_{Ox} = \frac{I_O(\text{max}) \times DC_x}{127} \quad , \qquad (2)$$

where DC_x is the programmed dot-correction value (0, 1, …127) for each output channel.

Dot correction data is entered for all channels at the same time. The complete dot correction data format consists of sixteen 7-bit words, which form a 112-bit (16 × 7) wide serial data packet. The data for each channel is sent in a continuous sequence, and all data is clocked in with the MSB first, as shown in figure 7.

To input data into the Dot Correction register, LE should be set low, and MODE must be set high. MODE sets the input shift register to 112-bit width. After all serial data is clocked in, a rising edge on the LE terminal latches the data into the Dot Correction register. The timing sequence is shown in figure 9.

All Channel Output Enable-Disable All OUT*x* channels of the A6285 can switched off using the $\overline{OE}$ pin. When $\overline{OE}$ is set high, all OUT*x* outputs are disabled, regardless of the on/off status of any OUT*x*. When $\overline{OE}$ is set to low, the on/off status of each OUT*x* is determined by the state of the latches in the On/Off register. $\overline{OE}$ can be PWMed to control the average current, which controls the LED brightness of all outputs, in addition to the DC function.

Individual Channel Output Enable-Disable Each OUT*x* channel can be switched on or off independently. Each of the channels can be programmed with a 1-bit word.

On/off data is entered for all channels at the same time. The complete on/off data format consists of sixteen 1-bit words, which form a 16-bit wide serial data packet. The data for each channel is sent in a continuous sequence, and all data is clocked in with the MSB first, as shown in figure 8.

To input data into the On/Off register, LE must be set low, and MODE must be set low. LE allows on/off data to enter the input shift register, and MODE sets the input shift register to 16-bit width. After all serial data is clocked in, a rising edge on the LE terminal latches the data into the On/Off register and moves the LOD data at the Open Circuit Detector into the input shift register. The timing sequence is shown in figure 9.

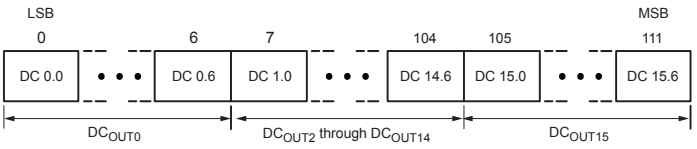


Figure 7. Dot Correction (DC) data format

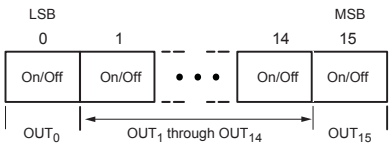


Figure 8. Individual output on-off data format

Delay Between Outputs The A6285 has graduated delay circuits between outputs. The fixed delay time is 20 ns (typical). OUT0 has no delay, OUT1 has a 20 ns delay, OUT2 has a 40 ns delay, and so forth. This delay prevents large in-rush currents that create ground bounce, which reduces power supply bypass capacitor requirements when the outputs turn on. The delays work during switch on and switch off of each output channel.

Serial Interface Data Transfer Rate The A6285 includes a flexible serial data interface, which can be connected to a microcontroller or a digital signal processor. Only 3 pins are required to input data into the device. The rising edge of a CLK signal shifts the data from SDI pin to the input shift register. After all data is clocked in, a rising edge of LE latches the serial data to the On/Off register. All data is clocked in with the MSB first, while LE is set low.

Multiple A6285 devices can be cascaded by connecting the SDO- pin of one device with the SDI pin of the following device. The SDO pin can also be connected to the microcontroller or micro-processor in order to transmit LOD information from the A6285.

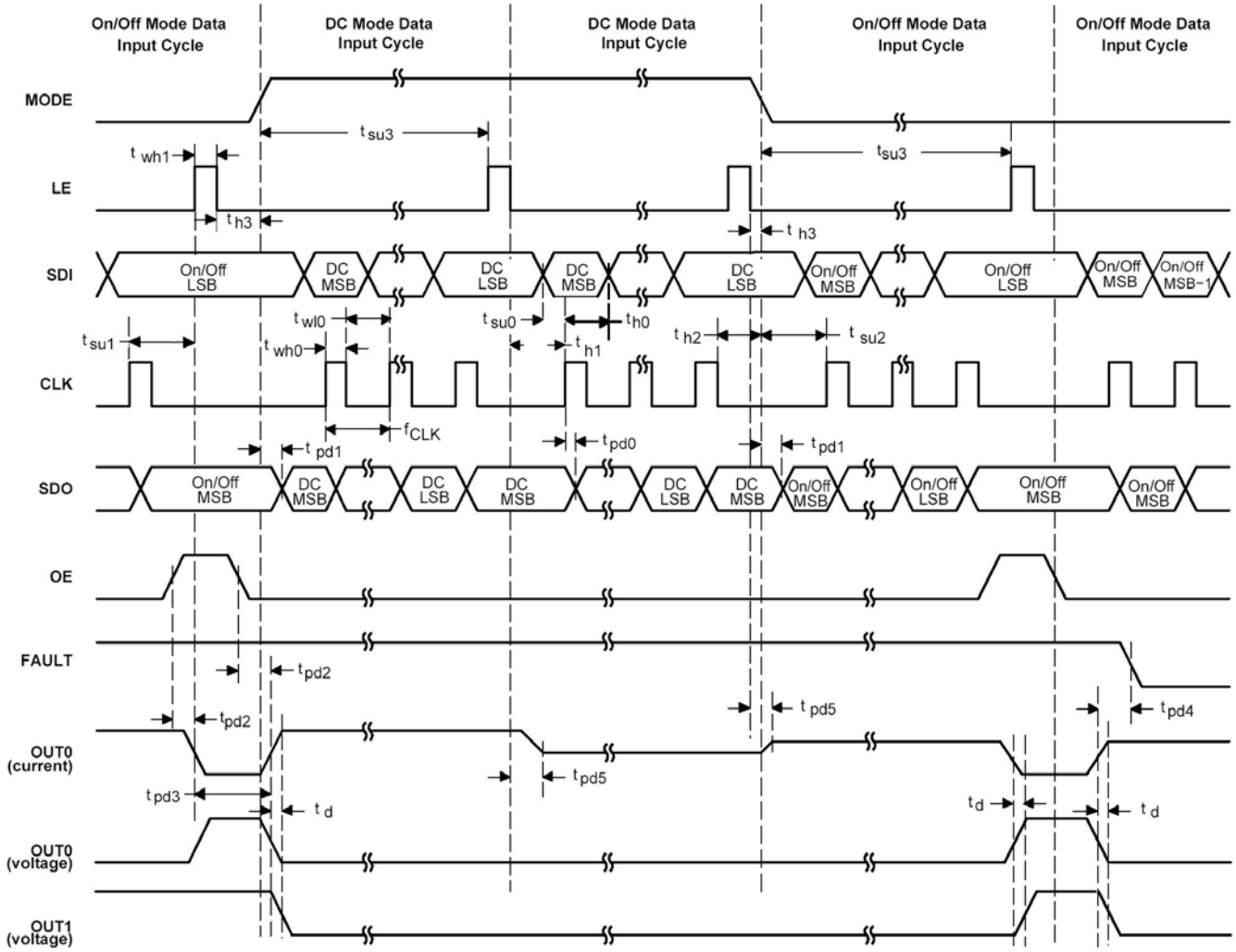


Figure 9. Output on-off and Dot Correction timing

Figure 10 shows an example application with *n* cascaded A6285 devices connected to a controller. The maximum number of cascaded devices depends on the application system and the data transfer rate. The minimum data input transfer rate is calculated as follows:

$$f_{CLK} = 112 \times f_{UPDATE} \times n \ , \qquad (3)$$

where:

f_{CLK} is the minimum data input frequency for CLK and SDI,

f_{UPDATE} is the update rate of the entire cascaded system, and

n is the number of cascaded A6285 devices.

Operating Modes The A6285 has two operating modes, determined by the MODE signal:

- On-Off mode (MODE = low)
- Dot Correction mode (MODE = high)

Fault Output, FAULT The open-drain output FAULT is used to report both of the fault flags, LOD and TSD. During normal operating conditions, the internal transistor connected to the FAULT pin is turned off. The voltage on FAULT is pulled up to V_{DD} through a external pull-up resistor.

If an LOD or TSD condition is detected, the internal transistor is turned on, and FAULT is pulled to PGND. Because FAULT is an open-drain output, multiple ICs can be ORed together and pulled-up to V_{DD} with a single pull-up resistor, as shown in figure 10. This reduces the number of signals needed to report faults.

To determine whether the fault is a TSD or an LOD, LOD can be masked by setting $\overline{OE}$ = high. However, it cannot be determined if both a TSD and an LOD condition are present. The FAULT Truth Table is shown on page 11.

Active Pull-up Enable, PE The A6285 provides active pull-ups on each output determined by the PE pin. When the LED supply, V_{LED}, is tied to the PE pin, the active pull-ups are enabled. When the PE pin is tied to ground, the active pull-ups are disabled. The Active Pull-up Enable is also current-limited to 2.8 mA typical, preventing possible damage to the device in the event of a short-to-ground. This feature can eliminate ghosting in multiplexing applications.

Undervoltage Lockout (UVLO) and Power-On Reset (POR) The A6285 includes an internal undervoltage lockout circuit that disables the outputs in the event that the logic supply voltage drops below a minimum acceptable level. This feature prevents the display of erroneous information, a function necessary for some critical applications. A Power-On Reset (POR) is performed upon recovery of the logic supply voltage after a UVLO event and at power-up. During POR, all internal shift registers and latches are set to 0.

Thermal Shutdown Protection and Fault Flag (TSD) The A6285 provides thermal protection when the device is overheated, typically a result of excessive power being dissipated in the outputs. If the junction temperature exceeds the threshold

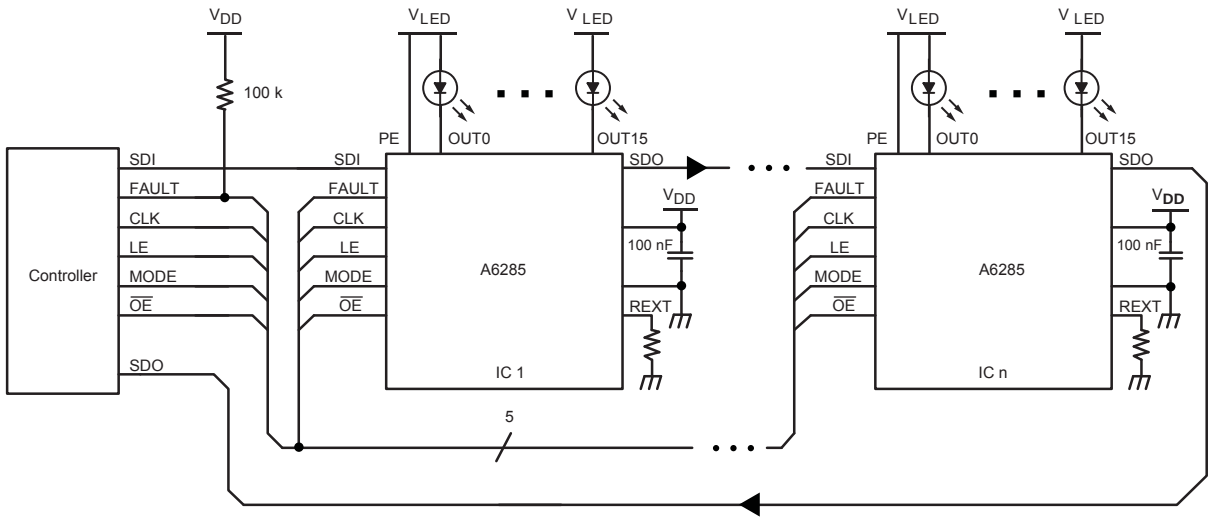


Figure 10. Schematic of cascaded A6285 devices

temperature, T_{TSDF}, of 165°C (typical), all driver outputs will be turned off and a TSD fault will be flagged. The TSD flag will pull the FAULT output pin to PGND (low). After a 15°C (typical) drop in junction temperature, the outputs will turn back on and the FAULT pin will be pulled back to VDD (high). The input shift register and the latch register will remain active during a TSD event. Therefore, there is no need to reset the data in the output latches. However, the TSD cycle will continue until the thermal problem is corrected.

LED Open Detection (LOD) The A6285 provides LED open circuit detection. This circuit flags a fault and pulls the FAULT pin to PGND (low) if any of the 16 OUT*x* LEDs are open or disconnected from the circuit.

The LOD circuit flags a fault when all of the following conditions are met:

- $\overline{OE}$ is set low
- The voltage at each OUTx pin is sampled after being turned on
- $V_{OUTx} < V_{LOD}$ (0.3 V typical)

MODE may be set either high or low. However, to perform a complete LOD cycle, which includes reading the LOD status of each OUTx, MODE must be set low.

A complete LOD cycle is described as follows:

1. On/Off data is clocked into the input shift register.
2. LE is pulsed to move the On/Off data into the On/Off Register. The data is moved on the rising edge of LE. If an LOD condition is present, the FAULT output is immediately pulled to PGND (low).
3. Data present at the Open Circuit Detector (sampled when data was moved into the On/Off Register on the previous transition of LE) is immediately moved into the input shift register on the same rising edge of LE.

   If no LOD condition was previously detected, all 0s are present at the Open Circuit Detector. Thus, all 0s are moved into the input shift register. This gives the appearance of "clearing" the input shift register every time On/Off data is moved into the On/Off Register, although in reality, the previous LOD status is being moved into the input shift register.

   If an LOD condition was previously detected, a 1 for each open LED will be moved from the Open Circuit Detector into the input shift register, where it can be read on the SDO pin.
4. The existing LOD condition is sampled within 2 µs of the outputs turning on and the resulting status data waits at the Open Circuit Detector until moved into the input shift register on the rising edge of the next LE pulse.
5. The cycle is repeated when new On/Off data is clocked into the input shift register. As new data is being clocked in, LOD status data is being clocked out of the SDO pin, where it can be read by a microprocessor.

Note: It is not necessary to load new On/Off data in order to view the LOD status waiting at the Open Circuit Detector. A second LE pulse will put the LOD data into the input shift register. However, LOD data that is presently in the input shift register will be moved into the On/Off Register, generating a "blank" display. Such a blank display may be undesirable; therefore, a second LE pulse should not be applied without first clocking in useful On/Off data for updating the display.

The update interval between LE pulses (LE1 to LE2), referred to as the LOD Sample and Read Time, t_{LOD}, must be at least 1660 ns to allow for settling and staggered delays. Figure 11 shows the LOD serial data format. The FAULT truth table is shown below.

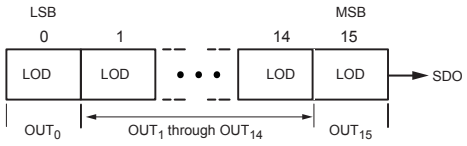


Figure 11. Individual output LOD data format

FAULT Truth Table

Conditions			Fault Output
Junction Temperature	**Outx Voltage**	**Output Enable, $\overline{OE}$**	
$T_J < T_{TSD}$	Outx > V_{LOD}	H	H
$T_J < T_{TSD}$	Outx < V_{LOD}	H	H
$T_J < T_{TSD}$	Outx > V_{LOD}	L	H
$T_J < T_{TSD}$	Outx < V_{LOD}	L	L
$T_J > T_{TSD}$	Outx > V_{LOD}	H	L
$T_J > T_{TSD}$	Outx < V_{LOD}	H	L
$T_J > T_{TSD}$	Outx > V_{LOD}	L	L
$T_J > T_{TSD}$	Outx < V_{LOD}	L	L

Application Information

Load Supply Voltage (V_{LED})

These devices are designed to operate with driver voltage drops (V_{DS}) of 1.0 to 3.0V, with one or more LED forward voltages, V_F, of 1.2 to 4.0 V. If higher voltages are dropped across the driver, package power dissipation will increase significantly. To minimize package power dissipation, it is recommended to use the lowest possible load supply voltage, V_{LED}, or to set any series voltage dropping, V_{DROP}, according to the following formula:

$$V_{DROP} = V_{LED} - V_F - V_{DS},$$

with $V_{DROP} = I_O \times R_{DROP}$ for a single driver or for a Zener diode (V_Z), or for a series string of silicon diodes (approximately 0.7 V per diode) for a group of drivers (see figure 3). If the available voltage source will cause unacceptable power dissipation and series resistors or diodes are undesirable, a voltage regulator can be used to provide V_{LED}.

For reference, typical LED forward voltages are:

LED Type	V_F (V)
White	3.5 to 4.0
Blue	3.0 to 4.0
Green	1.8 to 2.2
Yellow	2.0 to 2.1
Amber	1.9 to 2.65
Red	1.6 to 2.25
Infrared	1.2 to 1.5

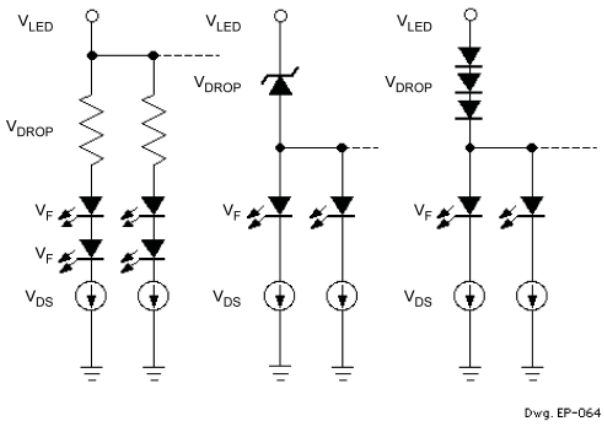


Figure 12. Typical application voltage drops

Pattern Layout

The logic and power grounds should be kept separate, terminated at one location. The exposed metal pad must be connected to a large power ground plane, allowing the copper to dissipate heat. Where multiple devices are cascaded, multilayer boards are recommended.

REXT should be placed as close as possible to the device, keeping a short distance between the REXT pin and ground.

Decoupling capacitors should be used liberally. 0.1 µF should be placed on the logic supply pin, and 10 µF placed between the common VLED line and the device ground at least at every second device.

Package Power Dissipation (P_D)

The maximum allowable package power dissipation based on package type is determined by:

$$P_{D(max)} = (150 - T_A) / R_{\theta JA},$$

where $R_{\theta JA}$ is the thermal resistance of the package mounted on the circuit board, determined experimentally. Power dissipation levels based on the package are shown in the Package Thermal Characteristics section (see page 7).

The actual package power dissipation is determined by:

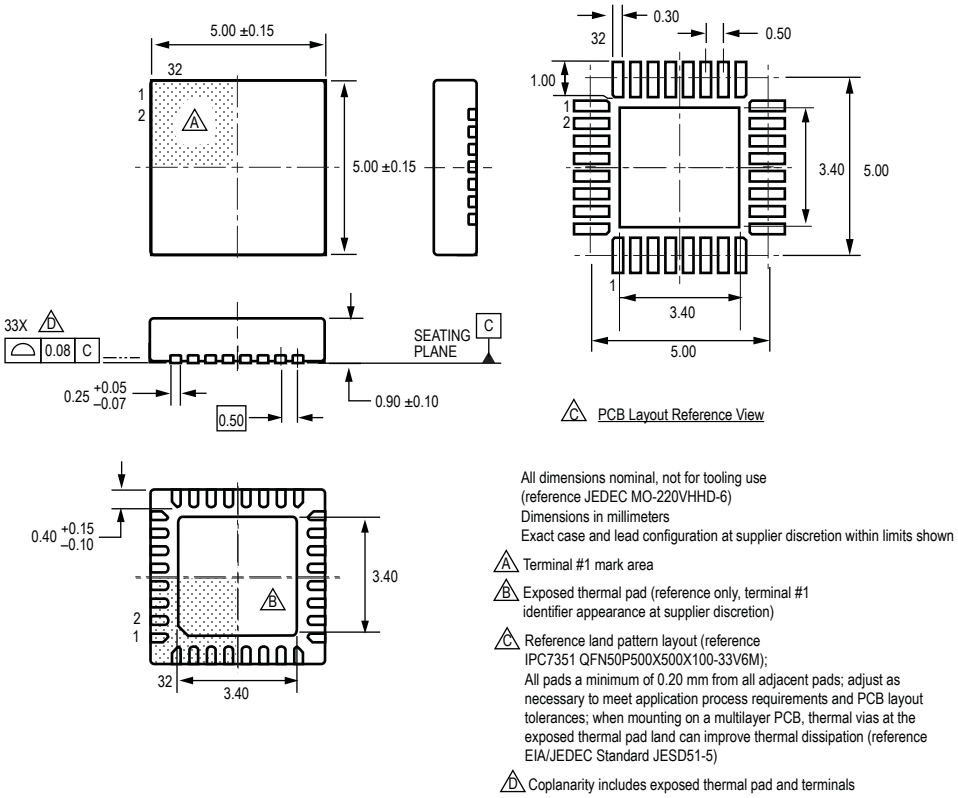
$$P_{D(act)} = DC \times (V_{DS} \times I_O \times 16) + (V_{DD} \times I_{DD}),$$

where DC is the duty cycle. The value *16* represents the maximum number of available device outputs.

When the load supply voltage, V_{LED}, is greater than 3 to 5 V, and $P_{D(act)} > P_{D(max)}$, an external voltage reducer (V_{DROP}) must be used (see figure 12).

Reducing the percent duty cycle, DC, will also reduce power dissipation.

Package ET, 5 mm x 5 mm, 32-pin QFN with Exposed Thermal Pad



All dimensions nominal, not for tooling use
(reference JEDEC MO-220VHHD-6)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

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