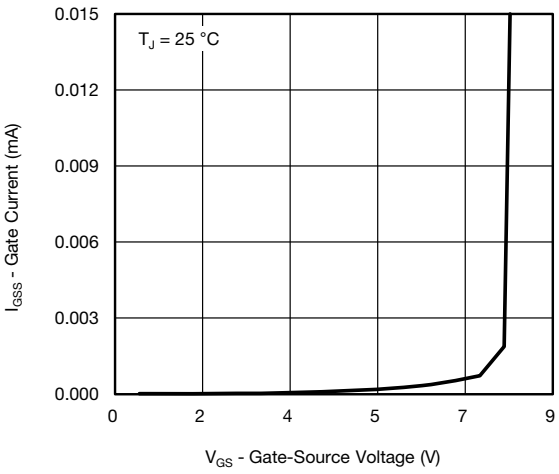
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 8			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 6.1		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.1		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.35		- 1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 5 V			± 20	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 8 V, V_{GS} = 0 V			- 1	
		V_{DS} = - 8 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 15			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 3 A		0.0265	0.0320	Ω
		V_{GS} = - 2.5 V, I_D = - 3 A		0.0360	0.0450	
		V_{GS} = - 1.8 V, I_D = - 1 A		0.0500	0.0630	
		V_{GS} = - 1.5 V, I_D = - 0.5 A		0.0600	0.1200	
		V_{GS} = - 1.2 V, I_D = - 0.5 A		0.1000	0.2300	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 4 V, I_D = - 7.4 A		18		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 4 V, V_{GS} = 0 V, f = 1 MHz		878		pF
Output Capacitance	C_{oss}			415		
Reverse Transfer Capacitance	C_{rss}			735		
Total Gate Charge	Q_g	V_{DS} = - 4 V, V_{GS} = - 5 V, I_D = - 7.4 A		12.3	18.5	nC
		V_{DS} = - 4 V, V_{GS} = - 4.5 V, I_D = - 7.4 A		11.3	17	
Gate-Source Charge	Q_{gs}			1.35		
Gate-Drain Charge	Q_{gd}			3.42		
Gate Resistance	R_g	f = 1 MHz	1.3	6.5	13	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 4 V, R_L = 0.68 Ω $I_D \cong$ - 5.9 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		19	29	ns
Rise Time	t_r			18	27	
Turn-Off Delay Time	$t_{d(off)}$			32	48	
Fall Time	t_f			19	29	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 9	A
Pulse Diode Forward Current	I_{SM}				- 15	
Body Diode Voltage	V_{SD}	I_S = - 5.9 A, V_{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 5.9 A, dI/dt = 100 A/µs, T_J = 25 °C		32	48	ns
Body Diode Reverse Recovery Charge	Q_{rr}			13	20	nC
Reverse Recovery Fall Time	t_a			14		ns
Reverse Recovery Rise Time	t_b			18		

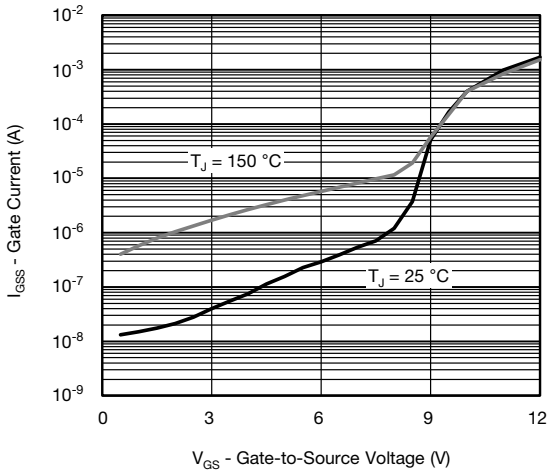
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

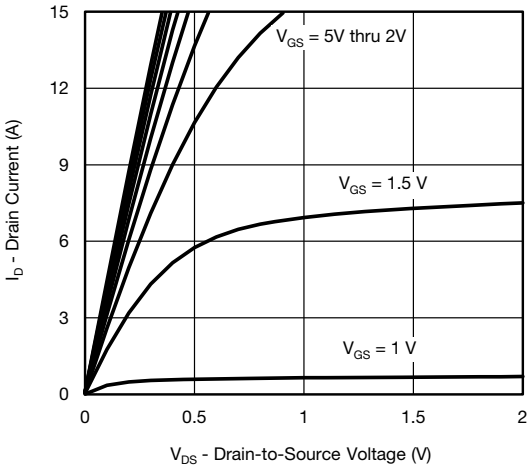
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



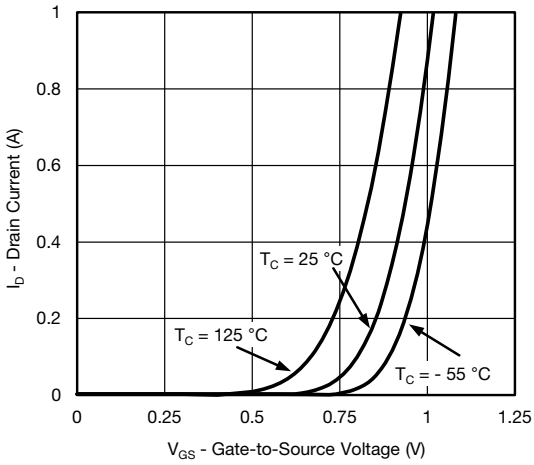
Gate Source Voltage vs. Gate Current



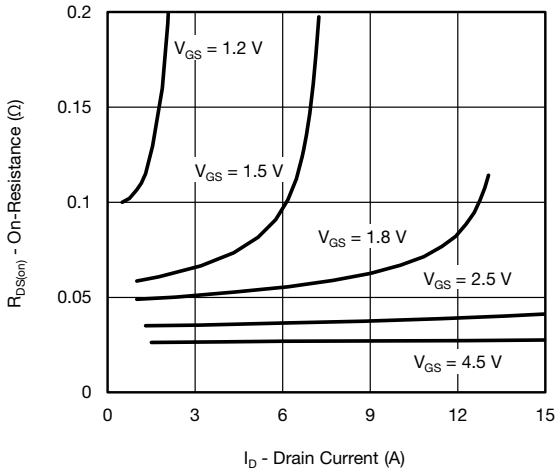
Gate Source Voltage vs. Gate Current



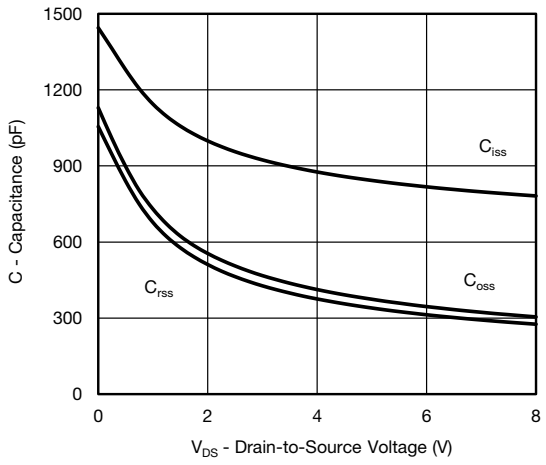
Output Characteristics



Transfer Characteristics

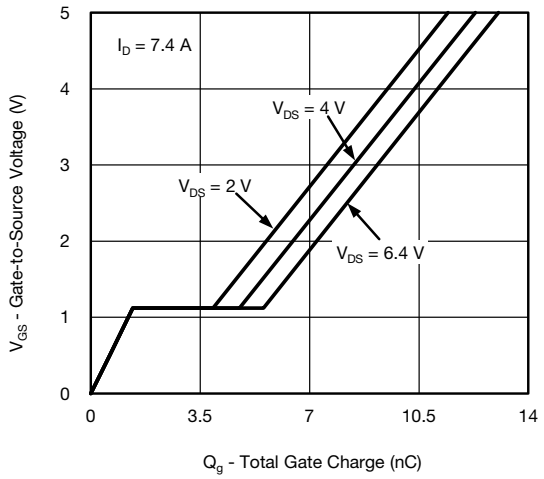


On-Resistance vs. Drain Current and Gate Voltage

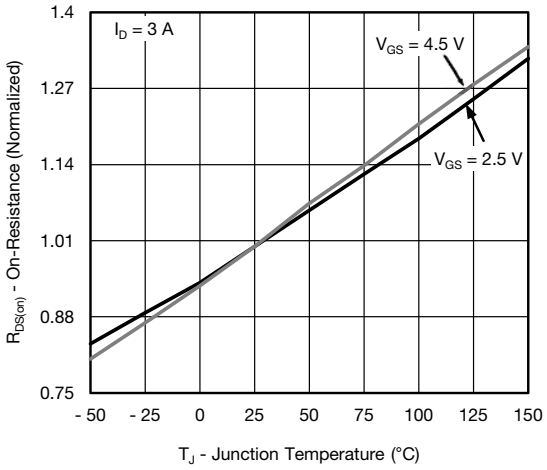


Capacitance

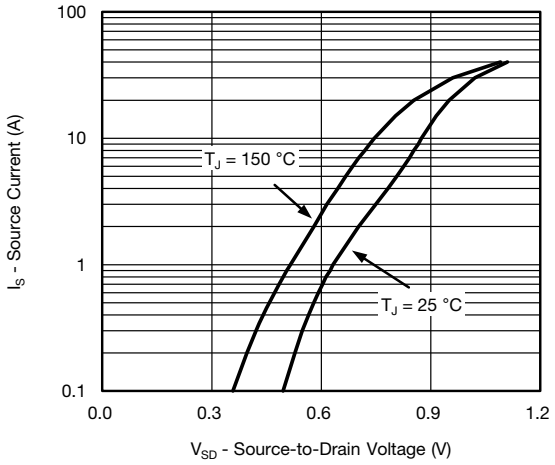
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



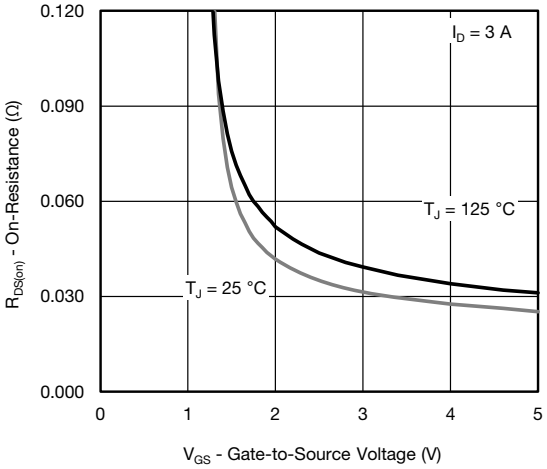
Gate Charge



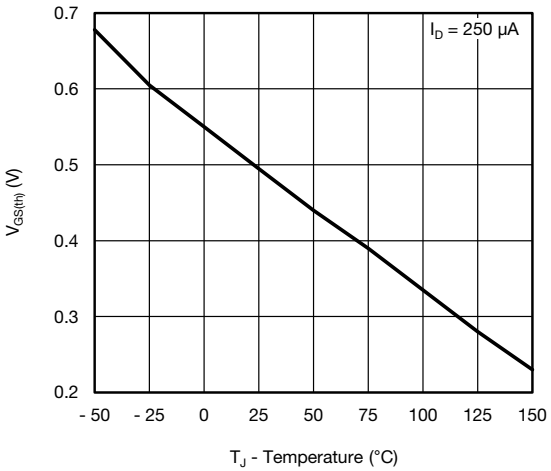
On-Resistance vs. Junction Temperature



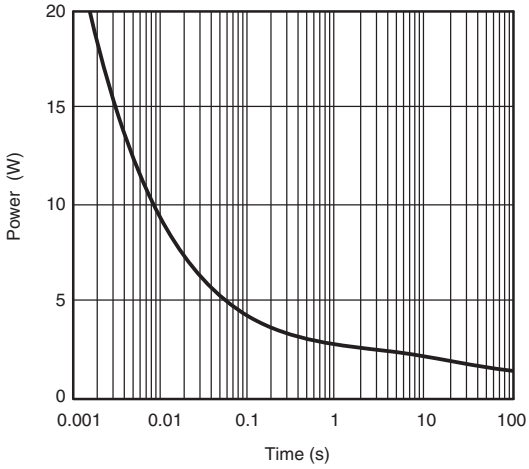
Soure-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



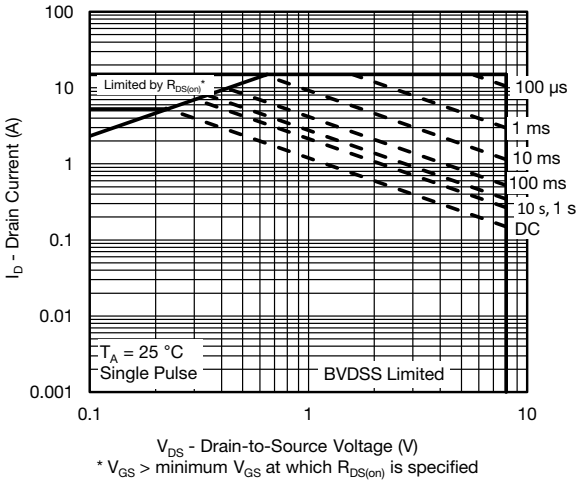
Threshold Voltage



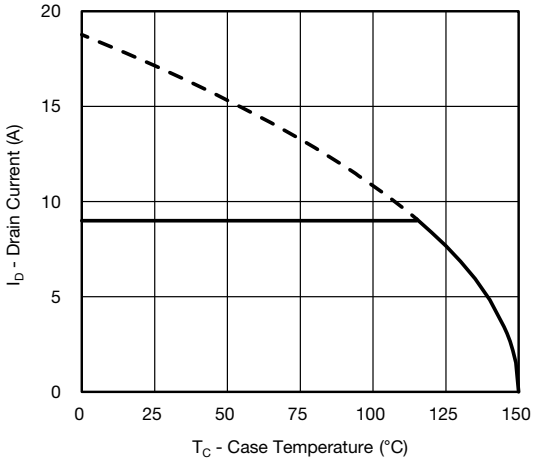
Single Pulse Power, Junction-to-Ambient

For technical questions, contact: pmostechsupport@vishay.com
Document Number: 63899
S12-2333-Rev. A, 01-Oct-12

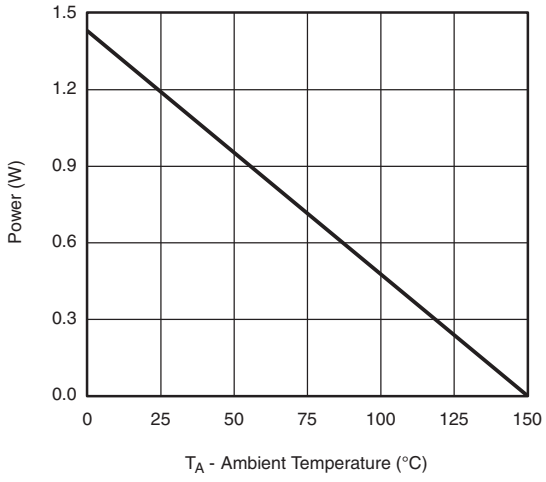
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



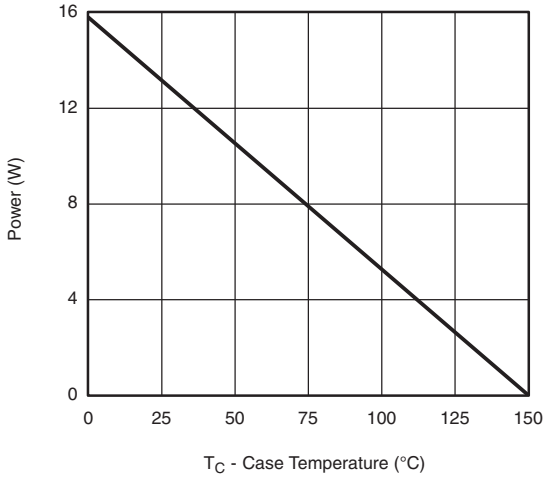
Safe Operating Area, Junction-to-Case



Current Derating**



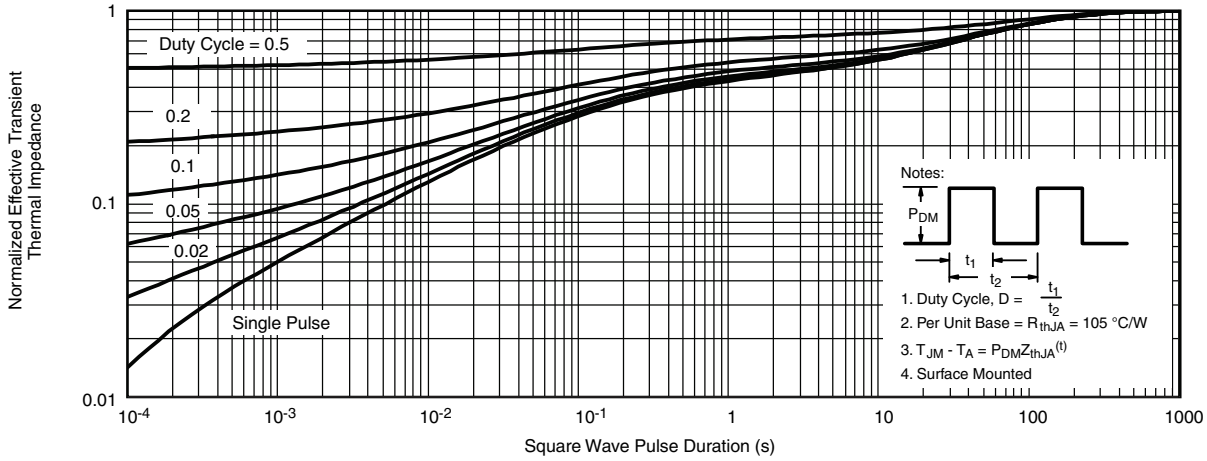
Power Junction-to-Ambient



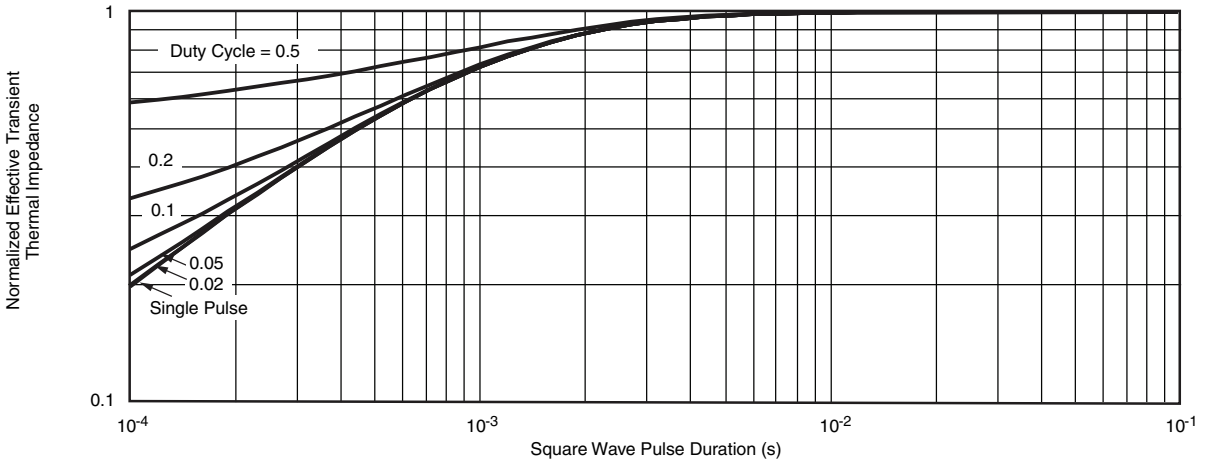
Power Junction-to-Case

** The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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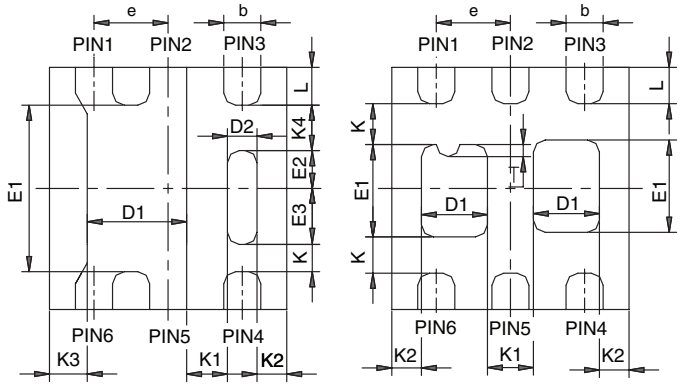
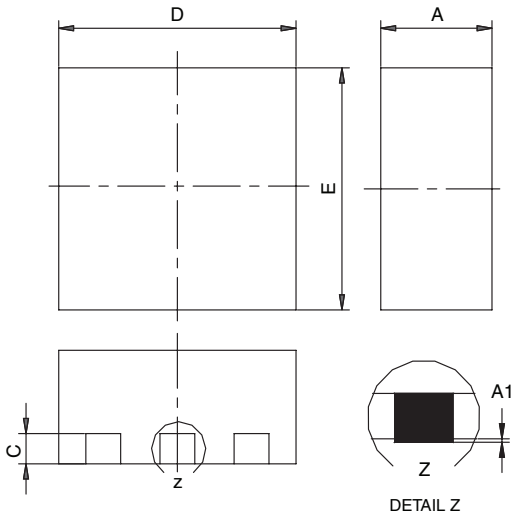
PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



DETAIL Z

Notes:
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

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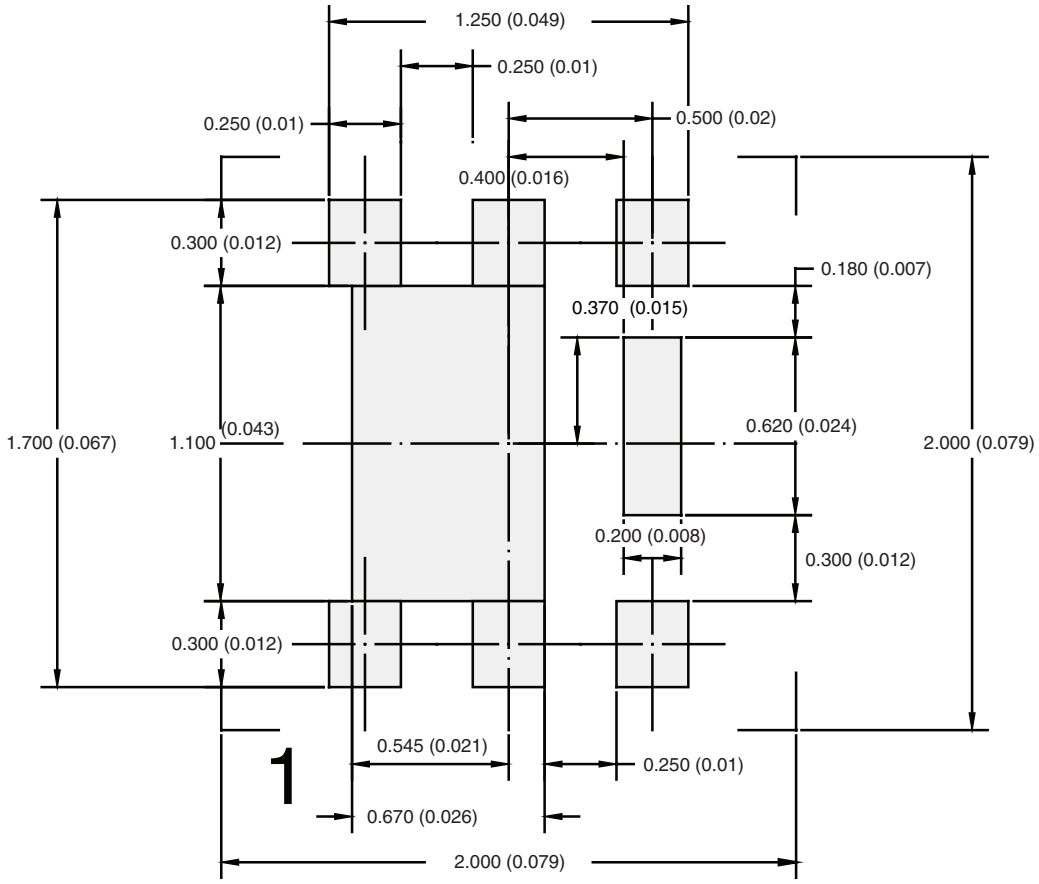
DWG: 5935

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single



Dimensions in mm/(Inches)

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