PACKAGE/ORDERING INFORMATION

MODEL	RESET THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM706B	4.63	SOIC-8	SGM706B-LXS8G/TR	SGM 706BLXS8 XXXXX	Tape and Reel, 4000
	4.63	MSOP-8	SGM706B-LXMS8G/TR	SGM706BL XMS8 XXXXX	Tape and Reel, 4000
	4.38	SOIC-8	SGM706B-MXS8G/TR	SGM 706BMXS8 XXXXX	Tape and Reel, 4000
	4.38	MSOP-8	SGM706B-MXMS8G/TR	SGM706BM XMS8 XXXXX	Tape and Reel, 4000
	4.0	SOIC-8	SGM706B-JXS8G/TR	SGM 706BJXS8 XXXXX	Tape and Reel, 4000
	4.0	MSOP-8	SGM706B-JXMS8G/TR	SGM706BJ XMS8 XXXXX	Tape and Reel, 4000
	3.08	SOIC-8	SGM706B-TXS8G/TR	SGM 706BTXS8 XXXXX	Tape and Reel, 4000
	3.08	MSOP-8	SGM706B-TXMS8G/TR	SGM706BT XMS8 XXXXX	Tape and Reel, 4000
	2.93	SOIC-8	SGM706B-SXS8G/TR	SGM 706BSXS8 XXXXX	Tape and Reel, 4000
	2.93	MSOP-8	SGM706B-SXMS8G/TR	SGM706BS XMS8 XXXXX	Tape and Reel, 4000
	2.63	SOIC-8	SGM706B-RXS8G/TR	SGM 706BRXS8 XXXXX	Tape and Reel, 4000
	2.63	MSOP-8	SGM706B-RXMS8G/TR	SGM706BR XMS8 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

X X X X X
- Vendor Code
- Trace Code
- Date Code - Year
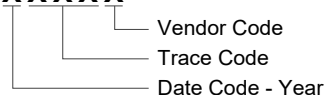
Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

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DECEMBER 2018

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ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (With Respect to GND)

V_{CC} .... -0.3V to 6.0V

All Other Inputs .... -0.3V to (V_{CC} + 0.3V)

Input Current

V_{CC} 20mA

GND 20mA

Output Current

All Outputs 20mA

Package Thermal Resistance

SOIC-8, θ_{JA} .... 145°C/W

MSOP-8, θ_{JA} .... 190°C/W

Junction Temperature .... +150°C

Storage Temperature Range .... -65°C to +150°C

Lead Temperature (Soldering, 10s) .... +260°C

ESD Susceptibility

HBM 4000V

MM 400V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Ambient Temperature Range .... -40°C to +125°C

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.
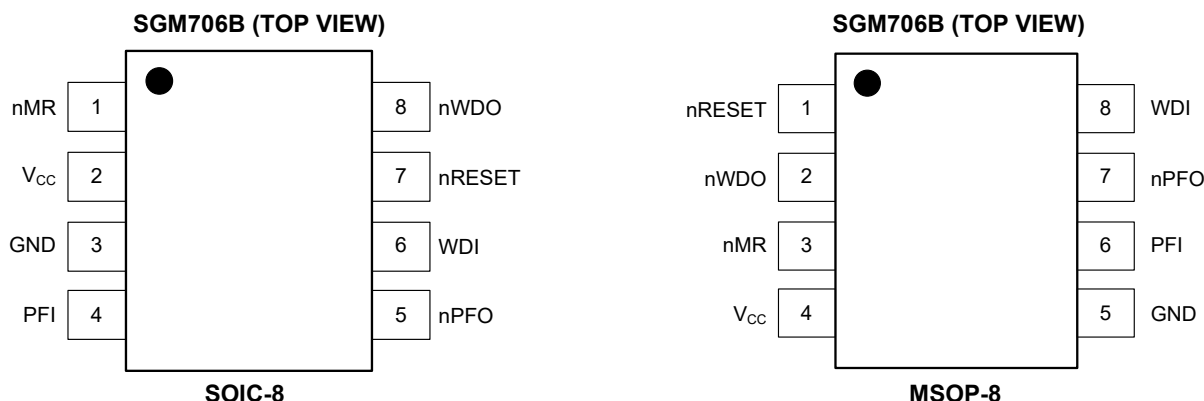
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

SGM706B (TOP VIEW)
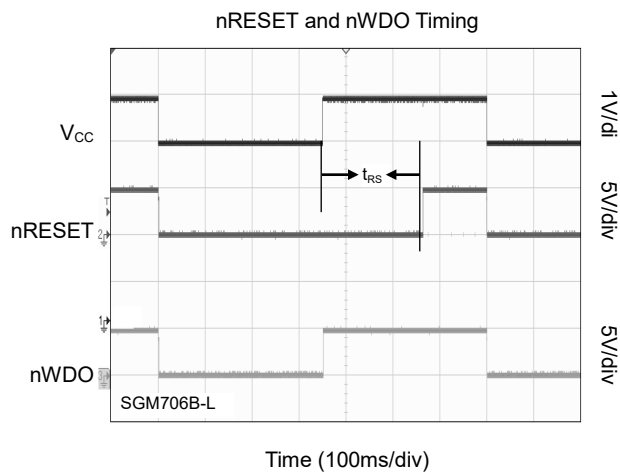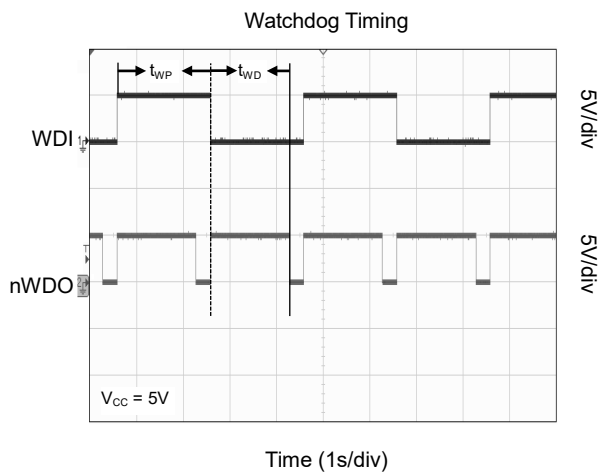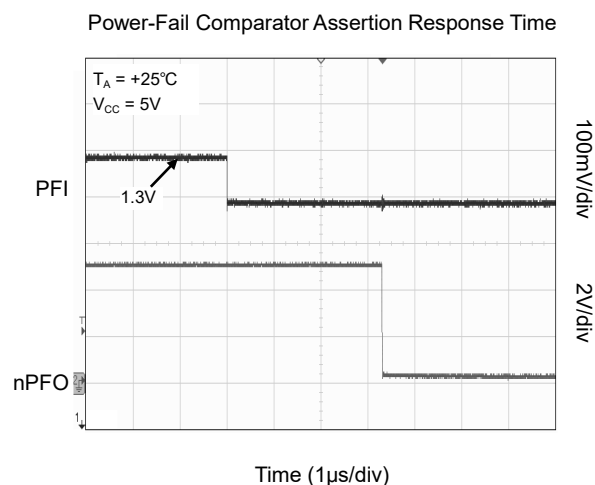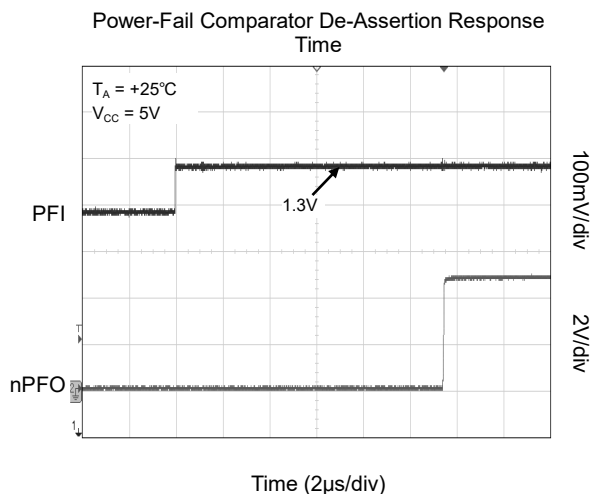
nMR	1	8	nWDO
V$_{CC}$	2	7	nRESET
GND	3	6	WDI
PFI	4	5	nPFO

SOIC-8

SGM706B (TOP VIEW)

nRESET	1	8	WDI
nWDO	2	7	nPFO
nMR	3	6	PFI
V$_{CC}$	4	5	GND

MSOP-8

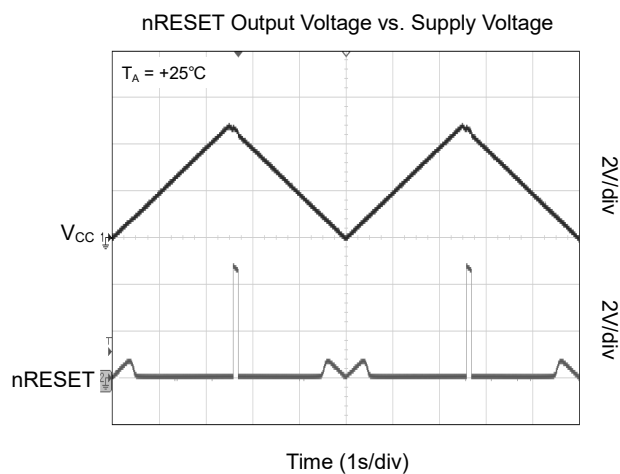## PIN DESCRIPTION

PIN		NAME	FUNCTION
SOIC-8	MSOP-8		
1	3	nMR	Manual Reset Input Pin. Manual reset input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 234µA (V$_{CC}$ = +5V) pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	4	V$_{CC}$	Power Supply Voltage. Power supply voltage that is monitored.
3	5	GND	Ground. 0V ground reference for all signals.
4	6	PFI	Power-Fail Voltage Monitor Input Pin. When PFI is less than 1.25V, nPFO goes low. Connect PFI to GND or V$_{CC}$ when not used.
5	7	nPFO	Power-Fail Output Pin. Power-fail output goes low and sinks current when PFI is less than 1.25V; otherwise nPFO stays high.
6	8	WDI	Watchdog Input Pin. If WDI remains high or low for 1.6s, the internal watchdog timer runs out and nWDO goes low. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge.
7	1	nRESET	Reset Pin. Active-low reset output pulses low for 200ms when triggered, and stays low whenever V$_{CC}$ is below the reset threshold (4.63V for SGM706B-L, 4.38V for SGM706B-M, 4.0V for SGM706B-J, 3.08V for SGM706B-T and 2.93V for SGM706B-S, 2.63V for SGM706B-R). It remains low for 200ms after V$_{CC}$ rises above the reset threshold or nMR goes from low to high. A watchdog timeout will not trigger nRESET unless nWDO is connected to nMR.
8	2	nWDO	Watchdog Output Pin. Watchdog output pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. nWDO also goes low during low-line conditions. Whenever V$_{CC}$ is below the reset threshold, nWDO stays low; however, unlike nRESET, nWDO does not have a minimum pulse width. As soon as V$_{CC}$ rises above the reset threshold, nWDO goes high with no delay.

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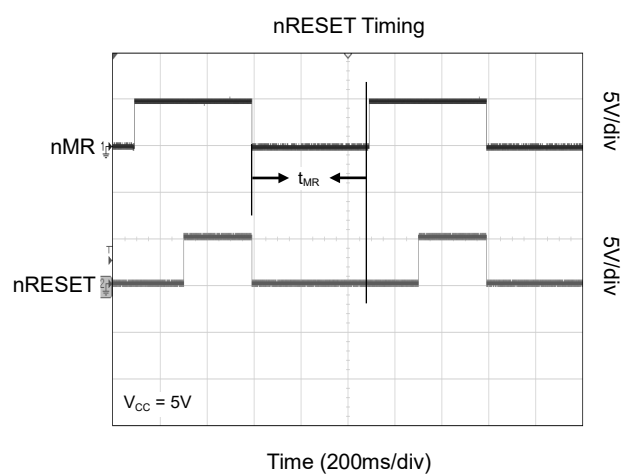www.sg-micro.com

ELECTRICAL CHARACTERISTICS

(T_A = +25℃, V_{CC} = 4.72V to 5.5V for SGM706B-L; V_{CC} = 4.47V to 5.5V for SGM706B-M; V_{CC} = 4.08V to 5.5V for SGM706B-J; V_{CC} = 3.15V to 5.5V for SGM706B-T; V_{CC} = 2.99V to 5.5V for SGM706B-S; V_{CC} = 2.69V to 5.5V for SGM706B-R, Full = -40℃ to +125℃, unless otherwise noted.)

PARAMETER	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
Operating Voltage Range (V_{CC})			Full	1.0		5.5	V
Supply Current (I_{SUPPLY})	V_{CC} = 3.6V		Full		0.6	1.2	µA
	V_{CC} = 5.5V		Full		0.8	1.5	µA
nRESET Threshold (V_{nRST})	SGM706B-L		+25℃	4.55	4.63	4.70	V
			Full	4.52	4.63	4.72	
	SGM706B-M		+25℃	4.30	4.38	4.45	
			Full	4.28	4.38	4.47	
	SGM706B-J		+25℃	3.93	4.0	4.07	
			Full	3.92	4.0	4.08	
	SGM706B-T		+25℃	3.03	3.08	3.14	
			Full	3.02	3.08	3.15	
	SGM706B-S		+25℃	2.88	2.93	2.98	
			Full	2.87	2.93	2.99	
	SGM706B-R		+25℃	2.58	2.63	2.68	
			Full	2.57	2.63	2.69	
nRESET Threshold Hysteresis	SGM706B-L		+25℃		20		mV
	SGM706B-M		+25℃		19		
	SGM706B-J		+25℃		17		
	SGM706B-T		+25℃		13		
	SGM706B-S		+25℃		13		
	SGM706B-R		+25℃		11		
nRESET Threshold Temperature Coefficient			Full		20		ppm/℃
nRESET Pulse Width (t_{RS})			Full	140	200	290	ms
nRESET Output Voltage	I_{SOURCE} = 800µA		Full	V_{CC} - 1.5			V
	I_{SINK} = 3.2mA		Full			0.4	
	V_{CC} = 1V, I_{SINK} = 50µA		Full			0.3	
Watchdog Timeout Period (t_{WD})			Full	1.1	1.6	2.4	s
WDI Pulse Width (t_{WP})	V_{IL} = 0V, V_{IH} = V_{CC}		Full	90			ns
WDI Input Threshold	Low	V_{CC} = 5V	Full			0.8	V
	High	V_{CC} = 5V	Full	3.5			
	Low	$V_{nRST(MAX)}$ < V_{CC} < 3.6V	Full			0.8	
	High	$V_{nRST(MAX)}$ < V_{CC} < 3.6V	Full	0.7 × V_{CC}			
WDI Input Current	WDI = V_{CC}		Full		0.01	1.0	µA
	WDI = 0V		Full	-1.0	-0.01		
nWDO Output Voltage	I_{SOURCE} = 800µA		Full	V_{CC} - 1.5			V
	I_{SINK} = 1.2mA		Full			0.2	
nMR Pull-Up Current	nMR = 0V, V_{CC} = 5V		Full	100		300	µA
nMR Pulse Width (t_{MR})			Full	300			ns
nMR Input Threshold	Low		Full			0.8	V
	High		Full	2			
nMR to nRESET Out Delay (t_{MD})			Full			420	ns
PFI Input Threshold	V_{CC} = 5V		Full	1.21	1.25	1.29	V
PFI Input Current			Full		0.2	50	nA
nPFO Output Voltage	I_{SOURCE} = 800µA		Full	V_{CC} - 1.5			V
	I_{SINK} = 3.2mA		Full			0.3	

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TYPICAL PERFORMANCE CHARACTERISTICS

nRESET Output Voltage vs. Supply Voltage

nRESET Response Time

Power-Fail Comparator De-Assertion Response Time

Power-Fail Comparator Assertion Response Time

Watchdog Timing

nRESET and nWDO Timing
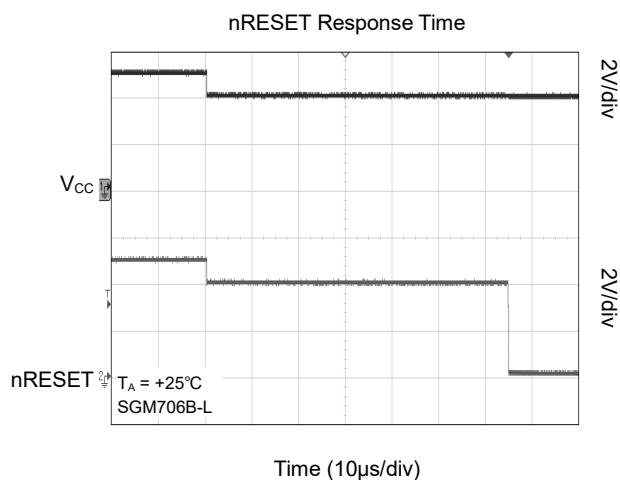
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

nRESET Timing

nMR

t_{MR}

5V/div

nRESET

5V/div

V_{CC} = 5V

Time (200ms/div)

FUNCTIONAL BLOCK DIAGRAM
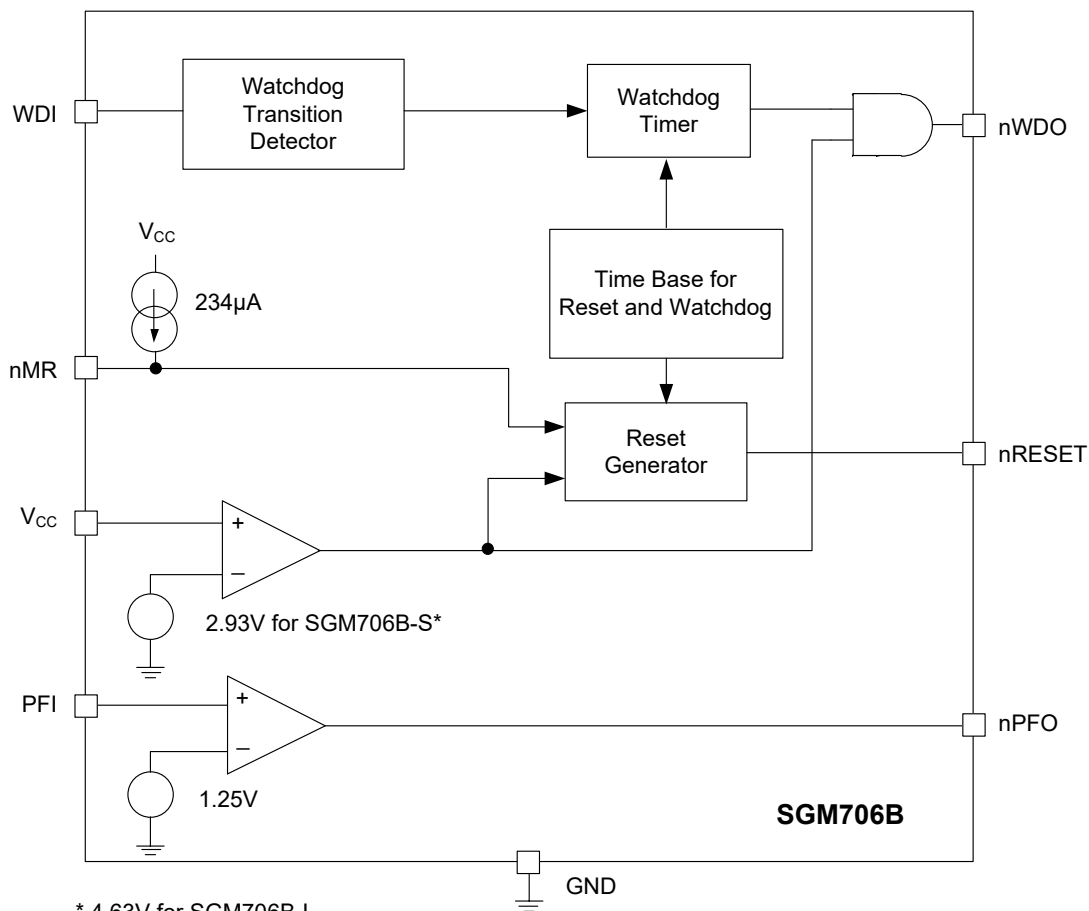
* 4.63V for SGM706B-L
  4.38V for SGM706B-M
  4.0V for SGM706B-J
  3.08V for SGM706B-T
  2.93V for SGM706B-S
  2.63V for SGM706B-R

APPLICATION NOTES

Ensuring a Valid nRESET Output Down to $V_{CC} = 0V$

When V_{CC} falls below 1V, the SGM706B nRESET output no longer sinks current, it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the nRESET pin as shown in Figure 1, any stray charge or leakage currents will be drained to ground, holding nRESET low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load nRESET and small enough to pull nRESET to ground.
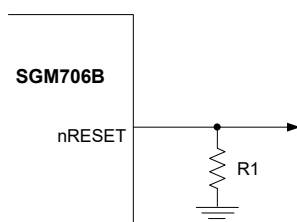
Figure 1. nRESET Valid to Ground Circuit

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and nPFO. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. nRESET can be asserted on other voltages in addition to the +5V V_{CC} line. Connect nPFO to nMR to initiate a nRESET pulse when PFI drops below 1.25V. Figure 2 shows the SGM706B configured to assert nRESET when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.
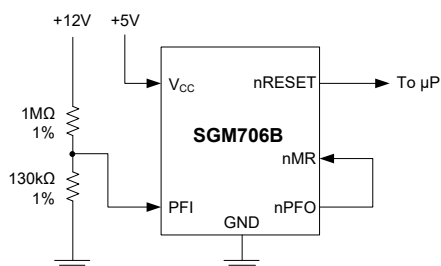

Figure 2. Monitoring Both +5V and +12V

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 3). When the negative rail is good (a negative voltage of large magnitude), nPFO is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), nPFO is high. By adding the resistors and transistor as shown, a high nPFO triggers reset. As long as nPFO remains high, the SGM706B will keep reset asserted (nRESET = low). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.
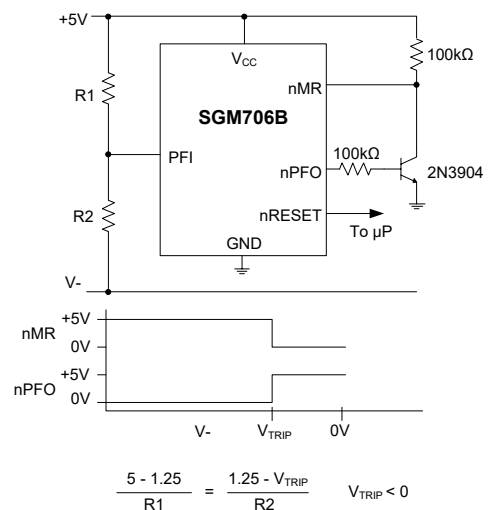

$$\frac{5 - 1.25}{R1} = \frac{1.25 - V_{TRIP}}{R2} \qquad V_{TRIP} < 0$$

Figure 3. Monitoring a Negative Voltage

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the SGM706B nRESET output. If, for example, the nRESET output is driven high and the microprocessor wants to pull it low, indeterminate logic levels may result in. To correct this, connect a 4.7kΩ resistor between the nRESET output and the µP reset I/O, as show in Figure 4. Buffer the nRESET output to other system components.
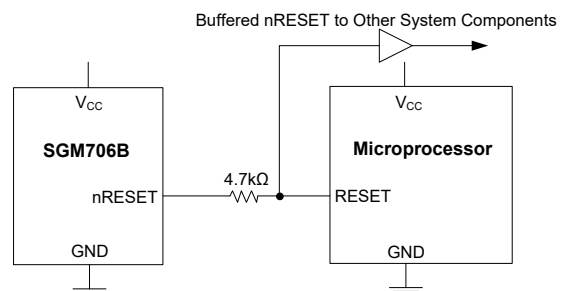

Figure 4. Interfacing to Microprocessors with Bidirectional Reset I/O
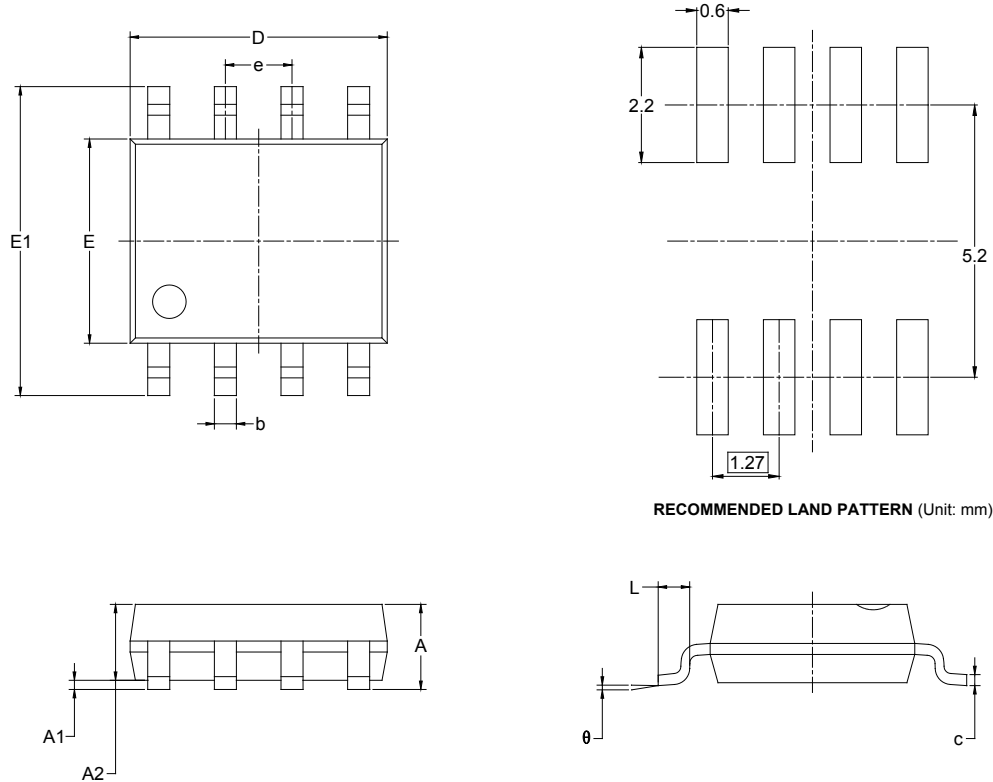
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2018) to REV.A

Changed from product preview to production data...All

PACKAGE OUTLINE DIMENSIONS

SOIC-8

RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°
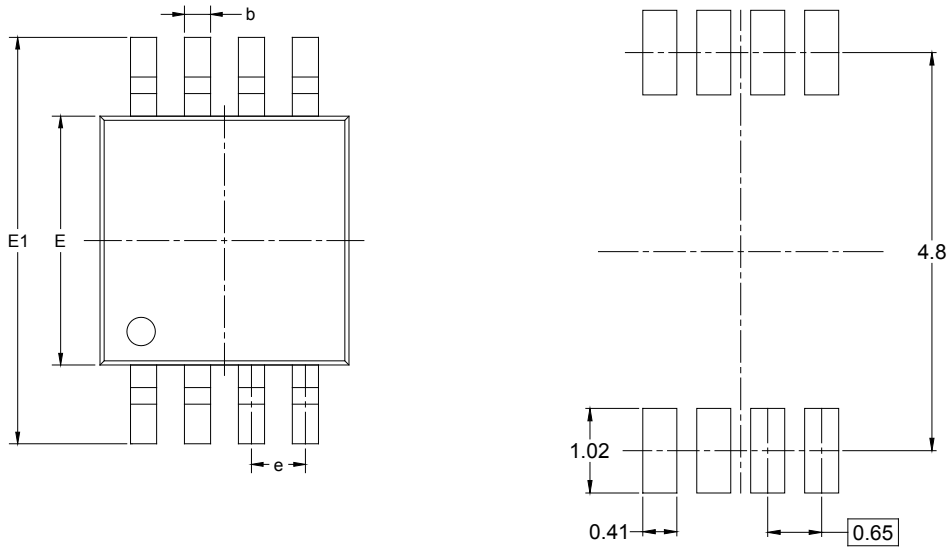
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PACKAGE OUTLINE DIMENSIONS

MSOP-8

RECOMMENDED LAND PATTERN (Unit: mm)
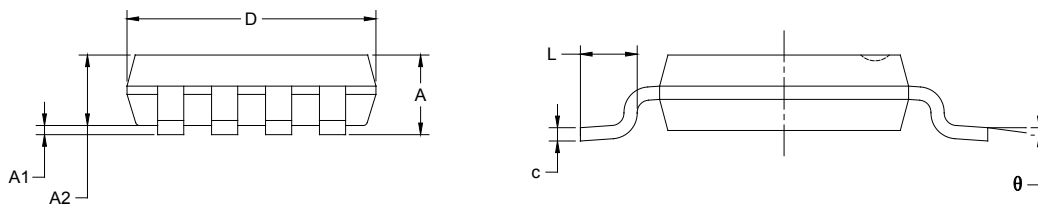
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.650 BSC		0.026 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

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TX00014.000
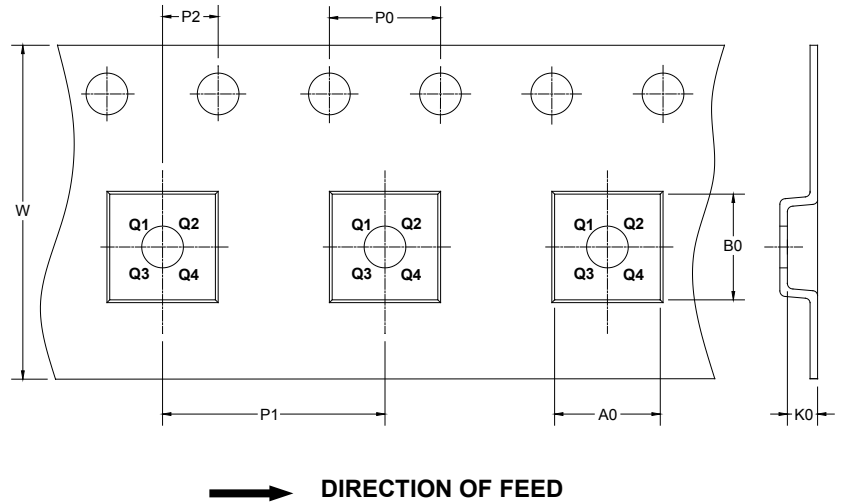
TAPE AND REEL INFORMATION

REEL DIMENSIONS
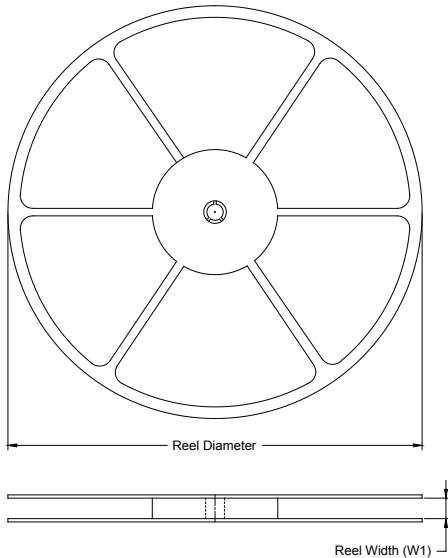
TAPE DIMENSIONS

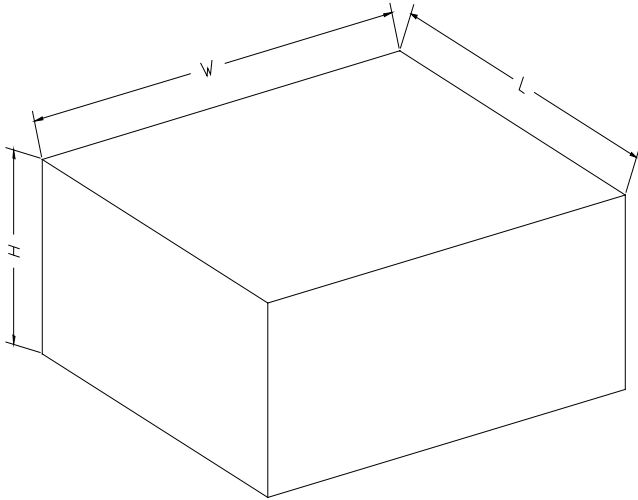NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13″	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1

DD0001

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CARTON BOX DIMENSIONS

NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002

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