ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 40V
Logic Inputs ..... -0.3V to 5.5V
Analog Inputs ..... -0.3V to V_{IN}
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Operating Junction Temperature
  Hermetic (J, L Packages) ..... 150°C
  Plastic (N, DW Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C
RoHS Peak Package Solder Reflow Temp. (40 sec. max. exp.)..... 260°C (+0, -5)

Note 1. Exceeding these ratings could cause damage to the device.

THERMAL DATA

J Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 25°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 70°C/W
N Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 30°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 60°C/W
DW Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 90°C/W
L Package:
  Thermal Resistance-Junction to Case, θ_{JC} ..... 35°C/W
  Thermal Resistance-Junction to Ambient, θ_{JA} ..... 120°C/W

Note A. Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
Note B. The above numbers for θ_{JC} are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θ_{JA} numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

RECOMMENDED OPERATING CONDITIONS (Note 2)

Input Voltage ..... 8V to 35V
Collector Supply Voltage ..... 4.5V to 35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 500kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 470pF to 20µF
Available Deadtime Range at 40kHz ..... 5% to 50%
Operating Junction Temperature Range:
  SG1526B ..... -55°C to 125°C
  SG2526B ..... -25°C to 85°C
  SG3526B ..... 0°C to 70°C

Note 2. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for SG1526B with -55°C ≤ T_A ≤ 125°C, SG2526B with -25°C ≤ T_A ≤ 85°C, SG3526B with 0°C ≤ T_A ≤ 70°C, and V_{IN} = 15V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Test Conditions	SG1526B/2526B			SG3526B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section (Note 3)								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	V_{IN} = 8 to 35V		7	10		10	20	mV
Load Regulation	I_L = 0 to 20mA		10	20		10	25	mV
Temperature Stability (Note 9)	Over Operating T_J		15	50		15	50	mV
Total Output Voltage Range (Note 9)		4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	125	25	50	125	mA
Undervoltage Lockout Section								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 4.8V	2.4	4.8		2.4	4.8		V

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions	SG1526B/2526B			SG3526B			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Oscillator Section (Note 4)								
Initial Accuracy	T_J = 25°C		±3	±8		±3	±8	%
Voltage Stability	V_{IN} = 8 to 35V		0.5	1.0		0.5	1.0	%
Temperature Stability (Note 9)	Over Operating T_J		7	10		3	5	%
Minimum Frequency (Note 9)	R_T = 150kΩ, C_T = 20µF			1.0			1.0	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	500			500			kHz
Sawtooth Peak Voltage	V_{IN} = 35V	2.5	3.0	3.5	2.5	3.0	3.5	V
Sawtooth Valley Voltage	V_{IN} = 8V	0.5	1.0	1.1	0.5	1.0	1.1	V
$\overline{\text{SYNC}}$ Pulse Width	R_L = 2.0kΩ to V_{REF}		1.0	2		1.0	2	µs
Error Amplifier Section (Note 5)								
Input Offset Voltage	R_S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ	64	72		60	72		dB
High Output Voltage	V_{PIN1} - V_{PIN2} ≥ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
Low Output Voltage	V_{PIN2} - V_{PIN1} ≥ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	V_{IN} = 8V to 35V	66	80		66	80		dB
PWM Comparator Section (Note 4)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = 0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = 3.6V	45	49		45	49		%
Digital Ports ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, and $\overline{\text{RESET}}$)								
HIGH Output Voltage	I_{SOURCE} = 40µA	2.4	4		2.4	4		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = 2.4V		-125	-200		-125	-200	µA
LOW Input Current	V_{IL} = 0.4V		-225	-360		-225	-360	µA
$\overline{\text{SHUTDOWN}}$ Delay to Output	(Note9)			200			200	ns
Current Limit Comparator Section (Note 6)								
Sense Voltage	R_S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Delay to Output (Note 9)				400			400	ns
Soft-Start Section								
Error Clamp Voltage	$\overline{\text{RESET}}$ = 0.4V		0.1	0.4.		0.1	0.4.	V
C_S Charging Current	$\overline{\text{RESET}}$ = 2.4V	50	100	150	50	100	150	µA
Output Drivers (each output) (Note 7)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2		1.2	2	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF		0.3	0.4		0.3	0.4	µs
Fall Time	C_L = 1000pF		0.1	0.15		0.1	0.15	µs
Power Consumption Section (Note 8)								
Standby Current	$\overline{\text{SHUTDOWN}}$ = 0.4V		18	30		18	30	mA

Note 3. I_L = 0mA
Note 4. F_{OSC} = 40kHz (R_T = 4.12kΩ ±1%, C_T = .01µF ±1%, R_D = 0Ω)
Note 5. V_{CM} = 0 to 5.2V
Note 6. V_{CM} = 0 to 12V
Note 7. V_C = 15V
Note 8. V_{IN} = 35V
Note 9. These parameters, although guaranteed over the recommended operating conditions, are not tested in production.

CHARACTERISTIC CURVES

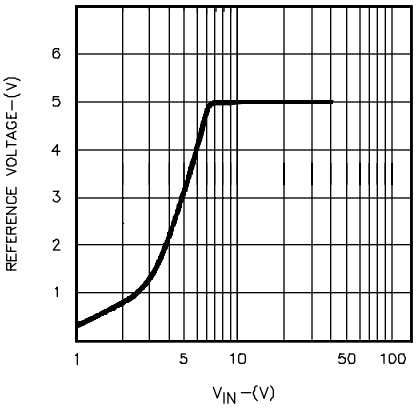


FIGURE 1.
REFERENCE VOLTAGE VS. SUPPLY VOLTAGE

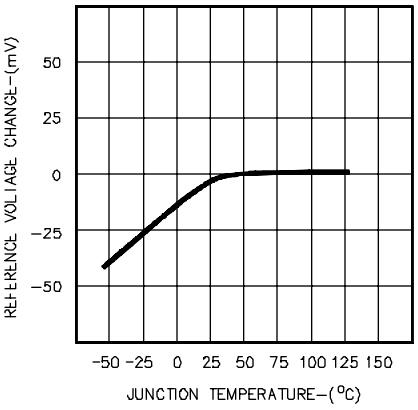


FIGURE 2.
REFERENCE TEMPERATURE STABILITY

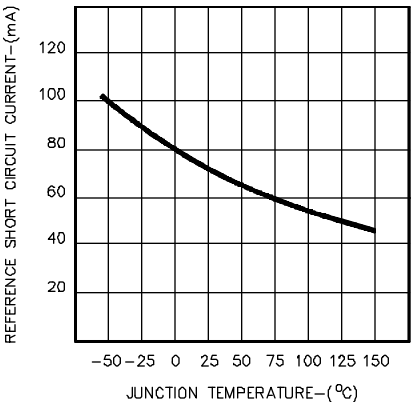


FIGURE 3.
REFERENCE SHORT CIRCUIT

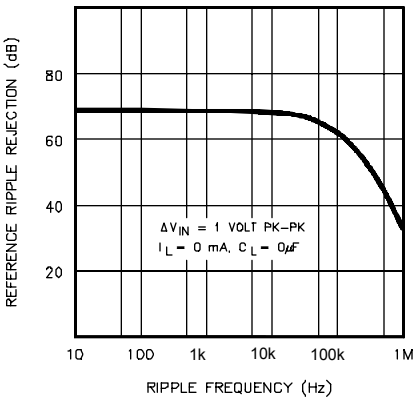


FIGURE 4.
REFERENCE RIPPLE REJECTION

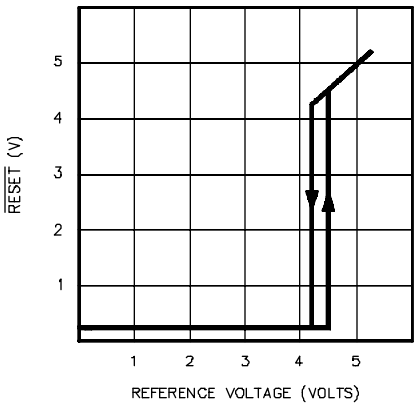


FIGURE 5.
UNDER VOLTAGE LOCKOUT

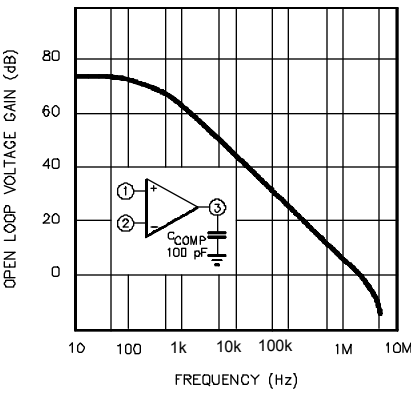


FIGURE 6.
ERROR AMPLIFIER OPEN LOOP GAIN
VS. FREQUENCY

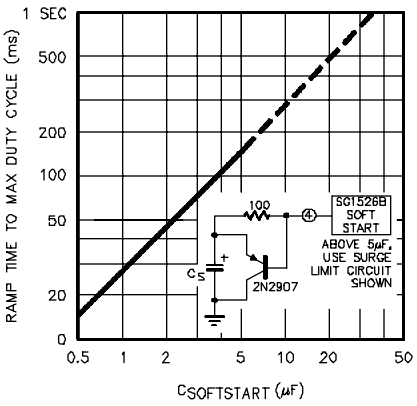


FIGURE 7.
SOFTSTART TIME CONSTANT VS. C_S

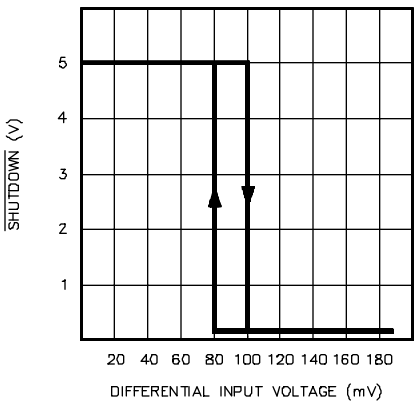


FIGURE 8.
CURRENT LIMIT TRANSFER FUNCTION

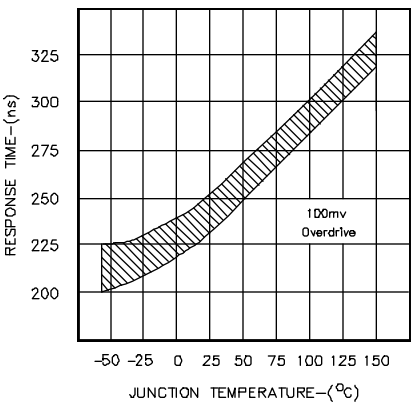


FIGURE 9.
COMPARATOR INPUT TO DRIVER OUTPUT DELAY

CHARACTERISTIC CURVES (continued)

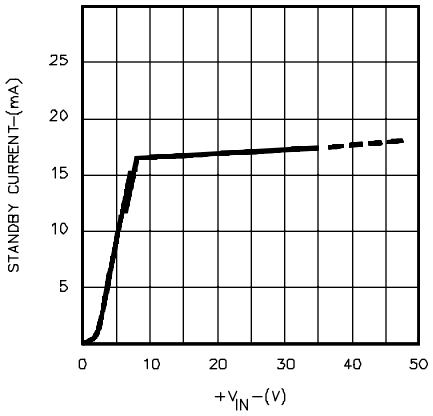


FIGURE 10.
STANDBY CURRENT VS. SUPPLY VOLTAGE

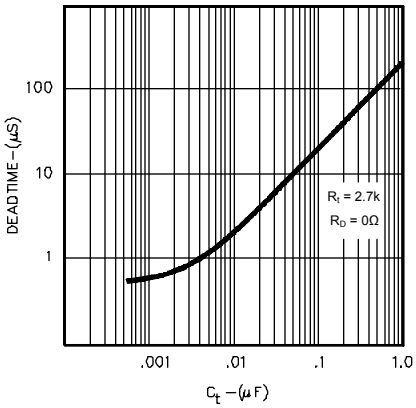


FIGURE 11.
OUTPUT DRIVER DEADTIME VS. C_T VALUE

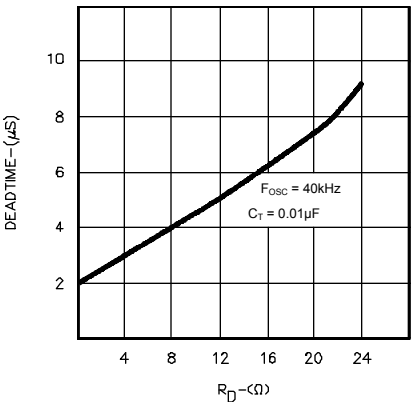


FIGURE 12.
OUTPUT DRIVER DEADTIME VS. R_D VALUE

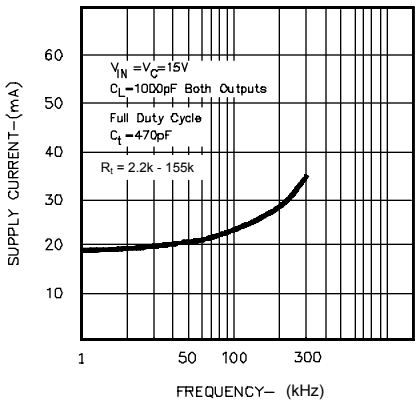


FIGURE 13.
SUPPLY CURRENT VS. OUTPUT FREQUENCY

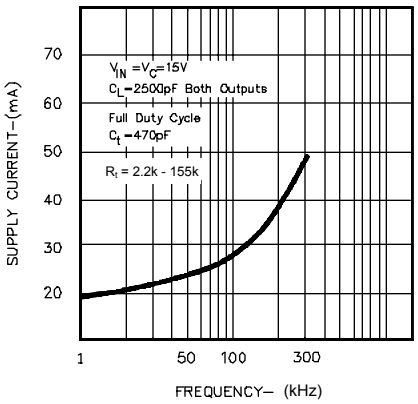


FIGURE 14.
SUPPLY CURRENT VS. OUTPUT FREQUENCY

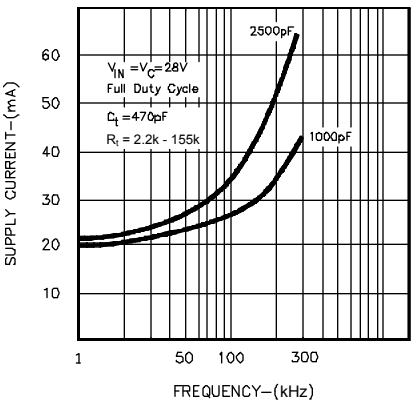


FIGURE 15.
SUPPLY CURRENT VS. OUTPUT FREQUENCY

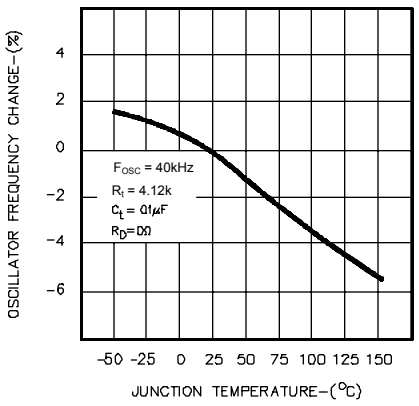


FIGURE 16.
OSCILLATOR FREQUENCY
TEMPERATURE STABILITY

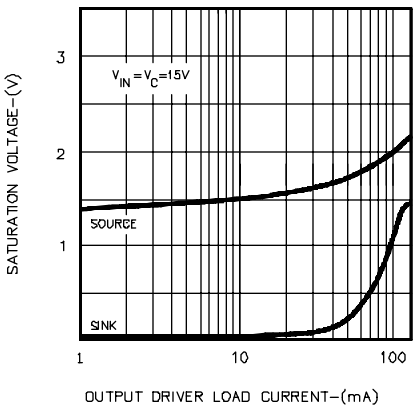


FIGURE 17.
OUTPUT DRIVER SATURATION VOLTAGE

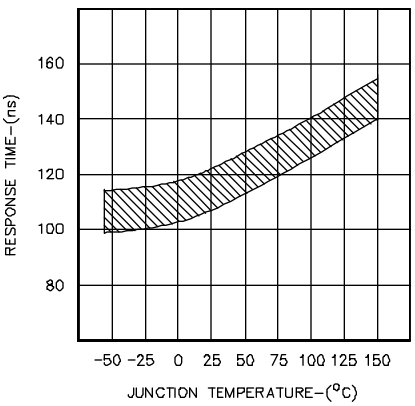


FIGURE 18.
SHUTDOWN INPUT TO DRIVER OUTPUT DELAY

CHARACTERISTIC CURVES (continued)

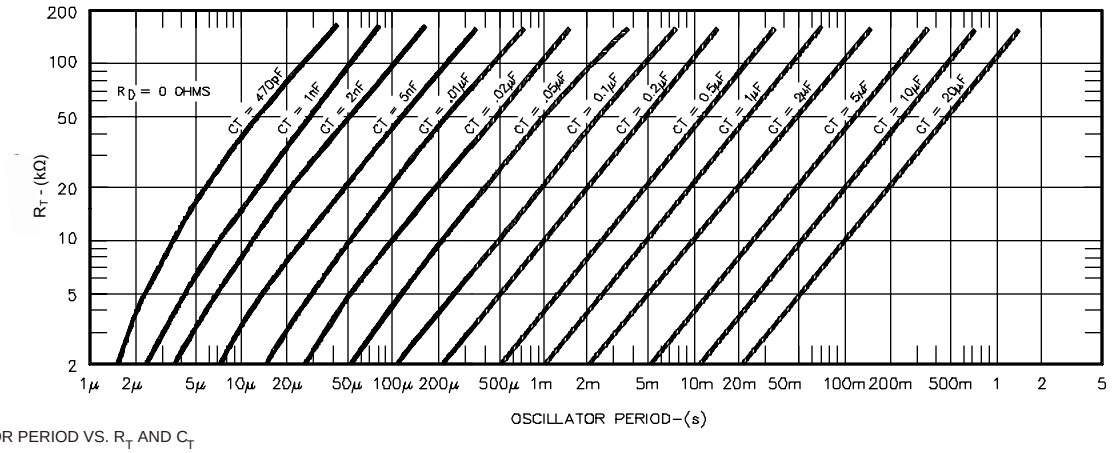


FIGURE 19.
OSCILLATOR PERIOD VS. R_T AND C_T

APPLICATION INFORMATION

VOLTAGE REFERENCE

The reference regulator of the SG1526B is a "band-gap" type; that is, the precision +5 volt output is derived from the very predictable base-emitter voltage of an NPN transistor. Since this is a sub-surface phenomenon, the resulting output exhibits excellent stability compared to earlier surface-breakdown Zener designs.

The reference output is stabilized at input voltages as low as +8 volts, and can provide up to 20mA of load current to external circuitry. An external PNP transistor can be used to boost the available current to many hundreds of mA. A rugged low-frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillation.

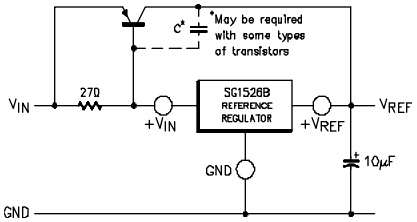


FIGURE 20.
EXTENDING REFERENCE OUTPUT CURRENT

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit protects the SG1526B and the power devices it controls from inadequate supply voltage. If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a merged bandgap reference and comparator circuit which is active when the reference voltage has risen to $2V_{BE}$ or 1.2 volts at 25°C. When the reference voltage rises to approximately +4.4 volts, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal softstart. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2 volts, the undervoltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The SG1526B can operate from a +5 volt supply regulated to within ±4% by connecting the V_{REF} pin to the $+V_{IN}$ pin.

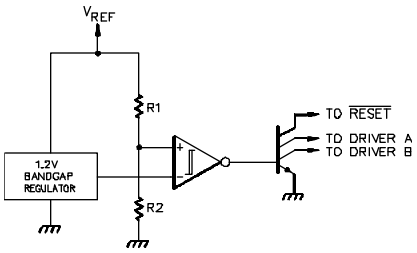


FIGURE 21.
SIMPLIFIED UNDERVOLTAGE LOCKOUT

SOFT-START CIRCUIT

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the SG1526B, the undervoltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100μA current source to charge C_S. Q2 clamps the error amplifier output to 1.0 V_{BE} above the voltage on C_S. As the soft-start voltage ramps up to +5 volts, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null. Figure 7 gives the timing relationship between C_S ramp time to 100% duty cycle.

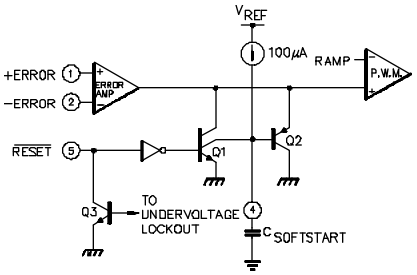


FIGURE 22.
SOFT-START CIRCUIT SCHEMATIC

APPLICATION INFORMATION (continued)

DIGITAL CONTROL PORTS

The three digital control ports of the SG1526B are bi-directional. Each pin can drive TTL and 5 volt CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators, fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1 volts at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

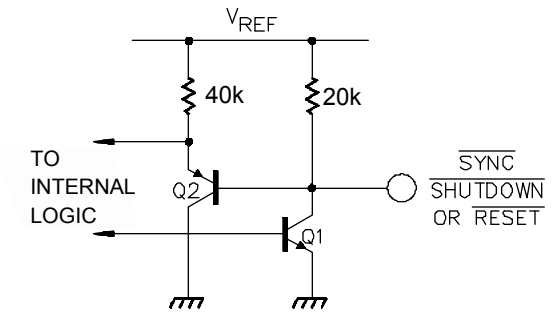


FIGURE 23
DIGITAL CONTROL PORT SCHEMATIC

OSCILLATOR

The oscillator is programmed for frequency and dead time with three components: R_T C_T, and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With R_D = 0Ω (pin 11 shorted to ground) select values for R_T and C_T from Figure 19 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.
2. If more dead time is required, select a larger value of R_D using Figure 12 as a guide. At 40 kHz dead time increases by 300 ns/Ω.
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The SG1526B can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5 µSec wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave R_T terminals should not be left open; at least 50k should be connected from each pin to ground. Slave R_D terminals may be either left open or grounded.

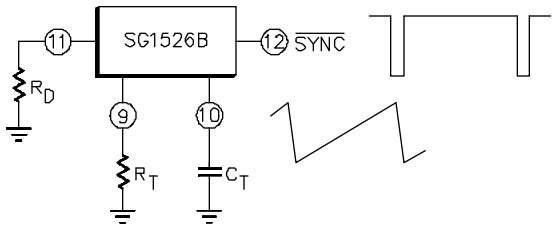


FIGURE 24.
OSCILLATOR CONNECTIONS AND WAVEFORMS

ERROR AMPLIFIER

The error amplifier is a transconductance design, with an output impedance of 2 megohms. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100 pF, the amplifier has an open-loop pole at 400 Hz.

The input connections to the error amplifier and determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0 volts and the feedback connections in Figure 25A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0 volt reference voltage, as shown in Figure 25B.

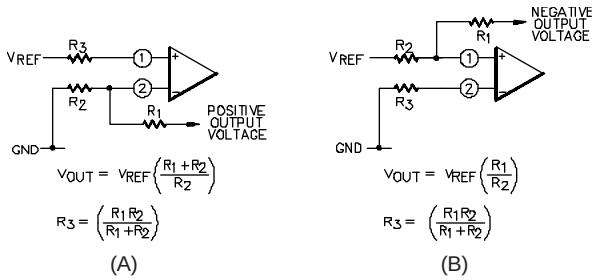


FIGURE 25.
ERROR AMPLIFIER CONNECTIONS

APPLICATION INFORMATION (continued)

OUTPUT DRIVERS

The totem-pole output drivers of the SG1526B are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$ pin, as required. Curves for the saturation voltage at these outputs as a function of load current are found in Figure 17.

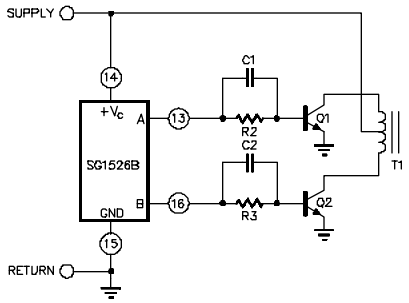


FIGURE 26.
PUSH-PULL CONFIGURATION

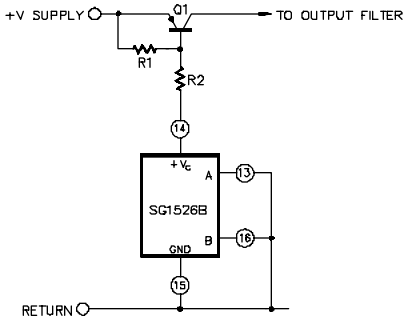


FIGURE 27.
SINGLE-ENDED CONFIGURATION

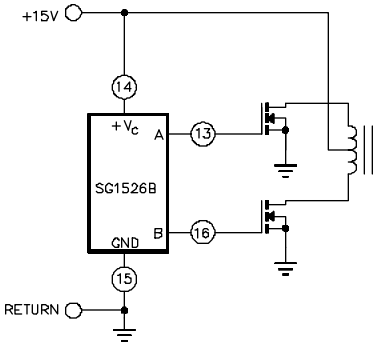
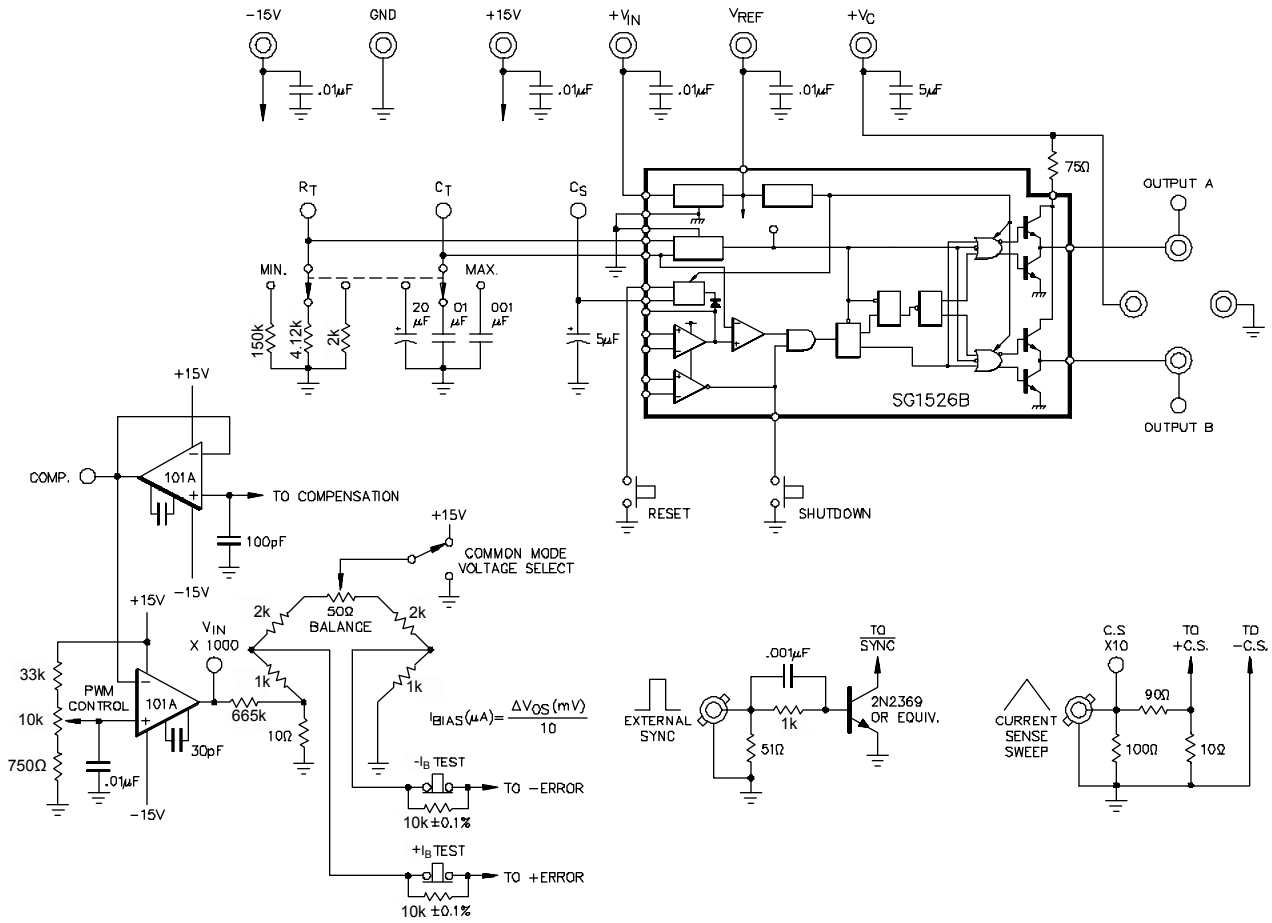
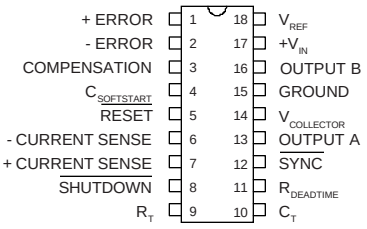
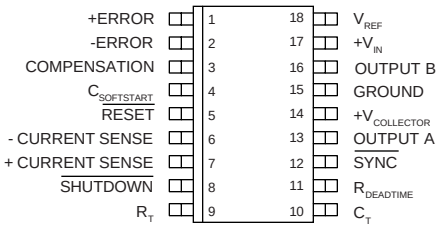
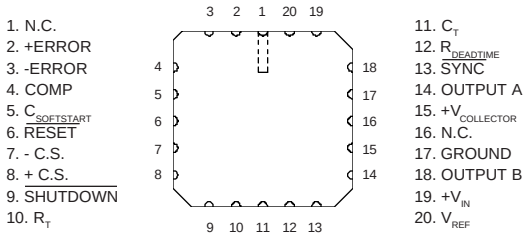


FIGURE 28.
DRIVING N-CHANNEL POWER MOSFETS

SG1526B LAB TEST FIXTURE



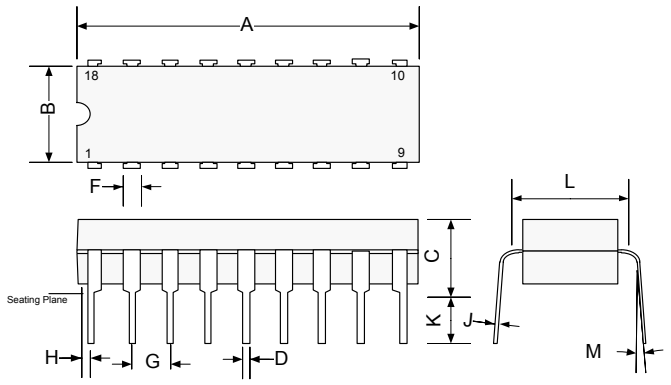
CONNECTION DIAGRAMS & ORDERING INFORMATION (See Notes Below)

Package	Part No.	Ambient Temperature Range	Connection Diagram
18-PIN CERAMIC DIP J - PACKAGE	SG1526BJ-883B SG1526BJ-JAN SG1526BJ-DESC SG1526BJ SG2526BJ SG3526BJ	-55°C to 125°C -55°C to 125°C -55°C to 125°C -55°C to 125°C -25°C to 85°C 0°C to 70°C	 N Package: RoHS Compliant / Pb-free Transition DC: 0503 N Package: RoHS / Pb-free 100% Matte Tin Lead Finish
18-PIN PLASTIC DIP N - PACKAGE	SG2526BN SG3526BN	-25°C to 85°C 0°C to 70°C	
18-PIN WIDE BODY PLASTIC SOIC DW - PACKAGE	SG2526BDW SG3526BDW	-25°C to 85°C 0°C to 70°C	 DW Package: RoHS Compliant / Pb-free Transition DC: 0516 DW Package: RoHS / Pb-free 100% Matte Tin Lead Finish
20-PIN CERAMIC LEADLESS CHIP CARRIER L- PACKAGE	SG1526BL-883B SG1526BL	-55°C to 125°C -55°C to 125°C	

Note 1. Contact factory for JAN and DESC product availability.
Note 2. All parts are viewed from the top.
Note 3. Hermetic Packages J and L use Pb37/SN63 hot solder lead finish, contact factory for availability of RoHS versions.

PACKAGE OUTLINE DIMENSIONS

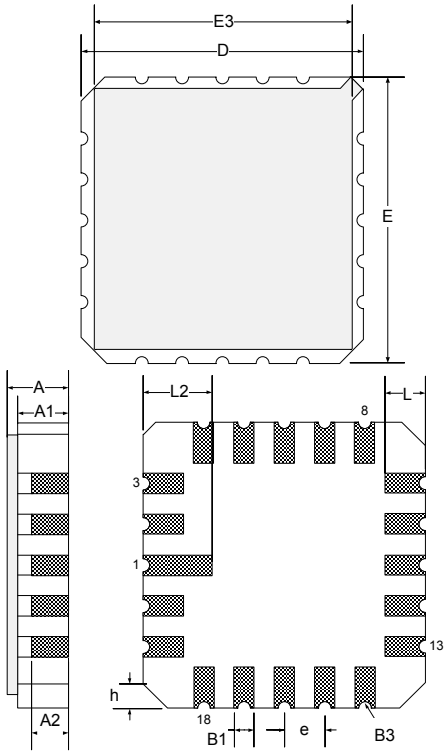
Controlling dimensions are in inches, metric equivalents are shown for general information.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	24.38	-	0.960
B	5.59	7.11	0.220	0.280
C	-	5.08	-	0.200
D	0.38	0.51	0.015	0.020
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	-	2.03	-	0.080
J	0.20	0.38	0.008	0.015
K	3.18	5.08	0.125	0.200
L	7.37	7.87	0.290	0.310
M	-	15°	-	15°

Note: Dimensions do not include protrusions; these shall not exceed 0.155mm (0.006″) on any side. Lead dimension shall not include solder coverage.

Figure 29 · J 18-Pin CERDIP Package Dimensions

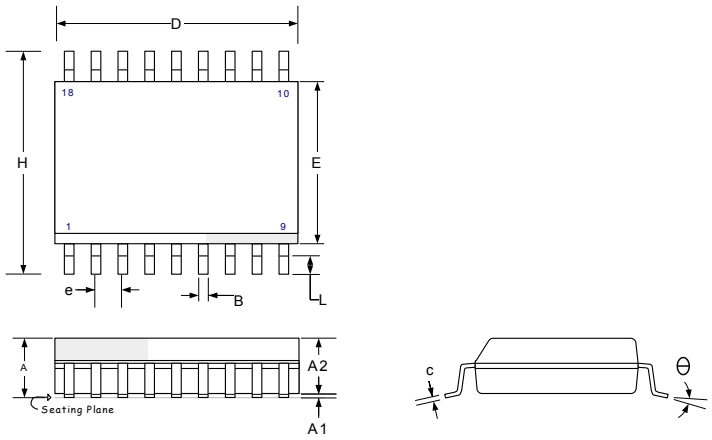


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
D/E	8.64	9.14	0.340	0.360
E3	-	8.128	-	0.320
e	1.270 BSC		0.050 BSC	
B1	0.635 TYP		0.025 TYP	
L	1.02	1.52	0.040	0.060
A	1.626	2.286	0.064	0.090
h	1.016 TYP		0.040 TYP	
A1	1.372	1.68	0.054	0.066
A2	-	1.168	-	0.046
L2	1.91	2.41	0.075	0.95
B3	0.203R		0.008R	

Note: All exposed metalized area shall be gold plated 60 µ-inch minimum thickness over nickel plated unless otherwise specified in purchase order.

Figure 30 · L 20-Pin Ceramic LCC Package Dimensions

PACKAGE OUTLINE DIMENSIONS (continued)

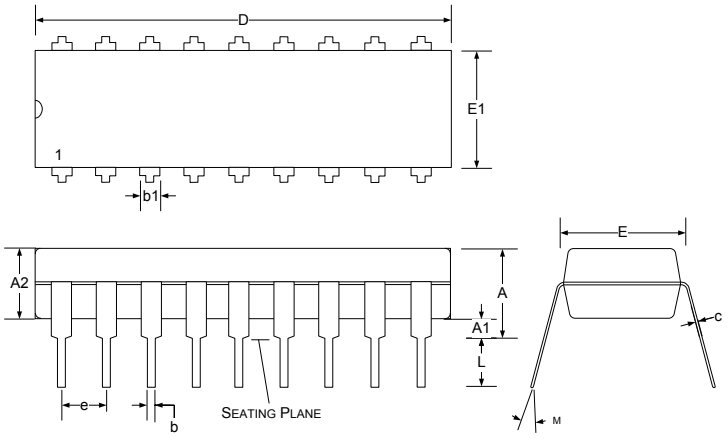


Dim	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
A2	2.20	2.55	0.086	0.100
B	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
D	11.40	11.70	0.449	0.461
E	7.40	7.60	0.291	0.299
e	1.27 BSC		0.05 BSC	
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
*LC	–	0.10	–	0.004

* Lead Coplanarity

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (0.006″) on any side. Lead dimension shall not include solder coverage.

Figure 31 · DW 18-Pin Plastic Wide-body SOIC (SOWB) Package Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		5.33		0.210
A1	0.38		0.015	
A2	3.30 Typ		0.130 Typ	
b	0.36	0.56	0.014	0.022
b1	1.14	1.78	0.045	0.070
c	0.20	0.36	0.008	0.014
D	22.35	23.34	0.880	0.920
e	2.54 BSC		0.100 BSC	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
L	2.92	3.81	0.115	0.150
M	-	15°	-	15°

Note: Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (0.006″) on any side. Lead dimension shall not include solder coverage.

Figure 32 · N 18-Pin Plastic Dual Inline Package Dimensions

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