CMOS 12-Bit Buffered Multiplying DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND .....-0.3V, +17V
Digital Input Voltage to DGND.....-0.3V, V_{DD} + 0.3V
V_{RFB}, V_{REF} to DGND .....±25V
OUT1 to DGND.....-0.3V, V_{DD} + 0.3V
AGND to DGND.....-0.3V, V_{DD} + 0.3V
Power Dissipation (Any Package) to +75°C 450mW
Derate Above +75°C by.....6mW/°C

Operating Temperature Ranges
MX7545AK/AL, MAX7645AC/BC .....0°C to +70°C
MX7545AB/AC/AKE, MAX7645AE/BE .....-40°C to +85°C
MX7545AT/AU, MAX7645AM/BM.....-55°C to +125°C
Storage Temperature .....-65°C to +150°C
Lead Temperature (Soldering, 10 sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MX7545A

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND. T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	Endpoint measurement				±1/2	LSB
Differential Non-Linearity	DNL	All grades guaranteed 12-bit monotonic over temperature range				±1	LSB
Gain Error	FSE	Measured using internal RFB; DAC register loaded with all 1s.	K,B,T T_A = +25°C			±3	LSB
			K,B,T T_A = T_{MIN} to T_{MAX}			±4	
			L,C,U T_A = +25°C			±1	
			L,C,U T_A = T_{MIN} to T_{MAX}			±2	
Gain Tempco ΔGain/ΔTemp. (Note 1)	TCFS				±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 1)	PSR	ΔV_{DD} = ±5%	T_A = +25°C			0.002	%/%
			T_A = T_{MIN} to T_{MAX}			0.004	
DYNAMIC PERFORMANCE							
Current Settling Time (Note 1)	t_S	To ±1/2 LSB. OUT1 load is 100Ω in parallel with 13pF. CS = 0V. DAC output measured from falling edge of WR.				1	µs
Propagation Delay (Notes 1, 2)	t_{PD}	From digital inputs, DB11-DB0, change to 90% of final analog output. OUT1 load is 100Ω in parallel with 13pF.	T_A = +25°C			200	ns
Digital to Analog Glitch Impulse (Notes 1, 2)		V_{REF} = AGND OUT1 load is 100Ω in parallel with 13pF.	T_A = +25°C		5		nV-s
AC Feedthrough at OUT1 (Notes 1, 3)	FTE	V_{REF} = ±10V, 10kHz sine wave, DB11-DB0 = 0V.			5		mVp-p
REFERENCE INPUT							
Input Resistance	R_{REF}	V_{REF} pin to AGND		10	15	20	kΩ
Input Resistance Tempco	TCR				-300		ppm/°C

ELECTRICAL CHARACTERISTICS—MX7545A (Continued)

(V_{DD} = +5V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND. T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG OUTPUTS							
OUT1 Capacitance (Note 1)	C_{OUT1}	DB11-DB0 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V			40 100	70 150	pF
OUT1 Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = 0V	All T_A = +25°C			10	nA
			K,B,L,C T_A = T_{MIN} to T_{MAX}			50	
			T,U T_A = T_{MIN} to T_{MAX}			200	
DIGITAL INPUTS							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	T_A = +25°C T_A = T_{MIN} to T_{MAX}		+0.001	±1 ±10	µA
Input Capacitance (Note 1)	C_{IN}	V_{IN} = 0V; DB11-DB0, $\overline{WR}$, $\overline{CS}$				8	pF
SWITCHING CHARACTERISTICS (Notes 1, 4)							
Chip Select to Write Setup Time	t_{CS}		All T_A = +25°C	100			ns
			K,B,L,C T_A = T_{MIN} to T_{MAX}	130			
			T, U T_A = T_{MIN} to T_{MAX}	170			
Chip Select to Write Hold Time	t_{CH}			0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	All T_A = +25°C	100			ns
			K,B,L,C T_A = T_{MIN} to T_{MAX}	130			
			T, U T_A = T_{MIN} to T_{MAX}	170			
Data Setup Time	t_{DS}		T_A = +25°C T_A = T_{MIN} to T_{MAX}	100 150			ns
Data Hold Time	t_{DH}			5			ns
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	±5% for specified performance			+5		V
Supply Current	I_{DD}	All digital inputs: V_{IL} or V_{IH} 0V or V_{DD}			 5	2 100	mA µA

Note 1: Sample tested to ensure compliance.
Note 2: DB11-DB0 changed from 0V to V_{DD} or V_{DD} to 0V.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: See timing diagram for definitions of the switching times.

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ELECTRICAL CHARACTERISTICS—MX7545A, MAX7645

(V_{DD} = +15V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND. T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	Endpoint measurement	MX7545A MAX7645A MAX7645B			±1/2 ±1/2 ±1	LSB
Differential Non-Linearity	DNL	All grades guaranteed 12-bit monotonic over temperature range				±1	LSB
Gain Error	FSE	Measured using internal RFB; DAC register loaded with all 1s.	K,B,T T_A = +25°C T_A = T_{MIN} to T_{MAX}			±3 ±4	LSB
			L,C,U T_A = +25°C T_A = T_{MIN} to T_{MAX}			±1 ±2	
Gain Tempco ΔGain/ΔTemp. (Note 1)	TCFS				±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 1)	PSR	ΔV_{DD} = ±5%	T_A = +25°C T_A = T_{MIN} to T_{MAX}			0.002 0.004	%/%
DYNAMIC PERFORMANCE							
Current Settling Time (Note 1)	t_S	To 1/2 LSB. OUT1 load is 100Ω in parallel with 13pF. $\overline{CS}$ = 0V. DAC output measured from falling edge of $\overline{WR}$.				1	µs
Propagation Delay (Notes 1, 2)	t_{PD}	From digital inputs, DB11-DB0, change to 90% of final analog output. OUT1 load is 100Ω in parallel with 13pF.	T_A = +25°C			150	ns
Digital to Analog Glitch Impulse (Notes 1, 2)	Q	V_{REF} = AGND OUT1 load is 100Ω in parallel with 13pF. Alternately loaded with all 0's and 1's.	T_A = +25°C		5		nV-s
AC Feedthrough at OUT1 (Notes 1, 3)	FTE	V_{REF} = ±10V, 10kHz sine wave, DB11-DB0 = 0V.			5		mVp-p
REFERENCE INPUT							
Input Resistance	R_{REF}	V_{REF} pin to AGND	MX7545A MAX7645	10 7	15 11	20 15	kΩ
Input Resistance Tempco	TCR				-300		ppm/°C
ANALOG OUTPUTS							
OUT1 Capacitance (Note 1)	C_{OUT1}	DB11-DB0 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V			40 100	70 150	pF pF
OUT1 Leakage Current	I_{LKG}	$\overline{WR}$ = $\overline{CS}$ = 0V DB11-DB0 = 0V	All T_A = +25°C			10	nA
			K,B,L,C T_A = T_{MIN} to T_{MAX}			50	
			T,U T_A = T_{MIN} to T_{MAX}			200	

ELECTRICAL CHARACTERISTICS—MX7545A, MAX7645 (Continued)

(V_{DD} = +15V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND. T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input High Voltage	V_{IH}		MX7545A MAX7645	13.5 2.4			V
Input Low Voltage	V_{IL}		MX7545A MAX7645			1.5 0.8	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	T_A = +25°C T_A = T_{MIN} to T_{MAX}		+0.001	±1 ±10	µA
Input Capacitance (Note 1)	C_{IN}	V_{IN} = 0V; DB11-DB0, $\overline{WR}$, $\overline{CS}$				8	pF
SWITCHING CHARACTERISTICS—MX7545A (Notes 1, 4)							
Chip Select to Write Setup Time	t_{CS}		All T_A = +25°C K,B,L,C T_A = T_{MIN} to T_{MAX} T,U T_A = T_{MIN} to T_{MAX}	75 85 95			ns
Chip Select to Write Hold Time	t_{CH}			0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	All T_A = +25°C K,B,L,C T_A = T_{MIN} to T_{MAX} T,U T_A = T_{MIN} to T_{MAX}	75 85 95			ns
Data Setup Time	t_{DS}		T_A = +25°C T_A = T_{MIN} to T_{MAX}	60 80			ns
Data Hold Time	t_{DH}			5			ns
SWITCHING CHARACTERISTICS—MAX7645 (Notes 1, 4)							
Chip Select to Write Setup Time	t_{CS}		T_A = +25°C T_A = T_{MIN} to T_{MAX}	150 210			ns
Chip Select to Write Hold Time	t_{CH}			0			ns
Write Pulse Width	t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$	T_A = +25°C T_A = T_{MIN} to T_{MAX}	150 210			ns
Data Setup Time	t_{DS}		T_A = +25°C T_A = T_{MIN} to T_{MAX}	225 300			ns
Data Hold Time	t_{DH}			10			ns
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	±5% for specified performance			+15		V
Supply Current	I_{DD}	All digital inputs:	V_{IL} or V_{IH} 0V or V_{DD}		5	2 100	mA µA

Note 1: Sample tested to ensure compliance.
Note 2: DB11-DB0 changed from 0V to V_{DD} or V_{DD} to 0V.
Note 3: In ceramic packages the feedthrough can be further reduced by grounding the metal lid of the package.
Note 4: See timing diagram for definitions of the switching times.

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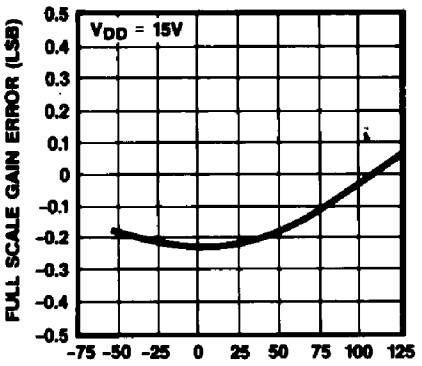
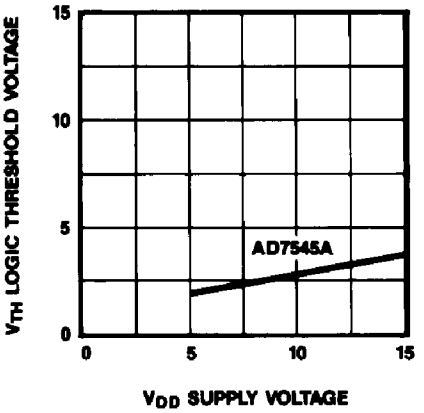
Typical Performance Characteristics

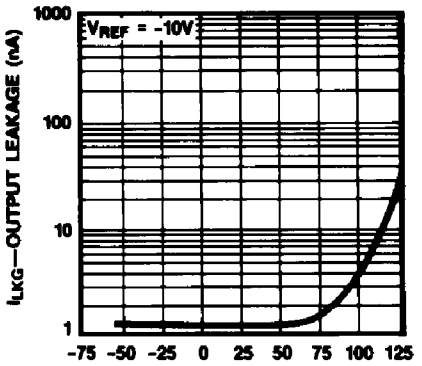
FULL SCALE GAIN ERROR vs TEMPERATURE



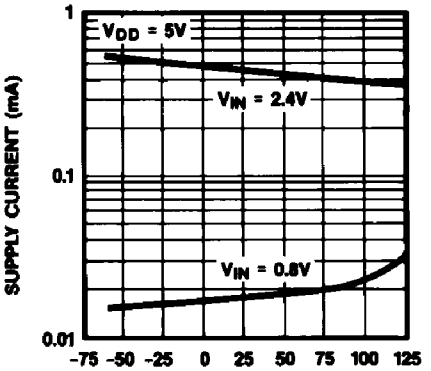
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



OUTPUT LEAKAGE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



Detailed Description

D/A Converter

The basic MX7545A/MAX7645 DAC circuit consists of a laser trimmed, thin-film R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or AGND depending on the status of each input data bit. Although the current at OUT1 and AGND depends on the digital input code, the sum of the two output currents are always equal to the input current at V_{REF}.

Either current output can be converted into a voltage by adding an external output amplifier (Figure 3). The V_{REF} input accepts a wide range of signals including fixed and time varying voltage or current inputs. If a current source is used for the reference input, then a low tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

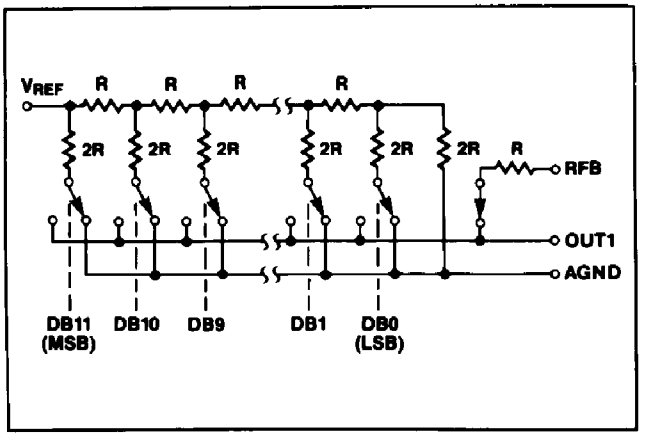


Figure 1. Simplified D/A Circuit of MX7545A/MAX7645

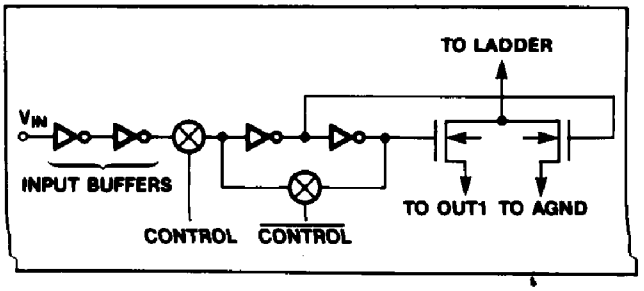


Figure 2. Digital Input Structure

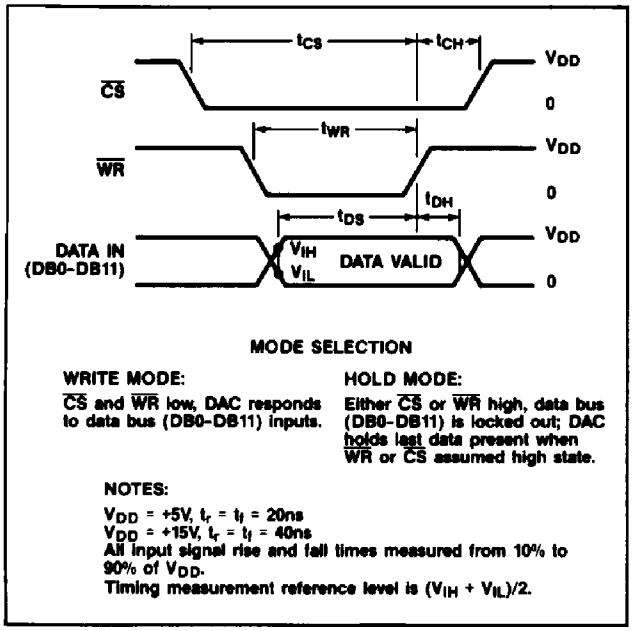
The internal feedback resistor R_{FB} is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent supply rejection and gain temperature coefficient.

The OUT1 pin output capacitance, C_{OUT1}, is code dependent and is typically 40pF with all switches to AGND and 100pF with all switches to OUT1.

Digital Circuit

The digital circuit for one bit is shown in Figure 2. The digital CONTROL signal is HIGH when $\overline{WR}$ and $\overline{CS}$ are both low. When $\overline{WR}$ and $\overline{CS}$ are tied low, the digital input directly controls the DAC switches.

The input buffer inverters act as level shifters converting TTL levels into CMOS logic levels. These input buffers are TTL compatible (0.8V and 2.4V) at V_{DD} = +5V for MX7545A, and V_{DD} = +15V for MAX7645. The MX7545A also works with V_{DD} = +15V where the input buffers are CMOS compatible (1.5V and 13.5V). When the digital input voltages are between 1V and 6V the input buffers operate in their linear regions drawing current from the power supply. Therefore to minimize high supply currents the digital input voltages should be kept as close to the supply and ground voltages (V_{DD} and DGND) as possible.



MODE SELECTION

WRITE MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.

HOLD MODE:
Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V, $t_r = t_f$ = 20ns
V_{DD} = +15V, $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Circuit Configurations

Unipolar Operation

The most common configuration for the MX7545A/MAX7645 is shown in Figure 3. This circuit is used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 1. Note that the polarity of the output is the inverse of the reference voltage, V_{REF}.

In many applications gain adjustment will not be necessary especially when using parts with maximum gain error of ±1LSB. In these cases, and when the gain is trimmed at the reference source, resistors R1 and R2 in Figure 3 can be omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, low tempco (<300ppm/°C) resistors should be used for R1 and R2.

The capacitor C1 provides phase compensation and helps reduce overshoot and ringing when fast amplifiers are used at the output of the DAC.

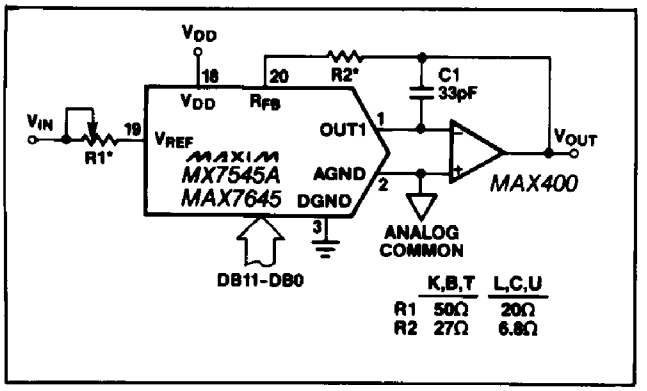


Figure 3. Unipolar Binary Operation

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{4095}{4096}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0 0 0 0 0 0 0 0 0 0 0 1	$-V_{IN}\left(\frac{1}{4096}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0

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Bipolar Operation

Figure 4 shows the MX7545A/MAX7645 operating in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors (R3, R4 and R5) are required. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature tracking characteristics, and should match to 0.01% for 12-bit performance. The output code is 2's complement and is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control amplitude. The U1 inverter on the MSB line converts the 2's complement input code to offset-binary code. If this inversion is done in software using an exclusive-OR instruction or the input code is in offset binary, the U1 inverter can be omitted. Table 3 shows the code relationships to output voltage for the offset binary operation.

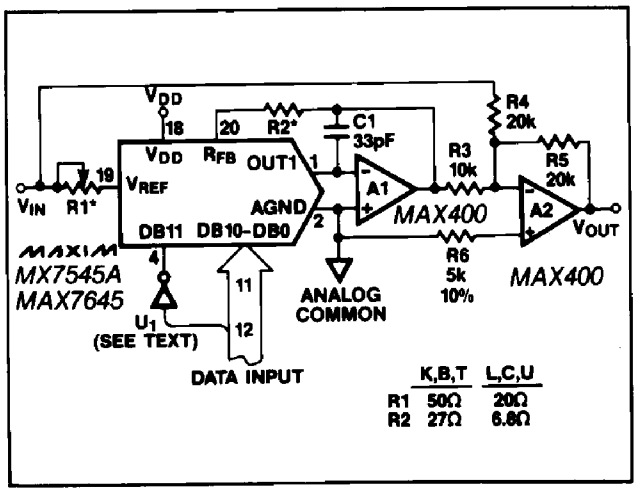

Figure 4. Bipolar Operation (2's Complement Code)

Table 2. 2's Complement Code Table for Circuit of Figure 4

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
0 1 1 1 1 1 1 1 1 1 1 1	$+V_{IN}\left(\frac{2047}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 1	$+V_{IN}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1	$-V_{IN}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	$-V_{IN}\left(\frac{2048}{2048}\right)$

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. In many applications the gain adjustment will not be necessary, especially when using the parts with guaranteed maximum ±1LSB gain errors. In those cases, the gain can be trimmed at the reference source and resistors R1 and R2 in Figure 4 omitted. However, if the trims are desired and the DAC is operated over a wide temperature range, then low tempco (<300ppm/°C) resistors should be used for R1 and R2.

(Voltage Mode) Single Supply

The MX7545A/MAX7645 can be conveniently used in single supply (voltage mode) operation with OUT1 and AGND biased at any voltage between DGND and V_{DD}. This is possible since the ladder termination resistor is connected to AGND. OUT1 and AGND must not be allowed to go 0.3V lower than the DGND or 0.3V higher than V_{DD}. Otherwise, internal diodes would turn on causing a high current flow from the supply which could possibly destroying the device.

Figure 5 shows the MX7545A/MAX7645 connected as a voltage output DAC. OUT1 is connected to the reference input and AGND is grounded. V_{REF} pin, now the DAC output, is a voltage source with a constant impedance equal to the reference input resistance. This output should be buffered with an op amp when a lower output impedance is required. R_{FB} pin is not used in this mode.

The input impedance of the reference input (OUT1) for this mode is code dependent, and the response time of the circuit depends on the behavior of the reference source with changing load conditions.

Table 3. Offset Binary Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{2047}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{2048}\right)$
1 0 0 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{2048}\right)$
0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{2048}{2048}\right)$

Two advantages of the voltage mode operation are single supply operation and that a negative reference is not required for a positive output. It should also be noted that the reference input (the voltage at OUT1) must always be positive and limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded linearity and differential nonlinearity (DNL). Figures 6 and 7 show the typical dependence of DNL on supply voltage, V_{DD}, and the reference voltage, V_{REF}. If the DAC is offset from DGND by biasing OUT1 and AGND at a voltage above DGND, this will effect DNL and its effect will be the same as reducing V_{DD} by the amount of the offset.

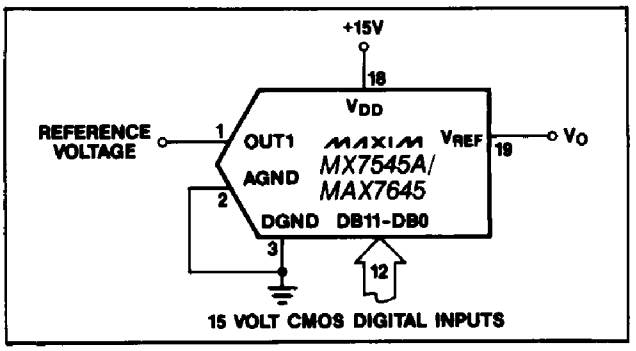

Figure 5. Single Supply Operation Using Voltage Switching Mode

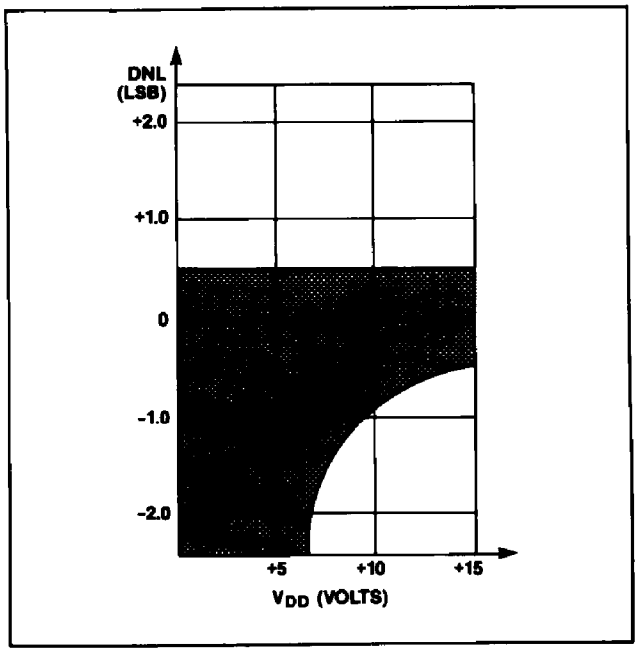

Figure 6. Differential Nonlinearity vs. V_{DD} for Figure 4 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode. Figure 8 shows the 2's complement bipolar circuit of Figure 4 modified to work with an output range of +2V to +8V around an offset ground potential of +5V from a single supply, V_{DD}, of +10V to +15V. The MAX673 reference is used to bias the AGND at +5V. Resistors R1 and R2 form a voltage divider together with the DAC reference

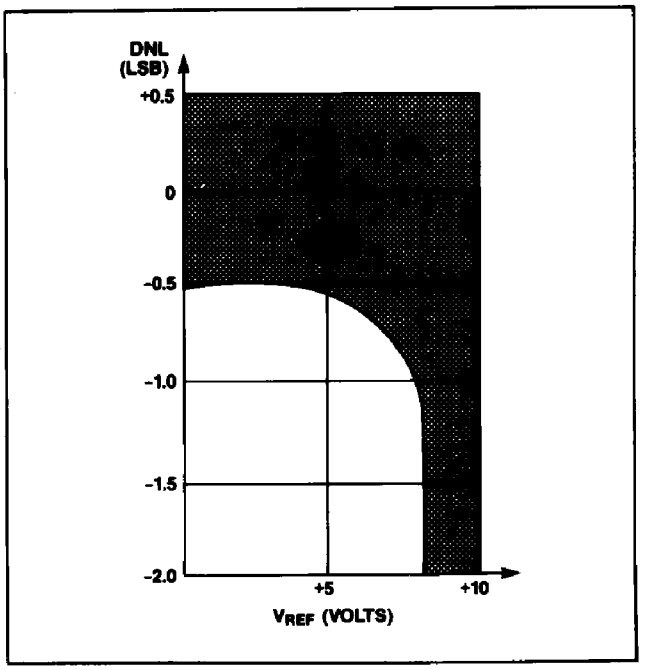

Figure 7. Differential Nonlinearity vs. Reference Voltage for Figure 4 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

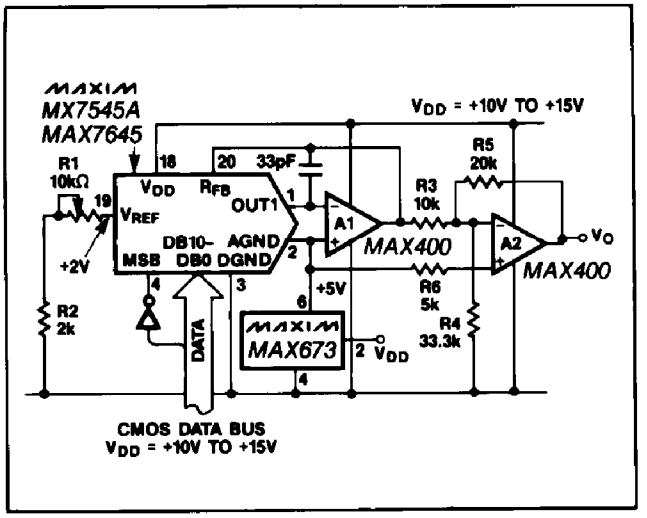

Figure 8. Single Supply "Bipolar" 2's Complement D/A Converter

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input resistor, supplying the DAC with +2V input voltage. If the application requires a wide temperature range, the +2V should be generated with an op amp to avoid drifts due to tempco matching of the DAC resistors to the external resistors. Output voltage ranges can be produced by changing R4 to change the offset, and (R1 + R2) to change the gain (slope) of the DAC transfer function. To ensure good linearity, the supply voltage, V_{DD}, must be kept at least +5V above the OUT1 voltage.

Microprocessor Interfacing

The MX7545A/MAX7645 directly interfaces to 8- and 16-bit microprocessors using standard $\overline{WR}$ and $\overline{CS}$ control signals and its 12-bit data latch.

Figure 9 shows a typical interface circuit for an 8-bit processor. This application uses two memory addresses for the lower 8-bits and the upper 4-bits of data to the DAC. A 4-bit external latch is required to implement the interface.

For processors with 16-bit wide address busses and 8-bit data busses, such as 6800, 8080 and Z80, the 12 lower address lines can be used to supply data to the DAC, as shown in Figure 10. The upper 4 bits contain the address of the DAC that is selected. This arrangement takes 4k bytes of address locations for each DAC and the data is written with a single instruction cycle.

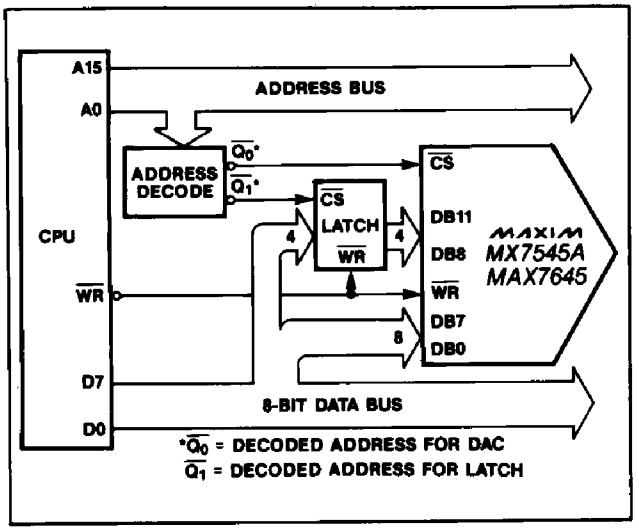


Figure 9. 8-Bit Processor to MX7545A/MAX7645 Interface

Application Information

Output Amplifier Offset

For best linearity, OUT1 and AGND should be terminated at exactly 0V. In most applications OUT1 is connected to the summing junction of an inverting op amp. The input offset voltage of the amplifier can degrade the linearity of the DAC by causing OUT1 to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\ (1 + R_{FB}/R)$$

where V_{OS} is the op amp's offset voltage and R_O is the output resistance of the DAC. R is a function of the digital input code, and varies from approximately 11kohms to 33kohms. The error voltage range is then typically 4/3 V_{OS} to 2 V_{OS}, a change of 2/3 V_{OS}. An amplifier with 3mV of offset will therefore degrade the

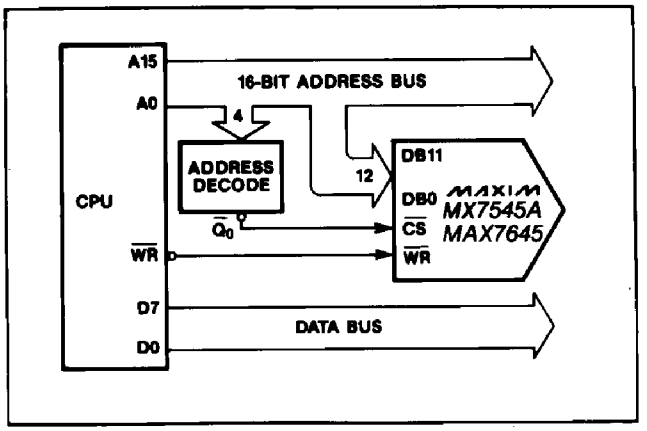


Figure 10. Connecting the MX7545A/MAX7645 to 8-Bit Processors via the Address Bus

linearity by 2mV, almost a full LSB with a 10V reference voltage. For best linearity, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to zero. A good rule of thumb is that V_{OS} should be no more than 1/10 LSB.

The output amplifier input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error. I_B should therefore be much less than the DAC output current for 1LSB, typically 250nA with V_{REF} = 10V. One tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias current compensation resistor". This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to ground.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} pin to OUT1. This normally is a function of board layout and lead-to-lead capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and OUT1 pins.

The DAC output follows the digital inputs when the $\overline{WR}$ and $\overline{CS}$ pins are low. In systems where the data is not valid for the full period when $\overline{WR}$ is low, invalid

outputs and voltage glitches can appear at the DAC output. Adjusting the timing of the $\overline{WR}$ signal so that it is low only when data valid can eliminate this problem.

Compensation

A compensation capacitor, C1, may be required when the DAC is used with a high speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance C_{OUT1} and the internal feedback resistor, R_{FB}. Its value depends on the type of op amp used but typically ranges from 10pF to 33pF. Too small a value causes output ringing while excess capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit board trace and stray capacitance at OUT1 as low as possible.

Grounding and Bypassing

Since OUT1, AGND and noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to "single point" ground through a separate, low resistance (less than 0.2 ohms) connection. The current at OUT1 and AGND varies with input code, creating a code dependent error if these terminals are connected to ground (or a "virtual ground") through a resistive path.

A 1μF bypass capacitor, in parallel with a 0.01μF ceramic capacitor, should be connected across the DAC V_{DD} and DGND as close to the pins as possible.

The MX7545A/MAX7645 has high-impedance digital inputs. To minimize noise pick-up, they should be tied to either V_{DD} or DGND when not used. It is good practice to connect active inputs to V_{DD} or DGND through high valued resistors (1Mohms) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected. It is also recommended that two back-to-back diodes be connected between the DGND and AGND pins in systems where these pins tie on the backplane.

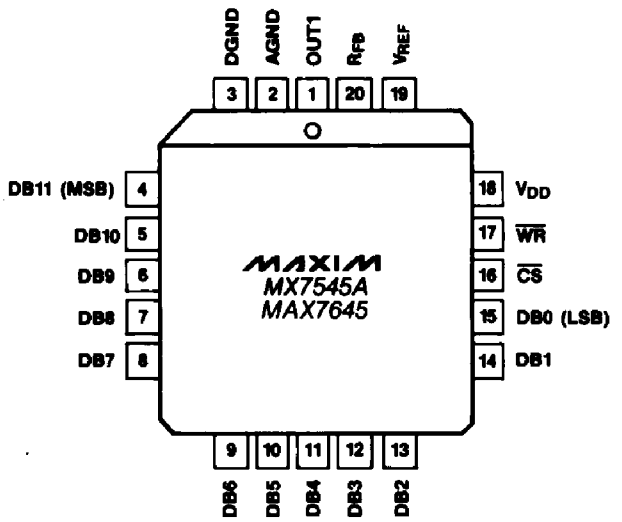
Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE	GAIN ERROR
MAX7645ACPP	0°C to +70°C	Plastic DIP	±1 LSB
MAX7645BCPP	0°C to +70°C	Plastic DIP	±3 LSB
MAX7645ACWP	0°C to +70°C	Wide SO	±1 LSB
MAX7645BCWP	0°C to +70°C	Wide SO	±3 LSB
MAX7645B/D	0°C to +70°C	Dice	±3 LSB
MAX7645ACQP	0°C to +70°C	PLCC	±1 LSB
MAX7645BCQP	0°C to +70°C	PLCC	±3 LSB
MAX7645AEJP	-40°C to +85°C	CERDIP	±1 LSB
MAX7645BEJP	-40°C to +85°C	CERDIP	±3 LSB
MAX7645AMJP	-55°C to +125°C	CERDIP	±1 LSB
MAX7645BMJP	-55°C to +125°C	CERDIP	±3 LSB

Maxim reserves the right to ship ceramic packages in lieu of CERDIP packages.

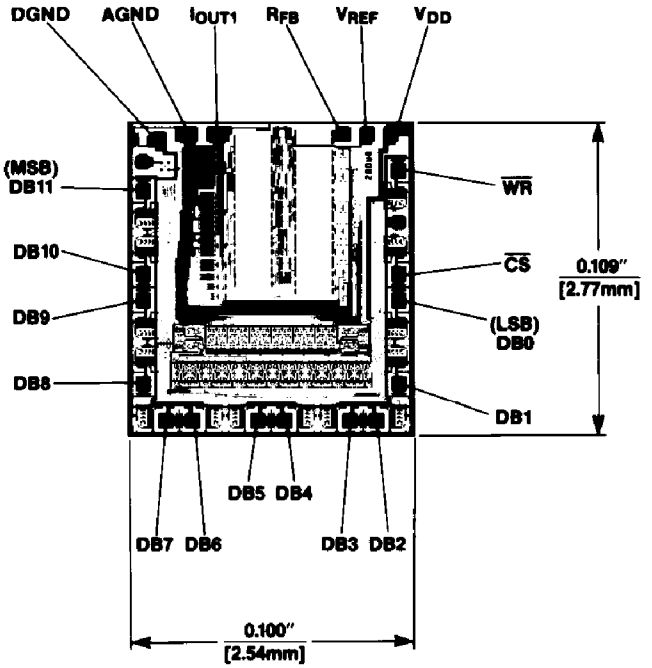
Pin Configuration (continued)

Top View



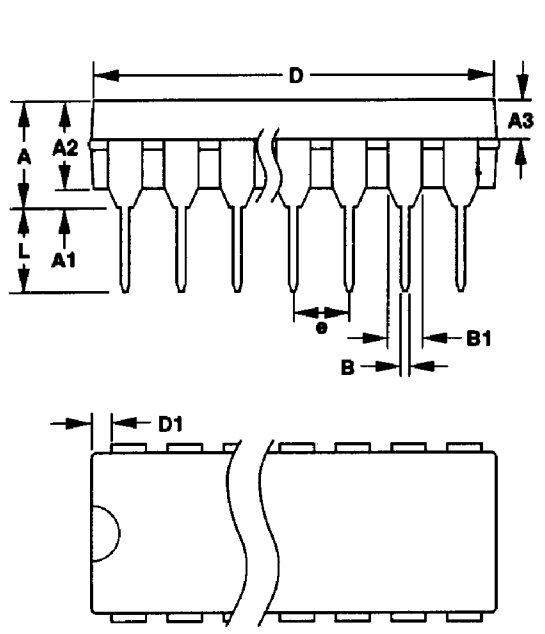
20 Lead Plastic Chip Carrier (Quad Pak)

Chip Topography



CMOS 12-Bit Buffered Multiplying DACs

Package Information

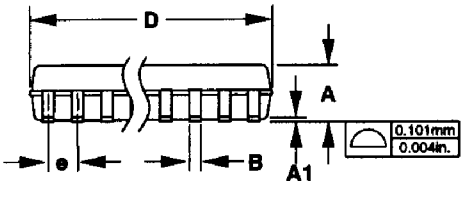


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

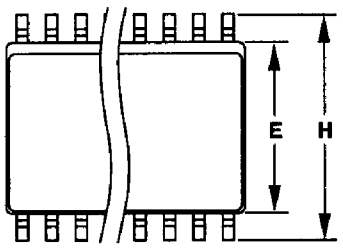
Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



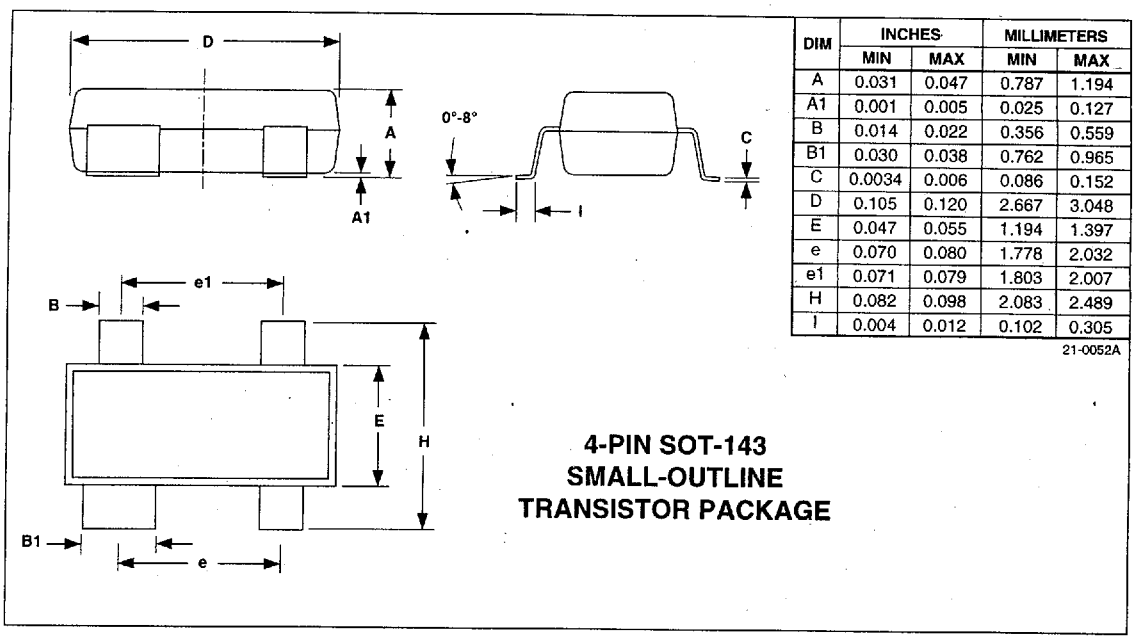
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27



Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

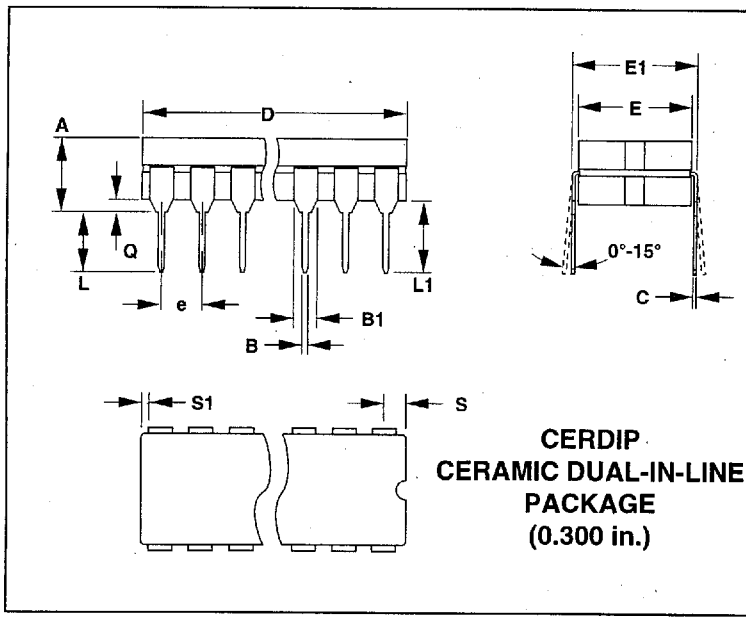
21-0042A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
B1	0.030	0.038	0.762	0.965
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e	0.070	0.080	1.778	2.032
e1	0.071	0.079	1.803	2.007
H	0.082	0.098	2.083	2.489
l	0.004	0.012	0.102	0.305

21-0052A

4-PIN SOT-143
SMALL-OUTLINE
TRANSISTOR PACKAGE

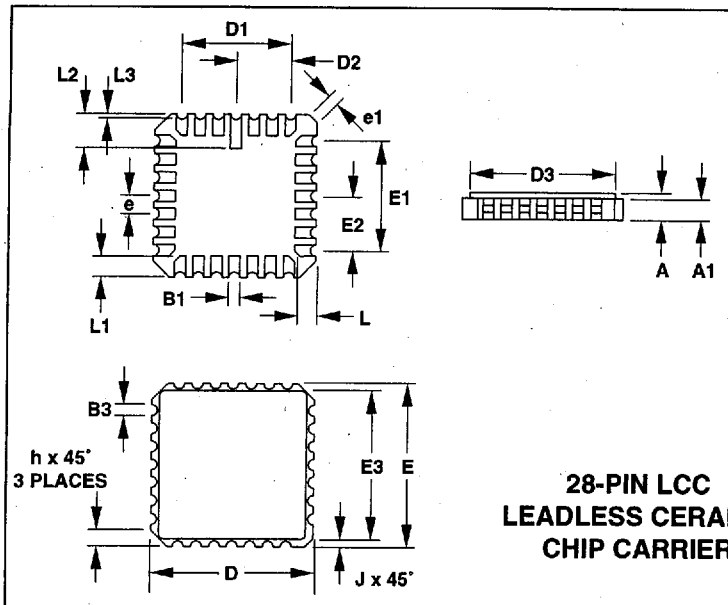


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

21-0045A

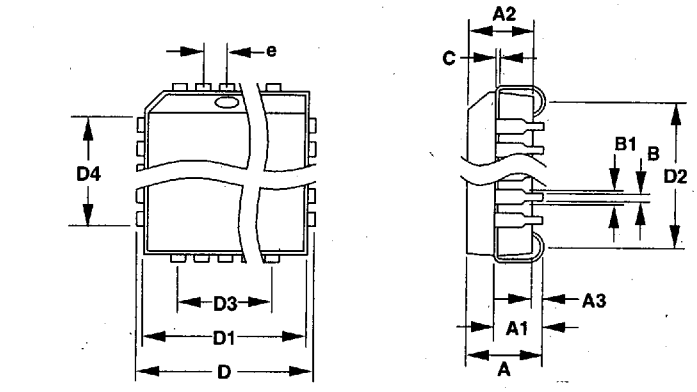
CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.442	0.460	11.23	11.68
D1/E1	0.300		7.62	
D2/E2	0.150		3.81	
D3/E3	–	0.460	–	11.68
e	0.050		1.27	
e1	0.015	–	0.38	–
h	0.040 REF		1.02 REF	
J	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

21-4497A

28-PIN LCC
LEADLESS CERAMIC
CHIP CARRIER



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	20	0.385	0.395	9.78	10.03
D1		0.350	0.356	8.89	9.04
D2		0.290	0.330	7.37	8.38
D3		0.200 REF		5.08 REF	
D	28	0.485	0.495	12.32	12.57
D1		0.450	0.456	11.43	11.58
D2		0.390	0.430	9.91	10.92
D3		0.300 REF		7.62 REF	
D4		0.300	–	7.62	–
D	44	0.685	0.695	17.40	17.65
D1		0.650	0.656	16.51	16.66
D2		0.590	0.630	14.99	16.00
D3		0.500 REF		12.70 REF	
D4		0.470	–	11.94	–
D	68	0.985	0.995	25.02	25.27
D1		0.950	0.958	24.13	24.33
D2		0.890	0.930	22.61	23.62
D3		0.800 REF		20.32 REF	
D4		0.625	–	15.87	–

21-0049B

PLCC
PLASTIC
LEADED CHIP CARRIER