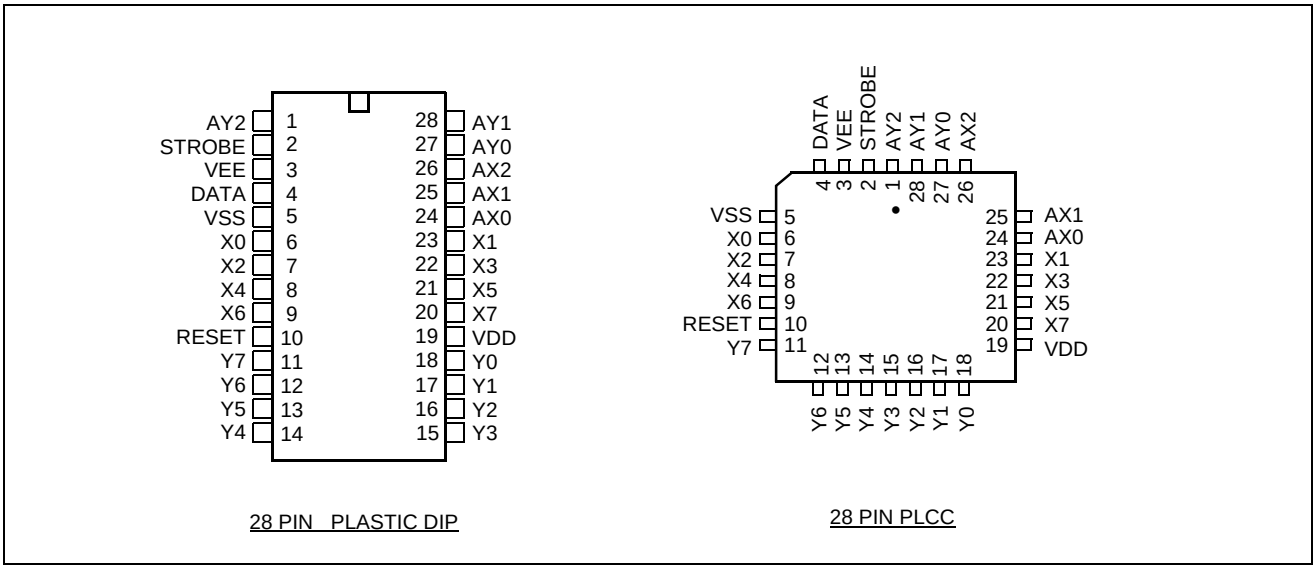



**Figure 2 - Pin Connections**

## Change Summary

Changes from the May 2005 issue to the September 2011 issue.

| Page | Item | Change |
|---|---|---|
| 1 | Ordering Information | Removed leaded packages as per PCN notice. |

### Pin Description

| Pin # | Name | Description |
|---|---|---|
| 1 | AY2 | **AY2 Address Line (Input)**. |
| 2 | STROBE | **STROBE (Input)**: enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High. |
| 3 | $V_{EE}$ | **Negative Power Supply.** |
| 4 | DATA | **DATA (Input)**: a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High. |
| 5 | $V_{SS}$ | **Digital Ground Reference.** |
| 6-9 | X0, X2, X4, X6 | **X0, X2, X4 and X6 Analog (Inputs/Outputs):** these are connected to the X0, X2, X4 and X6 rows of the switch array. |
| 10 | RESET | **Master RESET (Input):** this is used to turn off all switches. Active High. |
| 11-18 | Y7 - Y0 | **Y7 - Y0 Analog (Inputs/Outputs):** these are connected to the Y0 - Y7 columns of the switch array. |
| 19 | $V_{DD}$ | **Positive Power Supply.** |

**Pin Description**

| Pin # | Name | Description |
|---|---|---|
| 20-23 | X7, X5, X3, X1 | **X7, X5, X3 and X1 Analog (Inputs/Outputs):** these are connected to the X7, X5, X3 and X1 rows of the switch array. |
| 24-26 | AX0-AX2 | **AX0 - AX2 Address Lines (Inputs)**. |
| 27,28 | AY0, AY1 | **AY0 and AY1 Address Lines (Inputs)**. |

## Functional Description

The MT8808 is an analog switch matrix with an array size of 8 x 8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical “1” written into a memory cell turns the corresponding crosspoint switch on and a logical “0” turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical “1” on the RESET input will asynchronously return all memory locations to logical “0” turning off all crosspoint switches. Two voltage reference pins ($V_{SS}$ and $V_{EE}$) are provided for the MT8808 to enable switching of negative analog signals. The range for digital signals is from $V_{DD}$ to $V_{SS}$ while the range for analog signals is from $V_{DD}$ to $V_{EE}$. $V_{SS}$ and $V_{EE}$ pins can be tied together if a single voltage reference is needed.

## Address Decode

The six address inputs along with the STROBE are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

**Absolute Maximum Ratings*** - Voltages are with respect to $V_{EE}$ unless otherwise stated.

| | Parameter | Symbol | Min. | Max. | Units |
|---|---|---|---|---|---|
| 1 | Supply Voltage | $V_{DD}$<br>$V_{SS}$ | -0.3<br>-0.3 | 15.0<br>$V_{DD}$+0.3 | V<br>V |
| 2 | Analog Input Voltage | $V_{INA}$ | -0.3 | $V_{DD}$+0.3 | V |
| 3 | Digital Input Voltage | $V_{IN}$ | $V_{SS}$-0.3 | $V_{DD}$+0.3 | V |
| 4 | Current on any I/O Pin | I | | ±15 | mA |
| 5 | Storage Temperature | $T_S$ | -65 | +150 | °C |
| 6 | Package Power Dissipation PLASTIC DIP | $P_D$ | | 0.6 | W |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

**Recommended Operating Conditions** - Voltages are with respect to $V_{EE}$ unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Operating Temperature | $T_O$ | -40 | 25 | 85 | °C | |
| 2 | Supply Voltage | $V_{DD}$<br>$V_{SS}$ | 4.5<br>$V_{EE}$ | | 13.2<br>$V_{DD}$-4.5 | V<br>V | |
| 3 | Analog Input Voltage | $V_{INA}$ | $V_{EE}$ | | $V_{DD}$ | V | |
| 4 | Digital Input Voltage | $V_{IN}$ | $V_{SS}$ | | $V_{DD}$ | V | |

**DC Electrical Characteristics**† - Voltages are with respect to $V_{EE} = V_{SS} = 0$ V, $V_{DD} = 12$ V unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ.‡ | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Quiescent Supply Current | $I_{DD}$ | | 1 | 100 | µA | All digital inputs at $V_{IN} = V_{SS}$ or $V_{DD}$ |
| | | | | 0.4 | 1.5 | mA | All digital inputs at $V_{IN} = 2.4 + V_{SS}$ ; $V_{SS} = 7.0$ V |
| | | | | 5 | 15 | mA | All digital inputs at $V_{IN} = 3.4$ V |
| 2 | Off-state Leakage Current (See G.9 in Appendix) | $I_{OFF}$ | | ±1 | ±500 | nA | $IV_{Xi} - V_{Yj}I = V_{DD} - V_{EE}$<br>See Appendix, Fig. A.1 |
| 3 | Input Logic “0” level | $V_{IL}$ | | | 0.8+$V_{SS}$ | V | $V_{SS} = 7.5$ V; $V_{EE} = 0$ V |
| 4 | Input Logic “1” level | $V_{IH}$ | 2.0+$V_{SS}$ | | | V | $V_{SS} = 6.5$V; $V_{EE} = 0$ V |
| 5 | Input Logic “1” level | $V_{IH}$ | 3.3 | | | V | |
| 6 | Input Leakage (digital pins) | $I_{LEAK}$ | | 0.1 | 10 | µA | All digital inputs at $V_{IN} = V_{SS}$ or $V_{DD}$ |

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

**DC Electrical Characteristics- Switch Resistance** - $V_{DC}$ is the external DC offset applied at the analog I/O pins.

| | Characteristics | Sym. | 25°C | | 70°C | | 85°C | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Typ. | Max. | Typ. | Max. | Typ. | Max. | | |
| 1 | On-state $V_{DD}$ = 12 V<br>Resistance $V_{DD}$ = 10 V<br>$V_{DD}$ = 5 V<br>(See G.1, G.2, G.3 in Appendix) | $R_{ON}$ | 45<br>55<br>120 | 65<br>75<br>185 | | 75<br>85<br>215 | | 80<br>90<br>225 | Ω<br>Ω<br>Ω | $V_{SS}$=$V_{EE}$ = 0 V,$V_{DC}$ = $V_{DD}$/2, $IV_{Xi}$-$V_{Yj}$I = 0.4 V<br>See Appendix, Fig. A.2 |
| 2 | Difference in on-state resistance between two switches<br>(See G.4 in Appendix) | $\Delta R_{ON}$ | 5 | 10 | | 10 | | 10 | Ω | $V_{DD}$=12V, $V_{SS}$=$V_{EE}$=0, $V_{DC}$=$V_{DD}$/2, $IV_{Xi}$-$V_{Yj}$I = 0.4V<br>See Appendix, Fig. A.2 |

**AC Electrical Characteristics**† **- Crosspoint Performance**-Voltages are with respect to $V_{DD}$=5V, $V_{SS}$=0V, $V_{EE}$=-7V, unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ.‡ | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Switch I/O Capacitance | $C_S$ | | 20 | | pF | f = 1 MHz |
| 2 | Feedthrough Capacitance | $C_F$ | | 0.2 | | pF | f = 1 MHz |
| 3 | Frequency Response Channel “ON” 20LOG($V_{OUT}$/$V_{Xi}$)=-3 dB | $F_{3dB}$ | | 45 | | MHz | Switch is “ON”; $V_{INA}$ = 2 Vpp sinewave; $R_L$ = 1 kΩ<br>See Appendix, Fig. A.3 |
| 4 | Total Harmonic Distortion<br>(See G.5, G.6 in Appendix) | THD | | 0.01 | | % | Switch is “ON”; $V_{INA}$ = 2 Vpp sinewave f = 1kHz; $R_L$=1 kΩ |
| 5 | Feedthrough Channel “OFF” Feed.=20LOG ($V_{OUT}$/$V_{Xi}$)<br>(See G.8 in Appendix) | FDT | | -95 | | dB | All Switches “OFF”; $V_{INA}$= 2Vpp sinewave f = 1 kHz; $R_L$ = 1 kΩ.<br>See Appendix, Fig. A.4 |
| 6 | Crosstalk between any two channels for switches Xi-Yi and Xj-Yj.<br><br>Xtalk=20LOG ($V_{Yj}$/$V_{Xi}$).<br><br>(See G.7 in Appendix). | $X_{talk}$ | | -45 | | dB | $V_{INA}$ = 2 Vpp sinewave f = 10 MHz; $R_L$ = 75 Ω. |
| | | | | -90 | | dB | $V_{INA}$ = 2 Vpp sinewave f = 10 kHz; $R_L$ = 600 Ω. |
| | | | | -85 | | dB | $V_{INA}$ = 2 Vpp sinewave f = 10kHz; $R_L$ = 1 kΩ. |
| | | | | -80 | | dB | $V_{INA}$=2Vpp sinewave f = 1 kHz; $R_L$ = 10 kΩ.<br>Refer to Appendix, Fig. A.5 for test circuit. |
| 7 | Propagation delay through switch | $t_{PS}$ | | | 30 | ns | $R_L$ = 1 kΩ; $C_L$ = 50 pF |

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5 dB better.

**AC Electrical Characteristics† - Control and I/O Timings**- Voltages are with respect to $V_{DD}$=5V, $V_{SS}$=0V, $V_{EE}$=-7V, unless otherwise stated.

| | Characteristics | Sym. | Min. | Typ.‡ | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| 1 | Control Input crosstalk to switch (for CS, DATA, STROBE, Address) | $CX_{talk}$ | | 30 | | mVpp | $V_{IN}$ = 3 V squarewave; $R_{IN}$ = 1 kΩ, $R_L$ = 10 kΩ. See Appendix, Fig. A.6 |
| 2 | Digital Input Capacitance | $C_{DI}$ | | 10 | | pF | f = 1 MHz |
| 3 | Switching Frequency | $F_O$ | | | 20 | MHz | |
| 4 | Setup Time DATA to STROBE | $t_{DS}$ | 10 | | | ns | $R_L$ = 1 kΩ, $C_L$= 50 pF Å |
| 5 | Hold Time DATA to STROBE | $t_{DH}$ | 10 | | | ns | $R_L$ = 1 kΩ, $C_L$=50 pF Å |
| 6 | Setup Time Address to STROBE | $t_{AS}$ | 10 | | | ns | $R_L$= 1 kΩ, $C_L$=50 pF Å |
| 7 | Hold Time Address to STROBE | $t_{AH}$ | 10 | | | ns | $R_L$= 1 kΩ, $C_L$= 50 pF Å |
| 8 | STROBE Pulse Width | $t_{SPW}$ | 20 | | | ns | $R_L$ = 1 kΩ, $C_L$ = 50 pF Å |
| 9 | RESET Pulse Width | $t_{RPW}$ | 40 | | | ns | $R_L$ = 1 kΩ, $C_L$= 50 pF Å |
| 10 | STROBE to Switch Status Delay | $t_S$ | | 40 | 100 | ns | $R_L$ = 1 kΩ, $C_L$ = 50 pF Å |
| 11 | DATA to Switch Status Delay | $t_D$ | | 50 | 100 | ns | $R_L$ = 1 kΩ, $C_L$ = 50 pF Å |
| 12 | RESET to Switch Status Delay | $t_R$ | | 35 | 100 | ns | $R_L$ = 1 kΩ, $C_L$ = 50 pF Å |

† Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5 ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Å Refer to Appendix, Fig. A.7 for test circuit.

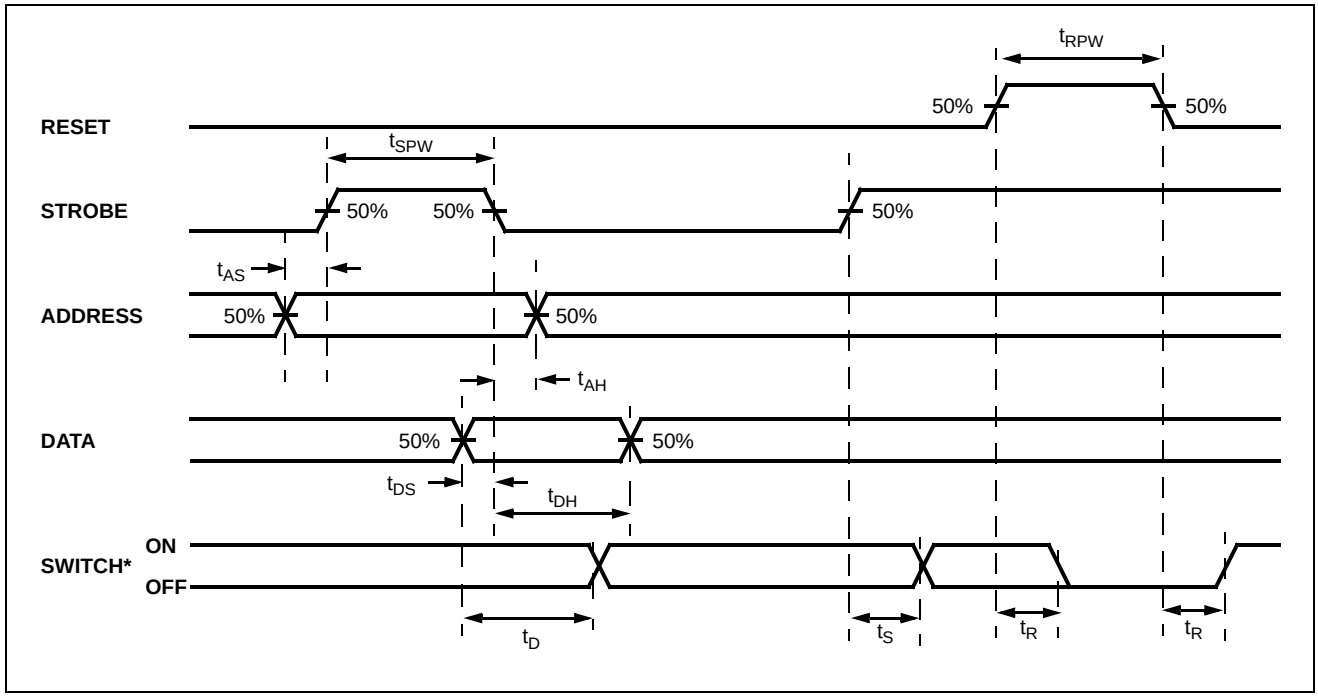
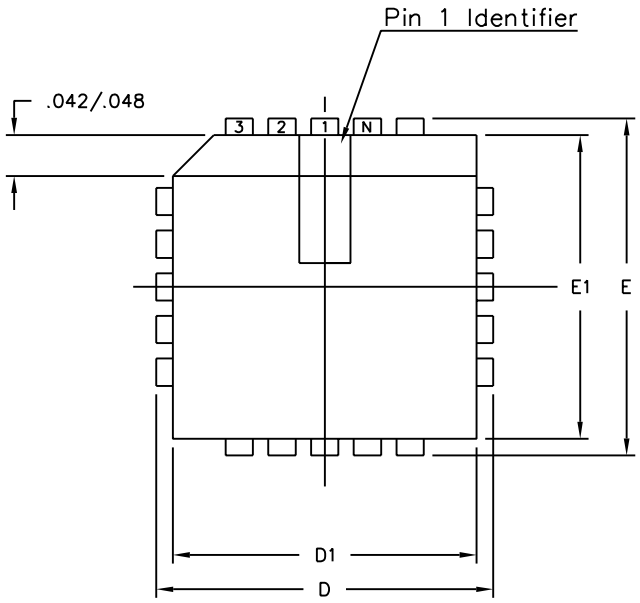


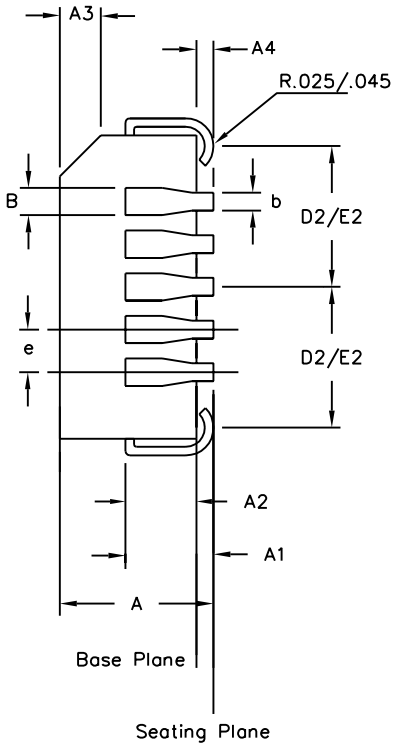

**Figure 3 - Control Memory Timing Diagram**

* See Appendix, Fig. A.7 for switching waveform

| AY2 | AY1 | AY0 | AX2 | AX1 | AX0 | Connection | AY2 | AY1 | AY0 | AX2 | AX1 | AX0 | Connection |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | X0 Y0 | 1 | 0 | 0 | 0 | 0 | 0 | X0 Y4 |
| 0 | 0 | 0 | 0 | 0 | 1 | X1 Y0 | 1 | 0 | 0 | 0 | 0 | 1 | X1 Y4 |
| 0 | 0 | 0 | 0 | 1 | 0 | X2 Y0 | 1 | 0 | 0 | 0 | 1 | 0 | X2 Y4 |
| 0 | 0 | 0 | 0 | 1 | 1 | X3 Y0 | 1 | 0 | 0 | 0 | 1 | 1 | X3 Y4 |
| 0 | 0 | 0 | 1 | 0 | 0 | X4 Y0 | 1 | 0 | 0 | 1 | 0 | 0 | X4 Y4 |
| 0 | 0 | 0 | 1 | 0 | 1 | X5 Y0 | 1 | 0 | 0 | 1 | 0 | 1 | X5 Y4 |
| 0 | 0 | 0 | 1 | 1 | 0 | X6 Y0 | 1 | 0 | 0 | 1 | 1 | 0 | X6 Y4 |
| 0 | 0 | 0 | 1 | 1 | 1 | X7 Y0 | 1 | 0 | 0 | 1 | 1 | 1 | X7 Y4 |
| 0 | 0 | 1 | 0 | 0 | 0 | X0 Y1 | 1 | 0 | 1 | 0 | 0 | 0 | X0 Y5 |
| 0 | 0 | 1 | 0 | 0 | 1 | X1 Y1 | 1 | 0 | 1 | 0 | 0 | 1 | X1 Y5 |
| 0 | 0 | 1 | 0 | 1 | 0 | X2 Y1 | 1 | 0 | 1 | 0 | 1 | 0 | X2 Y5 |
| 0 | 0 | 1 | 0 | 1 | 1 | X3 Y1 | 1 | 0 | 1 | 0 | 1 | 1 | X3 Y5 |
| 0 | 0 | 1 | 1 | 0 | 0 | X4 Y1 | 1 | 0 | 1 | 1 | 0 | 0 | X4 Y5 |
| 0 | 0 | 1 | 1 | 0 | 1 | X5 Y1 | 1 | 0 | 1 | 1 | 0 | 1 | X5 Y5 |
| 0 | 0 | 1 | 1 | 1 | 0 | X6 Y1 | 1 | 0 | 1 | 1 | 1 | 0 | X6 Y5 |
| 0 | 0 | 1 | 1 | 1 | 1 | X7 Y1 | 1 | 0 | 1 | 1 | 1 | 1 | X7 Y5 |
| 0 | 1 | 0 | 0 | 0 | 0 | X0 Y2 | 1 | 1 | 0 | 0 | 0 | 0 | X0 Y6 |
| 0 | 1 | 0 | 0 | 0 | 1 | X1 Y2 | 1 | 1 | 0 | 0 | 0 | 1 | X1 Y6 |
| 0 | 1 | 0 | 0 | 1 | 0 | X2 Y2 | 1 | 1 | 0 | 0 | 1 | 0 | X2 Y6 |
| 0 | 1 | 0 | 0 | 1 | 1 | X3 Y2 | 1 | 1 | 0 | 0 | 1 | 1 | X3 Y6 |
| 0 | 1 | 0 | 1 | 0 | 0 | X4 Y2 | 1 | 1 | 0 | 1 | 0 | 0 | X4 Y6 |
| 0 | 1 | 0 | 1 | 0 | 1 | X5 Y2 | 1 | 1 | 0 | 1 | 0 | 1 | X5 Y6 |
| 0 | 1 | 0 | 1 | 1 | 0 | X6 Y2 | 1 | 1 | 0 | 1 | 1 | 0 | X6 Y6 |
| 0 | 1 | 0 | 1 | 1 | 1 | X7 Y2 | 1 | 1 | 0 | 1 | 1 | 1 | X7 Y6 |
| 0 | 1 | 1 | 0 | 0 | 0 | X0 Y3 | 1 | 1 | 1 | 0 | 0 | 0 | X0 Y7 |
| 0 | 1 | 1 | 0 | 0 | 1 | X1 Y3 | 1 | 1 | 1 | 0 | 0 | 1 | X1 Y7 |
| 0 | 1 | 1 | 0 | 1 | 0 | X2 Y3 | 1 | 1 | 1 | 0 | 1 | 0 | X2 Y7 |
| 0 | 1 | 1 | 0 | 1 | 1 | X3 Y3 | 1 | 1 | 1 | 0 | 1 | 1 | X3 Y7 |
| 0 | 1 | 1 | 1 | 0 | 0 | X4 Y3 | 1 | 1 | 1 | 1 | 0 | 0 | X4 Y7 |
| 0 | 1 | 1 | 1 | 0 | 1 | X5 Y3 | 1 | 1 | 1 | 1 | 0 | 1 | X5 Y7 |
| 0 | 1 | 1 | 1 | 1 | 0 | X6 Y3 | 1 | 1 | 1 | 1 | 1 | 0 | X6 Y7 |
| 0 | 1 | 1 | 1 | 1 | 1 | X7 Y3 | 1 | 1 | 1 | 1 | 1 | 1 | X7 Y7 |

**Table 1 - Address Decode Truth Table**




| Symbol | Control Dimensions in inches | | Altern. Dimensions in millimetres | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.165 | 0.180 | 4.19 | 4.57 |
| A1 | 0.090 | 0.120 | 2.29 | 3.05 |
| A2 | 0.062 | 0.083 | 1.57 | 2.11 |
| A3 | 0.042 | 0.056 | 1.07 | 1.42 |
| A4 | 0.020 | – | 0.51 | – |
| D | 0.485 | 0.495 | 12.32 | 12.57 |
| D1 | 0.450 | 0.456 | 11.43 | 11.58 |
| D2 | 0.191 | 0.219 | 4.85 | 5.56 |
| E | 0.485 | 0.495 | 12.32 | 12.57 |
| E1 | 0.450 | 0.456 | 11.43 | 11.58 |
| E2 | 0.191 | 0.219 | 4.85 | 5.56 |
| B | 0.026 | 0.032 | 0.66 | 0.81 |
| b | 0.013 | 0.021 | 0.33 | 0.53 |
| e | 0.050 BSC | | 1.27 BSC | |
| | Pin features | | | |
| ND | 7 | | | |
| NE | 7 | | | |
| N | 28 | | | |
| Note | Square | | | |
| Conforms to JEDEC MS-018AB Iss. A | | | | |

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.



| ISSUE | 1 | 2 | 3 | |
|---|---|---|---|---|
| ACN | 5958 | 207469 | 212422 | |
| DATE | 15Aug94 | 10Sep99 | 22Mar02 | |
| APPRD. | | | | |

ZARLINK SEMICONDUCTOR

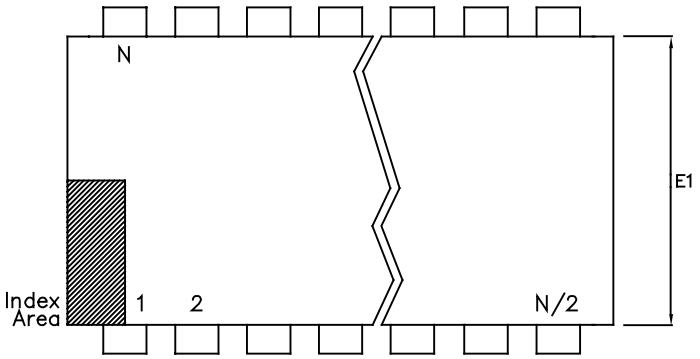
Previous package codes

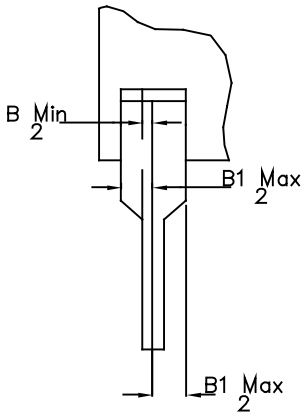
HP / P

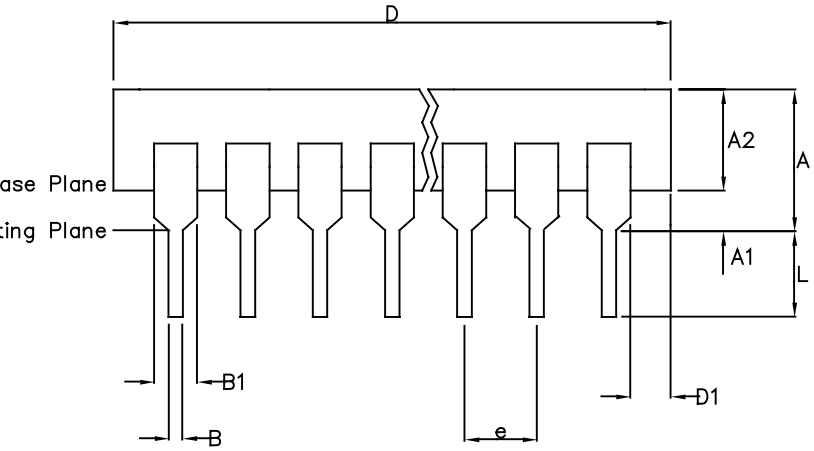
Package Code QA

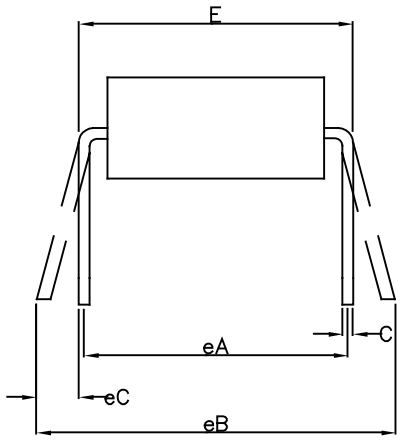
# Package Outline for 28 lead PLCC

GPD00002




| | Min mm | Max mm | Min Inches | Max Inches |
|---|---|---|---|---|
| A | | 6.35 | | 0.250 |
| A1 | 0.38 | | 0.015 | |
| A2 | 3.18 | 4.95 | 0.125 | 0.195 |
| B | 0.36 | 0.56 | 0.014 | 0.022 |
| B1 | 0.76 | 1.78 | 0.030 | 0.070 |
| C | 0.20 | 0.38 | 0.008 | 0.015 |
| D | 35.05 | 39.75 | 1.380 | 1.565 |
| D1 | 0.13 | | 0.005 | |
| E | 15.24 | 15.88 | 0.600 | 0.625 |
| E1 | 12.32 | 14.73 | 0.485 | 0.580 |
| e | 2.54 BSC | | 0.100 BSC | |
| eA | 15.24 BSC | | 0.600 BSC | |
| eB | | 17.78 | | 0.700 |
| L | 2.92 | 5.08 | 0.115 | 0.200 |
| N | 28 | | 28 | |
| Conforms to Jedec MS-011AB ISS.B | | | | |

tes:
Controlling Dimensions are in inches
Dimension A, A1 and L are measured with the package seated in the Seating Plane
Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.



| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| | 7010 | 203532 | 213102 | CDCA |
| | 20Apr95 | 25Nov97 | 15Jul02 | 02Dec05 |
| . | | | | |

ZARLINK SEMICONDUCTOR

Previous package codes

DP / E

Package Code DA

Package Outline for
28 lead 600mils PDIP

GPD00072

**For more information about all Zarlink products visit our Web Site at**

**www.zarlink.com**