■ FEATURES

Feature	Description
Technology	• 0.18µm CMOS
CPU	• F²MC-16FX CPU • Up to 56 MHz internal, 17.8 ns instruction cycle time • Optimized instruction set for controller applications (bit, byte, word and long-word data types; 23 different addressing modes; barrel shift; variety of pointers) • 8-byte instruction execution queue • Signed multiply (16-bit × 16-bit) and divide (32-bit/16-bit) instructions available
System clock	• On-chip PLL clock multiplier (x1 - x25, x1 when PLL stop) • 3 MHz - 16 MHz external crystal oscillator clock (maximum frequency when using ceramic resonator depends on Q-factor). • Up to 56 MHz external clock • 32-100 kHz subsystem quartz clock • 100kHz/2MHz internal RC clock for quick and safe startup, oscillator stop detection, watchdog • Clock source selectable from main- and subclock oscillator (part number suffix “W”) and on-chip RC oscillator, independently for CPU and 2 clock domains of peripherals. • Low Power Consumption - 13 operating modes : (different Run, Sleep, Timer modes, Stop mode) • Clock modulator
On-chip voltage regulator	• Internal voltage regulator supports reduced internal MCU voltage, offering low EMI and low power consumption figures
Low voltage reset	• Reset is generated when supply voltage is below minimum.
Code Security	• Protects ROM content from unintended read-out
Memory Patch Function	• Replaces ROM content • Can also be used to implement embedded debug support
DMA	• Automatic transfer function independent of CPU, can be assigned freely to resources
Interrupts	• Fast Interrupt processing • 8 programmable priority levels • Non-Maskable Interrupt (NMI)
Timers	• Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer) • Watchdog Timer

Feature	Description
CAN	• Supports CAN protocol version 2.0 part A and B • ISO16845 certified • Bit rates up to 1 Mbit/s • 32 message objects • Each message object has its own identifier mask • Programmable FIFO mode (concatenation of message objects) • Maskable interrupt • Disabled Automatic Retransmission mode for Time Triggered CAN applications • Programmable loop-back mode for self-test operation
USART	• Full duplex USARTs (SCI/LIN) • Wide range of baud rate settings using a dedicated reload timer • Special synchronous options for adapting to different synchronous serial protocols • LIN functionality working either as master or slave LIN device
I^2C	• Up to 400 kbps • Master and Slave functionality, 8-bit and 10-bit addressing
A/D converter	• SAR-type • 10-bit resolution • Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger or reload timer
Reload Timers	• 16-bit wide • Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency • Event count function
Free Running Timers	• Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4), Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$,$1/2^8$ of peripheral clock frequency
Input Capture Units	• 16-bit wide • Signals an interrupt upon external event • Rising edge, falling edge or rising & falling edge sensitive
Output Compare Units	• 16-bit wide • Signals an interrupt when a match with 16-bit I/O Timer occurs • A pair of compare registers can be used to generate an output signal.
Programmable Pulse Generator	• 16-bit down counter, cycle and duty setting registers • Interrupt at trigger, counter borrow and/or duty match • PWM operation and one-shot operation • Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock and Reload timer overflow as clock input • Can be triggered by software or reload timer

Feature	Description
Real Time Clock	• Can be clocked either from sub oscillator (devices with part number suffix “W”), main oscillator or from the RC oscillator • Facility to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration) • Read/write accessible second/minute/hour registers • Can signal interrupts every half second/second/minute/hour/day • Internal clock divider and prescaler provide exact 1s clock
External Interrupts	• Edge sensitive or level sensitive • Interrupt mask and pending bit per channel • Each available CAN channel RX has an external interrupt for wake-up • Selected USART channels SIN have an external interrupt for wake-up
Non Maskable Interrupt	• Disabled after reset • Once enabled, can not be disabled other than by reset. • Level high or level low sensitive • Pin shared with external interrupt 0.
External bus interface	• 8-bit or 16-bit bidirectional data • Up to 24-bit addresses • 6 chip select signals • Multiplexed address/data lines • Wait state request • External bus master possible • Timing programmable
I/O Ports	• Virtually all external pins can be used as general purpose I/O • All push-pull outputs (except when used as I2C SDA/SCL line) • Bit-wise programmable as input/output or peripheral signal • Bit-wise programmable input enable • Bit-wise programmable input levels: Automotive / CMOS-Schmitt trigger / TTL • Bit-wise programmable pull-up resistor • Bit-wise programmable output driving strength for EMI optimization
Packages	• 64-pin plastic LQFP M23/M24

Feature	Description
Flash Memory	• Supports automatic programming, Embedded Algorithm • Write/Erase/Erase-Suspend/Resume commands • A flag indicating completion of the algorithm • Number of erase cycles: 10,000 times • Data retention time: 20 years • Erase can be performed on each sector individually • Sector protection • Flash Security feature to protect the content of the Flash • Low voltage detection during Flash erase

■ PRODUCT LINEUP

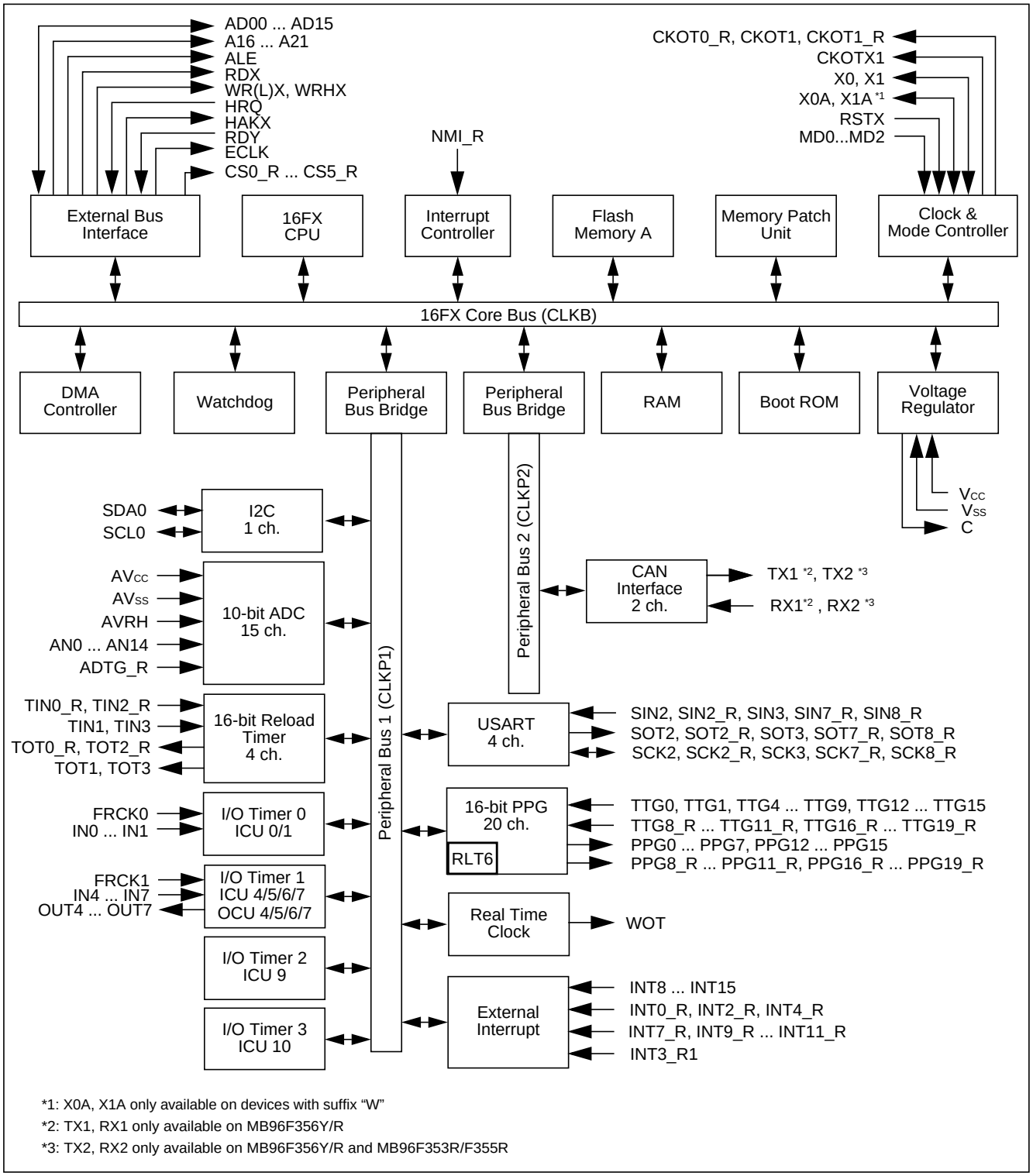
Features		MB96V300B	MB96(F)35x
Product type		Evaluation sample	Flash product: MB96F35x Mask ROM product: MB9635x
Product options			
YS		NA	Low voltage reset persistently on / Single clock devices
RS			Low voltage reset can be disabled / Single clock devices
YW			Low voltage reset persistently on / Dual clock devices
RW			Low voltage reset can be disabled / Dual clock devices
AS			No CAN / Low voltage reset can be disabled / Single clock devices
AW			No CAN / Low voltage reset can be disabled / Dual clock devices
Flash/ ROM	RAM		
96KB	8KB	ROM/Flash memory emulation by external RAM, 92KB internal RAM	MB96F353R, MB96F353A *1
160KB	8KB		MB96F355R, MB96F355A *1
288KB	12KB		MB96F356Y, MB96F356R, MB96F356A
Package		BGA416	FPT-64P-M23/24
DMA		16 channels	4 channels
USART		10 channels	4 channels
I2C		2 channels	1 channel
A/D Converter		40 channels	15 channels
A/D Converter Reference Voltage switch		yes	No
16-bit Reload Timer		6 channels + 1 channel (for PPG)	4 channels + 1 channel (for PPG)
16-bit Free-Running Timer		4 channels	4 channels (2 channels with external clock input pin)
16-bit Output Compare		12 channels	4 channels
16-bit Input Capture		12 channels	6 channels (plus 2 channels for LIN USART)
16-bit Programmable Pulse Generator		20 channels	20 channels
CAN Interface		5 channels	MB96F35xA: no MB96F353R/F355R: 1 channel MB96F356Y/R: 2 channels
External Interrupts		16 channels	13 channels
Non-Maskable Interrupt		1 channel	

Features	MB96V300B	MB96(F)35x
Real Time Clock	1	
I/O Ports	136	49 for part number with suffix "W", 51 for part number with suffix "S"
External bus interface	Yes	
Chip select	6 signals	
Clock output function	2 channels	
Low voltage reset	Yes	
On-chip RC-oscillator	Yes	

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

■ BLOCK DIAGRAM

Block diagram of MB96(F)35x



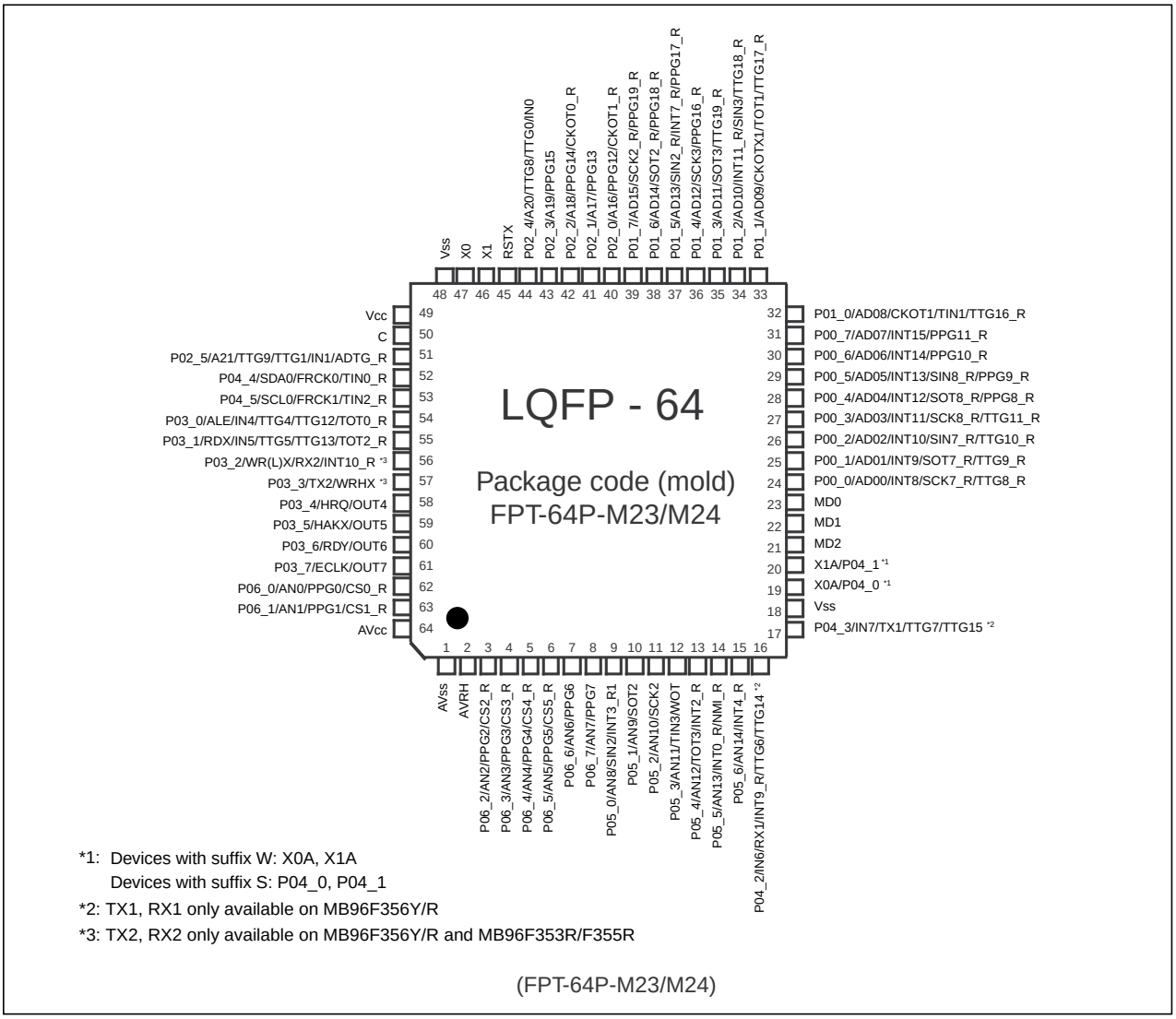
*1: X0A, X1A only available on devices with suffix “W”

*2: TX1, RX1 only available on MB96F356Y/R

*3: TX2, RX2 only available on MB96F356Y/R and MB96F353R/F355R

■ PIN ASSIGNMENTS

Pin assignment of MB96(F)35x



*1: Devices with suffix W: X0A, X1A
Devices with suffix S: P04_0, P04_1

*2: TX1, RX1 only available on MB96F356Y/R

*3: TX2, RX2 only available on MB96F356Y/R and MB96F353R/F355R

(FPT-64P-M23/M24)

Remark:

MB96(F)35x products are pin-compatible to F²MC-16LX family MB90350 series.

■ PIN FUNCTION DESCRIPTION

Pin Function description (1 of 2)

Pin name	Feature	Description
ADn	External bus	External bus interface (multiplexed mode) address output and data input/output
ADTG_R	ADC	Relocated A/D converter trigger input
ALE	External bus	External bus Address Latch Enable output
An	External bus	External bus address output
ANn	ADC	A/D converter channel n input
AV_{CC}	Supply	Analog circuits power supply
AVRH	ADC	A/D converter high reference voltage input
AV_{SS}	Supply	Analog circuits power supply
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock output function	Clock Output function n output
CKOTn_R	Clock output function	Relocated Clock Output function n output
CKOTXn	Clock output function	Clock Output function n inverted output
ECLK	External bus	External bus clock output
CSn_R	External bus	Relocated External bus chip select n output
FRCKn	Free Running Timer	Free Running Timer n input
HAKX	External bus	External bus Hold Acknowledge
HRQ	External bus	External bus Hold Request
INn	ICU	Input Capture Unit n input
INTn	External Interrupt	External Interrupt n input
INTn_R	External Interrupt	Relocated External Interrupt n input
MDn	Core	Input pins for specifying the operating mode.
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input
OUTn	OCU	Output Compare Unit n waveform output
Pxx_n	GPIO	General purpose IO
PPGn	PPG	Programmable Pulse Generator n output
PPGn_R	PPG	Relocated Programmable Pulse Generator n output
RDX	External bus	External bus interface read strobe output
RDY	External bus	External bus interface external wait state request input

Pin Function description (2 of 2)

Pin name	Feature	Description
RSTX	Core	Reset input
RXn	CAN	CAN interface n RX input
SCKn	USART	USART n serial clock input/output
SCKn_R	USART	Relocated USART n serial clock input/output
SCLn	I2C	I2C interface n clock I/O input/output
SDAn	I2C	I2C interface n serial data I/O input/output
SINn	USART	USART n serial data input
SINn_R	USART	Relocated USART n serial data input
SOTn	USART	USART n serial data output
SOTn_R	USART	Relocated USART n serial data output
TINn	Reload Timer	Reload Timer n event input
TINn_R	Reload Timer	Relocated Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TOTn_R	Reload Timer	Relocated Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TTGn_R	PPG	Relocated Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
V_{CC}	Supply	Power supply
V_{SS}	Supply	Power supply
WOT	RTC	Real Timer clock output
WRHX	External bus	External bus High byte write strobe output
WRLX/WRX	External bus	External bus Low byte / Word write strobe output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input (only for devices with suffix "W")
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output (only for devices with suffix "W")

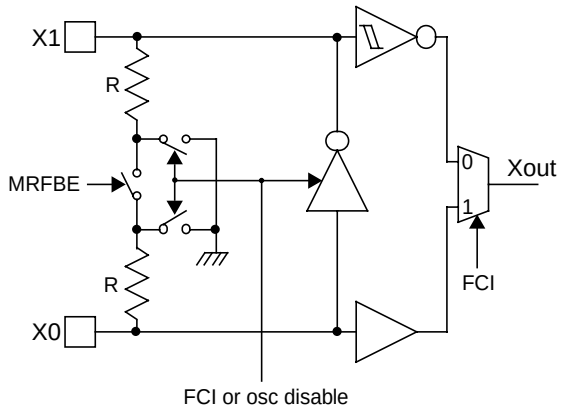
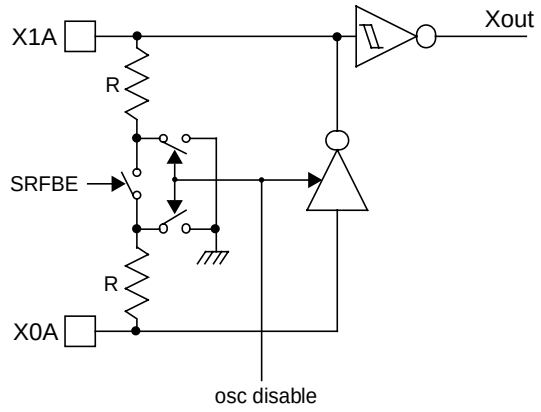
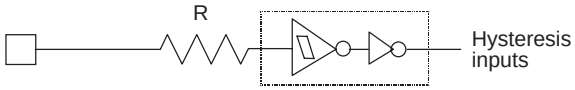
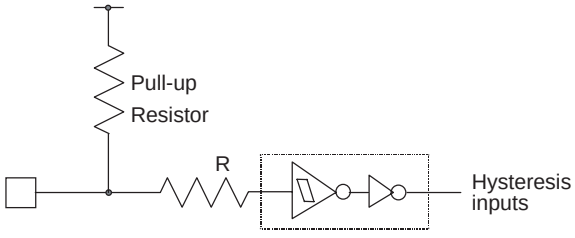
■ PIN CIRCUIT TYPE

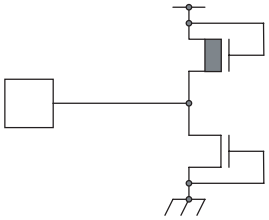
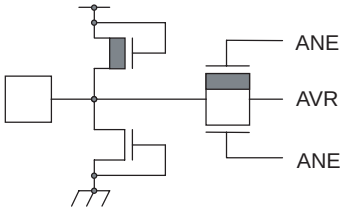
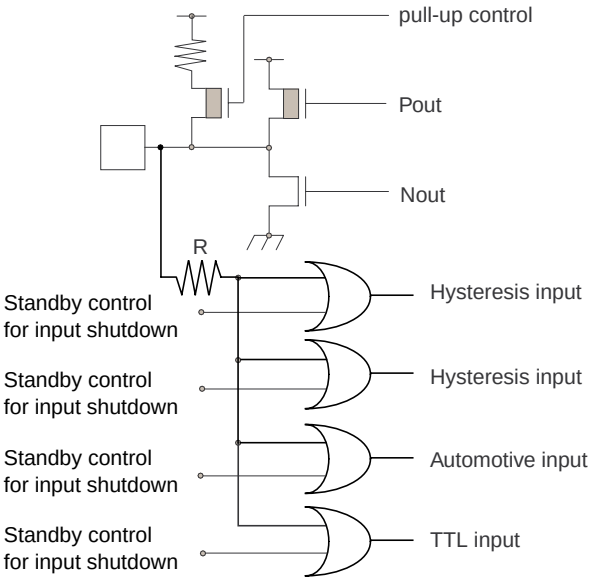
Pin circuit types

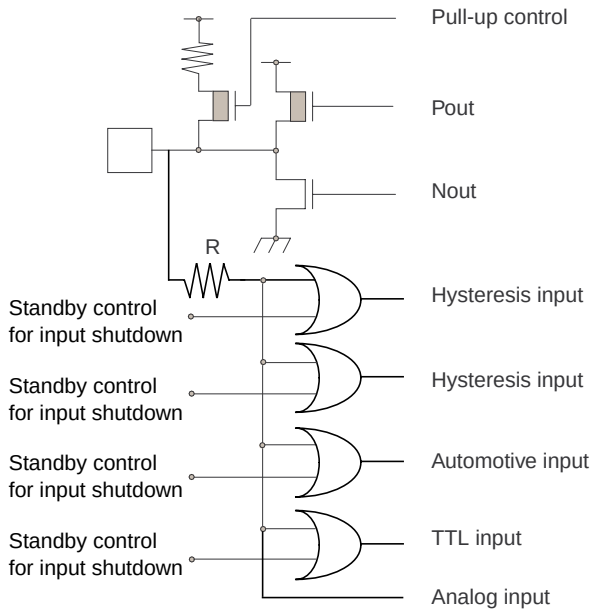
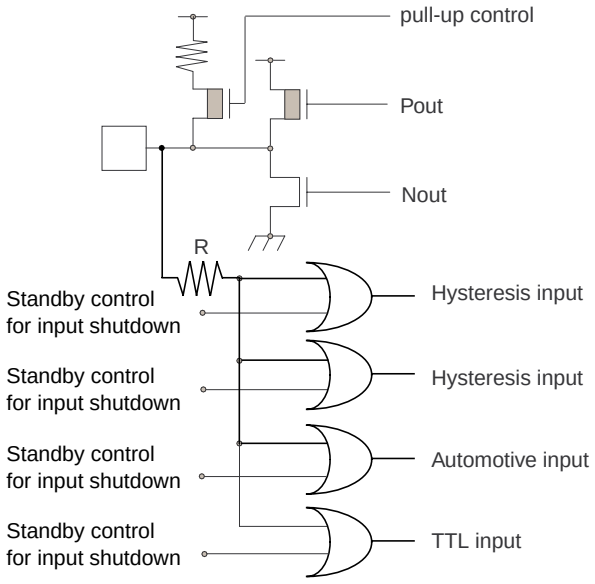
FPT-64P-M23/24	
Pin no.	Circuit type *1
1	Supply
2	G
3 to 15	I
16,17	H
18	Supply
19,20	B *2
19,20	H *3
21 to 23	C
24 to 44	H
45	E
46,47	A
48,49	Supply
50	F
51	H
52,53	N
54 to 61	H
62,63	I
64	Supply

*1: Please refer to “■ I/O CIRCUIT TYPE” for details on the I/O circuit types
*2: Devices with suffix ”W”
*3: Devices without suffix ”W”

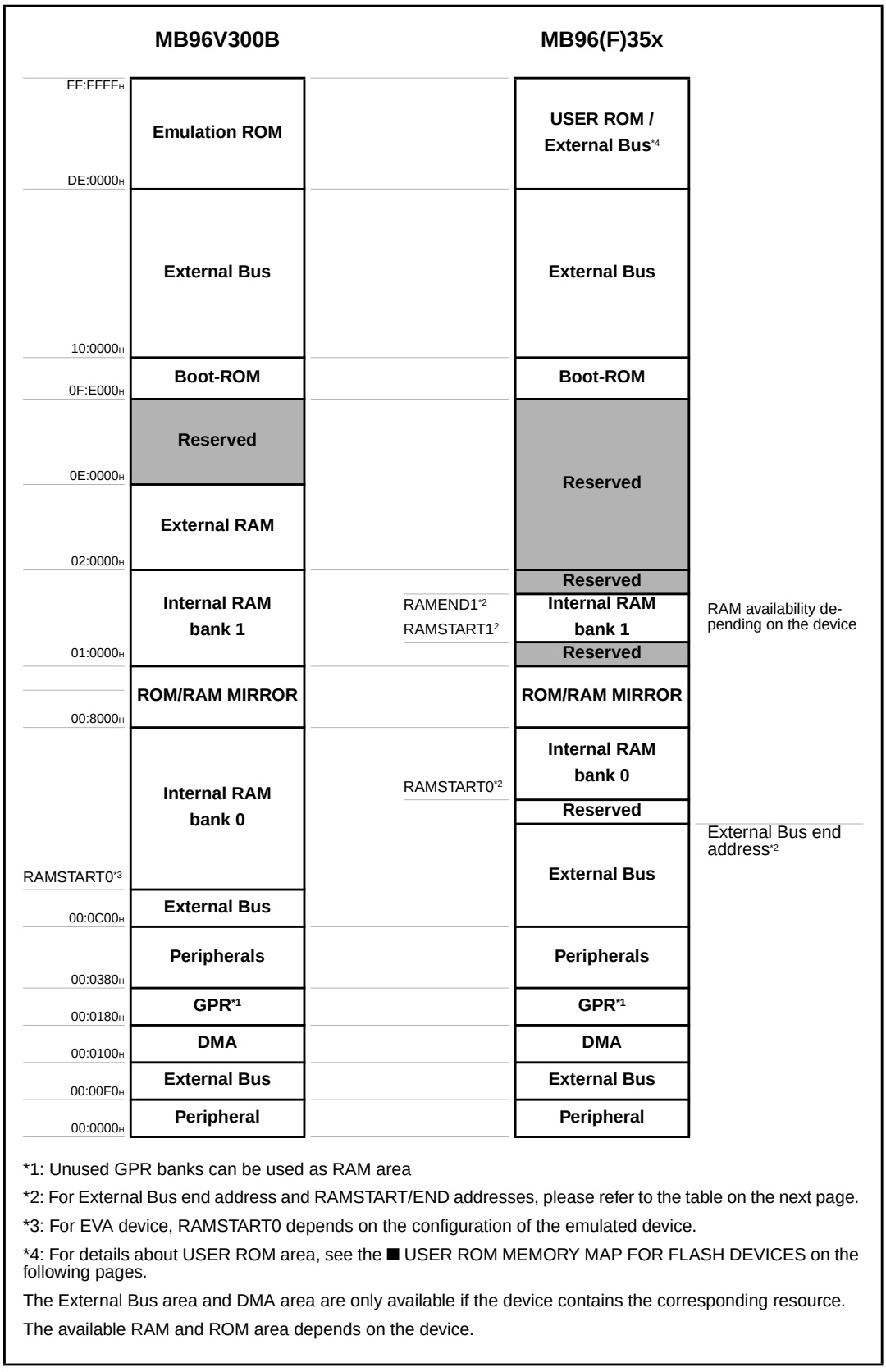
■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Programmable feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode
B		Low-speed oscillation circuit: • Programmable feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled
C		• Mask ROM and EVA device: CMOS Hysteresis input pin • Flash device: CMOS input pin
E		• CMOS Hysteresis input pin • Pull-up resistor value: approx. 50 kΩ

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Flash devices do not have a protection circuit against VCC for pin AVRH
H		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. * MB96F353/F355: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

Type	Circuit	Remarks
I		• CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function. • Programmable pull-up resistor: 50kΩ approx. • Analog input * MB96F353/F355: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • 2 different CMOS hysteresis inputs with input shutdown function • Automotive input with input shutdown function • TTL input with input shutdown function • Programmable pull-up resistor: 50kΩ approx. * MB96F353/F355: Only Automotive input and CMOS hysteresis input (0.7/0.3) are supported

■ MEMORY MAP



*1: Unused GPR banks can be used as RAM area

*2: For External Bus end address and RAMSTART/END addresses, please refer to the table on the next page.

*3: For EVA device, RAMSTART0 depends on the configuration of the emulated device.

*4: For details about USER ROM area, see the ■ USER ROM MEMORY MAP FOR FLASH DEVICES on the following pages.

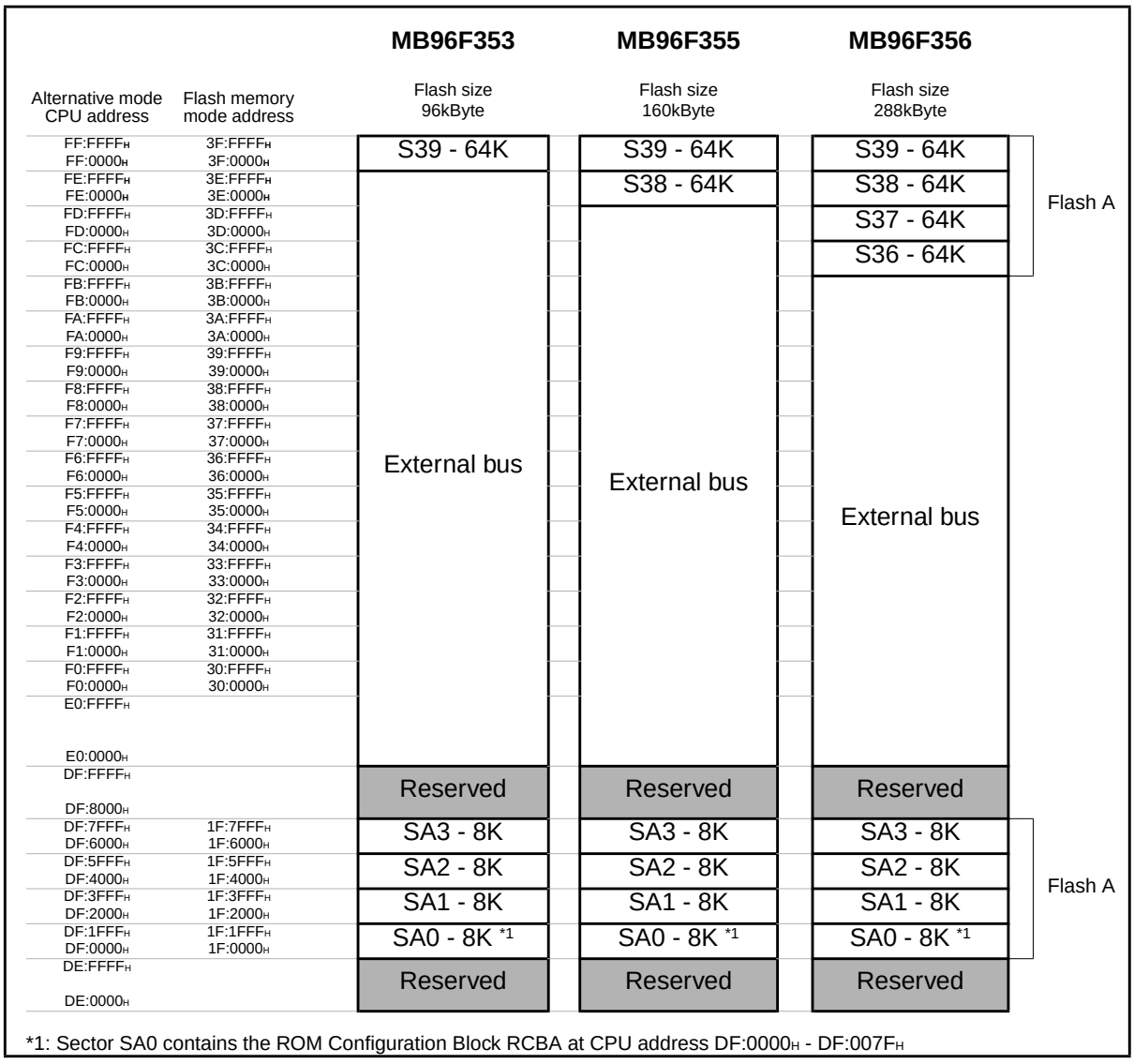
The External Bus area and DMA area are only available if the device contains the corresponding resource.

The available RAM and ROM area depends on the device.

■ RAMSTART/END AND EXTERNAL BUS END ADDRESSES

Devices	Bank 0 RAM size	Bank 1 RAM size	External Bus end address	RAMSTART0	RAMSTART1	RAMEND1
MB96F353/F355	8KByte	-	00:51FF$_H$	00:6240$_H$	-	-
MB96F356	12KByte	-	00:51FF$_H$	00:5240$_H$	-	-

■ USER ROM MEMORY MAP FOR FLASH DEVICES



*1: Sector SA0 contains the ROM Configuration Block RCBA at CPU address DF:0000H - DF:007FH

■ SERIAL PROGRAMMING COMMUNICATION INTERFACE

USART pins for Flash serial programming (MD[2:0] = 010)

MB96F35x		
Pin number	USART Number	Normal function
LQFP-64		
9	USART2	SIN2
10		SOT2
11		SCK2
34	USART3	SIN3
35		SOT3
36		SCK3
26	USART7	SIN7_R
25		SOT7_R
24		SCK7_R
29	USART8	SIN8_R
28		SOT8_R
27		SCK8_R

Note: If a Flash programmer and its software needs to use a handshaking pin, Fujitsu suggests to the tool vendor to support at least port P00_1 on pin 25.
If handshaking is used by the tool but P00_1 is not available in customer's application, Fujitsu suggests to the customer to check the tool manual or to contact the tool vendor for alternative handshaking pins.

■ I/O MAP

I/O map MB96(F)35x (1 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000000H	I/O Port P00 - Port Data Register	PDR00		R/W
000001H	I/O Port P01 - Port Data Register	PDR01		R/W
000002H	I/O Port P02 - Port Data Register	PDR02		R/W
000003H	I/O Port P03 - Port Data Register	PDR03		R/W
000004H	I/O Port P04 - Port Data Register	PDR04		R/W
000005H	I/O Port P05 - Port Data Register	PDR05		R/W
000006H	I/O Port P06 - Port Data Register	PDR06		R/W
000007H-000017H	Reserved			-
000018H	ADC0 - Control Status register Low	ADCSL	ADCS	R/W
000019H	ADC0 - Control Status register High	ADCSH		R/W
00001AH	ADC0 - Data Register Low	ADCRL	ADCR	R
00001BH	ADC0 - Data Register High	ADCRH		R
00001CH	ADC0 - Setting Register		ADSR	R/W
00001DH	ADC0 - Setting Register			R/W
00001EH	ADC0 - Extended Configuration Register	ADECR		R/W
00001FH	Reserved			-
000020H	FRT0 - Data register of free-running timer		TCDT0	R/W
000021H	FRT0 - Data register of free-running timer			R/W
000022H	FRT0 - Control status register of free-running timer Low	TCCSL0	TCCS0	R/W
000023H	FRT0 - Control status register of free-running timer High	TCCSH0		R/W
000024H	FRT1 - Data register of free-running timer		TCDT1	R/W
000025H	FRT1 - Data register of free-running timer			R/W
000026H	FRT1 - Control status register of free-running timer Low	TCCSL1	TCCS1	R/W
000027H	FRT1 - Control status register of free-running timer High	TCCSH1		R/W
000028H-000033H	Reserved			-

I/O map MB96(F)35x (2 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000034H	OCU4 - Output Compare Control Status	OCS4		R/W
000035H	OCU5 - Output Compare Control Status	OCS5		R/W
000036H	OCU4 - Compare Register		OCCP4	R/W
000037H	OCU4 - Compare Register			R/W
000038H	OCU5 - Compare Register		OCCP5	R/W
000039H	OCU5 - Compare Register			R/W
00003AH	OCU6 - Output Compare Control Status	OCS6		R/W
00003BH	OCU7 - Output Compare Control Status	OCS7		R/W
00003CH	OCU6 - Compare Register		OCCP6	R/W
00003DH	OCU6 - Compare Register			R/W
00003EH	OCU7 - Compare Register		OCCP7	R/W
00003FH	OCU7 - Compare Register			R/W
000040H	ICU0/ICU1 - Control Status Register	ICS01		R/W
000041H	ICU0/ICU1 - Edge register	ICE01		R/W
000042H	ICU0 - Capture Register Low	IPCPL0	IPCP0	R
000043H	ICU0 - Capture Register High	IPCPH0		R
000044H	ICU1 - Capture Register Low	IPCPL1	IPCP1	R
000045H	ICU1 - Capture Register High	IPCPH1		R
000046H - 00004BH	Reserved			
00004CH	ICU4/ICU5 - Control Status Register	ICS45		R/W
00004DH	ICU4/ICU5 - Edge register	ICE45		R/W
00004EH	ICU4 - Capture Register Low	IPCPL4	IPCP4	R
00004FH	ICU4 - Capture Register High	IPCPH4		R
000050H	ICU5 - Capture Register Low	IPCPL5	IPCP5	R
000051H	ICU5 - Capture Register High	IPCPH5		R
000052H	ICU6/ICU7 - Control Status Register	ICS67		R/W
000053H	ICU6/ICU7 - Edge register	ICE67		R/W
000054H	ICU6 - Capture Register Low	IPCPL6	IPCP6	R
000055H	ICU6 - Capture Register High	IPCPH6		R

I/O map MB96(F)35x (3 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000056H	ICU7 - Capture Register Low	IPCPL7	IPCP7	R
000057H	ICU7 - Capture Register High	IPCPH7		R
000058H	EXTINT0 - External Interrupt Enable Register	ENIR0		R/W
000059H	EXTINT0 - External Interrupt Interrupt request Register	EIRR0		R/W
00005AH	EXTINT0 - External Interrupt Level Select Low	ELVRL0	ELVR0	R/W
00005BH	EXTINT0 - External Interrupt Level Select High	ELVRH0		R/W
00005CH	EXTINT1 - External Interrupt Enable Register	ENIR1		R/W
00005DH	EXTINT1 - External Interrupt Interrupt request Register	EIRR1		R/W
00005EH	EXTINT1 - External Interrupt Level Select Low	ELVRL1	ELVR1	R/W
00005FH	EXTINT1 - External Interrupt Level Select High	ELVRH1		R/W
000060H	RLT0 - Timer Control Status Register Low	TMCSRL0	TMCSR0	R/W
000061H	RLT0 - Timer Control Status Register High	TMCSRH0		R/W
000062H	RLT0 - Reload Register - for writing		TMRLR0	W
000062H	RLT0 - Reload Register - for reading		TMR0	R
000063H	RLT0 - Reload Register - for writing			W
000063H	RLT0 - Reload Register - for reading			R
000064H	RLT1 - Timer Control Status Register Low	TMCSRL1	TMCSR1	R/W
000065H	RLT1 - Timer Control Status Register High	TMCSRH1		R/W
000066H	RLT1 - Reload Register - for writing		TMRLR1	W
000066H	RLT1 - Reload Register - for reading		TMR1	R
000067H	RLT1 - Reload Register - for writing			W
000067H	RLT1 - Reload Register - for reading			R
000068H	RLT2 - Timer Control Status Register Low	TMCSRL2	TMCSR2	R/W
000069H	RLT2 - Timer Control Status Register High	TMCSRH2		R/W
00006AH	RLT2 - Reload Register - for writing		TMRLR2	W
00006AH	RLT2 - Reload Register - for reading		TMR2	R
00006BH	RLT2 - Reload Register - for writing			W
00006BH	RLT2 - Reload Register - for reading			R
00006CH	RLT3 - Timer Control Status Register Low	TMCSRL3	TMCSR3	R/W

I/O map MB96(F)35x (4 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00006D$_H$	RLT3 - Timer Control Status Register High	TMCSRH3		R/W
00006E$_H$	RLT3 - Reload Register - for writing		TMRLR3	W
00006E$_H$	RLT3 - Reload Register - for reading		TMR3	R
00006F$_H$	RLT3 - Reload Register - for writing			W
00006F$_H$	RLT3 - Reload Register - for reading			R
000070$_H$	RLT6 - Timer Control Status Register Low (dedic. RLT for PPG)	TMCSRL6	TMCSR6	R/W
000071$_H$	RLT6 - Timer Control Status Register High (dedic. RLT for PPG)	TMCSRH6		R/W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing		TMRLR6	W
000072$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading		TMR6	R
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for writing			W
000073$_H$	RLT6 - Reload Register (dedic. RLT for PPG) - for reading			R
000074$_H$	PPG3-PPG0 - General Control register 1 Low	GCN1L0	GCN10	R/W
000075$_H$	PPG3-PPG0 - General Control register 1 High	GCN1H0		R/W
000076$_H$	PPG3-PPG0 - General Control register 2 Low	GCN2L0	GCN20	R/W
000077$_H$	PPG3-PPG0 - General Control register 2 High	GCN2H0		R/W
000078$_H$	PPG0 - Timer register		PTMR0	R
000079$_H$	PPG0 - Timer register			R
00007A$_H$	PPG0 - Period setting register		PCSR0	W
00007B$_H$	PPG0 - Period setting register			W
00007C$_H$	PPG0 - Duty cycle register		PDUT0	W
00007D$_H$	PPG0 - Duty cycle register			W
00007E$_H$	PPG0 - Control status register Low	PCNL0	PCN0	R/W
00007F$_H$	PPG0 - Control status register High	PCNH0		R/W
000080$_H$	PPG1 - Timer register		PTMR1	R
000081$_H$	PPG1 - Timer register			R
000082$_H$	PPG1 - Period setting register		PCSR1	W

I/O map MB96(F)35x (5 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000083H	PPG1 - Period setting register			W
000084H	PPG1 - Duty cycle register		PDUT1	W
000085H	PPG1 - Duty cycle register			W
000086H	PPG1 - Control status register Low	PCNL1	PCN1	R/W
000087H	PPG1 - Control status register High	PCNH1		R/W
000088H	PPG2 - Timer register		PTMR2	R
000089H	PPG2 - Timer register			R
00008AH	PPG2 - Period setting register		PCSR2	W
00008BH	PPG2 - Period setting register			W
00008CH	PPG2 - Duty cycle register		PDUT2	W
00008DH	PPG2 - Duty cycle register			W
00008EH	PPG2 - Control status register Low	PCNL2	PCN2	R/W
00008FH	PPG2 - Control status register High	PCNH2		R/W
000090H	PPG3 - Timer register		PTMR3	R
000091H	PPG3 - Timer register			R
000092H	PPG3 - Period setting register		PCSR3	W
000093H	PPG3 - Period setting register			W
000094H	PPG3 - Duty cycle register		PDUT3	W
000095H	PPG3 - Duty cycle register			W
000096H	PPG3 - Control status register Low	PCNL3	PCN3	R/W
000097H	PPG3 - Control status register High	PCNH3		R/W
000098H	PPG7-PPG4 - General Control register 1 Low	GCN1L1	GCN11	R/W
000099H	PPG7-PPG4 - General Control register 1 High	GCN1H1		R/W
00009AH	PPG7-PPG4 - General Control register 2 Low	GCN2L1	GCN21	R/W
00009BH	PPG7-PPG4 - General Control register 2 High	GCN2H1		R/W
00009CH	PPG4 - Timer register		PTMR4	R
00009DH	PPG4 - Timer register			R
00009EH	PPG4 - Period setting register		PCSR4	W
00009FH	PPG4 - Period setting register			W
0000A0H	PPG4 - Duty cycle register		PDUT4	W

I/O map MB96(F)35x (6 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000A1H	PPG4 - Duty cycle register			W
0000A2H	PPG4 - Control status register Low	PCNL4	PCN4	R/W
0000A3H	PPG4 - Control status register High	PCNH4		R/W
0000A4H	PPG5 - Timer register		PTMR5	R
0000A5H	PPG5 - Timer register			R
0000A6H	PPG5 - Period setting register		PCSR5	W
0000A7H	PPG5 - Period setting register			W
0000A8H	PPG5 - Duty cycle register		PDUT5	W
0000A9H	PPG5 - Duty cycle register			W
0000AAH	PPG5 - Control status register Low	PCNL5	PCN5	R/W
0000ABH	PPG5 - Control status register High	PCNH5		R/W
0000ACH	I2C0 - Bus Status Register	IBSR0		R
0000ADH	I2C0 - Bus Control Register	IBCR0		R/W
0000AEH	I2C0 - Ten bit Slave address Register Low	ITBAL0	ITBA0	R/W
0000AFH	I2C0 - Ten bit Slave address Register High	ITBAH0		R/W
0000B0H	I2C0 - Ten bit Address mask Register Low	ITMKL0	ITMK0	R/W
0000B1H	I2C0 - Ten bit Address mask Register High	ITMKH0		R/W
0000B2H	I2C0 - Seven bit Slave address Register	ISBA0		R/W
0000B3H	I2C0 - Seven bit Address mask Register	ISMK0		R/W
0000B4H	I2C0 - Data Register	IDAR0		R/W
0000B5H	I2C0 - Clock Control Register	ICCR0		R/W
0000B6H-0000D3H	Reserved			-
0000D4H	USART2 - Serial Mode Register	SMR2		R/W
0000D5H	USART2 - Serial Control Register	SCR2		R/W
0000D6H	USART2 - TX Register	TDR2		W
0000D6H	USART2 - RX Register	RDR2		R
0000D7H	USART2 - Serial Status	SSR2		R/W
0000D8H	USART2 - Control/Com. Register	ECCR2		R/W
0000D9H	USART2 - Ext. Status Register	ESCR2		R/W

I/O map MB96(F)35x (7 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0000DA$_H$	USART2 - Baud Rate Generator Register Low	BGRL2	BGR2	R/W
0000DB$_H$	USART2 - Baud Rate Generator Register High	BGRH2		R/W
0000DC$_H$	USART2 - Extended Serial Interrupt Register	ESIR2		R/W
0000DD$_H$	Reserved			-
0000DE$_H$	USART3 - Serial Mode Register	SMR3		R/W
0000DF$_H$	USART3 - Serial Control Register	SCR3		R/W
0000E0$_H$	USART3 - TX Register	TDR3		W
0000E0$_H$	USART3 - RX Register	RDR3		R
0000E1$_H$	USART3 - Serial Status	SSR3		R/W
0000E2$_H$	USART3 - Control/Com. Register	ECCR3		R/W
0000E3$_H$	USART3 - Ext. Status Register	ESCR3		R/W
0000E4$_H$	USART3 - Baud Rate Generator Register Low	BGRL3	BGR3	R/W
0000E5$_H$	USART3 - Baud Rate Generator Register High	BGRH3		R/W
0000E6$_H$	USART3 - Extended Serial Interrupt Register	ESIR3		R/W
0000E7$_H$-0000EF$_H$	Reserved			-
0000F0$_H$-0000FF$_H$	External Bus area	EXTBUS0		R/W
000100$_H$	DMA0 - Buffer address pointer low byte	BAPL0		R/W
000101$_H$	DMA0 - Buffer address pointer middle byte	BAPM0		R/W
000102$_H$	DMA0 - Buffer address pointer high byte	BAPH0		R/W
000103$_H$	DMA0 - DMA control register	DMACS0		R/W
000104$_H$	DMA0 - I/O register address pointer low byte	IOAL0	IOA0	R/W
000105$_H$	DMA0 - I/O register address pointer high byte	IOAH0		R/W
000106$_H$	DMA0 - Data counter low byte	DCTL0	DCT0	R/W
000107$_H$	DMA0 - Data counter high byte	DCTH0		R/W
000108$_H$	DMA1 - Buffer address pointer low byte	BAPL1		R/W
000109$_H$	DMA1 - Buffer address pointer middle byte	BAPM1		R/W
00010A$_H$	DMA1 - Buffer address pointer high byte	BAPH1		R/W
00010B$_H$	DMA1 - DMA control register	DMACS1		R/W
00010C$_H$	DMA1 - I/O register address pointer low byte	IOAL1	IOA1	R/W

I/O map MB96(F)35x (8 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00010D$_H$	DMA1 - I/O register address pointer high byte	IOAH1		R/W
00010E$_H$	DMA1 - Data counter low byte	DCTL1	DCT1	R/W
00010F$_H$	DMA1 - Data counter high byte	DCTH1		R/W
000110$_H$	DMA2 - Buffer address pointer low byte	BAPL2		R/W
000111$_H$	DMA2 - Buffer address pointer middle byte	BAPM2		R/W
000112$_H$	DMA2 - Buffer address pointer high byte	BAPH2		R/W
000113$_H$	DMA2 - DMA control register	DMACS2		R/W
000114$_H$	DMA2 - I/O register address pointer low byte	IOAL2	IOA2	R/W
000115$_H$	DMA2 - I/O register address pointer high byte	IOAH2		R/W
000116$_H$	DMA2 - Data counter low byte	DCTL2	DCT2	R/W
000117$_H$	DMA2 - Data counter high byte	DCTH2		R/W
000118$_H$	DMA3 - Buffer address pointer low byte	BAPL3		R/W
000119$_H$	DMA3 - Buffer address pointer middle byte	BAPM3		R/W
00011A$_H$	DMA3 - Buffer address pointer high byte	BAPH3		R/W
00011B$_H$	DMA3 - DMA control register	DMACS3		R/W
00011C$_H$	DMA3 - I/O register address pointer low byte	IOAL3	IOA3	R/W
00011D$_H$	DMA3 - I/O register address pointer high byte	IOAH3		R/W
00011E$_H$	DMA3 - Data counter low byte	DCTL3	DCT3	R/W
00011F$_H$	DMA3 - Data counter high byte	DCTH3		R/W
000120$_H$-00017F$_H$	Reserved			-
000180$_H$-00037F$_H$	CPU - General Purpose registers (RAM access)	GPR_RAM		R/W
000380$_H$	DMA0 - Interrupt select	DISEL0		R/W
000381$_H$	DMA1 - Interrupt select	DISEL1		R/W
000382$_H$	DMA2 - Interrupt select	DISEL2		R/W
000383$_H$	DMA3 - Interrupt select	DISEL3		R/W
000384$_H$-00038F$_H$	Reserved			-
000390$_H$	DMA - Status register low byte	DSRL	DSR	R/W
000391$_H$	DMA - Status register high byte	DSRH		R/W

I/O map MB96(F)35x (9 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000392H	DMA - Stop status register low byte	DSSRL	DSSR	R/W
000393H	DMA - Stop status register high byte	DSSRH		R/W
000394H	DMA - Enable register low byte	DERL	DER	R/W
000395H	DMA - Enable register high byte	DERH		R/W
000396H-00039FH	Reserved			-
0003A0H	Interrupt level register	ILR	ICR	R/W
0003A1H	Interrupt index register	IDX		R/W
0003A2H	Interrupt vector table base register Low	TBRL	TBR	R/W
0003A3H	Interrupt vector table base register High	TBRH		R/W
0003A4H	Delayed Interrupt register	DIRR		R/W
0003A5H	Non Maskable Interrupt register	NMI		R/W
0003A6H-0003ABH	Reserved			-
0003ACH	EDSU communication interrupt selection Low	EDSU2L	EDSU2	R/W
0003ADH	EDSU communication interrupt selection High	EDSU2H		R/W
0003AEH	ROM mirror control register	ROMM		R/W
0003AFH	EDSU configuration register	EDSU		R/W
0003B0H	Memory patch control/status register ch 0/1		PFCS0	R/W
0003B1H	Memory patch control/status register ch 0/1			R/W
0003B2H	Memory patch control/status register ch 2/3		PFCS1	R/W
0003B3H	Memory patch control/status register ch 2/3			R/W
0003B4H	Memory patch control/status register ch 4/5		PFCS2	R/W
0003B5H	Memory patch control/status register ch 4/5			R/W
0003B6H	Memory patch control/status register ch 6/7		PFCS3	R/W
0003B7H	Memory patch control/status register ch 6/7			R/W
0003B8H	Memory Patch function - Patch address 0 low	PFAL0		R/W
0003B9H	Memory Patch function - Patch address 0 middle	PFAM0		R/W
0003BAH	Memory Patch function - Patch address 0 high	PFAH0		R/W
0003BBH	Memory Patch function - Patch address 1 low	PFAL1		R/W
0003BCH	Memory Patch function - Patch address 1 middle	PFAM1		R/W

I/O map MB96(F)35x (10 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003BD$_H$	Memory Patch function - Patch address 1 high	PFAH1		R/W
0003BE$_H$	Memory Patch function - Patch address 2 low	PFAL2		R/W
0003BF$_H$	Memory Patch function - Patch address 2 middle	PFAM2		R/W
0003C0$_H$	Memory Patch function - Patch address 2 high	PFAH2		R/W
0003C1$_H$	Memory Patch function - Patch address 3 low	PFAL3		R/W
0003C2$_H$	Memory Patch function - Patch address 3 middle	PFAM3		R/W
0003C3$_H$	Memory Patch function - Patch address 3 high	PFAH3		R/W
0003C4$_H$	Memory Patch function - Patch address 4 low	PFAL4		R/W
0003C5$_H$	Memory Patch function - Patch address 4 middle	PFAM4		R/W
0003C6$_H$	Memory Patch function - Patch address 4 high	PFAH4		R/W
0003C7$_H$	Memory Patch function - Patch address 5 low	PFAL5		R/W
0003C8$_H$	Memory Patch function - Patch address 5 middle	PFAM5		R/W
0003C9$_H$	Memory Patch function - Patch address 5 high	PFAH5		R/W
0003CA$_H$	Memory Patch function - Patch address 6 low	PFAL6		R/W
0003CB$_H$	Memory Patch function - Patch address 6 middle	PFAM6		R/W
0003CC$_H$	Memory Patch function - Patch address 6 high	PFAH6		R/W
0003CD$_H$	Memory Patch function - Patch address 7 low	PFAL7		R/W
0003CE$_H$	Memory Patch function - Patch address 7 middle	PFAM7		R/W
0003CF$_H$	Memory Patch function - Patch address 7 high	PFAH7		R/W
0003D0$_H$	Memory Patch function - Patch data 0 Low	PFDL0	PFD0	R/W
0003D1$_H$	Memory Patch function - Patch data 0 High	PFDH0		R/W
0003D2$_H$	Memory Patch function - Patch data 1 Low	PFDL1	PFD1	R/W
0003D3$_H$	Memory Patch function - Patch data 1 High	PFDH1		R/W
0003D4$_H$	Memory Patch function - Patch data 2 Low	PFDL2	PFD2	R/W
0003D5$_H$	Memory Patch function - Patch data 2 High	PFDH2		R/W
0003D6$_H$	Memory Patch function - Patch data 3 Low	PFDL3	PFD3	R/W
0003D7$_H$	Memory Patch function - Patch data 3 High	PFDH3		R/W
0003D8$_H$	Memory Patch function - Patch data 4 Low	PFDL4	PFD4	R/W
0003D9$_H$	Memory Patch function - Patch data 4 High	PFDH4		R/W
0003DA$_H$	Memory Patch function - Patch data 5 Low	PFDL5	PFD5	R/W

I/O map MB96(F)35x (11 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0003DB$_H$	Memory Patch function - Patch data 5 High	PFDH5		R/W
0003DC$_H$	Memory Patch function - Patch data 6 Low	PFDL6	PFD6	R/W
0003DD$_H$	Memory Patch function - Patch data 6 High	PFDH6		R/W
0003DE$_H$	Memory Patch function - Patch data 7 Low	PFDL7	PFD7	R/W
0003DF$_H$	Memory Patch function - Patch data 7 High	PFDH7		R/W
0003E0$_H$-0003F0$_H$	Reserved			-
0003F1$_H$	Memory Control Status Register A	MCSRA		R/W
0003F2$_H$	Memory Timing Configuration Register A Low	MTCRAL	MTCRA	R/W
0003F3$_H$	Memory Timing Configuration Register A High	MTCRAH		R/W
0003F4$_H$-0003F8$_H$	Reserved			-
0003F9$_H$	Flash Memory Write Control register 1	FMWC1		R/W
0003FA$_H$	Flash Memory Write Control register 2	FMWC2		R/W
0003FB$_H$	Flash Memory Write Control register 3	FMWC3		R/W
0003FC$_H$	Flash Memory Write Control register 4	FMWC4		R/W
0003FD$_H$	Flash Memory Write Control register 5	FMWC5		R/W
0003FE$_H$-0003FF$_H$	Reserved			-
000400$_H$	Standby Mode control register	SMCR		R/W
000401$_H$	Clock select register	CKSR		R/W
000402$_H$	Clock Stabilisation select register	CKSSR		R/W
000403$_H$	Clock monitor register	CKMR		R
000404$_H$	Clock Frequency control register Low	CKFCRL	CKFCR	R/W
000405$_H$	Clock Frequency control register High	CKFCRH		R/W
000406$_H$	PLL Control register Low	PLLCRL	PLLCR	R/W
000407$_H$	PLL Control register High	PLLCRH		R/W
000408$_H$	RC clock timer control register	RCTCR		R/W
000409$_H$	Main clock timer control register	MCTCR		R/W
00040A$_H$	Sub clock timer control register	SCTCR		R/W

I/O map MB96(F)35x (12 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00040B$_H$	Reset cause and clock status register with clear function	RCCSRC		R
00040C$_H$	Reset configuration register	RCR		R/W
00040D$_H$	Reset cause and clock status register	RCCSR		R
00040E$_H$	Watch dog timer configuration register	WDTC		R/W
00040F$_H$	Watch dog timer clear pattern register	WDTCP		W
000410$_H$-000414$_H$	Reserved			-
000415$_H$	Clock output activation register	COAR		R/W
000416$_H$	Clock output configuration register 0	COCR0		R/W
000417$_H$	Clock output configuration register 1	COCR1		R/W
000418$_H$	Clock Modulator control register	CMCR		R/W
000419$_H$	Reserved			-
00041A$_H$	Clock Modulator Parameter register Low	CMPRL	CMPR	R/W
00041B$_H$	Clock Modulator Parameter register High	CMPRH		R/W
00041C$_H$-00042B$_H$	Reserved			-
00042C$_H$	Voltage Regulator Control register	VRCR		R/W
00042D$_H$	Clock Input and LVD Control Register	CILCR		R/W
00042E$_H$-00042F$_H$	Reserved			-
000430$_H$	I/O Port P00 - Data Direction Register	DDR00		R/W
000431$_H$	I/O Port P01 - Data Direction Register	DDR01		R/W
000432$_H$	I/O Port P02 - Data Direction Register	DDR02		R/W
000433$_H$	I/O Port P03 - Data Direction Register	DDR03		R/W
000434$_H$	I/O Port P04 - Data Direction Register	DDR04		R/W
000435$_H$	I/O Port P05 - Data Direction Register	DDR05		R/W
000436$_H$	I/O Port P06 - Data Direction Register	DDR06		R/W
000437$_H$-000443$_H$	Reserved			-
000444$_H$	I/O Port P00 - Port Input Enable Register	PIER00		R/W
000445$_H$	I/O Port P01 - Port Input Enable Register	PIER01		R/W

I/O map MB96(F)35x (13 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000446H	I/O Port P02 - Port Input Enable Register	PIER02		R/W
000447H	I/O Port P03 - Port Input Enable Register	PIER03		R/W
000448H	I/O Port P04 - Port Input Enable Register	PIER04		R/W
000449H	I/O Port P05 - Port Input Enable Register	PIER05		R/W
00044AH	I/O Port P06 - Port Input Enable Register	PIER06		R/W
00044BH-000457H	Reserved			-
000458H	I/O Port P00 - Port Input Level Register	PILR00		R/W
000459H	I/O Port P01 - Port Input Level Register	PILR01		R/W
00045AH	I/O Port P02 - Port Input Level Register	PILR02		R/W
00045BH	I/O Port P03 - Port Input Level Register	PILR03		R/W
00045CH	I/O Port P04 - Port Input Level Register	PILR04		R/W
00045DH	I/O Port P05 - Port Input Level Register	PILR05		R/W
00045EH	I/O Port P06 - Port Input Level Register	PILR06		R/W
00045FH-00046BH	Reserved			-
00046CH	I/O Port P00 - Extended Port Input Level Register	EPILR00		R/W
00046DH	I/O Port P01 - Extended Port Input Level Register	EPILR01		R/W
00046EH	I/O Port P02 - Extended Port Input Level Register	EPILR02		R/W
00046FH	I/O Port P03 - Extended Port Input Level Register	EPILR03		R/W
000470H	I/O Port P04 - Extended Port Input Level Register	EPILR04		R/W
000471H	I/O Port P05 - Extended Port Input Level Register	EPILR05		R/W
000472H	I/O Port P06 - Extended Port Input Level Register	EPILR06		R/W
000473H-00047FH	Reserved			-
000480H	I/O Port P00 - Port Output Drive Register	PODR00		R/W
000481H	I/O Port P01 - Port Output Drive Register	PODR01		R/W
000482H	I/O Port P02 - Port Output Drive Register	PODR02		R/W
000483H	I/O Port P03 - Port Output Drive Register	PODR03		R/W
000484H	I/O Port P04 - Port Output Drive Register	PODR04		R/W
000485H	I/O Port P05 - Port Output Drive Register	PODR05		R/W

I/O map MB96(F)35x (14 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000486H	I/O Port P06 - Port Output Drive Register	PODR06		R/W
000487H-0004A7H	Reserved			-
0004A8H	I/O Port P00 - Pull-Up resistor Control Register	PUCR00		R/W
0004A9H	I/O Port P01 - Pull-Up resistor Control Register	PUCR01		R/W
0004AAH	I/O Port P02 - Pull-Up resistor Control Register	PUCR02		R/W
0004ABH	I/O Port P03 - Pull-Up resistor Control Register	PUCR03		R/W
0004ACH	I/O Port P04 - Pull-Up resistor Control Register	PUCR04		R/W
0004ADH	I/O Port P05 - Pull-Up resistor Control Register	PUCR05		R/W
0004AEH	I/O Port P06 - Pull-Up resistor Control Register	PUCR06		R/W
0004AFH-0004BBH	Reserved			-
0004BCH	I/O Port P00 - External Pin State Register	EPSR00		R
0004BDH	I/O Port P01 - External Pin State Register	EPSR01		R
0004BEH	I/O Port P02 - External Pin State Register	EPSR02		R
0004BFH	I/O Port P03 - External Pin State Register	EPSR03		R
0004C0H	I/O Port P04 - External Pin State Register	EPSR04		R
0004C1H	I/O Port P05 - External Pin State Register	EPSR05		R
0004C2H	I/O Port P06 - External Pin State Register	EPSR06		R
0004C3H-0004CFH	Reserved			-
0004D0H	ADC analog input enable register 0	ADER0		R/W
0004D1H	ADC analog input enable register 1	ADER1		R/W
0004D2H	ADC analog input enable register 2	ADER2		R/W
0004D3H	ADC analog input enable register 3	ADER3		R/W
0004D4H	ADC analog input enable register 4	ADER4		R/W
0004D5H	Reserved			-
0004D6H	Peripheral Resource Relocation Register 0	PRRR0		R/W
0004D7H	Peripheral Resource Relocation Register 1	PRRR1		R/W
0004D8H	Peripheral Resource Relocation Register 2	PRRR2		R/W
0004D9H	Peripheral Resource Relocation Register 3	PRRR3		R/W

I/O map MB96(F)35x (15 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0004DA$_H$	Peripheral Resource Relocation Register 4	PRRR4		R/W
0004DB$_H$	Peripheral Resource Relocation Register 5	PRRR5		R/W
0004DC$_H$	Peripheral Resource Relocation Register 6	PRRR6		R/W
0004DD$_H$	Peripheral Resource Relocation Register 7	PRRR7		R/W
0004DE$_H$	Peripheral Resource Relocation Register 8	PRRR8		R/W
0004DF$_H$	Peripheral Resource Relocation Register 9	PRRR9		R/W
0004E0$_H$	RTC - Sub Second Register L	WTBRL0	WTBR0	R/W
0004E1$_H$	RTC - Sub Second Register M	WTBRH0		R/W
0004E2$_H$	RTC - Sub-Second Register H	WTBR1		R/W
0004E3$_H$	RTC - Second Register	WTSR		R/W
0004E4$_H$	RTC - Minutes	WTMR		R/W
0004E5$_H$	RTC - Hour	WTHR		R/W
0004E6$_H$	RTC - Timer Control Extended Register	WTCER		R/W
0004E7$_H$	RTC - Clock select register	WTCKSR		R/W
0004E8$_H$	RTC - Timer Control Register Low	WTCRL	WTCR	R/W
0004E9$_H$	RTC - Timer Control Register High	WTCRH		R/W
0004EA$_H$	CAL - Calibration unit Control register	CUCR		R/W
0004EB$_H$	Reserved			-
0004EC$_H$	CAL - Duration Timer Data Register Low	CUTDL	CUTD	R/W
0004ED$_H$	CAL - Duration Timer Data Register High	CUTDH		R/W
0004EE$_H$	CAL - Calibration Timer Register 2 Low	CUTR2L	CUTR2	R
0004EF$_H$	CAL - Calibration Timer Register 2 High	CUTR2H		R
0004F0$_H$	CAL - Calibration Timer Register 1 Low	CUTR1L	CUTR1	R
0004F1$_H$	CAL - Calibration Timer Register 1 High	CUTR1H		R
0004F2$_H$-0004F9$_H$	Reserved			-
0004FA$_H$	RLT - Timer input select (for Cascading)	TMISR		R/W
0004FB$_H$-0004FF$_H$	Reserved			-
000500$_H$	FRT2 - Data register of free-running timer		TCDT2	R/W
000501$_H$	FRT2 - Data register of free-running timer			R/W

I/O map MB96(F)35x (16 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000502H	FRT2 - Control status register of free-running timer Low	TCCSL2	TCCS2	R/W
000503H	FRT2 - Control status register of free-running timer High	TCCSH2		R/W
000504H	FRT3 - Data register of free-running timer		TCDT3	R/W
000505H	FRT3 - Data register of free-running timer			R/W
000506H	FRT3 - Control status register of free-running timer Low	TCCSL3	TCCS3	R/W
000507H	FRT3 - Control status register of free-running timer High	TCCSH3		R/W
000508H-000513H	Reserved			-
000514H	ICU8/ICU9 - Control Status Register	ICS89		R/W
000515H	ICU8/ICU9 - Edge Register	ICE89		R/W
000516H	ICU8 - Capture Register Low	IPCPL8	IPCP8	R
000517H	ICU8 - Capture Register High	IPCPH8		R
000518H	ICU9 - Capture Register Low	IPCPL9	IPCP9	R
000519H	ICU9 - Capture Register High	IPCPH9		R
00051AH	ICU10/ICU11 - Control Status Register	ICS1011		R/W
00051BH	ICU10/ICU11 - Edge Register	ICE1011		R/W
00051CH	ICU10 - Capture Register Low	IPCPL10	IPCP10	R
00051DH	ICU10 - Capture Register High	IPCPH10		R
00051EH	ICU11 - Capture Register Low	IPCPL11	IPCP11	R
00051FH	ICU11 - Capture Register High	IPCPH11		R
000520H-00053DH	Reserved			-
00053EH	USART7 - Serial Mode Register	SMR7		R/W
00053FH	USART7 - Serial Control Register	SCR7		R/W
000540H	USART7 - Serial TX Register	TDR7		W
000540H	USART7 - Serial RX Register	RDR7		R
000541H	USART7 - Serial Status Register	SSR7		R/W
000542H	USART7 - Ext. Control/Com. Register	ECCR7		R/W

I/O map MB96(F)35x (17 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000543H	USART7 - Ext. Status Com. Register	ESCR7		R/W
000544H	USART7 - Baud Rate Generator Register Low	BGRL7	BGR7	R/W
000545H	USART7 - Baud Rate Generator Register High	BGRH7		R/W
000546H	USART7 - Extended Serial Interrupt Register	ESIR7		R/W
000547H	Reserved			-
000548H	USART8 - Serial Mode Register	SMR8		R/W
000549H	USART8 - Serial Control Register	SCR8		R/W
00054AH	USART8 - Serial TX Register	TDR8		W
00054AH	USART8 - Serial RX Register	RDR8		R
00054BH	USART8 - Serial Status Register	SSR8		R/W
00054CH	USART8 - Ext. Control/Com. Register	ECCR8		R/W
00054DH	USART8 - Ext. Status Com. Register	ESCR8		R/W
00054EH	USART8 - Baud Rate Generator Register Low	BGRL8	BGR8	R/W
00054FH	USART8 - Baud Rate Generator Register High	BGRH8		R/W
000550H	USART8 - Extended Serial Interrupt Register	ESIR8		R/W
000551H-000563H	Reserved			-
000564H	PPG6 - Timer register		PTMR6	R
000565H	PPG6 - Timer register			R
000566H	PPG6 - Period setting register		PCSR6	W
000567H	PPG6 - Period setting register			W
000568H	PPG6 - Duty cycle register		PDUT6	W
000569H	PPG6 - Duty cycle register			W
00056AH	PPG6 - Control status register Low	PCNL6	PCN6	R/W
00056BH	PPG6 - Control status register High	PCNH6		R/W
00056CH	PPG7 - Timer register		PTMR7	R
00056DH	PPG7 - Timer register			R
00056EH	PPG7 - Period setting register		PCSR7	W
00056FH	PPG7 - Period setting register			W
000570H	PPG7 - Duty cycle register		PDUT7	W

I/O map MB96(F)35x (18 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000571H	PPG7 - Duty cycle register			W
000572H	PPG7 - Control status register Low	PCNL7	PCN7	R/W
000573H	PPG7 - Control status register High	PCNH7		R/W
000574H	PPG11-PPG8 - General Control register 1 Low	GCN1L2	GCN12	R/W
000575H	PPG11-PPG8 - General Control register 1 High	GCN1H2		R/W
000576H	PPG11-PPG8 - General Control register 2 Low	GCN2L2	GCN22	R/W
000577H	PPG11-PPG8 - General Control register 2 High	GCN2H2		R/W
000578H	PPG8 - Timer register		PTMR8	R
000579H	PPG8 - Timer register			R
00057AH	PPG8 - Period setting register		PCSR8	W
00057BH	PPG8 - Period setting register			W
00057CH	PPG8 - Duty cycle register		PDUT8	W
00057DH	PPG8 - Duty cycle register			W
00057EH	PPG8 - Control status register Low	PCNL8	PCN8	R/W
00057FH	PPG8 - Control status register High	PCNH8		R/W
000580H	PPG9 - Timer register		PTMR9	R
000581H	PPG9 - Timer register			R
000582H	PPG9 - Period setting register		PCSR9	W
000583H	PPG9 - Period setting register			W
000584H	PPG9 - Duty cycle register		PDUT9	W
000585H	PPG9 - Duty cycle register			W
000586H	PPG9 - Control status register Low	PCNL9	PCN9	R/W
000587H	PPG9 - Control status register High	PCNH9		R/W
000588H	PPG10 - Timer register		PTMR10	R
000589H	PPG10 - Timer register			R
00058AH	PPG10 - Period setting register		PCSR10	W
00058BH	PPG10 - Period setting register			W
00058CH	PPG10 - Duty cycle register		PDUT10	W
00058DH	PPG10 - Duty cycle register			W
00058EH	PPG10 - Control status register Low	PCNL10	PCN10	R/W

I/O map MB96(F)35x (19 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
00058F$_H$	PPG10 - Control status register High	PCNH10		R/W
000590$_H$	PPG11 - Timer register		PTMR11	R
000591$_H$	PPG11 - Timer register			R
000592$_H$	PPG11 - Period setting register		PCSR11	W
000593$_H$	PPG11 - Period setting register			W
000594$_H$	PPG11 - Duty cycle register		PDUT11	W
000595$_H$	PPG11 - Duty cycle register			W
000596$_H$	PPG11 - Control status register Low	PCNL11	PCN11	R/W
000597$_H$	PPG11 - Control status register High	PCNH11		R/W
000598$_H$	PPG15-PPG12 - General Control register 1 Low	GCN1L3	GCN13	R/W
000599$_H$	PPG15-PPG12 - General Control register 1 High	GCN1H3		R/W
00059A$_H$	PPG15-PPG12 - General Control register 2 Low	GCN2L3	GCN23	R/W
00059B$_H$	PPG15-PPG12 - General Control register 2 High	GCN2H3		R/W
00059C$_H$	PPG12 - Timer register		PTMR12	R
00059D$_H$	PPG12 - Timer register			R
00059E$_H$	PPG12 - Period setting register		PCSR12	W
00059F$_H$	PPG12 - Period setting register			W
0005A0$_H$	PPG12 - Duty cycle register		PDUT12	W
0005A1$_H$	PPG12 - Duty cycle register			W
0005A2$_H$	PPG12 - Control status register Low	PCNL12	PCN12	R/W
0005A3$_H$	PPG12 - Control status register High	PCNH12		R/W
0005A4$_H$	PPG13 - Timer register		PTMR13	R
0005A5$_H$	PPG13 - Timer register			R
0005A6$_H$	PPG13 - Period setting register		PCSR13	W
0005A7$_H$	PPG13 - Period setting register			W
0005A8$_H$	PPG13 - Duty cycle register		PDUT13	W
0005A9$_H$	PPG13 - Duty cycle register			W
0005AA$_H$	PPG13 - Control status register Low	PCNL13	PCN13	R/W
0005AB$_H$	PPG13 - Control status register High	PCNH13		R/W
0005AC$_H$	PPG14 - Timer register		PTMR14	R

I/O map MB96(F)35x (20 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005AD$_H$	PPG14 - Timer register			R
0005AE$_H$	PPG14 - Period setting register		PCSR14	W
0005AF$_H$	PPG14 - Period setting register			W
0005B0$_H$	PPG14 - Duty cycle register		PDUT14	W
0005B1$_H$	PPG14 - Duty cycle register			W
0005B2$_H$	PPG14 - Control status register Low	PCNL14	PCN14	R/W
0005B3$_H$	PPG14 - Control status register High	PCNH14		R/W
0005B4$_H$	PPG15 - Timer register		PTMR15	R
0005B5$_H$	PPG15 - Timer register			R
0005B6$_H$	PPG15 - Period setting register		PCSR15	W
0005B7$_H$	PPG15 - Period setting register			W
0005B8$_H$	PPG15 - Duty cycle register		PDUT15	W
0005B9$_H$	PPG15 - Duty cycle register			W
0005BA$_H$	PPG15 - Control status register Low	PCNL15	PCN15	R/W
0005BB$_H$	PPG15 - Control status register High	PCNH15		R/W
0005BC$_H$	PPG19-PPG16 - General Control register 1 Low	GCN1L4	GCN14	R/W
0005BD$_H$	PPG19-PPG16 - General Control register 1 High	GCN1H4		R/W
0005BE$_H$	PPG19-PPG16 - General Control register 2 Low	GCN2L4	GCN24	R/W
0005BF$_H$	PPG19-PPG16 - General Control register 2 High	GCN2H4		R/W
0005C0$_H$	PPG16 - Timer register		PTMR16	R
0005C1$_H$	PPG16 - Timer register			R
0005C2$_H$	PPG16 - Period setting register		PCSR16	W
0005C3$_H$	PPG16 - Period setting register			W
0005C4$_H$	PPG16 - Duty cycle register		PDUT16	W
0005C5$_H$	PPG16 - Duty cycle register			W
0005C6$_H$	PPG16 - Control status register Low	PCNL16	PCN16	R/W
0005C7$_H$	PPG16 - Control status register High	PCNH16		R/W
0005C8$_H$	PPG17 - Timer register		PTMR17	R
0005C9$_H$	PPG17 - Timer register			R
0005CA$_H$	PPG17 - Period setting register		PCSR17	W

I/O map MB96(F)35x (21 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0005CB$_H$	PPG17 - Period setting register			W
0005CC$_H$	PPG17 - Duty cycle register		PDUT17	W
0005CD$_H$	PPG17 - Duty cycle register			W
0005CE$_H$	PPG17 - Control status register Low	PCNL17	PCN17	R/W
0005CF$_H$	PPG17 - Control status register High	PCNH17		R/W
0005D0$_H$	PPG18 - Timer register		PTMR18	R
0005D1$_H$	PPG18 - Timer register			R
0005D2$_H$	PPG18 - Period setting register		PCSR18	W
0005D3$_H$	PPG18 - Period setting register			W
0005D4$_H$	PPG18 - Duty cycle register		PDUT18	W
0005D5$_H$	PPG18 - Duty cycle register			W
0005D6$_H$	PPG18 - Control status register Low	PCNL18	PCN18	R/W
0005D7$_H$	PPG18 - Control status register High	PCNH18		R/W
0005D8$_H$	PPG19 - Timer register		PTMR19	R
0005D9$_H$	PPG19 - Timer register			R
0005DA$_H$	PPG19 - Period setting register		PCSR19	W
0005DB$_H$	PPG19 - Period setting register			W
0005DC$_H$	PPG19 - Duty cycle register		PDUT19	W
0005DD$_H$	PPG19 - Duty cycle register			W
0005DE$_H$	PPG19 - Control status register Low	PCNL19	PCN19	R/W
0005DF$_H$	PPG19 - Control status register High	PCNH19		R/W
0005E0$_H$-00065F$_H$	Reserved			-
000660$_H$	Peripheral Resource Relocation Register 10	PRRR10		R/W
000661$_H$	Peripheral Resource Relocation Register 11	PRRR11		R/W
000662$_H$	Peripheral Resource Relocation Register 12	PRRR12		R/W
000663$_H$	Peripheral Resource Relocation Register 13	PRRR13		W
000664$_H$-0006DF$_H$	Reserved			-
0006E0$_H$	External Bus - Area configuration register 0 Low	EACL0	EAC0	R/W
0006E1$_H$	External Bus - Area configuration register 0 High	EACH0		R/W

I/O map MB96(F)35x (22 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
0006E2H	External Bus - Area configuration register 1 Low	EACL1	EAC1	R/W
0006E3H	External Bus - Area configuration register 1 High	EACH1		R/W
0006E4H	External Bus - Area configuration register 2 Low	EACL2	EAC2	R/W
0006E5H	External Bus - Area configuration register 2 High	EACH2		R/W
0006E6H	External Bus - Area configuration register 3 Low	EACL3	EAC3	R/W
0006E7H	External Bus - Area configuration register 3 High	EACH3		R/W
0006E8H	External Bus - Area configuration register 4 Low	EACL4	EAC4	R/W
0006E9H	External Bus - Area configuration register 4 High	EACH4		R/W
0006EAH	External Bus - Area configuration register 5 Low	EACL5	EAC5	R/W
0006EBH	External Bus - Area configuration register 5 High	EACH5		R/W
0006ECH	External Bus - Area select register 2	EAS2		R/W
0006EDH	External Bus - Area select register 3	EAS3		R/W
0006EEH	External Bus - Area select register 4	EAS4		R/W
0006EFH	External Bus - Area select register 5	EAS5		R/W
0006F0H	External Bus - Mode register	EBM		R/W
0006F1H	External Bus - Clock and Function register	EBCF		R/W
0006F2H	External Bus - Address output enable register 0	EBAE0		R/W
0006F3H	External Bus - Address output enable register 1	EBAE1		R/W
0006F4H	External Bus - Address output enable register 2	EBAE2		R/W
0006F5H	External Bus - Control signal register	EBCS		R/W
0006F6H-0007FFH	Reserved			-
000800H	CAN1 - Control register Low	CTRLRL1	CTRLR1	R/W
000801H	CAN1 - Control register High (reserved)	CTRLRH1		R
000802H	CAN1 - Status register Low	STATRL1	STATR1	R/W
000803H	CAN1 - Status register High (reserved)	STATRH1		R
000804H	CAN1 - Error Counter Low (Transmit)	ERRCNTL1	ERRCNT1	R
000805H	CAN1 - Error Counter High (Receive)	ERRCNTH1		R
000806H	CAN1 - Bit Timing Register Low	BTRL1	BTR1	R/W
000807H	CAN1 - Bit Timing Register High	BTRH1		R/W

I/O map MB96(F)35x (23 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000808H	CAN1 - Interrupt Register Low	INTRL1	INTR1	R
000809H	CAN1 - Interrupt Register High	INTRH1		R
00080AH	CAN1 - Test Register Low	TESTRL1	TESTR1	R/W
00080BH	CAN1 - Test Register High (reserved)	TESTRH1		R
00080CH	CAN1 - BRP Extension register Low	BRPERL1	BRPER1	R/W
00080DH	CAN1 - BRP Extension register High (reserved)	BRPERH1		R
00080EH-00080FH	Reserved			-
000810H	CAN1 - IF1 Command request register Low	IF1CREQL1	IF1CREQ1	R/W
000811H	CAN1 - IF1 Command request register High	IF1CREQH1		R/W
000812H	CAN1 - IF1 Command Mask register Low	IF1CMSKL1	IF1CMSK1	R/W
000813H	CAN1 - IF1 Command Mask register High (reserved)	IF1CMSKH1		R
000814H	CAN1 - IF1 Mask 1 Register Low	IF1MSK1L1	IF1MSK11	R/W
000815H	CAN1 - IF1 Mask 1 Register High	IF1MSK1H1		R/W
000816H	CAN1 - IF1 Mask 2 Register Low	IF1MSK2L1	IF1MSK21	R/W
000817H	CAN1 - IF1 Mask 2 Register High	IF1MSK2H1		R/W
000818H	CAN1 - IF1 Arbitration 1 Register Low	IF1ARB1L1	IF1ARB11	R/W
000819H	CAN1 - IF1 Arbitration 1 Register High	IF1ARB1H1		R/W
00081AH	CAN1 - IF1 Arbitration 2 Register Low	IF1ARB2L1	IF1ARB21	R/W
00081BH	CAN1 - IF1 Arbitration 2 Register High	IF1ARB2H1		R/W
00081CH	CAN1 - IF1 Message Control Register Low	IF1MCTRL1	IF1MCTR1	R/W
00081DH	CAN1 - IF1 Message Control Register High	IF1MCTRH1		R/W
00081EH	CAN1 - IF1 Data A1 Low	IF1DTA1L1	IF1DTA11	R/W
00081FH	CAN1 - IF1 Data A1 High	IF1DTA1H1		R/W
000820H	CAN1 - IF1 Data A2 Low	IF1DTA2L1	IF1DTA21	R/W
000821H	CAN1 - IF1 Data A2 High	IF1DTA2H1		R/W
000822H	CAN1 - IF1 Data B1 Low	IF1DTB1L1	IF1DTB11	R/W
000823H	CAN1 - IF1 Data B1 High	IF1DTB1H1		R/W
000824H	CAN1 - IF1 Data B2 Low	IF1DTB2L1	IF1DTB21	R/W
000825H	CAN1 - IF1 Data B2 High	IF1DTB2H1		R/W

I/O map MB96(F)35x (24 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000826H-00083FH	Reserved			-
000840H	CAN1 - IF2 Command request register Low	IF2CREQL1	IF2CREQ1	R/W
000841H	CAN1 - IF2 Command request register High	IF2CREQH1		R/W
000842H	CAN1 - IF2 Command Mask register Low	IF2CMSKL1	IF2CMSK1	R/W
000843H	CAN1 - IF2 Command Mask register High (reserved)	IF2CMSKH1		R
000844H	CAN1 - IF2 Mask 1 Register Low	IF2MSK1L1	IF2MSK11	R/W
000845H	CAN1 - IF2 Mask 1 Register High	IF2MSK1H1		R/W
000846H	CAN1 - IF2 Mask 2 Register Low	IF2MSK2L1	IF2MSK21	R/W
000847H	CAN1 - IF2 Mask 2 Register High	IF2MSK2H1		R/W
000848H	CAN1 - IF2 Arbitration 1 Register Low	IF2ARB1L1	IF2ARB11	R/W
000849H	CAN1 - IF2 Arbitration 1 Register High	IF2ARB1H1		R/W
00084AH	CAN1 - IF2 Arbitration 2 Register Low	IF2ARB2L1	IF2ARB21	R/W
00084BH	CAN1 - IF2 Arbitration 2 Register High	IF2ARB2H1		R/W
00084CH	CAN1 - IF2 Message Control Register Low	IF2MCTRL1	IF2MCTR1	R/W
00084DH	CAN1 - IF2 Message Control Register High	IF2MCTRH1		R/W
00084EH	CAN1 - IF2 Data A1 Low	IF2DTA1L1	IF2DTA11	R/W
00084FH	CAN1 - IF2 Data A1 High	IF2DTA1H1		R/W
000850H	CAN1 - IF2 Data A2 Low	IF2DTA2L1	IF2DTA21	R/W
000851H	CAN1 - IF2 Data A2 High	IF2DTA2H1		R/W
000852H	CAN1 - IF2 Data B1 Low	IF2DTB1L1	IF2DTB11	R/W
000853H	CAN1 - IF2 Data B1 High	IF2DTB1H1		R/W
000854H	CAN1 - IF2 Data B2 Low	IF2DTB2L1	IF2DTB21	R/W
000855H	CAN1 - IF2 Data B2 High	IF2DTB2H1		R/W
000856H-00087FH	Reserved			-
000880H	CAN1 - Transmission Request 1 Register Low	TREQR1L1	TREQR11	R
000881H	CAN1 - Transmission Request 1 Register High	TREQR1H1		R
000882H	CAN1 - Transmission Request 2 Register Low	TREQR2L1	TREQR21	R
000883H	CAN1 - Transmission Request 2 Register High	TREQR2H1		R

I/O map MB96(F)35x (25 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000884H-00088FH	Reserved			-
000890H	CAN1 - New Data 1 Register Low	NEWDT1L1	NEWDT11	R
000891H	CAN1 - New Data 1 Register High	NEWDT1H1		R
000892H	CAN1 - New Data 2 Register Low	NEWDT2L1	NEWDT21	R
000893H	CAN1 - New Data 2 Register High	NEWDT2H1		R
000894H-00089FH	Reserved			-
0008A0H	CAN1 - Interrupt Pending 1 Register Low	INTPND1L1	INTPND11	R
0008A1H	CAN1 - Interrupt Pending 1 Register High	INTPND1H1		R
0008A2H	CAN1 - Interrupt Pending 2 Register Low	INTPND2L1	INTPND21	R
0008A3H	CAN1 - Interrupt Pending 2 Register High	INTPND2H1		R
0008A4H-0008AFH	Reserved			-
0008B0H	CAN1 - Message Valid 1 Register Low	MSGVAL1L1	MSGVAL11	R
0008B1H	CAN1 - Message Valid 1 Register High	MSGVAL1H1		R
0008B2H	CAN1 - Message Valid 2 Register Low	MSGVAL2L1	MSGVAL21	R
0008B3H	CAN1 - Message Valid 2 Register High	MSGVAL2H1		R
0008B4H-0008CDH	Reserved			-
0008CEH	CAN1 - Output enable register	COER1		R/W
0008CFH-0008FFH	Reserved			-
000900H	CAN2 - Control register Low	CTRLRL2	CTRLR2	R/W
000901H	CAN2 - Control register High (reserved)	CTRLRH2		R
000902H	CAN2 - Status register Low	STATRL2	STATR2	R/W
000903H	CAN2 - Status register High (reserved)	STATRH2		R
000904H	CAN2 - Error Counter Low (Transmit)	ERRCNTL2	ERRCNT2	R
000905H	CAN2 - Error Counter High (Receive)	ERRCNTH2		R
000906H	CAN2 - Bit Timing Register Low	BTRL2	BTR2	R/W
000907H	CAN2 - Bit Timing Register High	BTRH2		R/W
000908H	CAN2 - Interrupt Register Low	INTRL2	INTR2	R

I/O map MB96(F)35x (26 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000909H	CAN2 - Interrupt Register High	INTRH2		R
00090AH	CAN2 - Test Register Low	TESTRL2	TESTR2	R/W
00090BH	CAN2 - Test Register High (reserved)	TESTRH2		R
00090CH	CAN2 - BRP Extension register Low	BRPERL2	BRPER2	R/W
00090DH	CAN2 - BRP Extension register High (reserved)	BRPERH2		R
00090EH-00090FH	Reserved			-
000910H	CAN2 - IF1 Command request register Low	IF1CREQL2	IF1CREQ2	R/W
000911H	CAN2 - IF1 Command request register High	IF1CREQH2		R/W
000912H	CAN2 - IF1 Command Mask register Low	IF1CMSKL2	IF1CMSK2	R/W
000913H	CAN2 - IF1 Command Mask register High (reserved)	IF1CMSKH2		R
000914H	CAN2 - IF1 Mask 1 Register Low	IF1MSK1L2	IF1MSK12	R/W
000915H	CAN2 - IF1 Mask 1 Register High	IF1MSK1H2		R/W
000916H	CAN2 - IF1 Mask 2 Register Low	IF1MSK2L2	IF1MSK22	R/W
000917H	CAN2 - IF1 Mask 2 Register High	IF1MSK2H2		R/W
000918H	CAN2 - IF1 Arbitration 1 Register Low	IF1ARB1L2	IF1ARB12	R/W
000919H	CAN2 - IF1 Arbitration 1 Register High	IF1ARB1H2		R/W
00091AH	CAN2 - IF1 Arbitration 2 Register Low	IF1ARB2L2	IF1ARB22	R/W
00091BH	CAN2 - IF1 Arbitration 2 Register High	IF1ARB2H2		R/W
00091CH	CAN2 - IF1 Message Control Register Low	IF1MCTRL2	IF1MCTR2	R/W
00091DH	CAN2 - IF1 Message Control Register High	IF1MCTRH2		R/W
00091EH	CAN2 - IF1 Data A1 Low	IF1DTA1L2	IF1DTA12	R/W
00091FH	CAN2 - IF1 Data A1 High	IF1DTA1H2		R/W
000920H	CAN2 - IF1 Data A2 Low	IF1DTA2L2	IF1DTA22	R/W
000921H	CAN2 - IF1 Data A2 High	IF1DTA2H2		R/W
000922H	CAN2 - IF1 Data B1 Low	IF1DTB1L2	IF1DTB12	R/W
000923H	CAN2 - IF1 Data B1 High	IF1DTB1H2		R/W
000924H	CAN2 - IF1 Data B2 Low	IF1DTB2L2	IF1DTB22	R/W
000925H	CAN2 - IF1 Data B2 High	IF1DTB2H2		R/W

I/O map MB96(F)35x (27 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000926H-00093FH	Reserved			-
000940H	CAN2 - IF2 Command request register Low	IF2CREQL2	IF2CREQ2	R/W
000941H	CAN2 - IF2 Command request register High	IF2CREQH2		R/W
000942H	CAN2 - IF2 Command Mask register Low	IF2CMSKL2	IF2CMSK2	R/W
000943H	CAN2 - IF2 Command Mask register High (reserved)	IF2CMSKH2		R
000944H	CAN2 - IF2 Mask 1 Register Low	IF2MSK1L2	IF2MSK12	R/W
000945H	CAN2 - IF2 Mask 1 Register High	IF2MSK1H2		R/W
000946H	CAN2 - IF2 Mask 2 Register Low	IF2MSK2L2	IF2MSK22	R/W
000947H	CAN2 - IF2 Mask 2 Register High	IF2MSK2H2		R/W
000948H	CAN2 - IF2 Arbitration 1 Register Low	IF2ARB1L2	IF2ARB12	R/W
000949H	CAN2 - IF2 Arbitration 1 Register High	IF2ARB1H2		R/W
00094AH	CAN2 - IF2 Arbitration 2 Register Low	IF2ARB2L2	IF2ARB22	R/W
00094BH	CAN2 - IF2 Arbitration 2 Register High	IF2ARB2H2		R/W
00094CH	CAN2 - IF2 Message Control Register Low	IF2MCTRL2	IF2MCTR2	R/W
00094DH	CAN2 - IF2 Message Control Register High	IF2MCTRH2		R/W
00094EH	CAN2 - IF2 Data A1 Low	IF2DTA1L2	IF2DTA12	R/W
00094FH	CAN2 - IF2 Data A1 High	IF2DTA1H2		R/W
000950H	CAN2 - IF2 Data A2 Low	IF2DTA2L2	IF2DTA22	R/W
000951H	CAN2 - IF2 Data A2 High	IF2DTA2H2		R/W
000952H	CAN2 - IF2 Data B1 Low	IF2DTB1L2	IF2DTB12	R/W
000953H	CAN2 - IF2 Data B1 High	IF2DTB1H2		R/W
000954H	CAN2 - IF2 Data B2 Low	IF2DTB2L2	IF2DTB22	R/W
000955H	CAN2 - IF2 Data B2 High	IF2DTB2H2		R/W
000956H-00097FH	Reserved			-
000980H	CAN2 - Transmission Request 1 Register Low	TREQR1L2	TREQR12	R
000981H	CAN2 - Transmission Request 1 Register High	TREQR1H2		R
000982H	CAN2 - Transmission Request 2 Register Low	TREQR2L2	TREQR22	R
000983H	CAN2 - Transmission Request 2 Register High	TREQR2H2		R

I/O map MB96(F)35x (28 of 28)

Address	Register	Abbreviation 8-bit access	Abbreviation 16-bit access	Access
000984H-00098FH	Reserved			-
000990H	CAN2 - New Data 1 Register Low	NEWDT1L2	NEWDT12	R
000991H	CAN2 - New Data 1 Register High	NEWDT1H2		R
000992H	CAN2 - New Data 2 Register Low	NEWDT2L2	NEWDT22	R
000993H	CAN2 - New Data 2 Register High	NEWDT2H2		R
000994H-00099FH	Reserved			-
0009A0H	CAN2 - Interrupt Pending 1 Register Low	INTPND1L2	INTPND12	R
0009A1H	CAN2 - Interrupt Pending 1 Register High	INTPND1H2		R
0009A2H	CAN2 - Interrupt Pending 2 Register Low	INTPND2L2	INTPND22	R
0009A3H	CAN2 - Interrupt Pending 2 Register High	INTPND2H2		R
0009A4H-0009AFH	Reserved			-
0009B0H	CAN2 - Message Valid 1 Register Low	MSGVAL1L2	MSGVAL12	R
0009B1H	CAN2 - Message Valid 1 Register High	MSGVAL1H2		R
0009B2H	CAN2 - Message Valid 2 Register Low	MSGVAL2L2	MSGVAL22	R
0009B3H	CAN2 - Message Valid 2 Register High	MSGVAL2H2		R
0009B4H-0009CDH	Reserved			-
0009CEH	CAN2 - Output enable register	COER2		R/W
0009CFH-000BFFH	Reserved			-

Note: Any write access to reserved addresses in the I/O map should not be performed. A read access to a reserved address results in reading ‘X’.
Registers of resources which are described in this table, but which are not supported by the device, should also be handled as “Reserved”.

■ INTERRUPT VECTOR TABLE

Interrupt vector table MB96(F)35x (1 of 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	3FC$_H$	CALLV0	No	-	
1	3F8$_H$	CALLV1	No	-	
2	3F4$_H$	CALLV2	No	-	
3	3F0$_H$	CALLV3	No	-	
4	3EC$_H$	CALLV4	No	-	
5	3E8$_H$	CALLV5	No	-	
6	3E4$_H$	CALLV6	No	-	
7	3E0$_H$	CALLV7	No	-	
8	3DC$_H$	RESET	No	-	
9	3D8$_H$	INT9	No	-	
10	3D4$_H$	EXCEPTION	No	-	
11	3D0$_H$	NMI	No	-	Non-Maskable Interrupt
12	3CC$_H$	DLY	No	12	Delayed Interrupt
13	3C8$_H$	RC_TIMER	No	13	RC Timer
14	3C4$_H$	MC_TIMER	No	14	Main Clock Timer
15	3C0$_H$	SC_TIMER	No	15	Sub Clock Timer
16	3BC$_H$	PLL_UNLOCK	No	16	Reserved
17	3B8$_H$	EXTINT0	Yes	17	External Interrupt 0
18	3B4$_H$				Reserved
19	3B0$_H$	EXTINT2	Yes	19	External Interrupt 2
20	3AC$_H$	EXTINT3	Yes	20	External Interrupt 3
21	3A8$_H$	EXTINT4	Yes	21	External Interrupt 4
22	3A4$_H$				Reserved
23	3A0$_H$	EXTINT7	Yes	23	External Interrupt 7
24	39C$_H$	EXTINT8	Yes	24	External Interrupt 8
25	398$_H$	EXTINT9	Yes	25	External Interrupt 9
26	394$_H$	EXTINT10	Yes	26	External Interrupt 10
27	390$_H$	EXTINT11	Yes	27	External Interrupt 11
28	38C$_H$	EXTINT12	Yes	28	External Interrupt 12
29	388$_H$	EXTINT13	Yes	29	External Interrupt 13
30	384$_H$	EXTINT14	Yes	30	External Interrupt 14
31	380$_H$	EXTINT15	Yes	31	External Interrupt 15
32	37C$_H$	CAN1	No	32	CAN Controller 1 (only MB96F356Y/R)

Interrupt vector table MB96(F)35x (2 of 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
33	378H	CAN2	No	33	CAN Controller 2 (only MB96F356Y/R and MB96F353R/F355R)
34	374H	PPG0	Yes	34	Programmable Pulse Generator 0
35	370H	PPG1	Yes	35	Programmable Pulse Generator 1
36	36CH	PPG2	Yes	36	Programmable Pulse Generator 2
37	368H	PPG3	Yes	37	Programmable Pulse Generator 3
38	364H	PPG4	Yes	38	Programmable Pulse Generator 4
39	360	PPG5	Yes	39	Programmable Pulse Generator 5
40	35CH	PPG6	Yes	40	Programmable Pulse Generator 6
41	358H	PPG7	Yes	41	Programmable Pulse Generator 7
42	354H	PPG8	Yes	42	Programmable Pulse Generator 8
43	350H	PPG9	Yes	43	Programmable Pulse Generator 9
44	34CH	PPG10	Yes	44	Programmable Pulse Generator 10
45	348H	PPG11	Yes	45	Programmable Pulse Generator 11
46	344H	PPG12	Yes	46	Programmable Pulse Generator 12
47	340H	PPG13	Yes	47	Programmable Pulse Generator 13
48	33CH	PPG14	Yes	48	Programmable Pulse Generator 14
49	338H	PPG15	Yes	49	Programmable Pulse Generator 15
50	334H	PPG16	Yes	50	Programmable Pulse Generator 16
51	330H	PPG17	Yes	51	Programmable Pulse Generator 17
52	32CH	PPG18	Yes	52	Programmable Pulse Generator 18
53	328H	PPG19	Yes	53	Programmable Pulse Generator 19
54	324H	RLT0	Yes	54	Reload Timer 0
55	320H	RLT1	Yes	55	Reload Timer 1
56	31CH	RLT2	Yes	56	Reload Timer 2
57	318H	RLT3	Yes	57	Reload Timer 3
58	314H	PPGRLT	Yes	58	Reload Timer 6 - dedicated for PPG
59	310H	ICU0	Yes	59	Input Capture Unit 0
60	30CH	ICU1	Yes	60	Input Capture Unit 1
61	308H				Reserved
62	304H				Reserved
63	300H	ICU4	Yes	63	Input Capture Unit 4
64	2FCH	ICU5	Yes	64	Input Capture Unit 5
65	2F8H	ICU6	Yes	65	Input Capture Unit 6
66	2F4H	ICU7	Yes	66	Input Capture Unit 7

Interrupt vector table MB96(F)35x (3 of 3)

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
67	2F0H				Reserved
68	2ECH	ICU9	Yes	68	Input Capture Unit 9
69	2E8H	ICU10	Yes	69	Input Capture Unit 10
70	2E4H				Reserved
71	2E0H	OCU4	Yes	71	Output Compare Unit 4
72	2DCH	OCU5	Yes	72	Output Compare Unit 5
73	2D8H	OCU6	Yes	73	Output Compare Unit 6
74	2D4H	OCU7	Yes	74	Output Compare Unit 7
75	2D0H				Reserved
76	2CCH				Reserved
77	2C8H	FRT0	Yes	77	Free Running Timer 0
78	2C4H	FRT1	Yes	78	Free Running Timer 1
79	2C0H	FRT2	Yes	79	Free Running Timer 2
80	2BCH	FRT3	Yes	80	Free Running Timer 3
81	2B8H	RTC0	No	81	Real Timer Clock
82	2B4H	CAL0	No	82	Clock Calibration Unit
83	2B0H	IIC0	Yes	83	I2C interface
84	2ACH	ADC0	Yes	84	A/D Converter
85	2A8H	LINR2	Yes	85	LIN USART 2 RX
86	2A4H	LINT2	Yes	86	LIN USART 2 TX
87	2A0H	LINR3	Yes	87	LIN USART 3 RX
88	29CH	LINT3	Yes	88	LIN USART 3 TX
89	298H	LINR7	Yes	89	LIN USART 7 RX
90	294H	LINT7	Yes	90	LIN USART 7 TX
91	290H	LINR8	Yes	91	LIN USART 8 RX
92	28CH	LINT8	Yes	92	LIN USART 8 TX
93	288H	FLASH_A	No	93	Flash memory A (only Flash devices)

■ HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Unused sub clock signal
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on energization
- Stabilization of power supply voltage
- Serial communication

1. Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

2. Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. They must therefore be pulled up or pulled down through resistors. To prevent latch-up, those resistors should be more than 2 kΩ.

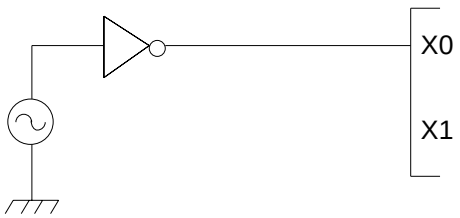
Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

3. External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration. See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

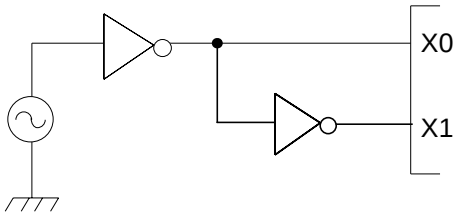
1. Single phase external clock

- When using a single phase external clock, X0 pin must be driven and X1 pin left open.



2. Opposite phase external clock

- When using an opposite phase external clock, X1 (X1A) must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins.



4. Unused sub clock signal

If the pins X0A and X1A are not connected to an oscillator, a pull-down resistor must be connected on the X0A pin and the X1A pin must be left open.

5. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

6. Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between V_{CC} and V_{SS} as close as possible to V_{CC} and V_{SS} pins.

7. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

8. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AV_{CC} (turning the analog and digital power supplies simultaneously on or off is acceptable).

9. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

10. Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2 V to 2.7 V.

11. Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the Vcc power supply voltage, a malfunction may occur. The Vcc power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that Vcc ripple fluctuations (peak to peak value) in the commercial frequencies (50 to 60 Hz) fall within 10% of the standard Vcc power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

12. Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

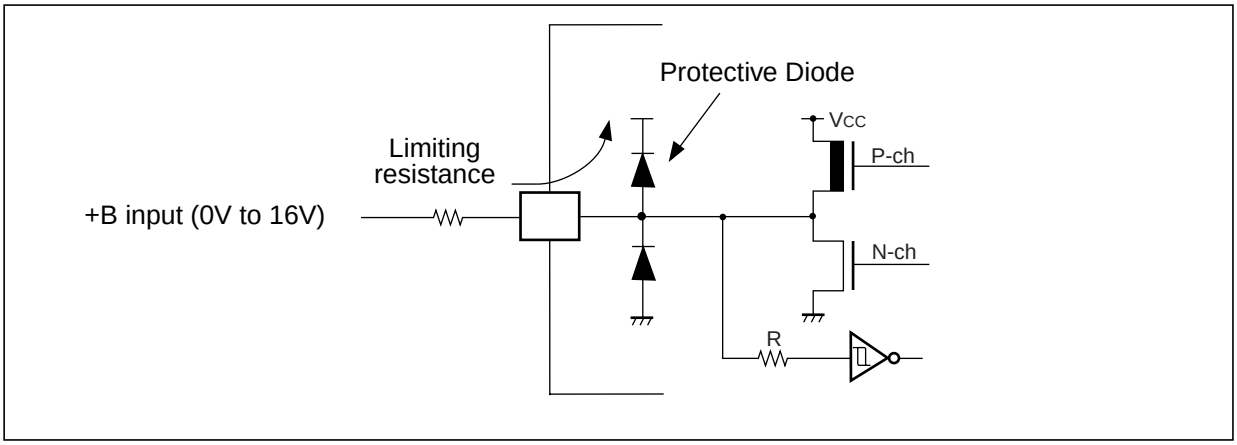
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$ *1
AD Converter voltage references	AVRH, AVRL	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, $AVRH > AVRL$, $AVRL \geq AV_{SS}$
Input voltage	V_I	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V *2
Output voltage	V_O	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V *2
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	Applicable to general purpose I/O pins *3
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	40	mA	Applicable to general purpose I/O pins *3
“L” level maximum output current	I_{OL1}	-	15	mA	Normal outputs with driving strength set to 5mA
“L” level average output current	I_{OLAV1}	-	5	mA	Normal outputs with driving strength set to 5mA
“L” level maximum overall output current	ΣI_{OL1}	-	100	mA	Normal outputs
“L” level average overall output current	ΣI_{OLAV1}	-	50	mA	Normal outputs
”H” level maximum output current	I_{OH1}	-	-15	mA	Normal outputs with driving strength set to 5mA
”H” level average output current	I_{OHAV1}	-	-5	mA	Normal outputs with driving strength set to 5mA
”H” level maximum overall output current	ΣI_{OH1}	-	-100	mA	Normal outputs
”H” level average overall output current	ΣI_{OHAV1}	-	-50	mA	Normal outputs
Permitted Power dissipation (Flash devices) *4	P_D	-	320*5	mW	T_A=105°C
		-	640*5	mW	T_A=85°C
		-	800*5	mW	T_A=75°C
		-	400*5	mW	T_A=125°C, no Flash program/ erase *6
		-	560*5	mW	T_A=115°C, no Flash program/ erase *6
Operating ambient temperature	T_A	0	+70	°C	MB96V300B
		-40	+105		
		-40	+125		*6
Storage temperature	T_{STG}	-55	+150	°C	

*1: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} neither when the power is switched on.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should also not exceed the specified ratings. However if the maximum current to/from a input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/output voltages of standard ports depend on V_{CC}.

*3:
- Applicable to all general purpose I/O pins (Pnn_m)
- Use within recommended operating conditions.
- Use at DC voltage (current)
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset (except devices with persistent low voltage reset in internal vector mode).

- Sample recommended circuits:



*4: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \sum (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{CC} * (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming or the clock modulator.
I_A is the analog current consumption into AV_{CC}.

*5: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*6: Please contact Fujitsu for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.0	-	5.5	V	
Smoothing capacitor at C pin	C_S	3.5	4.7 - 10	15	µF	Use a low inductance capacitor (for example X7R ceramic capacitor)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC characteristics

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IH}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			CMOS Hysteresis 0.7/0.3 input selected	0.7 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} \geq 4.5V$
				0.74 V_{CC}	-	V_{CC} + 0.3	V	$V_{CC} < 4.5V$
			AUTOMOTIVE Hysteresis input selected	0.8 V_{CC}	-	V_{CC} + 0.3	V	
			TTL input selected	2.0	-	V_{CC} + 0.3	V	
	V_{IHX0F}	X0	External clock in “Fast Clock Input mode”	0.8 V_{CC}	-	V_{CC} + 0.3	V	
	V_{IHX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	2.5	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	0.8 V_{CC}	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD2-MD0	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	
Input L voltage	V_{IL}	Port inputs Pnn_m	CMOS Hysteresis 0.8/0.2 input selected	V_{SS} - 0.3	-	0.2 V_{CC}	V	
			CMOS Hysteresis 0.7/0.3 input selected	V_{SS} - 0.3	-	0.3 V_{CC}	V	
			AUTOMOTIVE Hysteresis input selected	V_{SS} - 0.3	-	0.5 V_{CC}	V	$V_{CC} \geq 4.5V$
				V_{SS} - 0.3	-	0.46 V_{CC}		$V_{CC} < 4.5V$
			TTL input selected	V_{SS} - 0.3	-	0.8	V	
	V_{ILX0F}	X0	External clock in “Fast Clock Input mode”	V_{SS} - 0.3	-	0.2 V_{CC}	V	
	V_{ILX0S}	X0,X1, X0A,X1A	External clock in “oscillation mode”	V_{SS} - 0.3	-	0.4	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	0.2 V_{CC}	V	CMOS Hysteresis input
	V_{ILM}	MD2-MD0	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output H voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -2mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -1.6mA	V_{CC} - 0.5	-	-	V	Driving strength set to 2mA
	V_{OH5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -5mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -3mA	V_{CC} - 0.5	-	-	V	Driving strength set to 5mA
	V_{OH3}	3mA out-puts	4.5V ≤ V_{CC} ≤ 5.5V I_{OH} = -3mA 3.0V ≤ V_{CC} < 4.5V I_{OH} = -2mA	V_{CC} - 0.5	-	-	V	
Output L voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +2mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +1.6mA	-	-	0.4	V	Driving strength set to 2mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{CC} ≤ 5.5V I_{OL} = +5mA 3.0V ≤ V_{CC} < 4.5V I_{OL} = +3mA	-	-	0.4	V	Driving strength set to 5mA
	V_{OL3}	3mA out-puts	3.0V ≤ V_{CC} ≤ 5.5V I_{OL} = +3mA	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	V_{SS} < V_I < V_{CC} AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	-1	-	+1	µA	Single port pin
Pull-up resistance	R_{UP}	Pnn_m, RSTX	V_{CC} = 3.3V ± 10%	40	100	160	kΩ	
			V_{CC} = 5.0V ± 10%	25	50	100	kΩ	

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCPLL}	PLL Run mode with CLKS1/2 = 48MHz, CLKB = CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	35	44	mA	0 Flash wait states
			+125˚C	36	47		
		PLL Run mode with CLKS1/2 = CLKB = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	44	57	mA	2 Flash wait states
			+125˚C	45	60		
		PLL Run mode with CLKS1/2 = 96MHz, CLKB = CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	49	62	mA	1 Flash wait state
			+125˚C	50	65		
	I_{CCMAIN}	Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25˚C	4.5	5.5	mA	1 Flash wait state
			+125˚C	5.1	8.5		
	I_{CCRCH}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25˚C	2.9	4	mA	1 Flash wait state
			+125˚C	3.5	6.5		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Run modes*	I_{CCRCL}	RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.4	0.6	mA	MB96F356 at 1 Flash wait state
			+125˚C	0.9	3.5		
			+25˚C	0.18	0.3	mA	MB96F353/F355 at 1 Flash wait state
			+125˚C	0.68	3.3		
		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = 100kHz, SMCR:LPMS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode, no Flash programming/erasing allowed)	+25˚C	0.15	0.25	mA	1 Flash wait state
			+125˚C	0.65	3.2		
	I_{CCSUB}	Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped, no Flash programming/erasing allowed)	+25˚C	0.1	0.2	mA	1 Flash wait state
			+125˚C	0.6	3		
Power supply current in Sleep modes*	I_{CCSPLL}	PLL Sleep mode with CLKS1/2 = 48MHz, CLKP1/2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	9	10.5	mA	
			+125˚C	9.7	13		
		PLL Sleep mode with CLKS1/2 = CLKP1= 56MHz, CLKP2 = 28MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	14	15.5	mA	
			+125˚C	14.8	18		
		PLL Sleep mode with CLKS1/2 = 96MHz, CLKP1= 48MHz, CLKP2 = 24MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	15	16.5	mA	
			+125˚C	15.8	19		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Sleep modes*	$I_{CCSMAIN}$	Main Sleep mode with CLKS1/2 = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	+25˚C	1.5	1.8	mA	
			+125˚C	2	4.5		
	I_{CCSRCH}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 2MHz (CLKMC, CLKPLL and CLKSC stopped)	+25˚C	0.8	1.3	mA	
			+125˚C	1.4	4		
	I_{CCSRCL}	RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.3	0.5	mA	MB96F356
			+125˚C	0.8	3.4		
			+25˚C	0.09	0.2	mA	MB96F353/F355
			+125˚C	0.59	3.1		
		RC Sleep mode with CLKS1/2 = CLKP1/2 = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.06	0.15	mA	
			+125˚C	0.56	3		
	I_{CCSSUB}	Sub Sleep mode with CLKS1/2 = CLKP1/2 = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25˚C	0.04	0.12	mA	
			+125˚C	0.54	2.9		
Power supply current in Timer modes*	I_{CCTPLL}	PLL Timer mode with CLKMC = 4MHz, CLKPLL = 48MHz (CLKRC and CLKSC stopped. Core voltage at 1.9V)	+25˚C	1.6	2	mA	
			+125˚C	2.1	4.8		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Timer modes*	$I_{CCTMAIN}$	Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.35	0.5	mA	MB96F356
			+125˚C	0.85	3.3		
			+25˚C	0.13	0.2	mA	MB96F353/F355
			+125˚C	0.63	3		
		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 1 (CLKPLL, CLKRC and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.1	0.15	mA	
			+125˚C	0.6	2.9		
	I_{CCTRCH}	RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.35	0.5	mA	MB96F356
			+125˚C	0.85	3.3		
			+25˚C	0.13	0.2	mA	MB96F353/F355
			+125˚C	0.63	3		
		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.1	0.15	mA	
			+125˚C	0.6	2.9		
	I_{CCTRCL}	RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in high power mode)	+25˚C	0.3	0.45	mA	MB96F356
			+125˚C	0.8	3.2		
			+25˚C	0.08	0.15	mA	MB96F353/F355
			+125˚C	0.58	2.95		
		RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 1 (CLKMC, CLKPLL and CLKSC stopped. Voltage regulator in low power mode)	+25˚C	0.05	0.1	mA	
			+125˚C	0.55	2.85		
	I_{CCTSUB}	Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	+25˚C	0.03	0.1	mA	
			+125˚C	0.53	2.85		

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Condition (at T_A)		Value			Remarks
				Typ	Max	Unit	
Power supply current in Stop Mode	I_{CCH}	VRCR:LPMB[2:0] = 110_B (Core voltage at 1.8V)	+25˚C	0.02	0.08	mA	
			+125˚C	0.52	2.8		
		VRCR:LPMB[2:0] = 000_B (Core voltage at 1.2V)	+25˚C	0.015	0.06	mA	
			+125˚C	0.4	2.3		
Power supply current for active Low Voltage detector	I_{CCLVD}	Low voltage detector enabled (RCR:LVDE = 1)	-	5	10	µA	MB96F353/F355 Must be added to all current above
			+25˚C	90	140	µA	MB96F356 Must be added to all current above
			+125˚C	100	150		
Power supply current for active Clock modulator	$I_{CCCLOMO}$	Clock modulator enabled (CMCR:PDX = 1)	-	3	4.5	mA	Must be added to all current above
Flash Write/Erase current	$I_{CCFLASH}$	Current for one Flash module	-	15	40	mA	Must be added to all current above
Input capacitance	C_{IN}	-	-	5	15	pF	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}

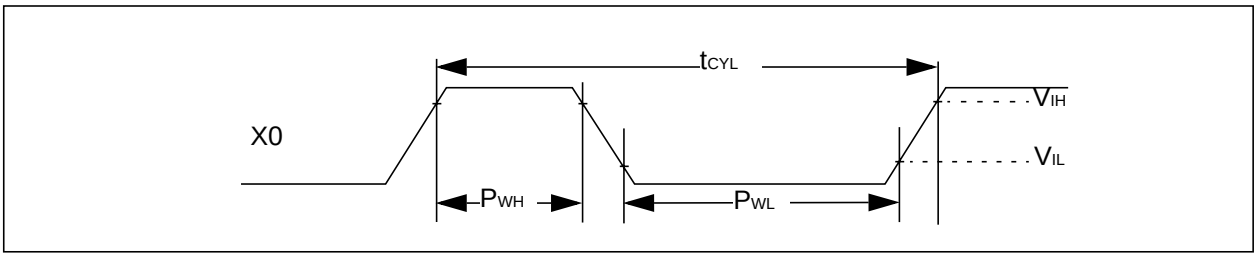
* The power supply current is measured with a 4MHz external clock connected to the Main oscillator and a 32kHz external clock connected to the Sub oscillator. See chapter “Standby mode and voltage regulator control circuit” of the Hardware Manual for further details about voltage regulator control.

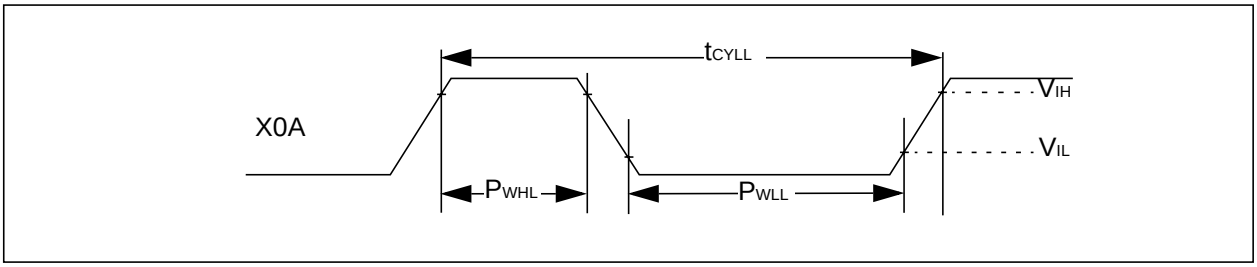
4. AC Characteristics

Source Clock timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	-	16	MHz	When using a crystal oscillator, PLL off
			0	-	16	MHz	When using an opposite phase external clock, PLL off
			3.5	-	16	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Clock frequency	f_{FCI}	X0	0	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL off
			3.5	-	56	MHz	When using a single phase external clock in “Fast Clock Input mode” , PLL on
Clock frequency	f_{CL}	X0A, X1A	32	32.768	100	kHz	When using an oscillation circuit
			0	-	100	kHz	When using an opposite phase external clock
		X0A	0	-	50	kHz	When using a single phase external clock
Clock frequency	f_{CR}	-	50	100	200	kHz	When using slow frequency of RC oscillator
			1	2	4	MHz	When using fast frequency of RC oscillator
PLL Clock frequency	f_{CLKVCO}	-	64	-	200	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL Phase Jitter	T_{PSKEW}	-	-	-	± 5	ns	For CLKMC (PLL input clock) ≥ 4MHz
Input clock pulse width	P_{WH}, P_{WL}	X0,X1	8	-	-	ns	Duty ratio is about 30% to 70%
Input clock pulse width	P_{WHL}, P_{WLL}	X0A,X1A	5	-	-	µs	





Internal Clock timing

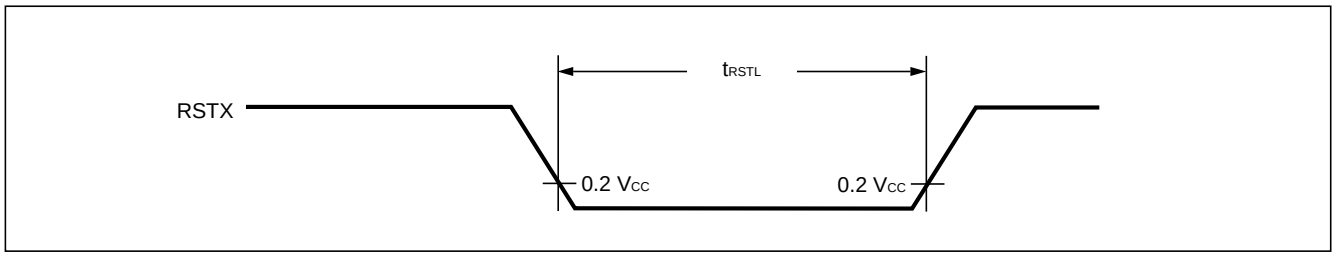
(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Core Voltage Settings				Unit	Remarks
		1.8V		1.9V			
		Min	Max	Min	Max		
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	0	92	0	96	MHz	Others than below
		0	88	0	96	MHz	MB96F356
Internal CPU clock frequency (CLKB), internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	0	52	0	56	MHz	
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	0	28	0	32	MHz	

External Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

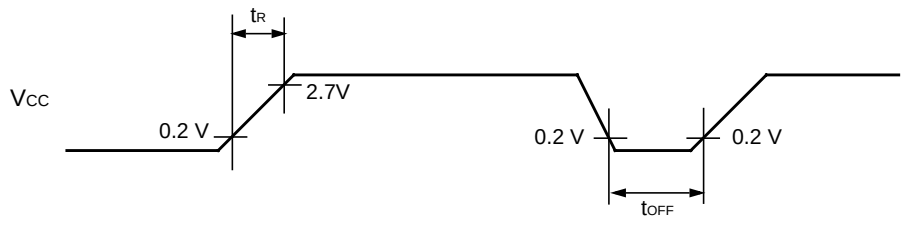
Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Reset input time	t_{RSTL}	RSTX	500	-	-	ns	



Power On Reset timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Power on rise time	t_R	Vcc	0.05	-	30	ms	
Power off time	t_{OFF}	Vcc	1	-	-	ms	



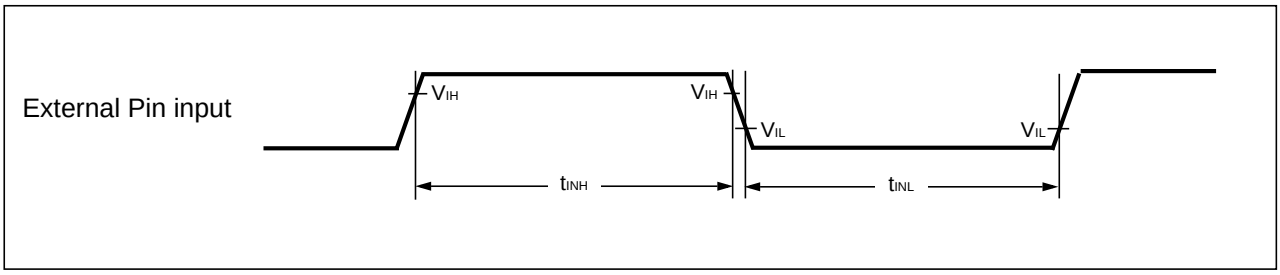
If the power supply is changed too rapidly, a power-on reset may occur.
We recommend a smooth startup by restraining voltages when changing the power supply voltage during operation, as shown in the figure below.

External Input timing

(T_A = -40˚C to 125˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Condition	Value		Unit	Used Pin input function
				Min	Max		
Input pulse width	t_{INH} t_{INL}	INTn(_R)	—	200	—	ns	External Interrupt
		NMI(_R)					NMI
		Pnn_m		$2*t_{CLKP1}$ + 200 (t_{CLKP1}=1/ f_{CLKP1})	—	ns	General Purpose IO
		TINn(_R)					Reload Timer
		TTGn(_R)					PPG Trigger input
		ADTG(_R)					AD Converter Trigger
		FRCKn(_R)					Free Running Timer external clock
		INn(_R)					Input Capture

Note : Relocated Resource Inputs have same characteristics



External Bus timing

Note: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

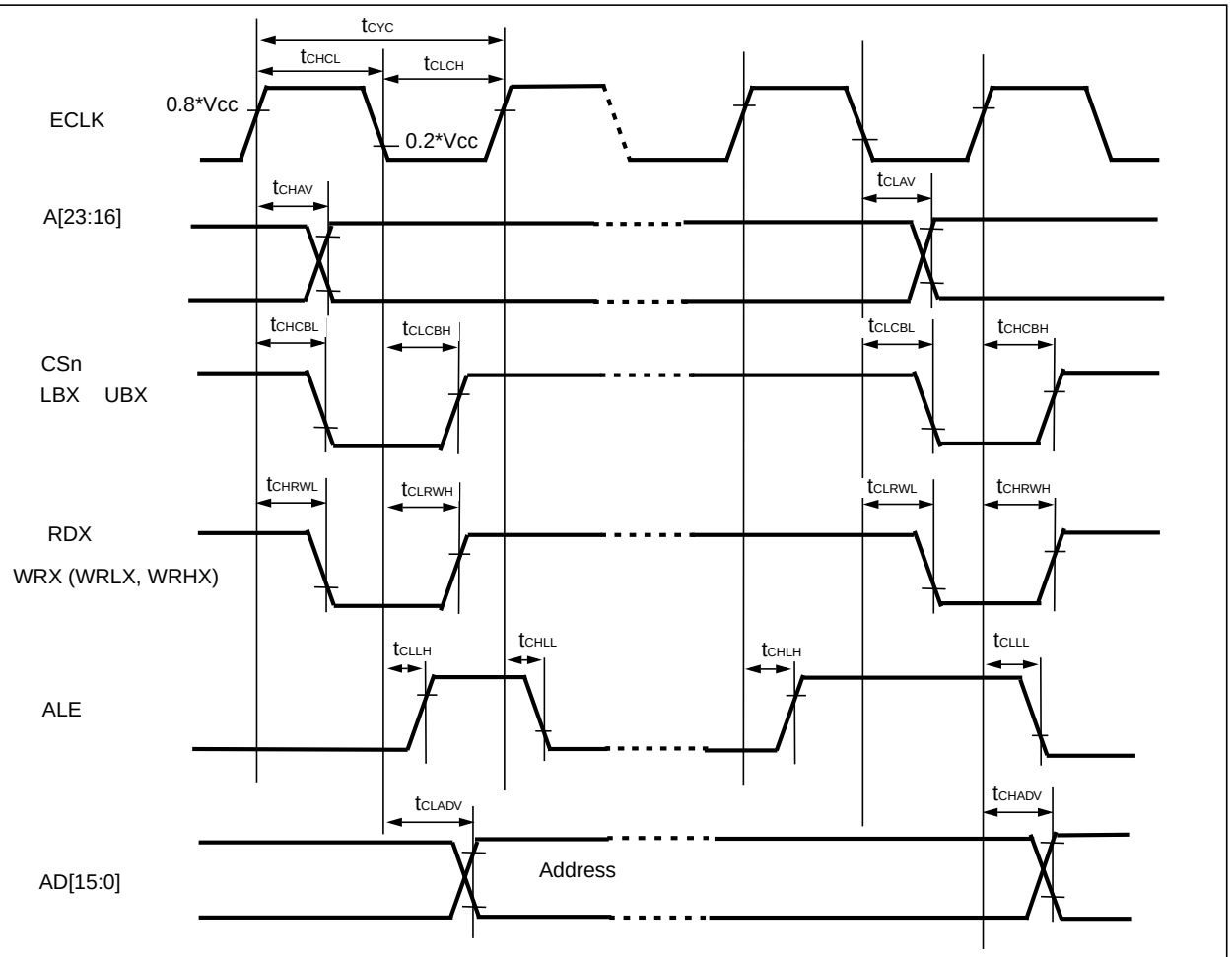
Basic Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	25	—	ns	
	t_{CHCL}			t_{CYC}/2-5	t_{CYC}/2+5		
	t_{CLCH}			t_{CYC}/2-5	t_{CYC}/2+5		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-20	20	ns	
	t_{CHCBL}			-20	20		
	t_{CLCBH}			-20	20		
	t_{CLCBL}			-20	20		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-10	10	ns	
	t_{CHLL}			-10	10		
	t_{CLLH}			-10	10		
	t_{CLLL}			-10	10		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	—	-15	15	ns	
	t_{CLAV}			-15	15		
	t_{CLADV}	AD[15:0], ECLK	—	-15	15	ns	
	t_{CHADV}			-15	15		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX,WRHX, ECLK	—	-10	10	ns	
	t_{CHRWL}			-10	10		
	t_{CLRWH}			-10	10		
	t_{CLRWL}			-10	10		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ECLK	t_{CYC}	ECLK	—	30	—	ns	
	t_{CHCL}			t_{CYC}/2-8	t_{CYC}/2+8		
	t_{CLCH}			t_{CYC}/2-8	t_{CYC}/2+8		
ECLK → UBX/ LBX / CSn time	t_{CHCBH}	CSn, UBX, LBX, ECLK	—	-25	25	ns	
	t_{CHCBL}			-25	25		
	t_{CLCBH}			-25	25		
	t_{CLCBL}			-25	25		
ECLK → ALE time	t_{CHLH}	ALE, ECLK	—	-15	15	ns	
	t_{CHLL}			-15	15		
	t_{CLLH}			-15	15		
	t_{CLLL}			-15	15		
ECLK → address valid time	t_{CHAV}	A[23:16], ECLK	—	-20	20	ns	
	t_{CLAV}			-20	20		
	t_{CLADV}	AD[15:0], ECLK	—	-20	20	ns	
	t_{CHADV}			-20	20		
ECLK → RDX /WRX time	t_{CHRWH}	RDX, WRX, WRLX, WRHX, ECLK	—	-15	15	ns	
	t_{CHRWL}			-15	15		
	t_{CLRWH}			-15	15		
	t_{CLRWL}			-15	15		



Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Read)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 5$	—	ns	
			EACL:STS=1	$t_{CYC} - 5$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 5$	—		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 15$	—		
	t_{ADVLL}	ALE,AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 15$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 15$	—		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	-15	—		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 15$	—	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 15$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 15$	—	ns	
			EACL:ACE=1	$2t_{CYC} - 15$	—		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	—	$3t_{CYC} - 55$	ns	w/o cycle extension
			EACL:ACE=1	—	$4t_{CYC} - 55$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	—	$5t_{CYC}/2 - 55$	ns	w/o cycle extension
			EACL:ACE=1	—	$7t_{CYC}/2 - 55$		
RDX pulse width	t_{RLRH}	RDX	—	$3\ t_{CYC}/2 - 5$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3\ t_{CYC}/2 - 50$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

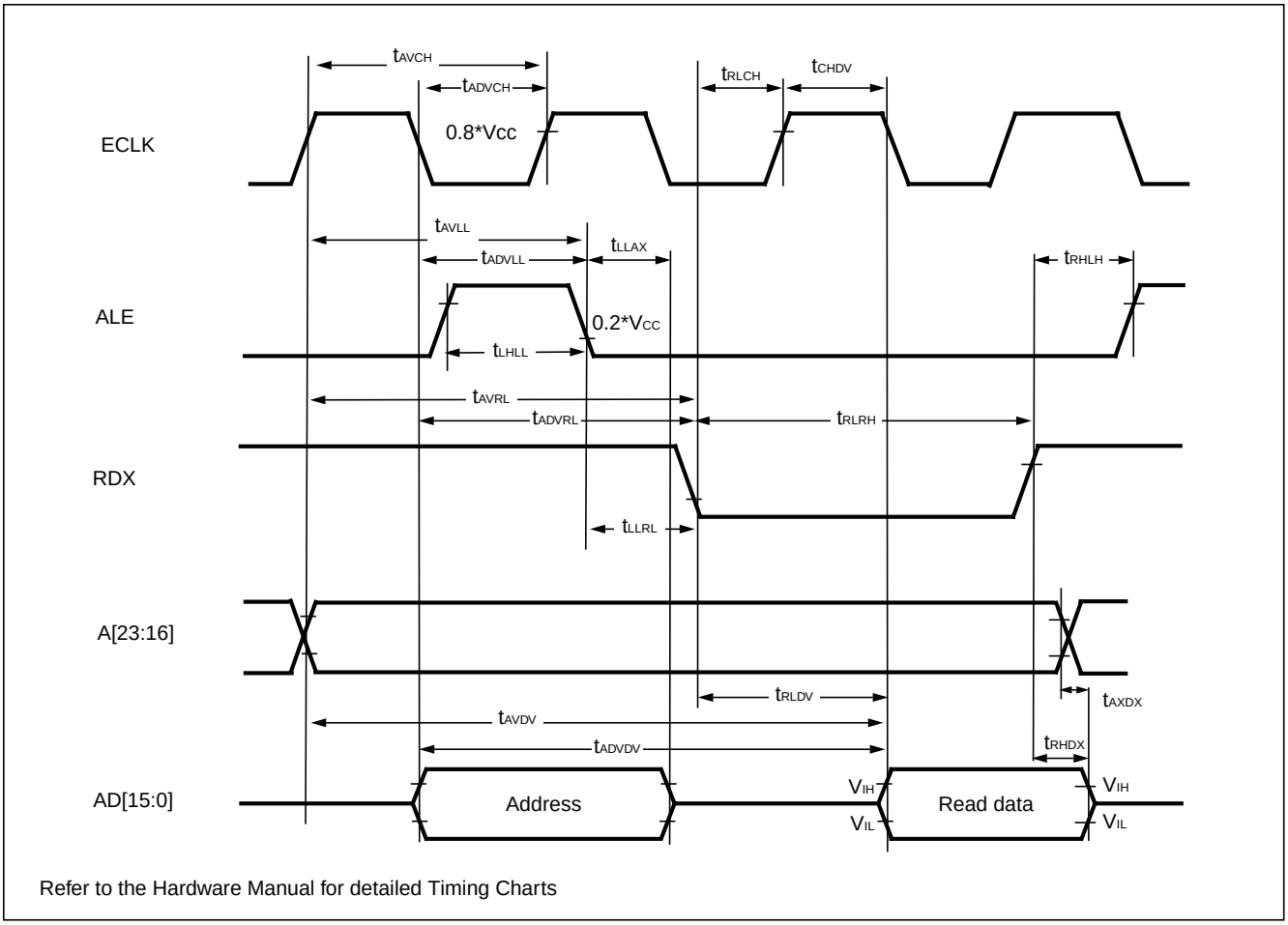
Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16], AD[15:0]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 10$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 10$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	—	$t_{CYC} - 15$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 15$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 10$	—	ns	
			EACL:STS=1	– 10	—		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 50$	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 8$	—	ns	
			EACL:STS=1	$t_{CYC} - 8$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 8$	—		
Valid address ⇒ ALE ↓ time	t_{AVLL}	ALE, A[23:16],	EACL:STS=0 and EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$3t_{CYC}/2 - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$2t_{CYC} - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVLL}	ALE, AD[15:0]	EACL:STS=0 and EACL:ACE=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1 and EACL:ACE=0	$t_{CYC} - 20$	—		
			EACL:STS=0 and EACL:ACE=1	$3t_{CYC}/2 - 20$	—		
			EACL:STS=1 and EACL:ACE=1	$2t_{CYC} - 20$	—		
ALE ↓ ⇒ Address valid time	t_{LLAX}	ALE, AD[15:0]	EACL:STS=0	$t_{CYC}/2 - 20$	—	ns	
			EACL:STS=1	-20	—		

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Sym-bol	Pin	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ RDX ↓ time	t_{AVRL}	RDX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVRL}	RDX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	—		
Valid address ⇒ Valid data input	t_{AVDV}	A[23:16], AD[15:0]	EACL:ACE=0	—	$3t_{CYC} - 60$	ns	w/o cycle extension
			EACL:ACE=1	—	$4t_{CYC} - 60$		
	t_{ADVDV}	AD[15:0]	EACL:ACE=0	—	$5t_{CYC}/2 - 60$	ns	w/o cycle extension
			EACL:ACE=1	—	$7t_{CYC}/2 - 60$		
RDX pulse width	t_{RLRH}	RDX	—	$3t_{CYC}/2 - 8$	—	ns	w/o cycle extension
RDX ↓ ⇒ Valid data input	t_{RLDV}	RDX, AD[15:0]	—	—	$3t_{CYC}/2 - 55$	ns	w/o cycle extension
RDX ↑ ⇒ Data hold time	t_{RHDX}	RDX, AD[15:0]	—	0	—	ns	
Address valid ⇒ Data hold time	t_{AXDX}	A[23:16]	—	0	—	ns	
RDX ↑ ⇒ ALE ↑ time	t_{RHLH}	RDX, ALE	EACL:STS=1 and EACL:ACE=1	$3t_{CYC}/2 - 15$	—	ns	
			other ECL:STS, EACL:ACE setting	$t_{CYC}/2 - 15$	—		
Valid address ⇒ ECLK ↑ time	t_{AVCH}	A[23:16], ECLK	—	$t_{CYC} - 20$	—	ns	
	t_{ADVCH}	AD[15:0], ECLK		$t_{CYC}/2 - 20$	—		
RDX ↓ ⇒ ECLK ↑ time	t_{RLCH}	RDX, ECLK	—	$t_{CYC}/2 - 15$	—	ns	
ALE ↓ ⇒ RDX ↓ time	t_{LLRL}	ALE, RDX	EACL:STS=0	$t_{CYC}/2 - 15$	—	ns	
			EACL:STS=1	– 15	—		
ECLK↑ ⇒ Valid data input	t_{CHDV}	AD[15:0], ECLK	—	—	$t_{CYC} - 55$	ns	



Refer to the Hardware Manual for detailed Timing Charts

Bus Timing (Write)

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2$ – 15	—	ns	
			EACL:ACE=1	$5t_{CYC}/2$ – 15	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	t_{CYC} – 15	—	ns	
			EACL:ACE=1	$2t_{CYC}$ – 15	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	t_{CYC} – 5	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	t_{CYC} – 20	—	ns	w/o cycle extension

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

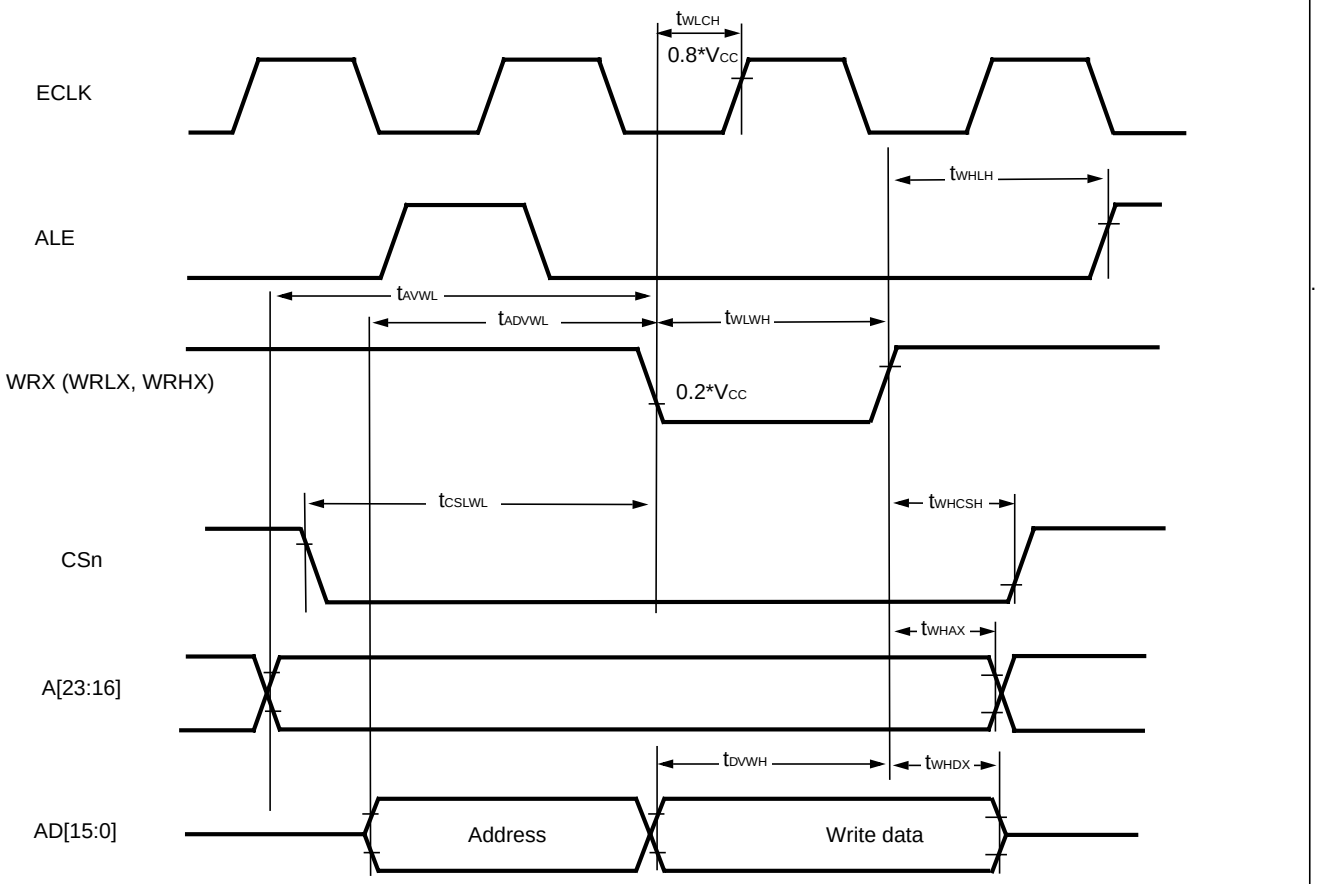
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	—	$t_{CYC}/2 - 15$	—	ns	
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC} - 10$	—	ns	
			other EBM:ACE and EACL:STS setting	$t_{CYC} - 10$	—		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2 - 10$	—	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	—	$3t_{CYC}/2 - 15$	ns	
			EACL:ACE=1	—	$5t_{CYC}/2 - 15$		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	—	$t_{CYC}/2 - 15$	—	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address ⇒ WRX ↓ time	t_{AVWL}	WRX, WRLX, WRHX, A[23:16]	EACL:ACE=0	$3t_{CYC}/2 - 20$	—	ns	
			EACL:ACE=1	$5t_{CYC}/2 - 20$	—		
	t_{ADVWL}	WRX, WRLX, WRHX, AD[15:0]	EACL:ACE=0	$t_{CYC} - 20$	—	ns	
			EACL:ACE=1	$2t_{CYC} - 20$	—		
WRX pulse width	t_{WLWH}	WRX, WRXL, WRHX	—	$t_{CYC} - 8$	—	ns	w/o cycle extension
Valid data output ⇒ WRX ↑ time	t_{DVWH}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC} - 25$	—	ns	w/o cycle extension
WRX ↑ ⇒ Data hold time	t_{WHDX}	WRX, WRLX, WRHX, AD[15:0]	—	$t_{CYC}/2 - 20$	—	ns	
WRX ↑ ⇒ Address valid time	t_{WHAX}	WRX, WRLX, WRHX, A[23:16]	—	$t_{CYC}/2 - 20$	—	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
WRX ↑ ⇒ ALE ↑ time	t_{WHLH}	WRX, WRLX, WRHX, ALE	EBM:ACE=1 and EACL:STS=1	$2t_{CYC}$ – 15	—	ns	
			other EBM:ACE and EACL:STS setting	t_{CYC} – 15	—		
WRX ↓ ⇒ ECLK ↑ time	t_{WLCH}	WRX, WRLX, WRHX, ECLK	—	$t_{CYC}/2$ – 15	—	ns	
CSn ⇒ WRX time	t_{CSLWL}	WRX, WRLX, WRHX, CSn	EACL:ACE=0	—	$3t_{CYC}/2$ – 20	ns	
			EACL:ACE=1	—	$5t_{CYC}/2$ – 20		
WRX ⇒ CSn time	t_{WHCSH}	WRX, WRLX, WRHX, CSn	—	$t_{CYC}/2$ – 20	—	ns	



Refer to the Hardware Manual for detailed Timing Charts

Ready Input Timing

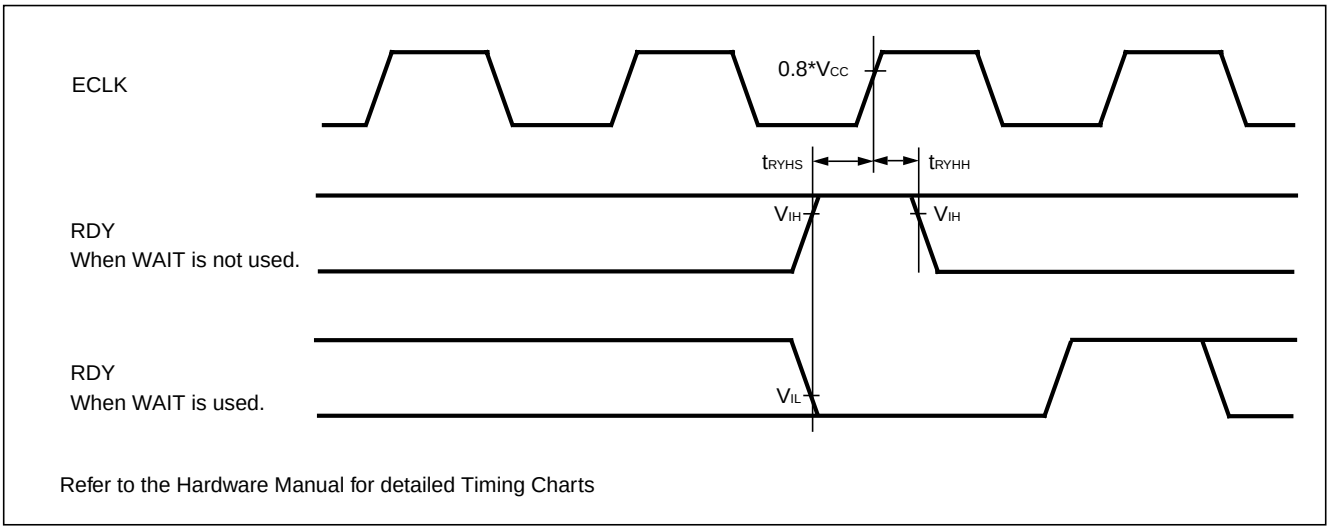
(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Test Condition	Rated Value		Units	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	45	—	ns	
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.



Refer to the Hardware Manual for detailed Timing Charts

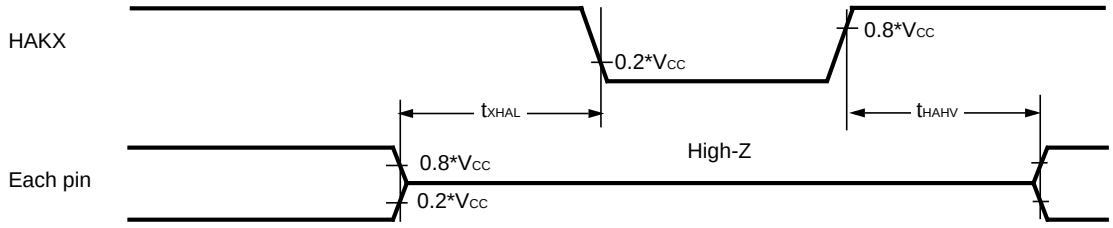
Hold Timing

(T_A = –40 °C to +125 °C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	—	t_{CYC} – 20	t_{CYC} + 20	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 20	t_{CYC} + 20	ns	

(T_A = –40 °C to +125 °C, V_{CC} = 3.0 to 4.5V, V_{SS} = 0.0 V, IO_{drive} = 5mA, C_L = 50pF)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating ⇒ HAKX ↓ time	t_{XHAL}	HAKX	—	t_{CYC} – 25	t_{CYC} + 25	ns	
HAKX ↑ time ⇒ Pin valid time	t_{HAHV}	HAKX		t_{CYC} – 25	t_{CYC} + 25	ns	



Refer to the Hardware Manual for detailed Timing Charts

USART timing

WARNING: The values given below are for an I/O driving strength IO_{drive} = 5mA. If IO_{drive} is 2mA, all the maximum output timing described in the different tables must then be increased by 10ns.

(T_A = -40˚C to 125˚C, V_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V, IO_{drive} = 5mA, C_L = 50pF)

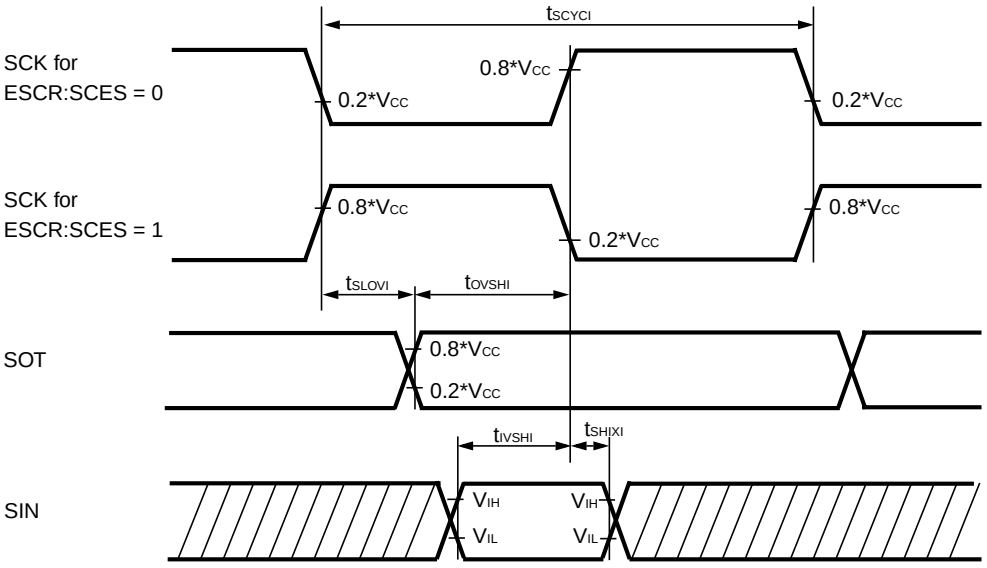
Parameter	Symbol	Pin	Condition	V_{CC} = AV_{CC}= 4.5V to 5.5V		V_{CC} = AV_{CC}= 3.0V to 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal Shift Clock Mode	4 t_{CLKP1}	—	4 t_{CLKP1}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		-20	+20	-30	+30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N*t_{CLKP1}$ - 20 *1	—	$N*t_{CLKP1}$ - 30 *1	—	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	—	t_{CLKP1} + 55	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}	SCKn, SINn		0	—	0	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn	External Shift Clock Mode	t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		—	2 t_{CLKP1} + 45	—	2 t_{CLKP1} + 55	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCKn, SINn		t_{CLKP1}/2 + 10	—	t_{CLKP1}/2 + 10	—	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	—	t_{CLKP1} + 10	—	ns
SCK fall time	t_{FE}	SCKn		—	20	—	20	ns
SCK rise time	t_{RE}	SCKn		—	20	—	20	ns

Notes:
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96300 Super series HARDWARE MANUAL”
- t_{CLKP1} is the cycle time of the peripheral clock 1 (CLKP1), Unit : ns

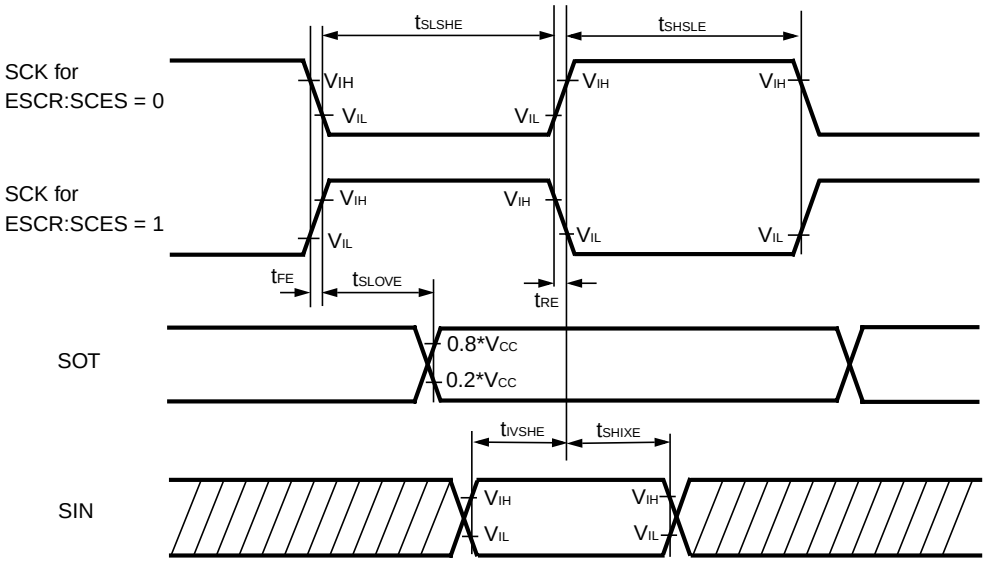
*1: Parameter N depends on t_{SCYCI} and can be calculated as follows:
- if t_{SCYCI} = 2*k*t_{CLKP1}, then N = k, where k is an integer > 2
- if t_{SCYCI} = (2*k+1)*t_{CLKP1}, then N = k+1, where k is an integer > 1

Examples:

t_{SCYCI}	N
4*t_{CLKP1}	2
5*t_{CLKP1}, 6*t_{CLKP1}	3
7*t_{CLKP1}, 8*t_{CLKP1}	4
...	...



Internal Shift Clock Mode



External Shift Clock Mode

I²C Timing

(T_A = -40°C to 125°C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} =0V)

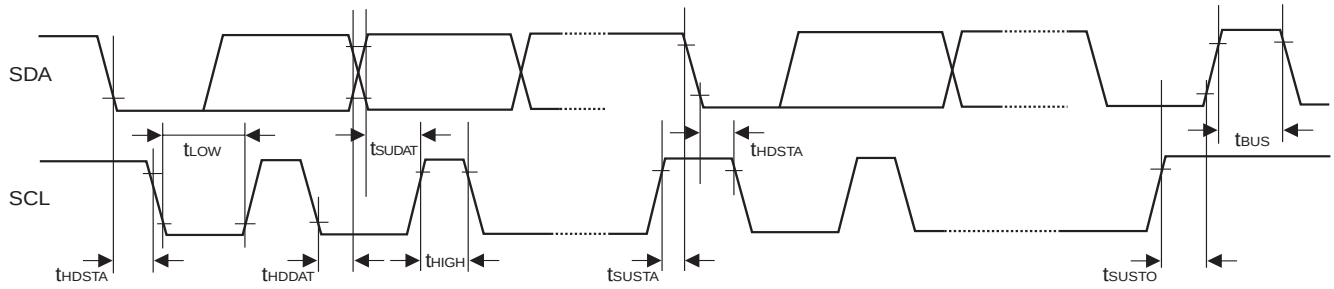
Parameter	Symbol	Condition	Standard-mode		Fast-mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓→SCL↓	t_{HDSTA}		4.0	—	0.6	—	µs
"L" width of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
"H" width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up time for a repeated START condition SCL↑→SDA↓	t_{SUSTA}		4.7	—	0.6	—	µs
Data hold time SCL↓→SDA↓↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data set-up time SDA↓↑→SCL↑	t_{SUDAT}		250	—	100	—	ns
Set-up time for STOP condition SCL↑→SDA↑	t_{SUSTO}		4.0	—	0.6	—	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	—	1.3	—	µs

*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} have only to be met if the device does not stretch the "L" width (t_{LOW}) of the SCL signal.

*3 : A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

*4 : For use at over 100 kHz, set the peripheral clock 1 to at least 6 MHz.



5. Analog Digital Converter

(T_A = -40 ˚C to +125 ˚C, 3.0 V ≤ AVRH - AVRL, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	-3	-	+3	LSB	
Nonlinearity error	-	-	-2.5	-	+2.5	LSB	
Differential nonlinearity error	-	-	-1.9	-	+1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL - 1.5	AVRL+ 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	ANn	AVRH - 3.5	AVRH - 1.5	AVRH + 0.5	LSB	
Compare time	-	-	1.0	-	16,500	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			2.0	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Sampling time	-	-	0.5	-	-	µs	4.5V ≤ AV_{CC} ≤ 5.5V
			1.2	-	-	µs	3.0V ≤ AV_{CC} < 4.5V
Analog port input current	I_{AIN}	ANn	-3	-	+3	µA	AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog port input current	I_{AIN}	ANn	-1	-	+1	µA	T_A = 25 ˚C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
			-3	-	+3	µA	T_A = 125 ˚C, AV_{SS}, AVRL < V_I < AV_{CC}, AVRH
Analog input voltage range	V_{AIN}	ANn	AVRL	-	AVRH	V	
Reference voltage range	AVRH	AVRH	0.75 AVcc	-	AVcc	V	
	AVRL	AVRL	AV_{SS}	-	0.25 AV_{CC}	V	
Power supply current	I_A	AVcc	-	2.5	5	mA	A/D Converter active
	I_{AH}	AVcc	-	-	5	µA	A/D Converter not operated
Reference voltage current	I_R	AVRH/ AVRL	-	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH/ AVRL	-	-	5	µA	A/D Converter not operated
Offset between input channels	-	ANn	-	-	4	LSB	

Note: The accuracy gets worse as |AVRH - AVRL| becomes smaller.

Definition of A/D Converter Terms

Resolution: Analog variation that is recognized by an A/D converter.

Total error: Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error and nonlinearity error.

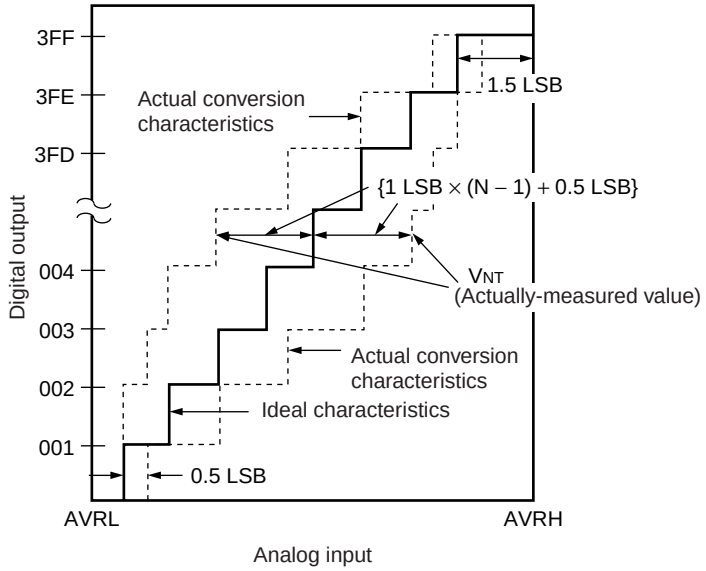
Nonlinearity error: Deviation between a line across zero-transition line (“00 0000 0000” <--> “00 0000 0001”) and full-scale transition line (“11 1111 1110” <--> “11 1111 1111”) and actual conversion characteristics.

Differential nonlinearity error: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

Zero reading voltage: Input voltage which results in the minimum conversion value.

Full scale reading voltage: Input voltage which results in the maximum conversion value.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

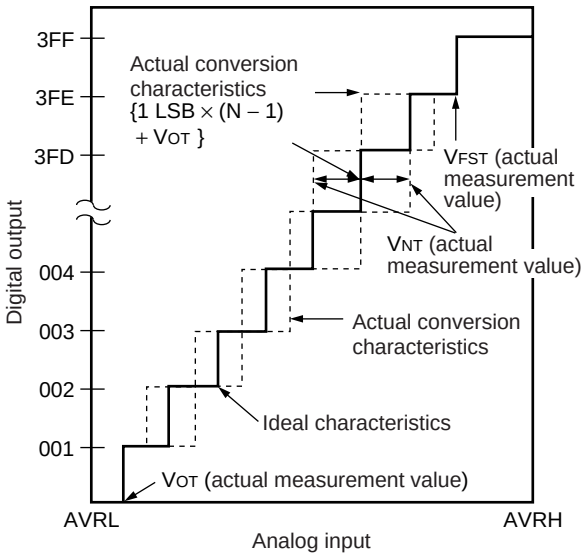
N: A/D converter digital output value

V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

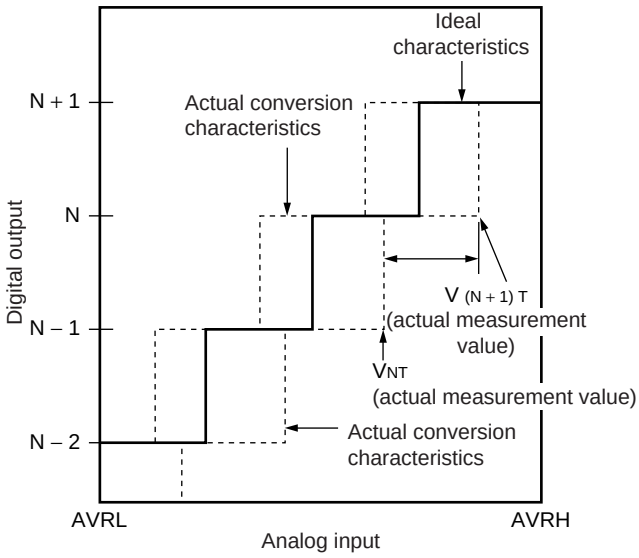
V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which digital output transitions from (N – 1) to N.

Nonlinearity error



Differential nonlinearity error



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times\ (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ \text{[LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)\,T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB [LSB]}$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{[V]}$$

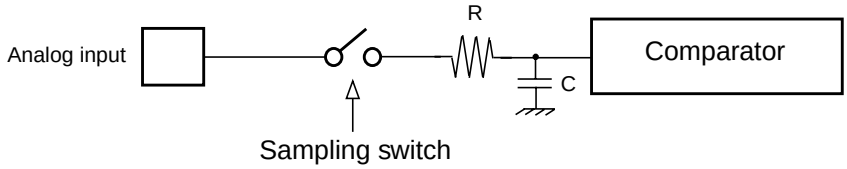
N : A/D converter digital output value
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

Notes on A/D Converter Section

- About the external impedance of the analog input and the sampling time of the A/D converter (with sample and hold circuit):

If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- analog input circuit model:



Reference value:

- C = 8.5 pF (Max)

To satisfy the A/D conversion precision standard, the relationship between the external impedance and minimum sampling time must be considered and then either the resistor value and operating frequency must be adjusted or the external impedance must be decreased so that the sampling time (T_{samp}) is longer than the minimum value. Usually, this value is set to 7τ, where $\tau = RC$. If the external input resistance (R_{ext}) connected to the analog input is included, the sampling time is expressed as follows:

T_{samp} [min] = $7 \times (R_{ext} + 2.6k\Omega) \times C$ for $4.5 \leq AV_{cc} \leq 5.5$

T_{samp} [min] = $7 \times (R_{ext} + 12.1k\Omega) \times C$ for $3.0 \leq AV_{cc} \leq 4.5$

If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- About the error

The accuracy gets worse as |AVRH - AVRL| becomes smaller.

6. Low Voltage Detector characteristics

(T_A = -40 ˚C to +125 ˚C, V_{CC} = AV_{CC} = 3.0V - 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value *1		Value *2		Unit	Remarks
		Min	Max	Min	Max		
Stabilization time	$T_{LVDSTAB}$	-	75	-	110	µs	After power-up or change of detection level
Level 0	V_{DL0}	2.7	2.9	2.65	2.95	V	CILCR:LVL[3:0]="0000"
Level 1	V_{DL1}	2.9	3.1	2.85	3.2	V	CILCR:LVL[3:0]="0001"
Level 2	V_{DL2}	3.1	3.3	3.05	3.4	V	CILCR:LVL[3:0]="0010"
Level 3	V_{DL3}	3.5	3.75	3.45	3.85	V	CILCR:LVL[3:0]="0011"
Level 4	V_{DL4}	3.6	3.85	3.55	3.95	V	CILCR:LVL[3:0]="0100"
Level 5	V_{DL5}	3.7	3.95	3.65	4.1	V	CILCR:LVL[3:0]="0101"
Level 6	V_{DL6}	3.8	4.05	3.75	4.2	V	CILCR:LVL[3:0]="0110"
Level 7	V_{DL7}	3.9	4.15	3.85	4.3	V	CILCR:LVL[3:0]="0111"
Level 8	V_{DL8}	4.0	4.25	3.95	4.4	V	CILCR:LVL[3:0]="1000"
Level 9	V_{DL9}	4.1	4.35	4.05	4.5	V	CILCR:LVL[3:0]="1001"
Level 10	V_{DL10}	not used		not used			
Level 11	V_{DL11}	not used		not used			
Level 12	V_{DL12}	not used		not used			
Level 13	V_{DL13}	not used		not used			
Level 14	V_{DL14}	not used		not used			
Level 15	V_{DL15}	not used		not used			

*1: valid for all devices except devices listed under "*2"

*2: valid for: MB96F353/F355

CILCR:LVL[3:0] are the low voltage detector level select bits of the CILCR register.

Levels 10 to 15 are not used in this device.

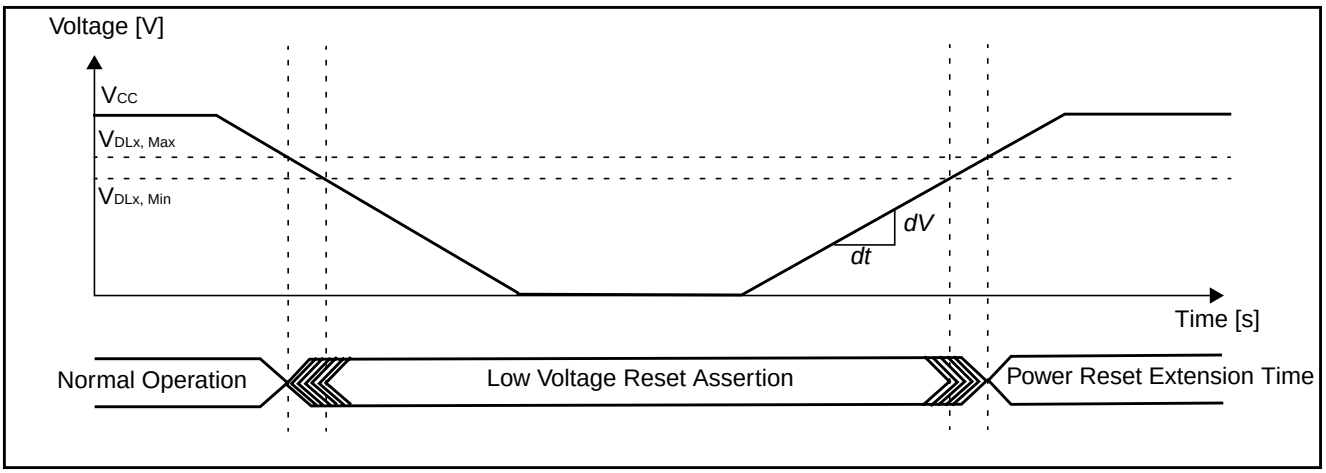
For correct detection, the slope of the voltage level must satisfy $\left|\frac{dV}{dt}\right| \leq 0.004\frac{V}{\mu s}$.

Faster variations are regarded as noise and may not be detected.

The functional operation of the MCU is guaranteed down to the minimum low voltage detection level of Vcc = 2.7V. The electrical characteristics however are only valid in the specified range (usually down to 3.0V).

Low Voltage Detector Operation

In the following figure, the occurrence of a low voltage condition is illustrated. For a detailed description of the reset and startup behavior, please refer to the corresponding hardware manual chapter.



7. FLASH memory program/erase characteristics

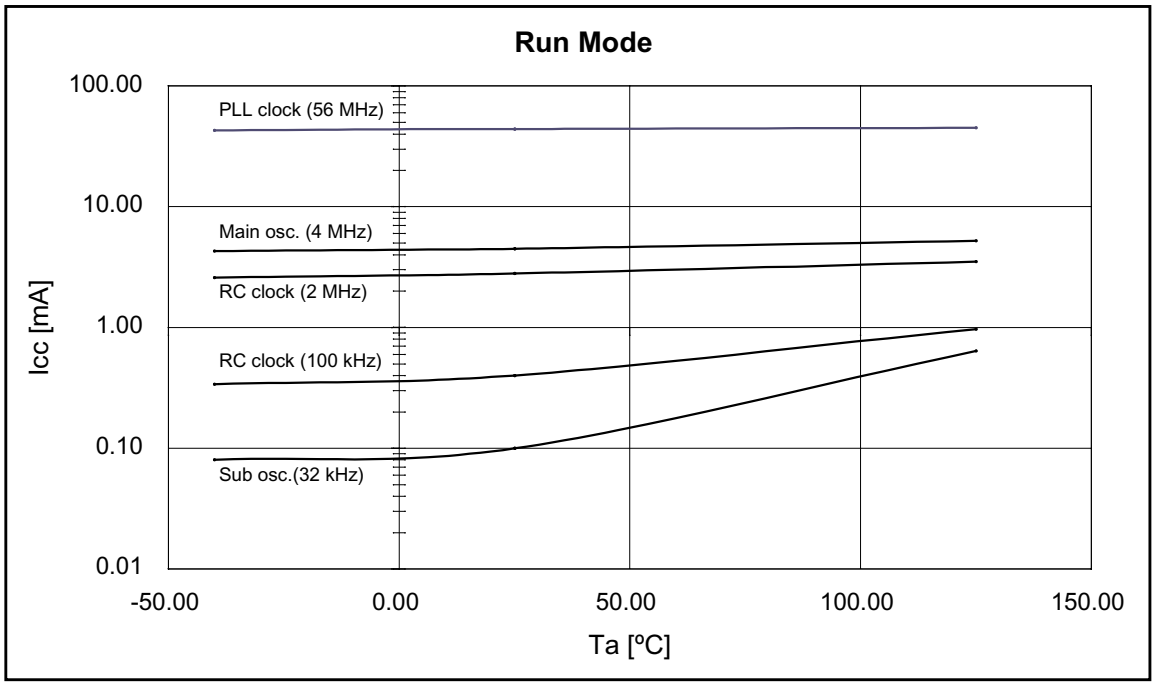
(T_A = -40˚C to 105˚C, V_{CC} = AV_{CC} = 3.0V to 5.5V, V_{SS} = AV_{SS} = 0V)

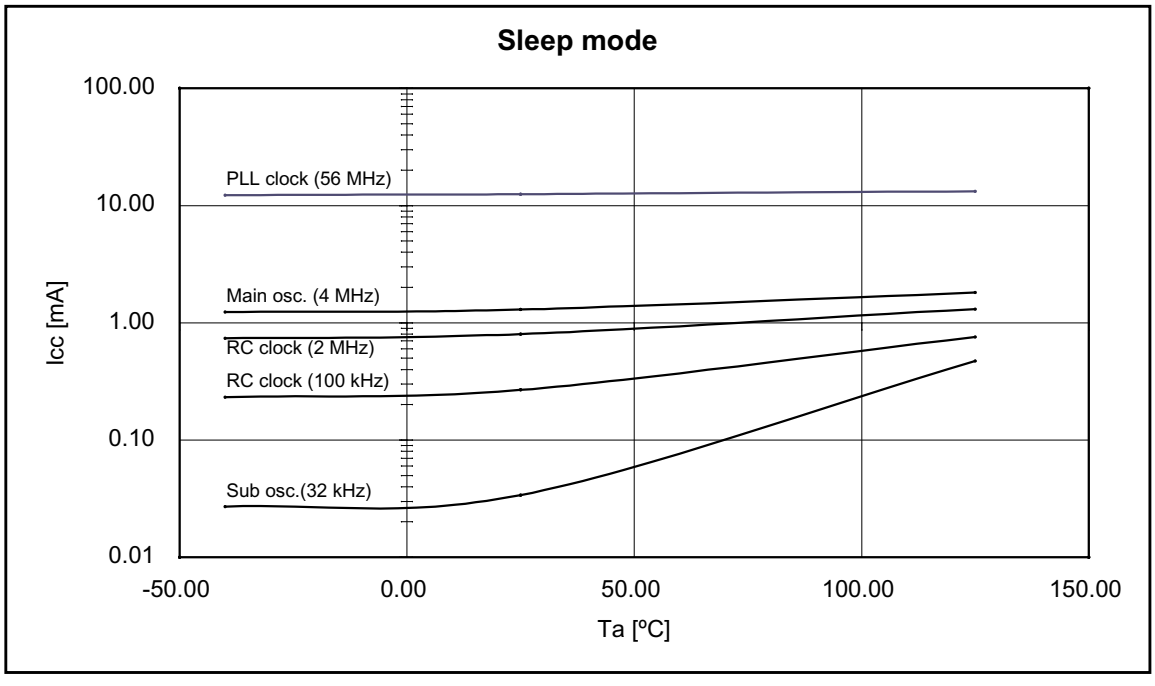
Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Without erasure pre-programming time
Chip erase time	-	n*0.9	n*3.6	s	Without erasure pre-programming time (n is the number of Flash sector of the device)
Word (16-bit width) programming time	-	23	370	us	Without overhead time for submitting write command
Program/Erase cycle	10 000	-	-	cycle	
Flash data retention time	20	-	-	year	*1

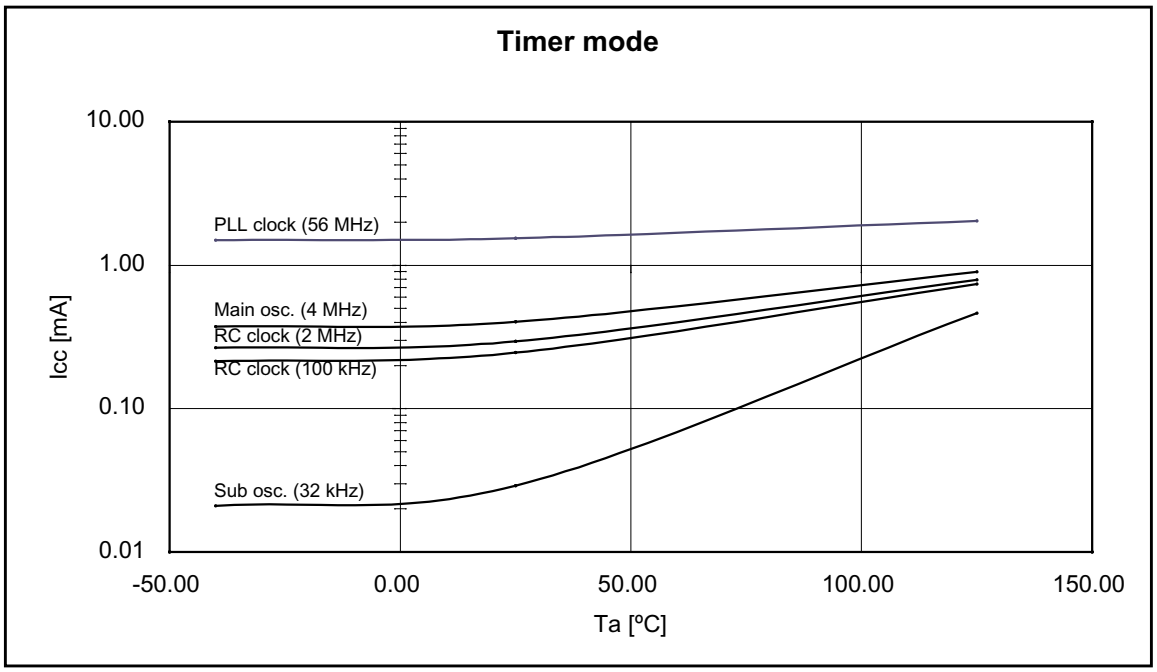
*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85ºC)

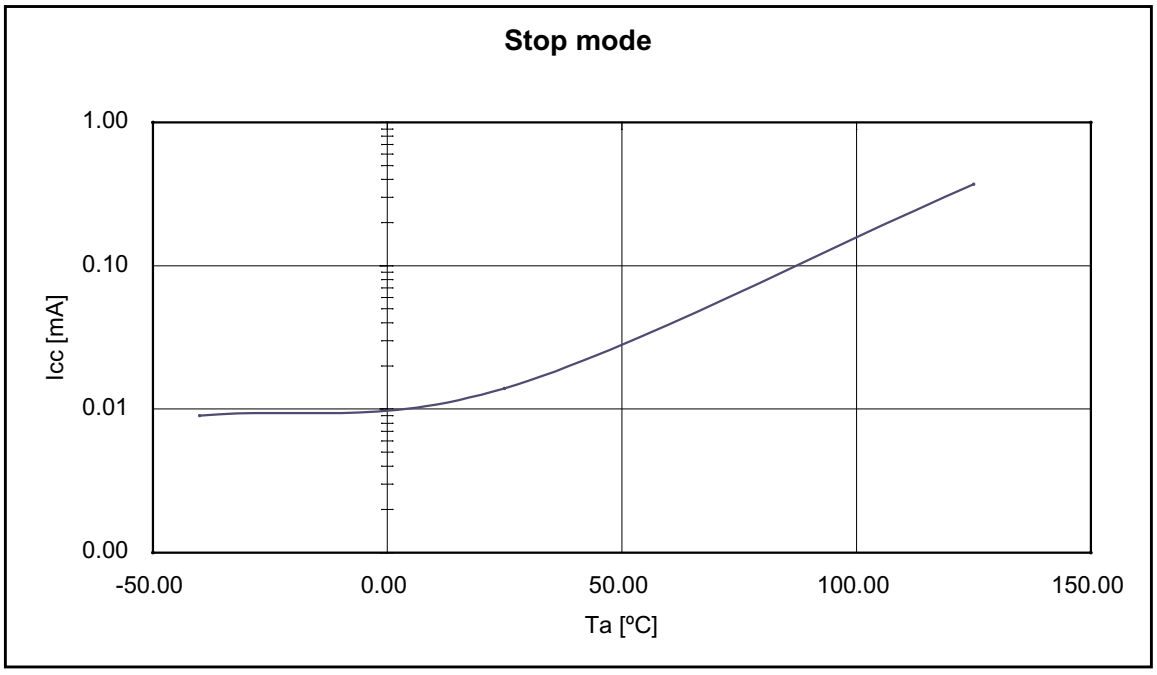
■ EXAMPLE CHARACTERISTICS

The diagrams below show the characteristics of one measured sample with typical process parameters.









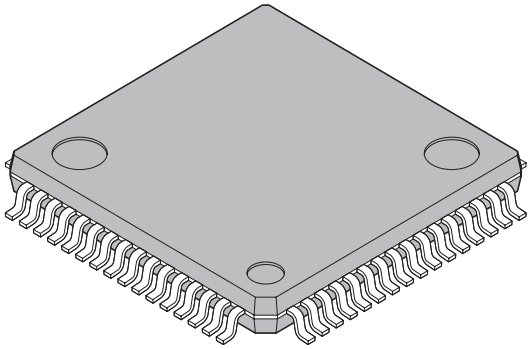
Used settings

Mode	Selected Source Clock	Clock/Regulator Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = 56 MHz CLKP2 = 28 MHz Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2 MHz Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100 kHz Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32 kHz Regulator in Low Power Mode A Core Voltage = 1.8 V
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = 56 MHz CLKP2 = 28 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.9 V
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2 MHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100 kHz (CLKB is stopped in this mode) Regulator in High Power Mode Core Voltage = 1.8 V
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32 kHz (CLKB is stopped in this mode) Regulator in Low Power Mode A Core Voltage = 1.8 V

Used settings

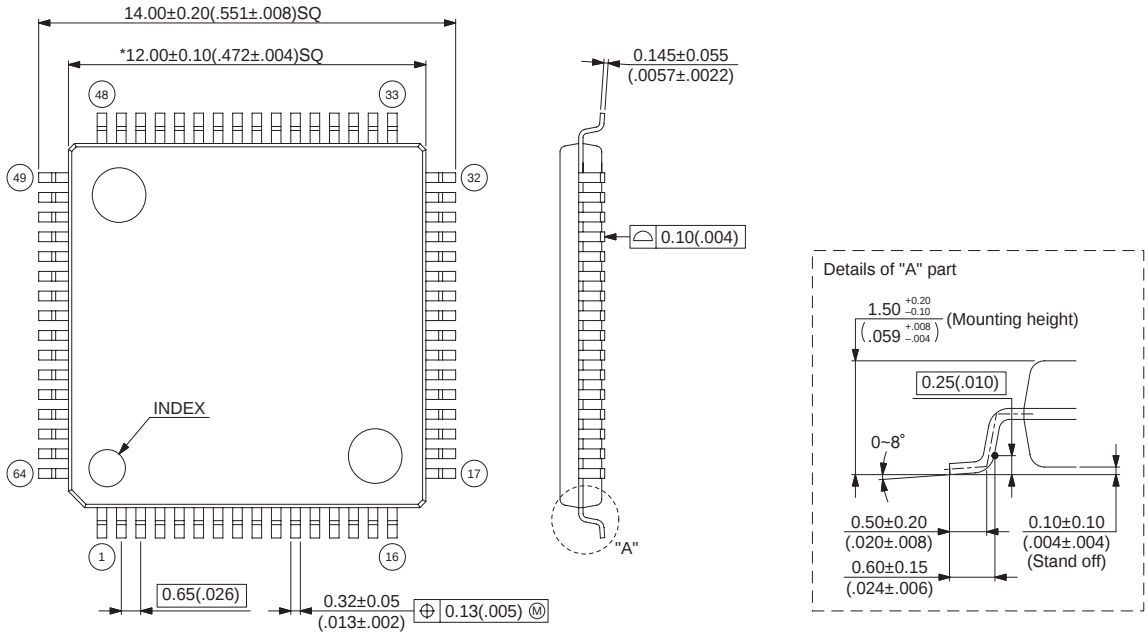
Mode	Selected Source Clock	Clock/Regulator Settings
Timer mode	PLL	CLKMC = 4 MHz, CLKPLL = 56 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.9 V
	Main osc.	CLKMC = 4 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock fast	CLKRC = 2 MHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	RC clock slow	CLKRC = 100 kHz (System clocks are stopped in this mode) Regulator in High Power Mode, Core Voltage = 1.8 V
	Sub osc.	CLKSC = 100 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode A, Core Voltage = 1.8 V
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode B, Core Voltage = 1.8 V

■ PACKAGE DIMENSION MB96(F)35x LQFP 64 - M23

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Code (Reference)	P-LFQFP64-12×12-0.65
(FPT-64P-M23)		

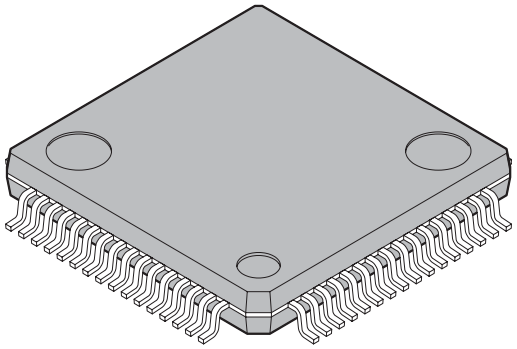
64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



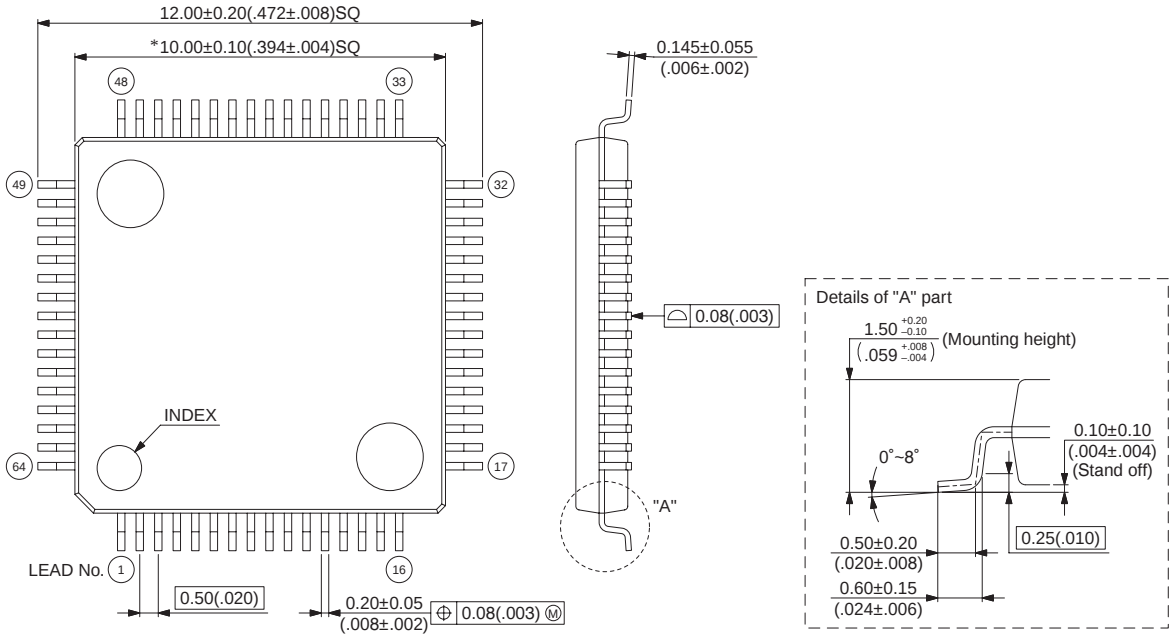
Dimensions in mm (inches).
Note: The values in parentheses are reference values

■ PACKAGE DIMENSION MB96(F)35x LQFP 64 - M24

64-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	10.0 × 10.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.32 g
(FPT-64P-M24)	Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

■ ORDERING INFORMATION

MCU with CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F353RSA PMC-GSE2 *1	Flash A (96KB)	No	No	64 pins Plastic LQFP (FPT-64P-M23)
MB96F353RWA PMC-GSE2 *1		Yes		
MB96F353RSA PMC1-GSE2 *1		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F353RWA PMC1-GSE2 *1		Yes		
MB96F355RSA PMC-GSE2 *1	Flash A (160KB)	No		64 pins Plastic LQFP (FPT-64P-M23)
MB96F355RWA PMC-GSE2 *1		Yes		
MB96F355RSA PMC1-GSE2 *1		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F355RWA PMC1-GSE2 *1		Yes		
MB96F356YSB PMC-GSE2	Flash A (288KB)	No	Yes	64 pins Plastic LQFP (FPT-64P-M23)
MB96F356RSB PMC-GSE2			No	
MB96F356YWB PMC-GSE2		Yes	Yes	
MB96F356RWB PMC-GSE2			No	
MB96F356YSB PMC1-GSE2		No	Yes	64 pins Plastic LQFP (FPT-64P-M24)
MB96F356RSB PMC1-GSE2			No	
MB96F356YWB PMC1-GSE2		Yes	Yes	
MB96F356RWB PMC1-GSE2			No	
MB96V300BRB-ES (for evaluation)	Emulated by ext. RAM	Yes	No	416 pin Plastic BGA (BGA-416P-M02)

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

MCU without CAN controller

Part number	Flash/ROM	Subclock	Persistent Low Voltage Reset	Package
MB96F353ASA PMC-GSE2 *1	Flash A (96KB)	No	No	64 pins Plastic LQFP (FPT-64P-M23)
MB96F353AWA PMC-GSE2 *1		Yes		
MB96F353ASA PMC1-GSE2 *1		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F353AWA PMC1-GSE2 *1		Yes		
MB96F355ASA PMC-GSE2 *1	Flash A (160KB)	No		64 pins Plastic LQFP (FPT-64P-M23)
MB96F355AWA PMC-GSE2 *1		Yes		
MB96F355ASA PMC1-GSE2 *1		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F355AWA PMC1-GSE2 *1		Yes		
MB96F356ASB PMC-GSE2	Flash A (288KB)	No		64 pins Plastic LQFP (FPT-64P-M23)
MB96F356AWB PMC-GSE2		Yes		
MB96F356ASB PMC1-GSE2		No		64 pins Plastic LQFP (FPT-64P-M24)
MB96F356AWB PMC1-GSE2		Yes		

*1: These devices are under development and specification is preliminary. These products under development may change its specification without notice.

This datasheet is also valid for the following outdated devices:

MB96F356YSA, MB96F356RSA, MB96F356YWA, MB96F356RWA, MB96F356ASA, MB96F356AWA

■ REVISION HISTORY

Revision	Date	Modification
Prelim 1	2007-05-03	Creation
Prelim 2	2007-05-25	Electrical characteristics update
Prelim 3	2007-11-27	Package description is removed from cover page. Typos corrections in product lineup. Product option details added Electrical characteristics update Update of the block diagram Update of the IO map Pin circuit type, LVD characteristics and example characteristics chapters added
Prelim 4	2007-12-20	Update of the block diagram: external bus address lines, clock output function pins, AVRL removed from ADC block, relayout. RAMSTART value is corrected IO map regenerated Memory map and Flash configuration reworked Few typos corrected accross the document. Flash bank renaming. Ordering information: package type corrected. IO circuit drawings modified.
Prelim 5	2008-02-04	• Reload Timer RLT 6 for PPGs added • Block diagram corrected: ICU2 deleted, TTG2,3 deleted, TTG8,9 added • Pin function description corrected with all existing pin types • I/O circuit type diagrams corrected • Memory map cleaned up • "Flash sector configuration" replaced by corrected "User ROM Memory map for Flash devices" • Parallel Flash programming spec removed • IO map table regenerated: - Port register: Naming style corrected - Memory control registers renamed (Main -> A) - addresses after 000BFFh removed • Handling devices: AD converter items added • Absolute maximum ratings: Pd and Ta specified more precisely • Run and Sleep mode currents: more conditions added (1WS settings) • Run mode current spec in 48/24MHz mode corrected • Maximum CLKS1 frequency corrected at 1.8V • External bus timings: missing conditions added and readability improved • Ordering information updated • Typos and formatting corrected

Revision	Date	Modification
6	2009-01-09	• Format adjusted to official Fujitsu Microelectronics datasheet standard (mainly style changes and official notes and disclaimer added) • Numbering of Electrical Characteristics subchapters automated • CANless devices added (MB96F356A) • I/O map: Added node about reserved registers • Serial programming interface: Note about handshaking pins improved • specified AD converter channel offset to 4LSB • package code of MB96V300 corrected in ordering information • Added voltage condition to pull-up resistance spec • Ordering information: column “Flash/ROM” added, column “Remarks” removed • Official package dimension drawing with additional notes added • Empty pages removed • Handling devices: Notes added about Serial communication and about using ceramic resonators. • Feature list and AC Characteristics: 16MHz maximum frequency is valid for crystal oscillators. For resonators, maximum frequency depends on Q-factor • AC characteristics: PLL phase skew spec added, CLKVCO min=64MHz • VOL3 spec improved: spec valid for 3mA load for full Vcc range • MB96F353/F355 added (under development) • Free running timer (I/O Timer) 2 and 3 added (without clock input pin) • Input capture ICU9 and ICU10 added (without input pin, only for LIN USART) • C-Pin cap spec updated: 4.7uF-10uF capacitor with tolerance permitted • “Preliminary” watermark removed

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