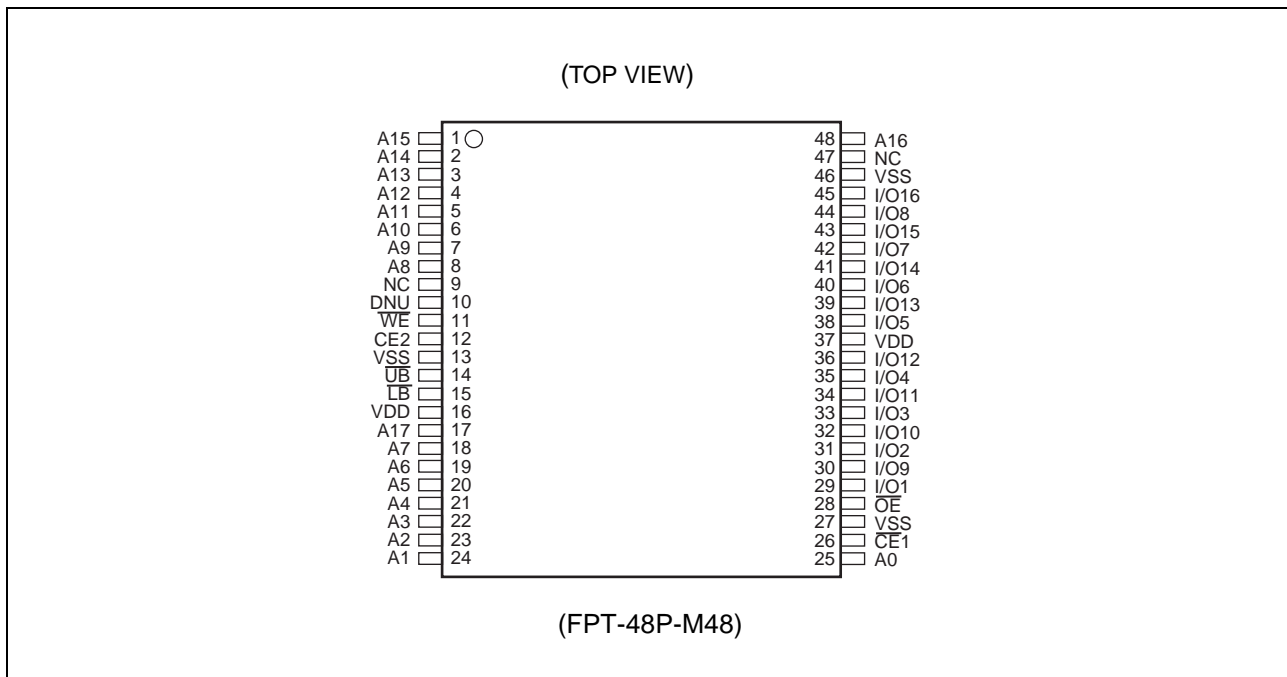


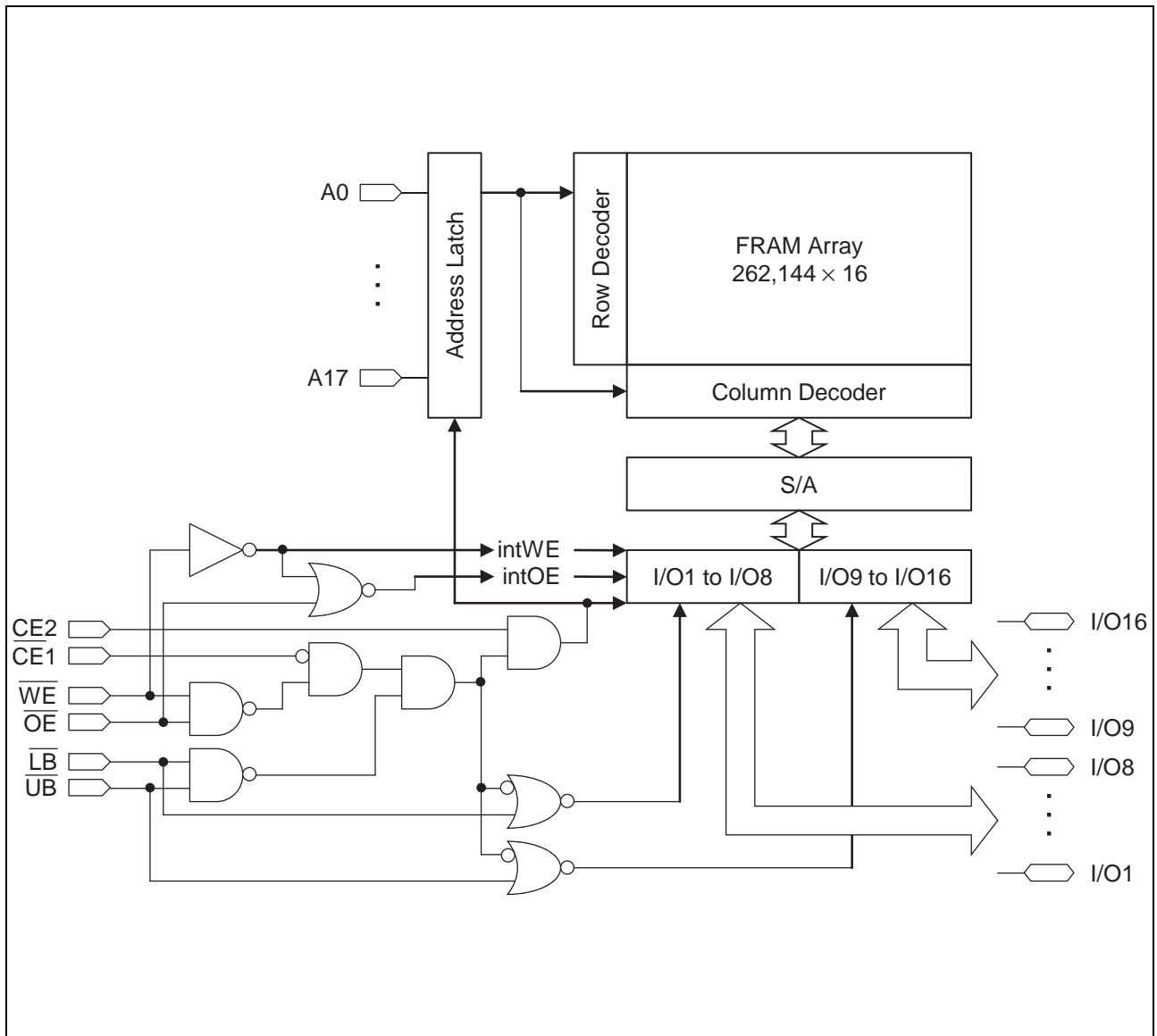
## PIN ASSIGNMENTS



## PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 8, 17 to 25, 48	A0 to A17	Address Input pins
29 to 36, 38 to 45	I/O1 to I/O16	Data Input/Output pins
26	$\overline{CE}1$	Chip Enable 1 Input pin
12	CE2	Chip Enable 2 Input pin
11	$\overline{WE}$	Write Enable Input pin
28	$\overline{OE}$	Output Enable Input pin
14, 15	$\overline{LB}$ , $\overline{UB}$	Data Byte Control Input pins
16, 37	VDD	Supply Voltage pins Connect all two pins to the power supply.
13, 27, 46	VSS	Ground pins Connect all three pins to ground.
9, 47	NC	No Connect pins Leave these pins open, or connect to VDD or VSS.
10	DNU	Do Not Use pin Make sure to connect this pin to VDD.

## ■ BLOCK DIAGRAM



## ■ FUNCTIONAL TRUTH TABLE

Mode	$\overline{CE}1$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	Supply Current
Standby Precharge	H	X	X	X	X	X	Hi-Z	Hi-Z	Standby ( $I_{SB}$ )
	X	L	X	X	X	X			
	X	X	H	H	X	X			
	X	X	X	X	H	H			
Read	$\downarrow$	H	H	L	L	L	Data Output	Data Output	Operation ( $I_{DD}$ )
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
	L	$\uparrow$	H	L	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Read (Pseudo-SRAM, $\overline{OE}$ control*1)	L	H	H	$\downarrow$	L	L	Data Output	Data Output	
					L	H	Data Output	Hi-Z	
					H	L	Hi-Z	Data Output	
Write	$\downarrow$	H	L	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	
	L	$\uparrow$	L	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	
Write (Pseudo-SRAM, $\overline{WE}$ control*2)	L	H	$\downarrow$	H	L	L	Data Input	Data Input	
					L	H	Data Input	Hi-Z	
					H	L	Hi-Z	Data Input	

Note: L =  $V_{IL}$ , H =  $V_{IH}$ , X can be either H, L,  $\downarrow$  or  $\uparrow$ , Hi-Z = High Impedance

$\downarrow$  : Latch address and latch data at falling edge,  $\uparrow$  : Latch address and latch data at rising edge

\*1 :  $\overline{OE}$  control of the Pseudo-SRAM means the valid address at the falling edge of  $\overline{OE}$  to read.

\*2 :  $\overline{WE}$  control of the Pseudo-SRAM means the valid address and data at the falling edge of  $\overline{WE}$  to write.

## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V <sub>DD</sub>	−0.5	+4.0	V
Input Pin Voltage*	V <sub>IN</sub>	−0.5	V <sub>DD</sub> + 0.5 ( ≤ 4.0)	V
Output Pin Voltage*	V <sub>OUT</sub>	−0.5	V <sub>DD</sub> + 0.5 ( ≤ 4.0)	V
Operation Ambient Temperature	T <sub>A</sub>	−40	+85	°C
Storage Temperature	T <sub>STG</sub>	−55	+125	°C

\* : All voltages are referenced to VSS (ground 0 V).

**WARNING:** Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.  
Do not exceed any of these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage* <sup>1</sup>	V <sub>DD</sub>	3.0	3.3	3.6	V
Operation Ambient Temperature* <sup>2</sup>	T <sub>A</sub>	−40	—	+85	°C

\*1 : All voltages are referenced to VSS (ground 0 V).

\*2 : Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current*1	$ I_{LI} $	$V_{IN} = 0 \text{ V to } V_{DD}$	—	—	10	$\mu\text{A}$
Output Leakage Current	$ I_{LO} $	$V_{OUT} = 0 \text{ V to } V_{DD}$ , $\overline{CE1} = V_{IH}$ or $\overline{OE} = V_{IH}$	—	—	10	$\mu\text{A}$
Operating Power Supply Current*2	$I_{DD}$	$\overline{CE1} = 0.2 \text{ V}$ , $CE2 = V_{DD} - 0.2 \text{ V}$ , $I_{out} = 0 \text{ mA}$	—	15	20	mA
Standby Current*3	$I_{SB}$	$\overline{CE1} \geq V_{DD} - 0.2 \text{ V}$	—	50	150	$\mu\text{A}$
		$CE2 \leq 0.2 \text{ V}$				
		$\overline{OE} \geq V_{DD} - 0.2 \text{ V}$ , $\overline{WE} \geq V_{DD} - 0.2 \text{ V}$				
		$\overline{LB} \geq V_{DD} - 0.2 \text{ V}$ , $\overline{UB} \geq V_{DD} - 0.2 \text{ V}$				
High Level Input Voltage	$V_{IH}$	$V_{DD} = 3.0 \text{ V to } 3.6 \text{ V}$	$V_{DD} \times 0.8$	—	$V_{DD} + 0.5$ ( $\leq 4.0$ )	V
Low Level Input Voltage	$V_{IL}$	$V_{DD} = 3.0 \text{ V to } 3.6 \text{ V}$	-0.5	—	+0.6	V
High Level Output Voltage	$V_{OH}$	$I_{OH} = -1.0 \text{ mA}$	$V_{DD} \times 0.8$	—	—	V
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 2.0 \text{ mA}$	—	—	0.4	V

\*1 : This also applies to DNU pins.

\*2 : During the measurement of  $I_{DD}$ , the Address and Data In were taken to only change once per active cycle.  
I<sub>out</sub> : output current

\*3 : All pins other than setting pins shall be input at the CMOS level voltages such as  $H \geq V_{DD} - 0.2 \text{ V}$ ,  $L \leq 0.2 \text{ V}$ .

## 2. AC Characteristics

### • AC Test Conditions

Power Supply Voltage	: 3.0 V to 3.6 V
Operation Ambient Temperature	: -40 °C to +85 °C
Input Voltage Amplitude	: 0.3 V to 2.7 V
Input Rising Time	: 5 ns
Input Falling Time	: 5 ns
Input Evaluation Level	: 2.0 V / 0.8 V
Output Evaluation Level	: 2.0 V / 0.8 V
Output Load Capacitance	: 50 pF

### (1) Read Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle time	$t_{RC}$	150	—	ns
$\overline{CE1}$ Active Time	$t_{CA1}$	120	—	ns
$\overline{CE2}$ Active Time	$t_{CA2}$	120	—	ns
$\overline{OE}$ Active Time	$t_{RP}$	120	—	ns
$\overline{LB}$ , $\overline{UB}$ Active Time	$t_{BP}$	120	—	ns
Precharge Time	$t_{PC}$	20	—	ns
Address Setup Time	$t_{AS}$	0	—	ns
Address Hold Time	$t_{AH}$	50	—	ns
$\overline{OE}$ Setup Time	$t_{ES}$	0	—	ns
$\overline{LB}$ , $\overline{UB}$ Setup Time	$t_{BS}$	5	—	ns
Output Data Hold time	$t_{OH}$	0	—	ns
Output Set Time	$t_{LZ}$	30	—	ns
$\overline{CE1}$ Access Time	$t_{CE1}$	—	120	ns
$\overline{CE2}$ Access Time	$t_{CE2}$	—	120	ns
$\overline{OE}$ Access Time	$t_{OE}$	—	120	ns
Output Floating Time	$t_{OHZ}$	—	20	ns

## (2) Write Cycle

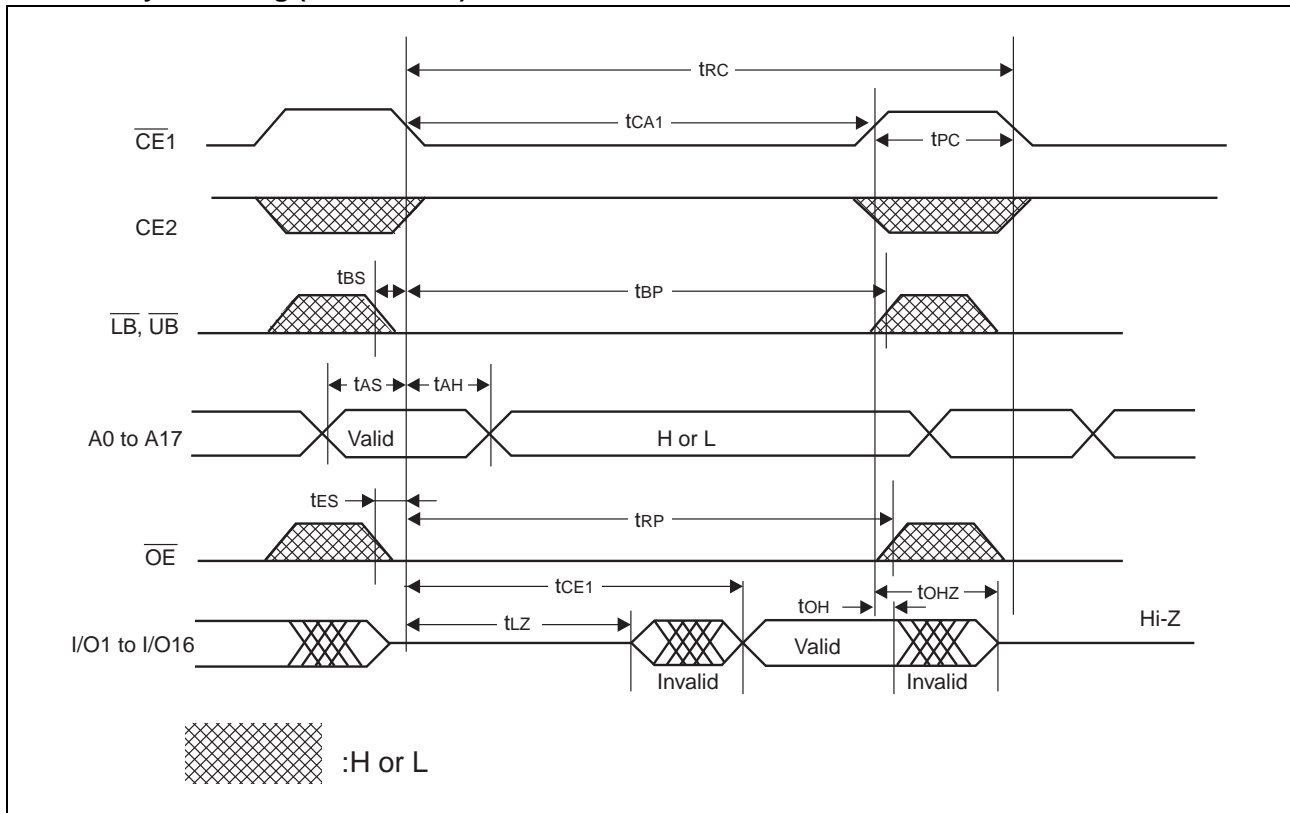
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	$t_{WC}$	150	—	ns
$\overline{CE1}$ Active Time	$t_{CA1}$	120	—	ns
CE2 Active Time	$t_{CA2}$	120	—	ns
$\overline{LB}$ , $\overline{UB}$ Active Time	$t_{BP}$	120	—	ns
Precharge Time	$t_{PC}$	20	—	ns
Address Setup Time	$t_{AS}$	0	—	ns
Address Hold Time	$t_{AH}$	50	—	ns
$\overline{LB}$ , $\overline{UB}$ Setup Time	$t_{BS}$	5	—	ns
Write Pulse Width	$t_{WP}$	120	—	ns
Data Setup Time	$t_{DS}$	0	—	ns
Data Hold Time	$t_{DH}$	50	—	ns
Write Setup Time	$t_{WS}$	0	—	ns

## 3. Pin Capacitance

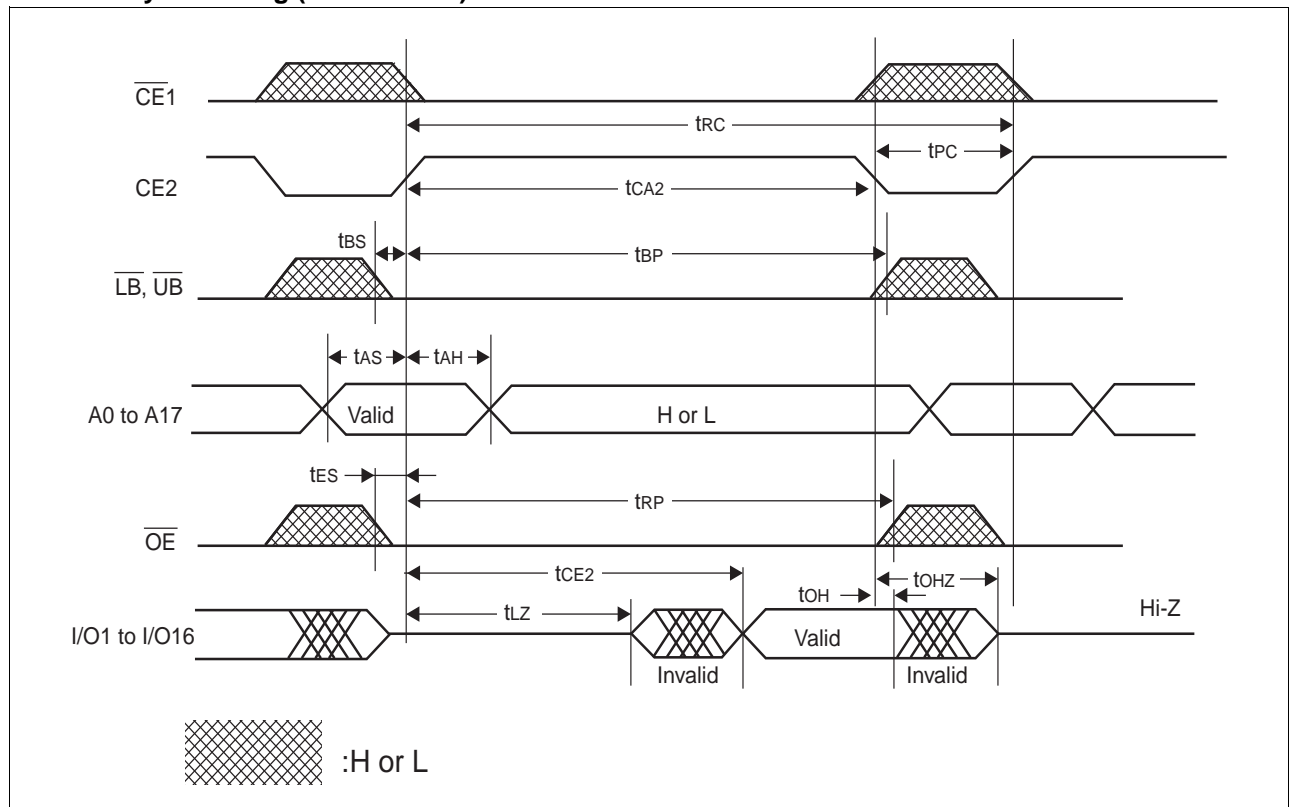
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	$C_{IN}$	$V_{DD} = V_{IN} = V_{OUT} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $T_A = +25\text{ °C}$	—	—	10	pF
Output Capacitance	$C_{OUT}$		—	—	10	pF
DNU Pin Input Capacitance	$C_{DNU}$		—	—	10	pF

## ■ TIMING DIAGRAMS

### 1. Read Cycle Timing ( $\overline{\text{CE1}}$ Control)

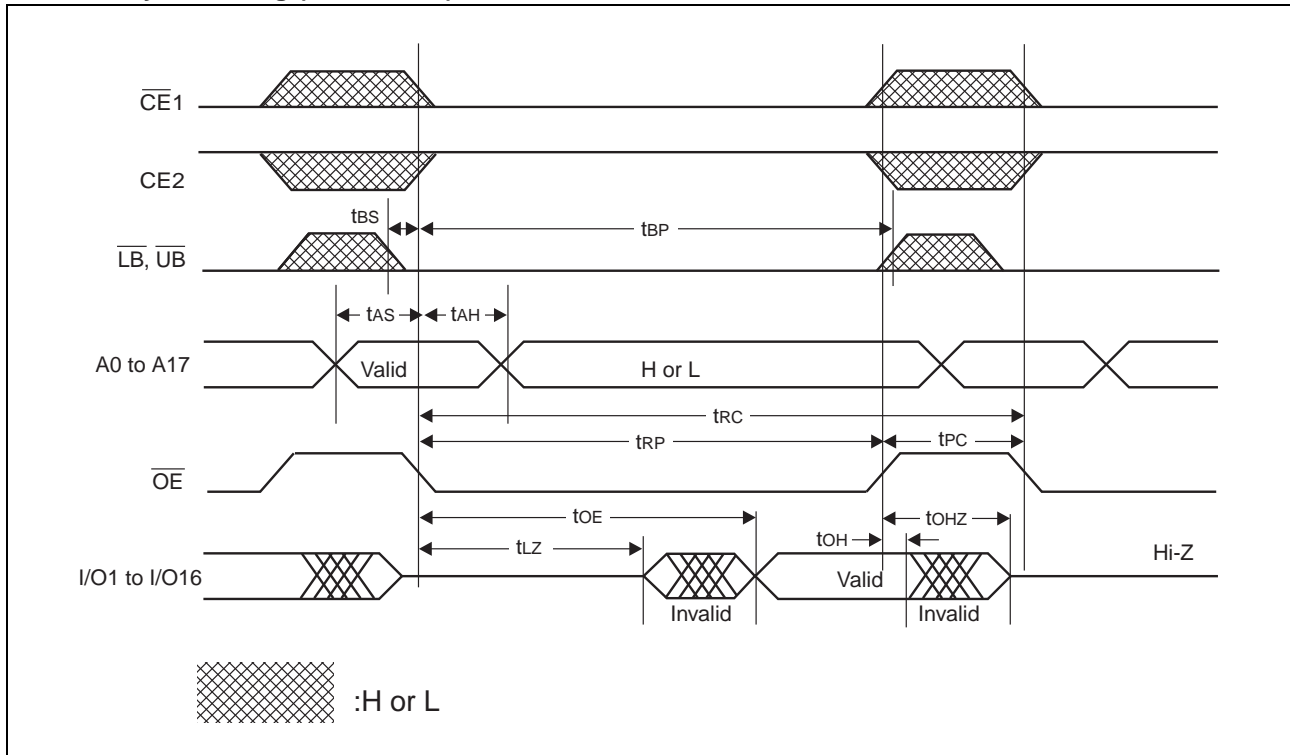


### 2. Read Cycle Timing ( $\text{CE2}$ Control)

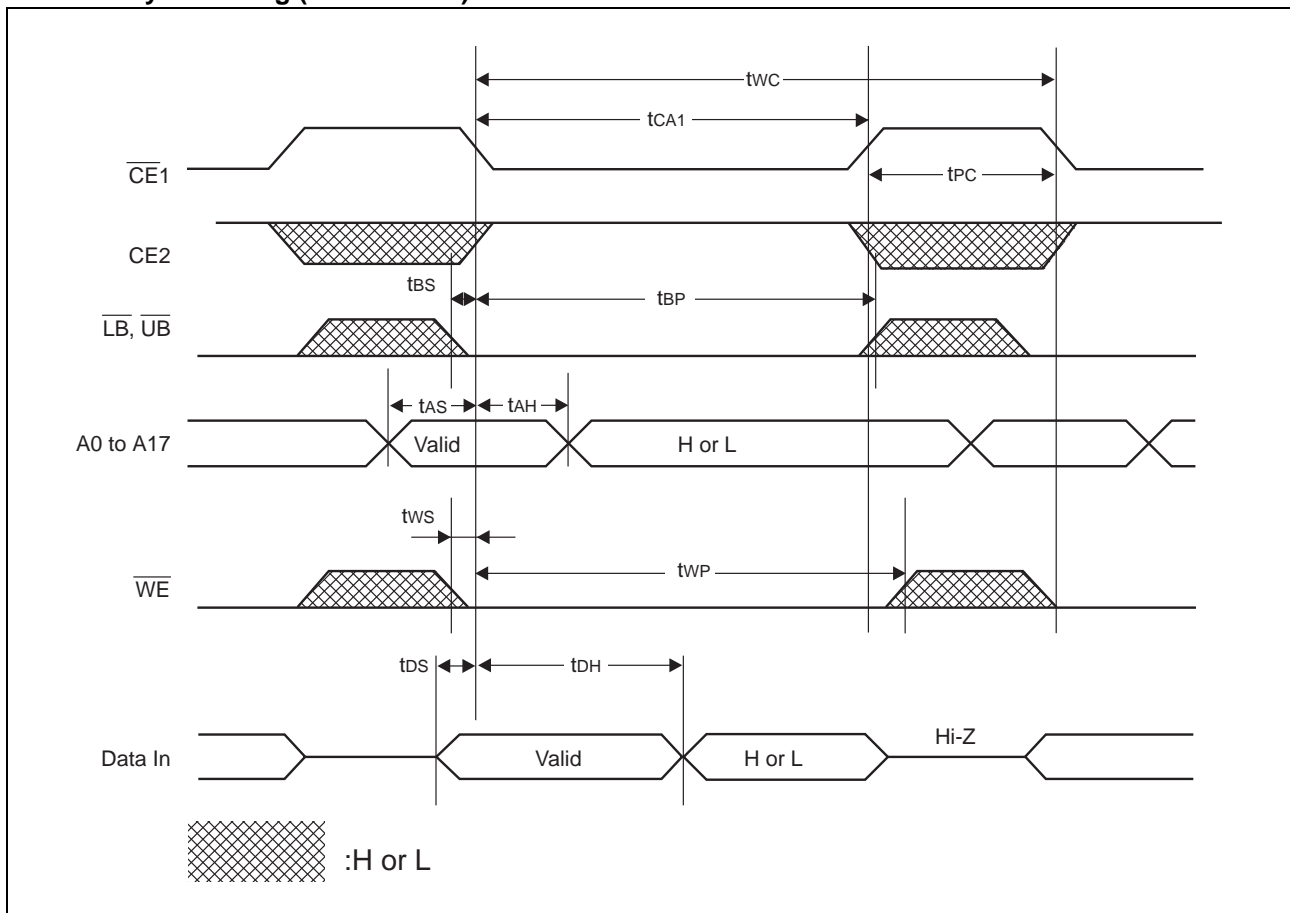




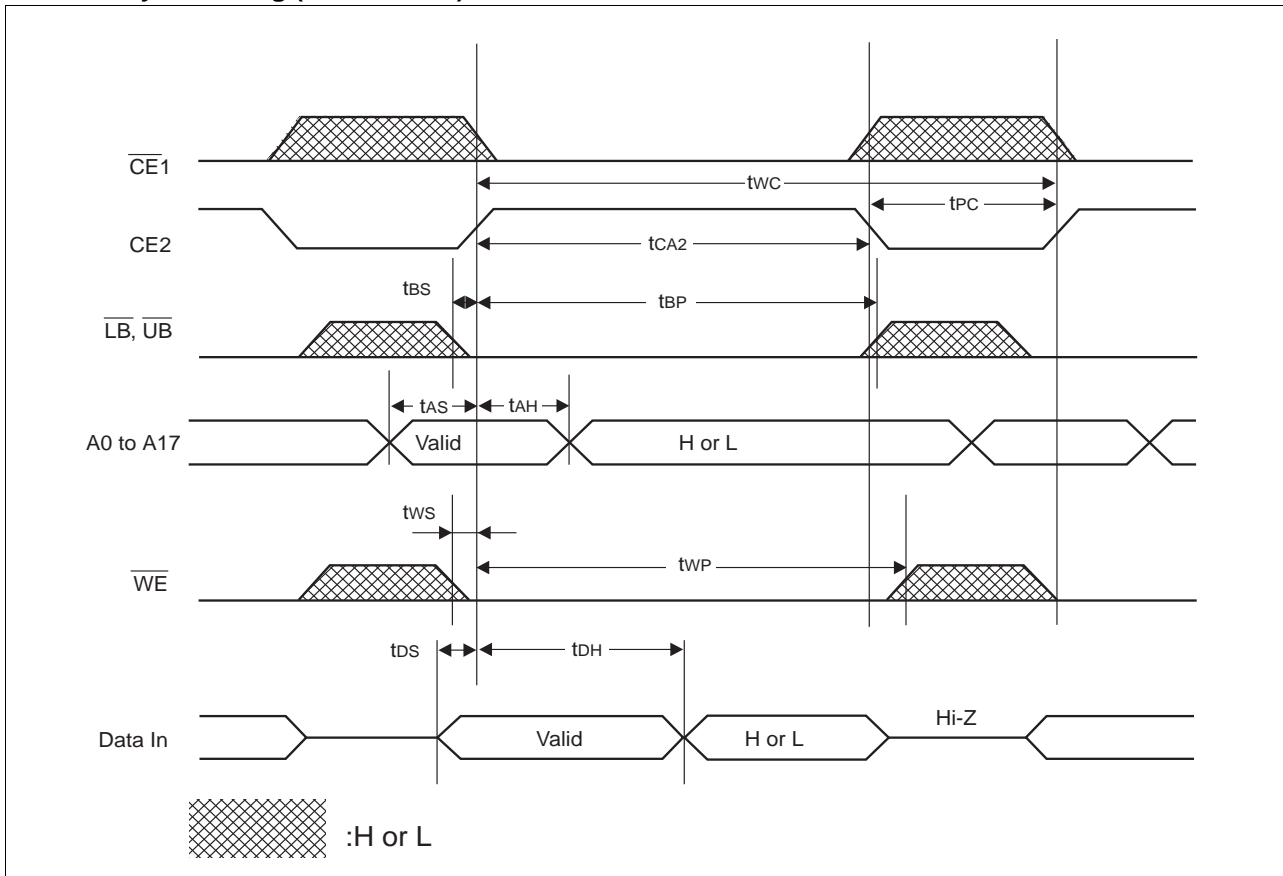
## 3. Read Cycle Timing ( $\overline{\text{OE}}$ Control)



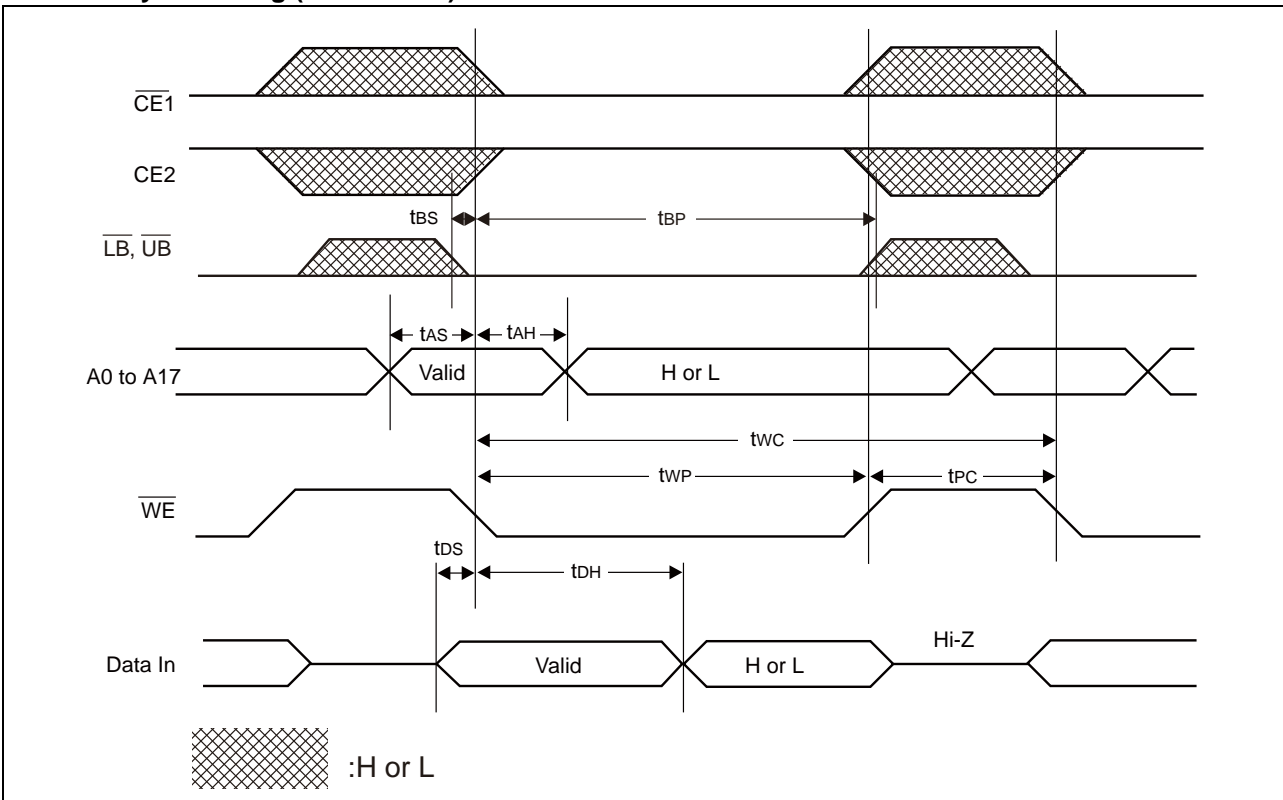
## 4. Write Cycle Timing ( $\overline{\text{CE1}}$ Control)



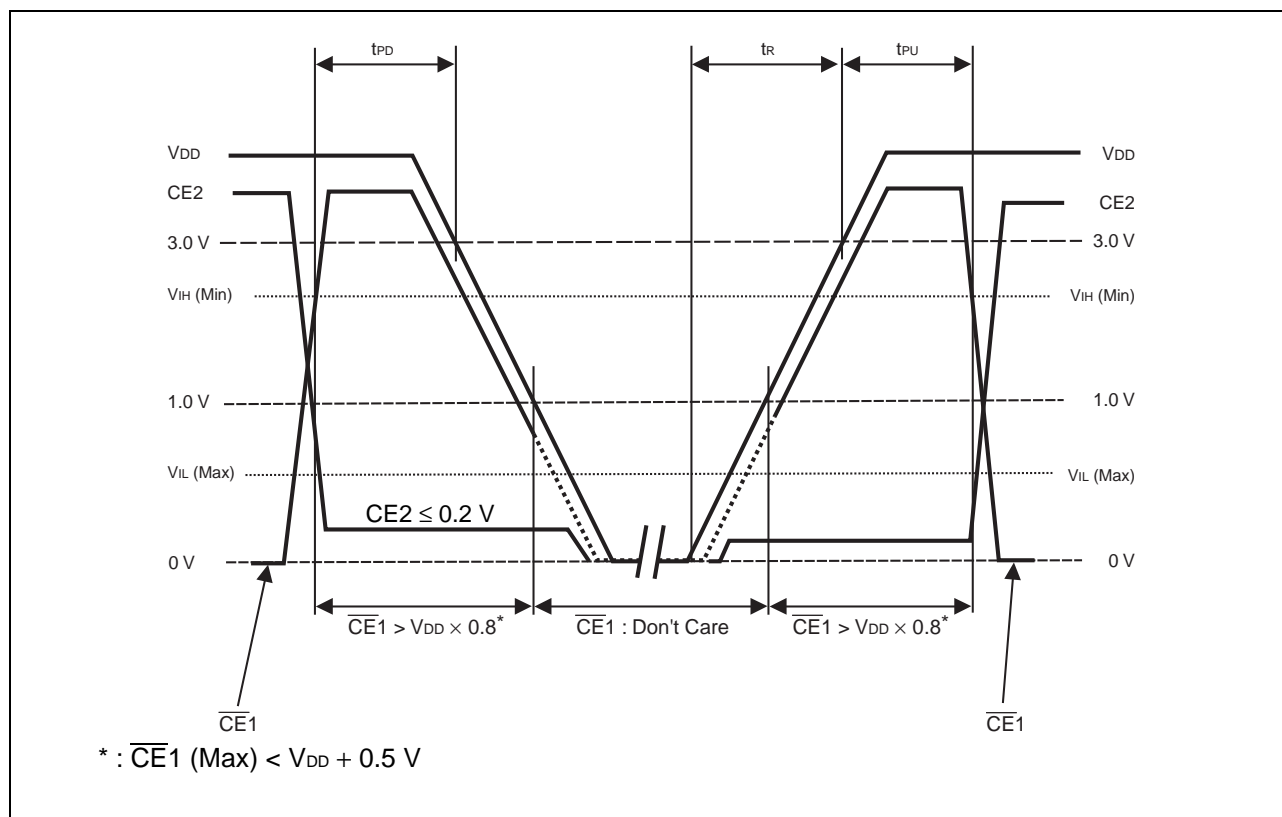
## 5. Write Cycle Timing (CE2 Control)



## 6. Write Cycle Timing (WE Control)



## ■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CE1}$ level hold time for Power OFF	$t_{PD}$	85	—	—	ns
$\overline{CE1}$ level hold time for Power ON	$t_{PU}$	85	—	—	ns
Power supply rising time	$t_r$	0.05	—	200	ms

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

In case the power is turned on or off, use the power supply reset IC and fix the CE2 to low level, to prevent unexpected writing. Use either of  $\overline{CE1}$  or CE2, or both to disable control of the device.

## ■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	$10^{10}$	—	Times/byte	Operation Ambient Temperature $T_A = +85\text{ }^{\circ}\text{C}$
Data Retention*2	10	—	Years	Operation Ambient Temperature $T_A = +55\text{ }^{\circ}\text{C}$
	55	—		Operation Ambient Temperature $T_A = +35\text{ }^{\circ}\text{C}$

\*1 : Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

\*2 : Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

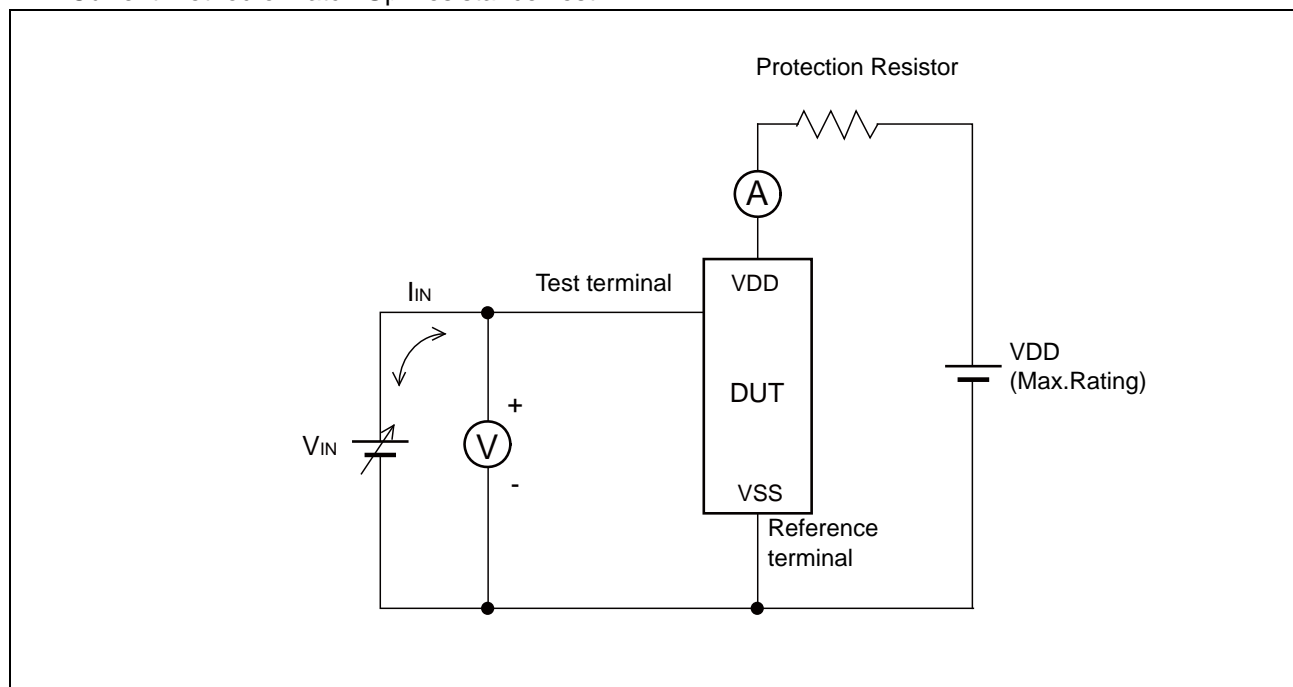
## ■ NOTES ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

## ■ ESD AND LATCH-UP

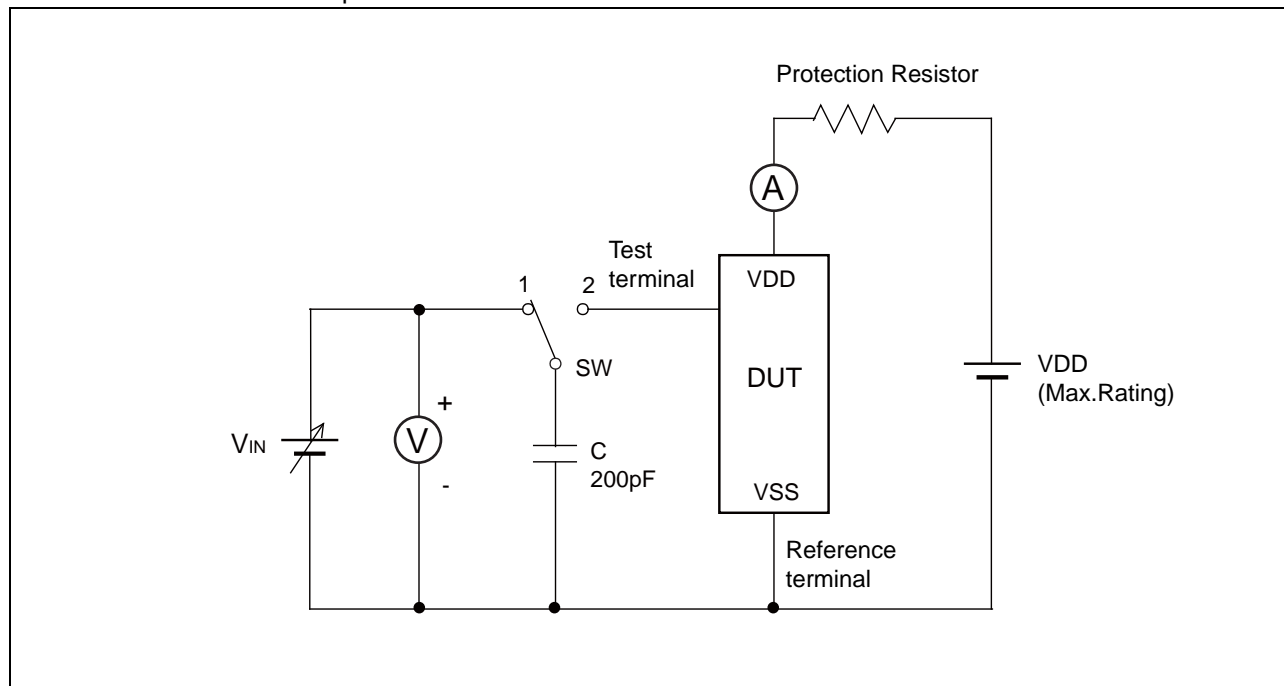
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R4002ANC-GE1	$\geq  2000 \text{ V} $
ESD MM (Machine Model) JESD22-A115 compliant		$\geq  200 \text{ V} $
ESD CDM (Charged Device Model) JESD22-C101 compliant		—
Latch-Up (I-test) JESD78 compliant		—
Latch-Up ( $V_{\text{supply}}$ overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		$\geq  300 \text{ mA} $
Latch-Up (C-V Method) Proprietary method		—

### • Current method of Latch-Up Resistance Test



Note : The voltage  $V_{IN}$  is increased gradually and the current  $I_{IN}$  of 300 mA at maximum shall flow.  
 Confirm the latch up does not occur under  $I_{IN} = \pm 300 \text{ mA}$ .  
 In case the specific requirement is specified for I/O and  $I_{IN}$  cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

- C-V method of Latch-Up Resistance Test



Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle.  
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5 times, this test must be stopped immediately.

## ■ REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

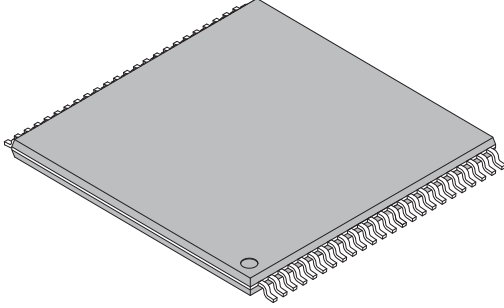
## ■ ORDERING INFORMATION

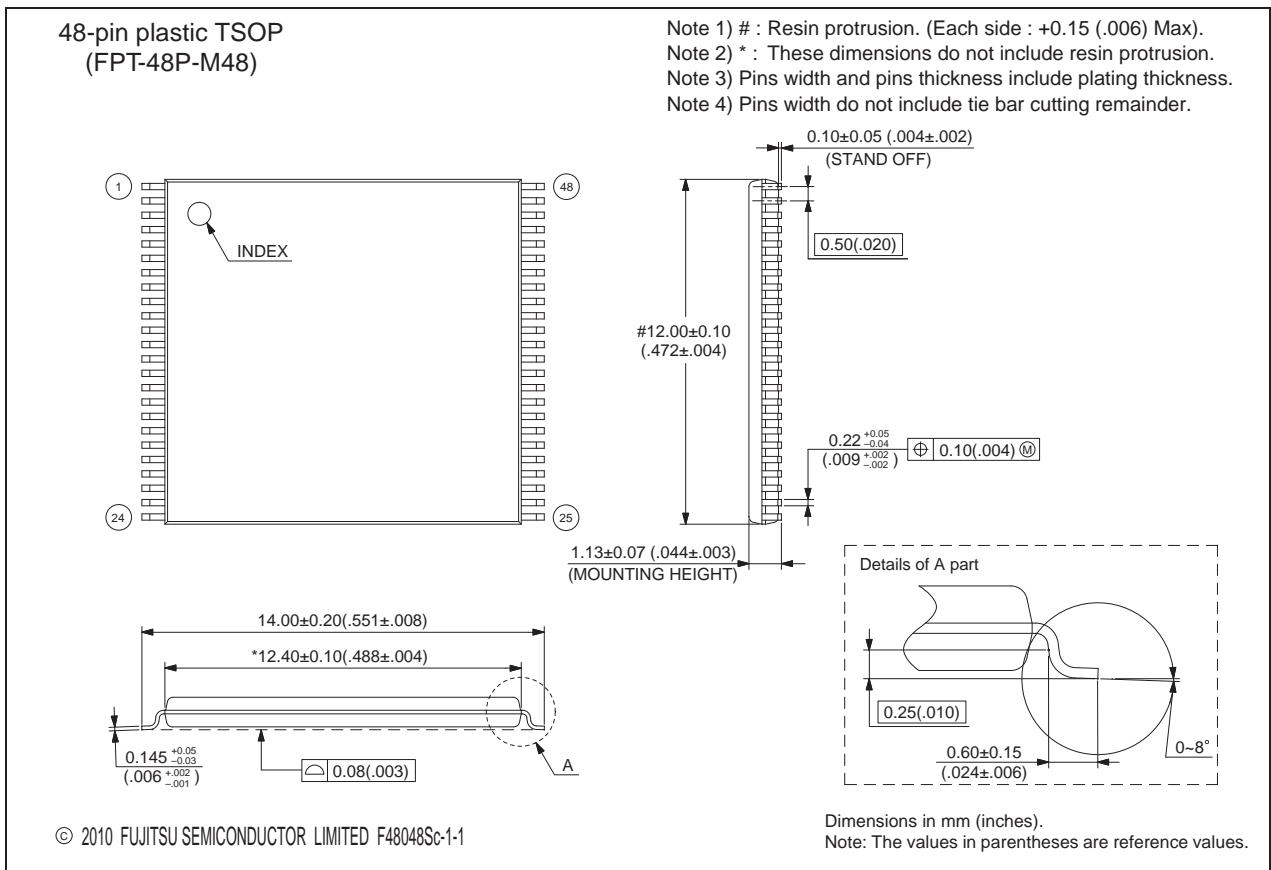
Part Number	Package	Shipping form	Minimum shipping quantity
MB85R4002ANC-GE1	48-pin plastic TSOP (FPT-48P-M48)	Tray	—*

\*: Please contact our sales office about minimum shipping quantity.

# MB85R4002A

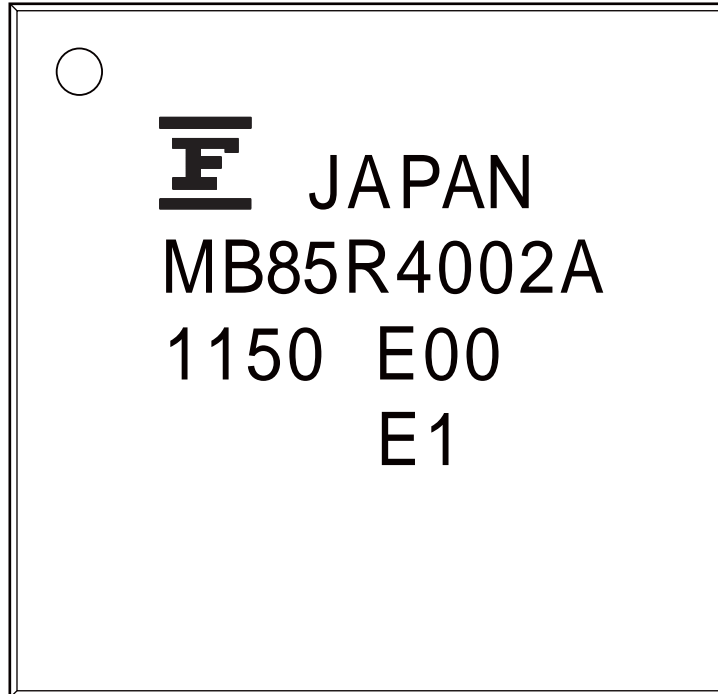
## ■ PACKAGE DIMENSIONS

<div>48-pin plastic TSOP</div>  <div>(FPT-48P-M48)</div>	Lead pitch	0.50 mm
	Package width × package length	12.00 mm × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.36 g



## ■ MARKING

[MB85R4002ANC-GE1]

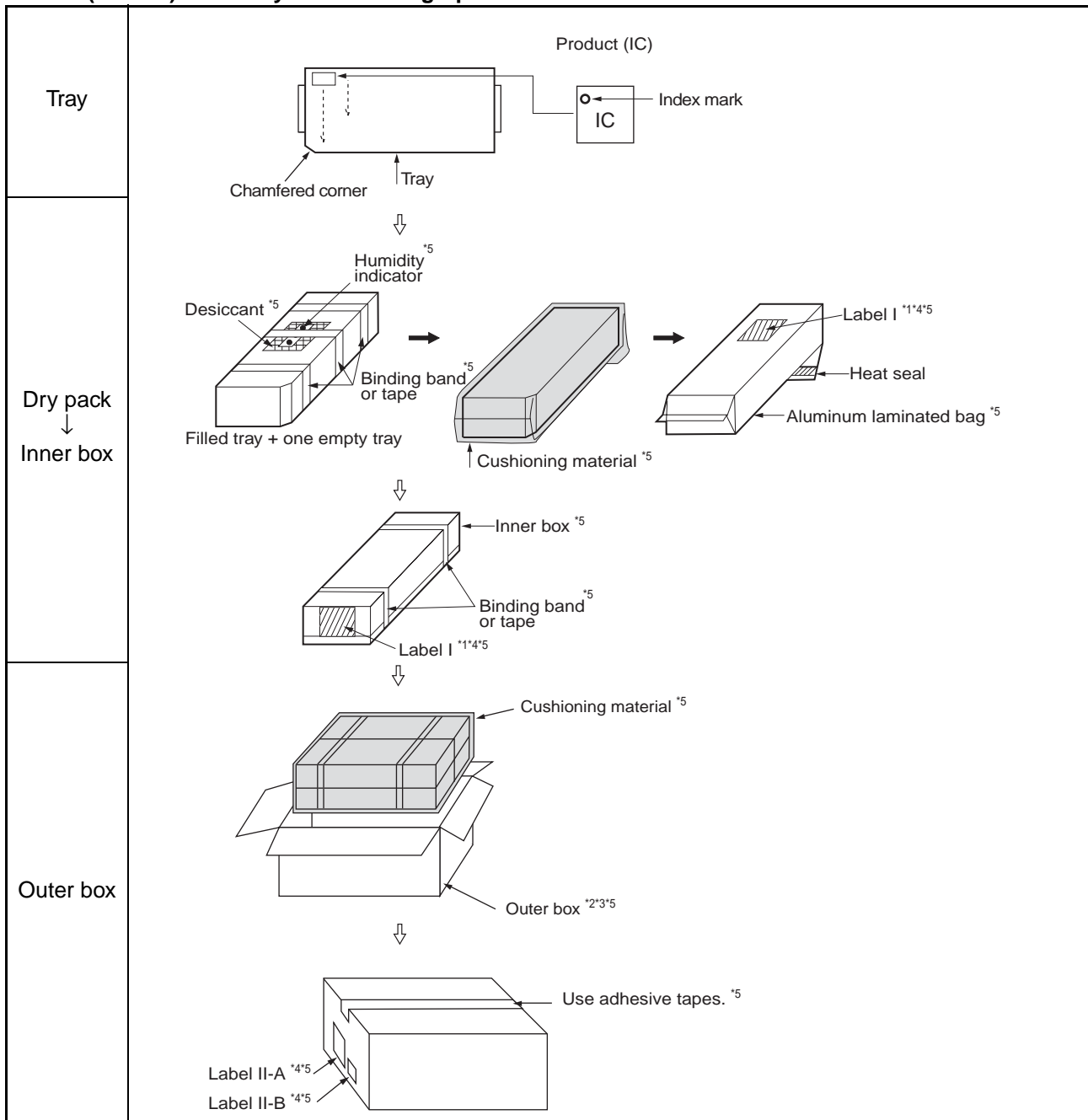


[FPT-48P-M48]





## 1.2 IEC (JEDEC) TRAY Dry Pack Packing Specifications



\*1: For a product of which part number is suffixed with "E1", a "G" (Pb) marks is display to the moisture barrier bag and the inner boxes.

\*2: The size of the outer box may be changed depending on the quantity of inner boxes.

\*3: The space in the outer box will be filled with empty inner boxes, or cushions, etc.

\*4: Please refer to an attached sheet about the indication label.

\*5: The packing materials except tray may differ slightly from the color and dimensions depend on country of manufacture.

Note: The packing specifications may not be applied when the product is delivered via a distributor.

# MB85R4002A

## 1.3 Product label indicators

**Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss tapping)**  
**[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]**

XXXXXXXXXXXXXXXX (Customer part number or FJ part number)	← C-3 Label
(3N)1 XXXXXXXXXXXXXXXX XXX (LEAD FREE mark) (Part number and quantity) QC PASS	
(3N)2 XXXXXXXXXXXX XXXXXX (FJ control number)	← Perforated line
XXX pcs (Quantity) XXXXXXXXXXXXXXXX (Customer part number or FJ part number) (Customer part number or FJ part number bar code)	
XXXX/XX/XX (Packed years/month/day) ASSEMBLED IN xxxx	← Supplemental Label
XXXXXXXXXXXXXXXX (Customer part number or FJ part number) (FJ control number bar code)	
XXXXXXXXXXXXXXXX (Package count) XXX-XXX XXX XXXXXXXXXXXX (FJ control number) (Lot Number and quantity) XXXXXXXXXXXXXXXX (Comment)	

**Label II-A: Label on Outer box [D Label] (100mm x 100mm)**

← D Label	
発注者 XXXXXXXXXXXX (Customer Name) (CUST.)	受注者 (VENDOR) 富士通
受渡場所名 XXXXXXXXXXXX (Delivery Address) (DELIVERY POINT)	セミコンダクター株式会社
納品キー番号 XXXXXXXXXXXXXXXX (TRANS.NO.) (FJ control number)	XXX (FJ control number)
品名コード XXXXXXXXXXXXXXXX (PART NO.) (Customer part number or FJ part number)	XXX (FJ control number)
品名 (PART NAME) XXXXXXXXXXXXXXXX (Part number)	XXXXXXXXXXXXXXXX (Part number)
人数／納入数量 XXX/XXX (Q'TY/TOTAL Q'TY)	単位 XX (UNIT)
発注者用備考 (CUSTOMER'S REMARKS) XXXXXXXXXXXXXXXXXXXXX	梱包個数 (PACKAGE COUNT) XXX/XXX
(3N)3 XXXXXXXXXXXXXXXX XXX (FJ control number + Product quantity) (FJ control number + Product quantity bar code)	
(3N)4 XXXXXXXXXXXXXXXX XXX (Part number + Product quantity) (Part number + Product quantity bar code)	
(3N)5 XXXXXXXXXXXXXXXX (FJ control number) (FJ control number bar code)	

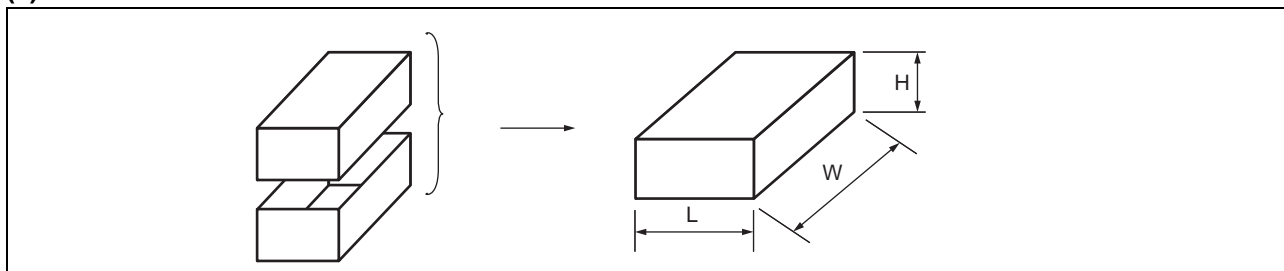
**Label II-B: Outer boxes product indicate**

XXXXXXXXXXXXXXXX (Part number)		
(Lot Number)	(Count)	(Quantity)
XXXX-XXX	X 箱	XXX 個
XXXX-XXX	X 箱	XXX 個
	計	XXX 個

Note: Depending on shipment state, "Label II-A" and "Label II-B" on the external boxes might not be printed.

## 1.4 Dimensions for Containers

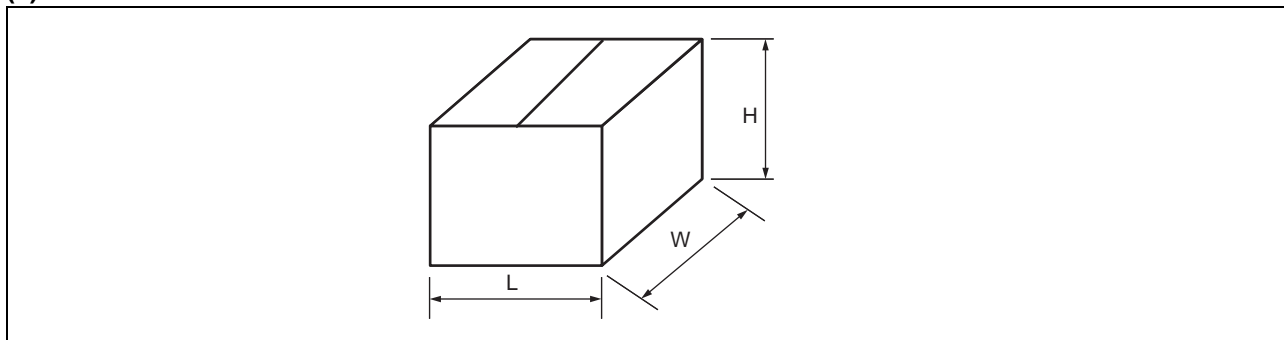
### (1) Dimensions for inner box



L	W	H
165	360	75

(Dimensions in mm)

### (2) Dimensions for outer box



L	W	H
355	385	195

(Dimensions in mm)

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

Page	Section	Change Results
1	■ DESCRIPTIONS	Deleted the “that is compatible with conventional asynchronous SRAM.”
5	■ RECOMMENDED OPERATING CONDITIONS	Added note on the Operation Ambient Temperature. Moved the “High Level Input Voltage” and “Low Level Input Voltage” to DC Characteristics.
6	1. DC Characteristics	Moved the “High Level Input Voltage” and “Low Level Input Voltage” from RECOMMENDED OPERATING CONDITIONS.
14	■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES	Deleted the URL info.

**MEMO**

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Edited: System Memory Business Division