Stereo 3.7W Class D Amplifier

ABSOLUTE MAXIMUM RATINGS

Voltage
- PVDD to PGND ..... -0.3V to +6V
- OUTL+, OUTR+, OUTL-, OUTR- to PGND ..... -0.3V to (V_{PVDD} + 0.3V)
- All Other Pins to PGND ..... -0.3V to +6V

Current
- Continuous Current Into/Out of PVDD, PGND, OUTL+, OUTR+, OUTL-, OUTR- ..... ±800mA
- Continuous Input Current (all other pins) ..... ±20mA

Duration of Short Circuit
- OUTL+, OUTR+, OUTL-, OUTR- to PGND or PVDD .... Continuous
- OUTL+ to OUTL- or OUTR+ to OUTR- ..... Continuous

Continuous Power Dissipation for a MultiLayer Board (T_A = +70°C)
- TDFN (deration 24.4mW/°C above +70°C) 1951.2mW

Junction Temperature ..... +150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (10s, soldering) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 41°C/W
Junction-to-Case Thermal Resistance (θ_{JA}) ..... 8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{PVDD} = $V_{\overline{SHDN}}$ = 3.7V, V_{PGND} = 0V, A_V = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Voltage Range	V_{PVDD}	Guaranteed by PSRR test	2.6		5.5	V
Undervoltage Lockout	UVLO			1.8	2.3	V
Quiescent Supply Current	I_{PVDD}	V_{PVDD} = 3.7V		2	2.7	mA
		V_{PVDD} = 5.0V		2.6		
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0, T_A = +25°C		< 1	10	µA
Turn On Time	t_{ON}			3.2	10	ms
Bias Voltage	V_{BIAS}		1.62	V_{PVDD}/2	2.15	V
Voltage Gain	A_V	GAIN = PGND	17.5	18	18.5	dB
		GAIN = 100kΩ to PGND	14.5	15	15.5	
		GAIN = PVDD	11.5	12	12.5	
		GAIN = 100kΩ to PVDD	8.5	9	9.5	
		GAIN = unconnected	5.5	6	6.5	
Channel-to-Channel Gain Tracking				0.1		%
Input Resistance	R_{IN}	A_V = 18dB (GAIN = PGND)	22	33		kΩ
		A_V = 15Db (GAIN = 100kΩ to PGND)	31	46		
		A_V = 12dB (GAIN = PVDD)	44	65		
		A_V = 9dB (GAIN = 100kΩ to PVDD)	62	93		
		A_V = 6dB (GAIN = unconnected)	89	131		
Common-Mode Rejection Ratio	CMRR	f_{IN} = 1kHz, input referred		79		dB
Output Offset Voltage	V_{OS}	T_A = +25°C (Note 3)		±1	±3	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 3.7V, V_{PGND} = 0V, A_V = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C A-weighted, 32 samples per second (Notes 3, 4)	Into shutdown		-79		dBV
			Out of shutdown		-73		
Power-Supply Rejection Ratio	PSRR	T_A = +25°C (Note 3)	V_{PVDD} = 2.6V to 5.5V, T_A = +25°C	70	95		dB
			f = 217Hz, 200mV_{P-P} ripple		83		
			f = 1kHz, 200mV_{P-P} ripple		83		
			f = 10kHz, 200mV_{P-P} ripple		77		
Output Power	P_{OUT}	THD+N = 10%	Z_{SPK} = 3Ω + 22µH, V_{PVDD} = 5.0V		3.7		W
			Z_{SPK} = 4Ω + 33µH, V_{PVDD} = 5.0V		3		
			Z_{SPK} = 8Ω + 68µH, V_{PVDD} = 5.0V		1.7		
			Z_{SPK} = 8Ω + 68µH, V_{PVDD} = 3.7V		0.9		
		THD+N = 1%	Z_{SPK} = 3Ω + 22µH, V_{PVDD} = 5.0V		2.9		
			Z_{SPK} = 4Ω + 33µH, V_{PVDD} = 5.0V		2.4		
			Z_{SPK} = 8Ω +68µH V_{PVDD} = 5.0V		1.4		
			Z_{SPK} = 8Ω +68µH V_{PVDD} = 3.7V		0.75		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz T_A = +25°C	Z_{SPK} = 3Ω +22µH, P_{OUT} = 1.6W, P_{VDD} = 5.0V		0.05		%
			Z_{SPK} = 4Ω +33µH, P_{OUT} = 650mW, P_{VDD} = 3.7V		0.05	0.75	
			Z_{SPK} = 4Ω +33µH, P_{OUT} = 1.3W, V_{PVDD} = 5.0V		0.04		
			Z_{SPK} = 8Ω +68µH, P_{OUT} = 725mW, P_{VDD} = 5.0V		0.03		
Output Noise		A-weighted (Note 3)			29		$µV_{RMS}$

Stereo 3.7W Class D Amplifier

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 3.7V, V_{PGND} = 0V, A_V = 12dB (GAIN = PVDD), R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

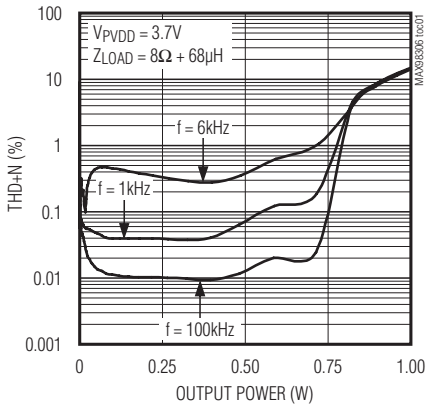
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	Z_{SPK} = 8Ω +68µH, P_{OUT} at 1% THD+N		99		dB
Efficiency	η	Z_{SPK} = 8Ω +68µH, P_{OUT} = 1.4W, f = 1kHz		92		%
Oscillator Frequency	f_{OSC}		160	320	540	kHz
Spread-Spectrum Bandwidth				20		kHz
Current Limit		T_A = +25°C		3		A
Thermal-Shutdown Level				+150		°C
Thermal Hysteresis				20		°C
DIGITAL INPUT ($\overline{SHDN}$)						
Input-Voltage High	V_{IH}		1.4			V
Input-Voltage Low	V_{IL}				0.4	V
Input Leakage Current		T_A = +25°C, $\overline{SHDN}$ = 0			±1	µA

Note 2: This device is 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: Amplifier inputs AC-coupled to ground.
Note 4: Specified at room temperature with an 8Ω resistive load in series with a 68µH inductive load.

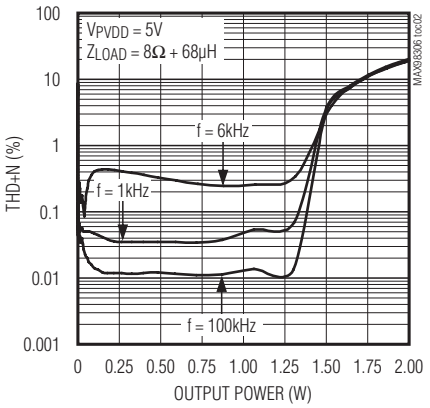
Typical Operating Characteristics

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)

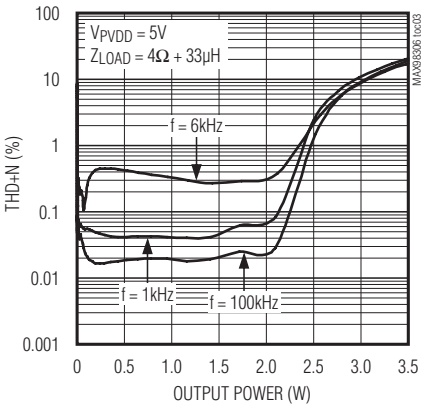
THD+N vs. OUTPUT POWER



THD+N vs. OUTPUT POWER



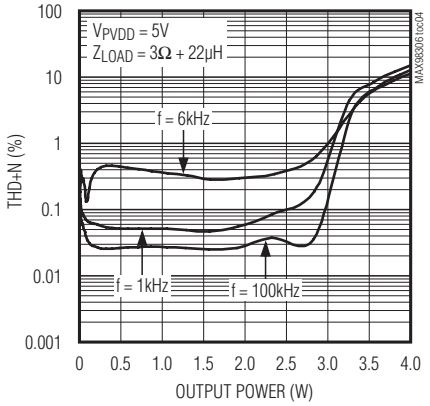
THD+N vs. OUTPUT POWER



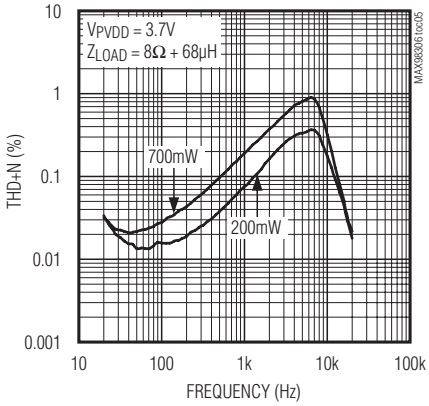
Typical Operating Characteristics (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)

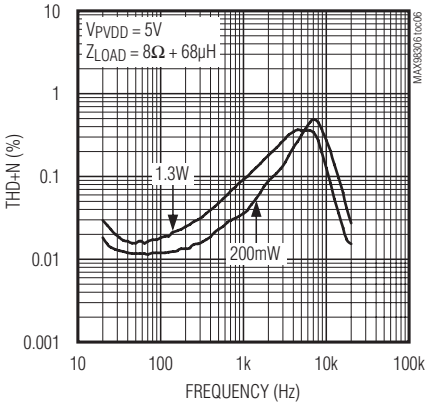
THD+N vs. OUTPUT POWER



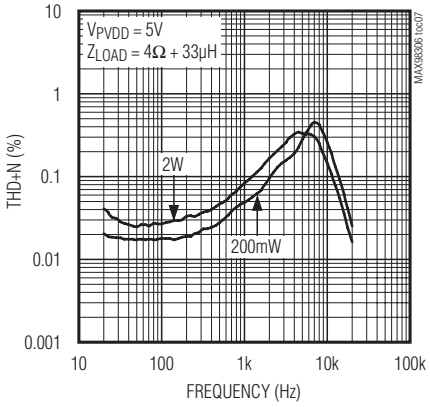
THD+N vs. FREQUENCY



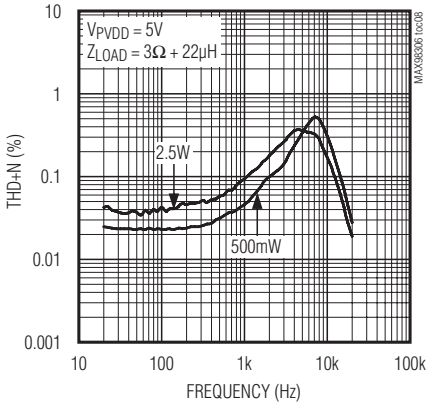
THD+N vs. FREQUENCY



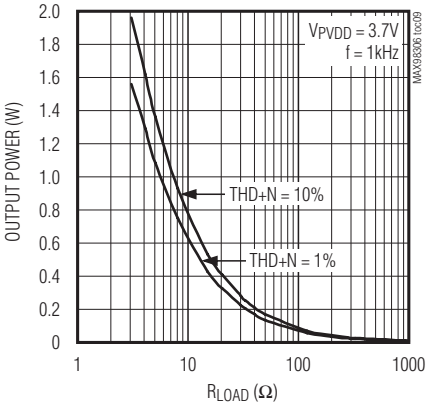
THD+N vs. FREQUENCY



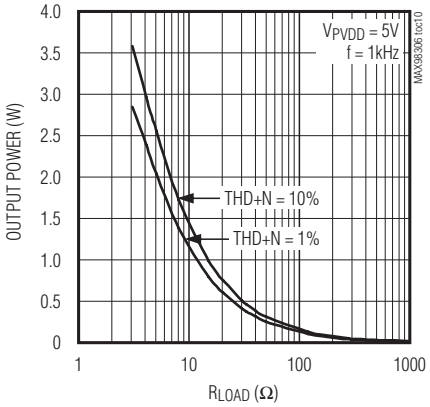
THD+N vs. FREQUENCY



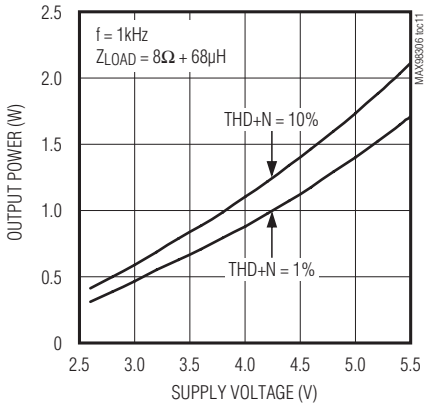
OUTPUT POWER vs. LOAD RESISTANCE



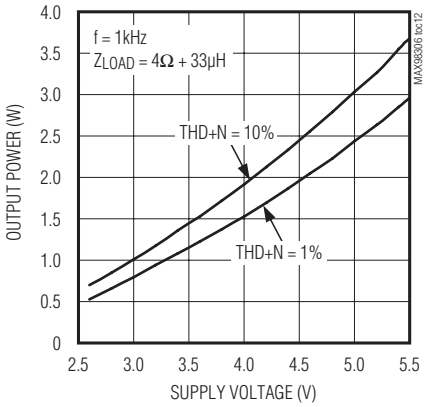
OUTPUT POWER vs. LOAD RESISTANCE



OUTPUT POWER vs. SUPPLY VOLTAGE



OUTPUT POWER vs. SUPPLY VOLTAGE

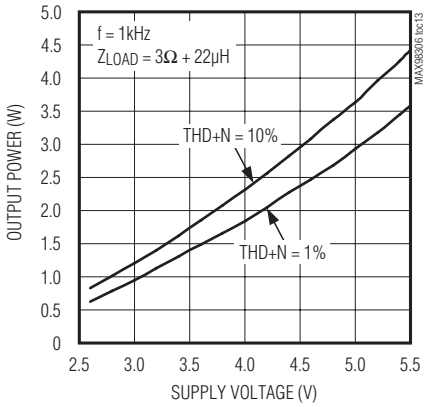


Stereo 3.7W Class D Amplifier

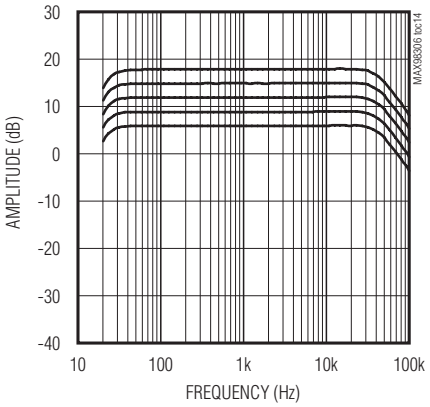
Typical Operating Characteristics (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)

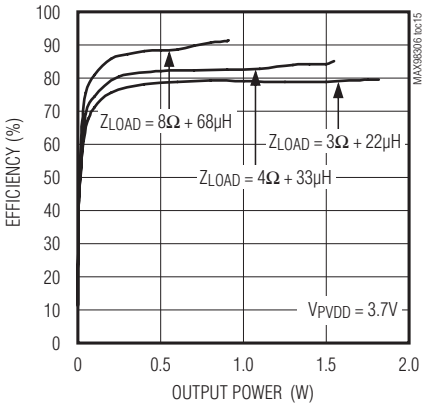
OUTPUT POWER vs. SUPPLY VOLTAGE



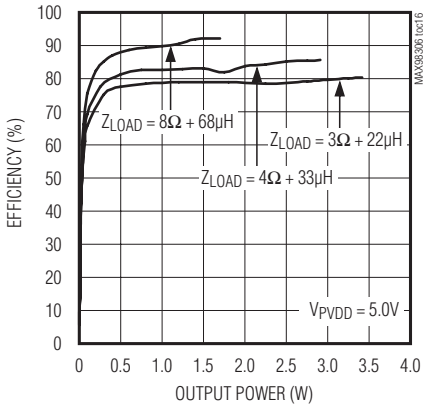
GAIN vs. FREQUENCY



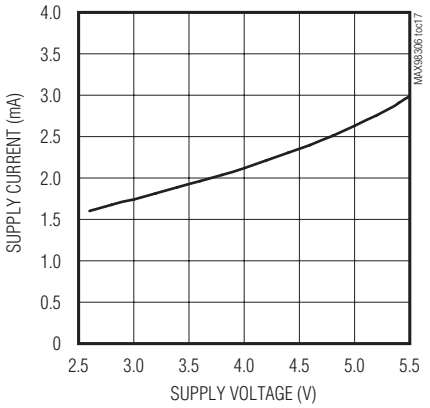
EFFICIENCY vs. OUTPUT POWER



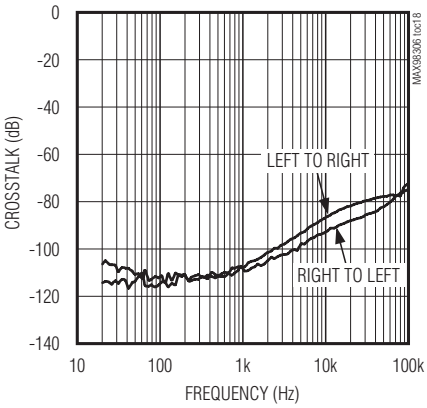
EFFICIENCY vs. OUTPUT POWER



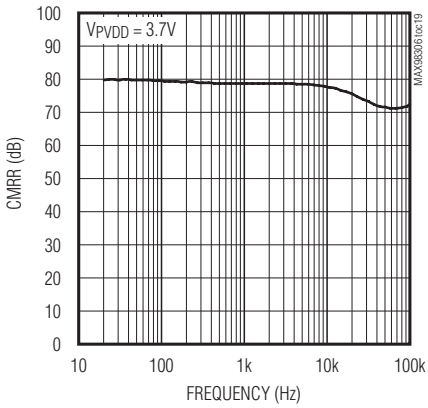
SUPPLY CURRENT vs. SUPPLY VOLTAGE



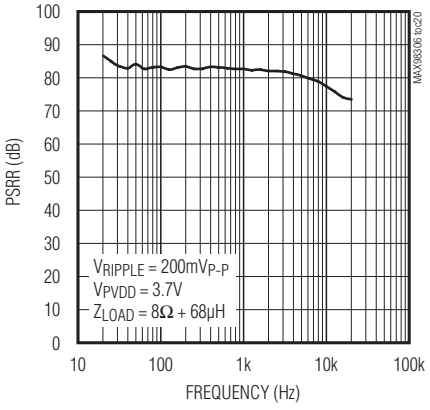
CROSSTALK vs. FREQUENCY



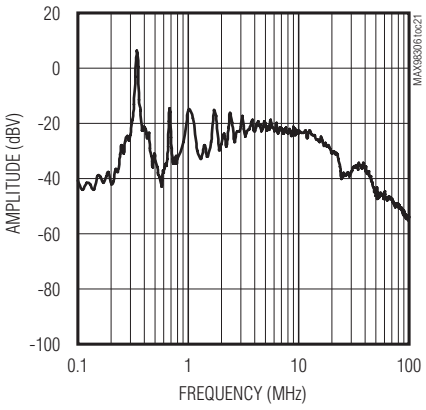
COMMON-MODE REJECTION RATIO vs. FREQUENCY



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



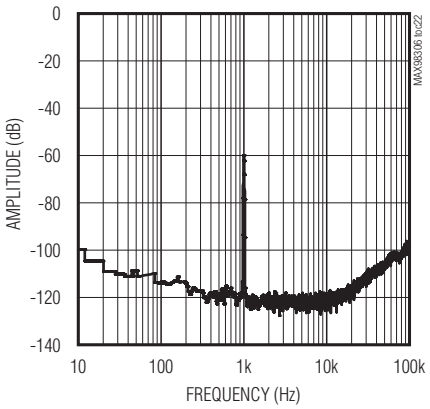
WIDEBAND vs. FREQUENCY



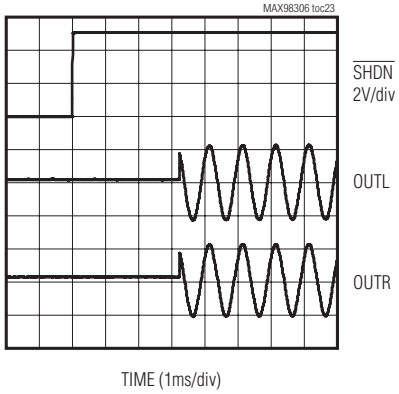
Typical Operating Characteristics (continued)

(V_{PVDD} = $V_{\overline{SHDN}}$ = 5.0V, V_{PGND} = 0V, A_V = 12dB, R_L = ∞, R_L connected between OUT_+ to OUT_-, 20Hz to 22kHz AC measurement bandwidth, T_A = +25°C, unless otherwise noted.)

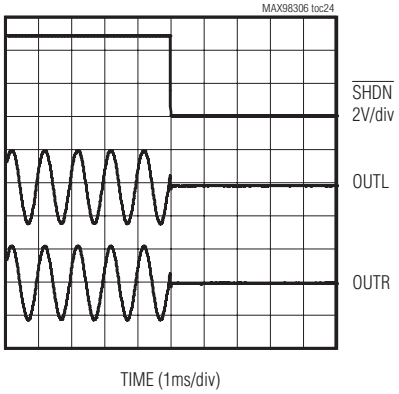
IN-BAND vs. FREQUENCY



STARTUP RESPONSE

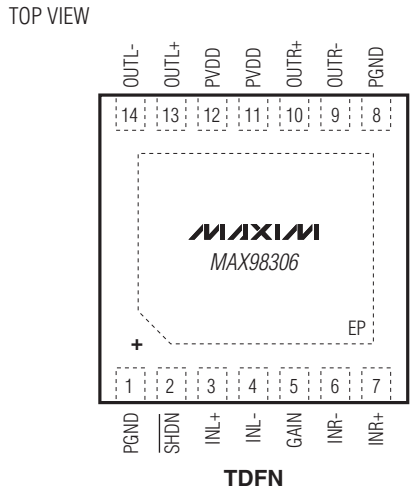


SHUTDOWN RESPONSE



Stereo 3.7W Class D Amplifier

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 8	PGND	Ground
2	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Drive $\overline{\text{SHDN}}$ to PGND to place the device into shutdown. Drive $\overline{\text{SHDN}}$ above 1.4V for normal operation.
3	INL+	Noninverting Audio Left Input
4	INL-	Inverting Audio Left Input
5	GAIN	Gain Select
6	INR-	Inverting Audio Right Input
7	INR+	Noninverting Audio Right Input
9	OUTR-	Negative Right Speaker Output
10	OUTR+	Positive Right Speaker Output
11, 12	PVDD	Power Supply. Bypass PVDD to PGND with a 0.1µF capacitor in parallel with a 10µF capacitor placed as close as possible to the device.
13	OUTL+	Positive Left Speaker Output
14	OUTL-	Negative Left Speaker Output
—	EP	Exposed Pad. Connect the exposed pad directly to ground.

Detailed Description

The MAX98306 features low quiescent current, a low-power shutdown mode, comprehensive click-and-pop suppression, and excellent RF immunity.

The IC offers Class AB audio performance with Class D efficiency in a minimal board-space solution.

The Class D amplifier features spread-spectrum modulation, active emissions limiting, edge-rate, and overshoot control circuitry that offers significant improvements to switch-mode amplifier radiated emissions.

The amplifier also features click-and-pop suppression that reduces audible transients on startup and shutdown, as well as thermal-overload and short-circuit protection.

Class D Speaker Amplifier

The filterless Class D amplifier output stage offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the pulse-width modulated (PWM) rail-to-rail switching operation of the output stage transistors. This ensures that any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active-emissions-limiting edge-rate control circuitry and spread-spectrum modulation reduce EMI emissions, while maintaining up to 92% efficiency.

Spread-spectrum modulation and active emissions limiting limit wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The IC's spread-spectrum modulator randomly varies the switching frequency by ±20kHz around the center frequency (320kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 1).

Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (3A typ), the IC disables the outputs for approximately 100µs. At the end of 100µs, the outputs are reenabled. If the fault condition still exists, the IC continues to disable and reenable the outputs until the fault condition is removed.

Table 1. Gain Control Configuration

GAIN PIN	MAXIMUM GAIN (dB)
Connect to PGND	18
Connect to PGND through 100kΩ ±5% resistor	15
Connect to PVDD	12
Connect to PVDD through 100kΩ ±5% resistor	9
Unconnected	6

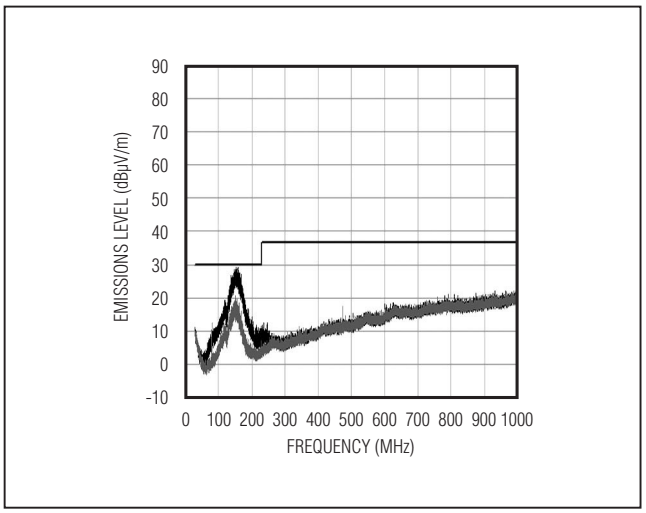


Figure 1. EMI with 12in of Speaker Cable and No Output Filter

Selectable Gain

The IC offers five programmable gains selected using the GAIN input.

Shutdown

The IC features a low-power shutdown mode, drawing ≤ 1µA (typ) of supply current. Drive $\overline{SHDN}$ low to place the MAX98306 into shutdown. Drive $\overline{SHDN}$ above 1.4V for normal operation.

Click-and-Pop Suppression

The IC speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces any audible transient sources internal to the device. When entering shutdown, the differential speaker outputs ramp down to PGND quickly and simultaneously.

Applications Information

Filterless Class D Operation

Traditional Class D amplifiers require an output filter. The filter adds cost and size and decreases THD performance. The IC's filterless modulation scheme does not require an output filter.

Because the switching frequency of the IC is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Component Selection

Power-Supply Input (PVDD)

PVDD powers the speaker amplifier. PVDD ranges from 2.6V to 5.5V. Bypass PVDD with 0.1µF and 10µF capacitors to PGND. Apply additional bulk capacitance at the device if long input traces between PVDD and the power source are used.

Input Filtering

The input-coupling capacitor (C_{IN}), in conjunction with the amplifier's internal input resistance (R_{IN}), forms a highpass filter that removes the DC bias from the incoming signal. These capacitors allow the amplifier to bias the signal to an optimum DC level.

Assuming zero source impedance, C_{IN} is:

$$C_{IN} = \frac{1}{2\pi f_{-3dB} \times R_{IN}}$$

where f_{-3dB} is the -3dB corner frequency and R_{IN} is the typical value as specified in the *Electrical Characteristics* table. Use capacitors with adequately low-voltage coefficients for best low-frequency THD performance. Table 2 shows calculated capacitance values based on a 20Hz highpass filter.

Table 2. Capacitance Value for 20Hz Highpass Filter

GAIN	R_{IN} (kΩ)	C_{IN} for 20Hz (nF)
18	33	241
15	46	173
12	65	122
9	93	86
6	131	61

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

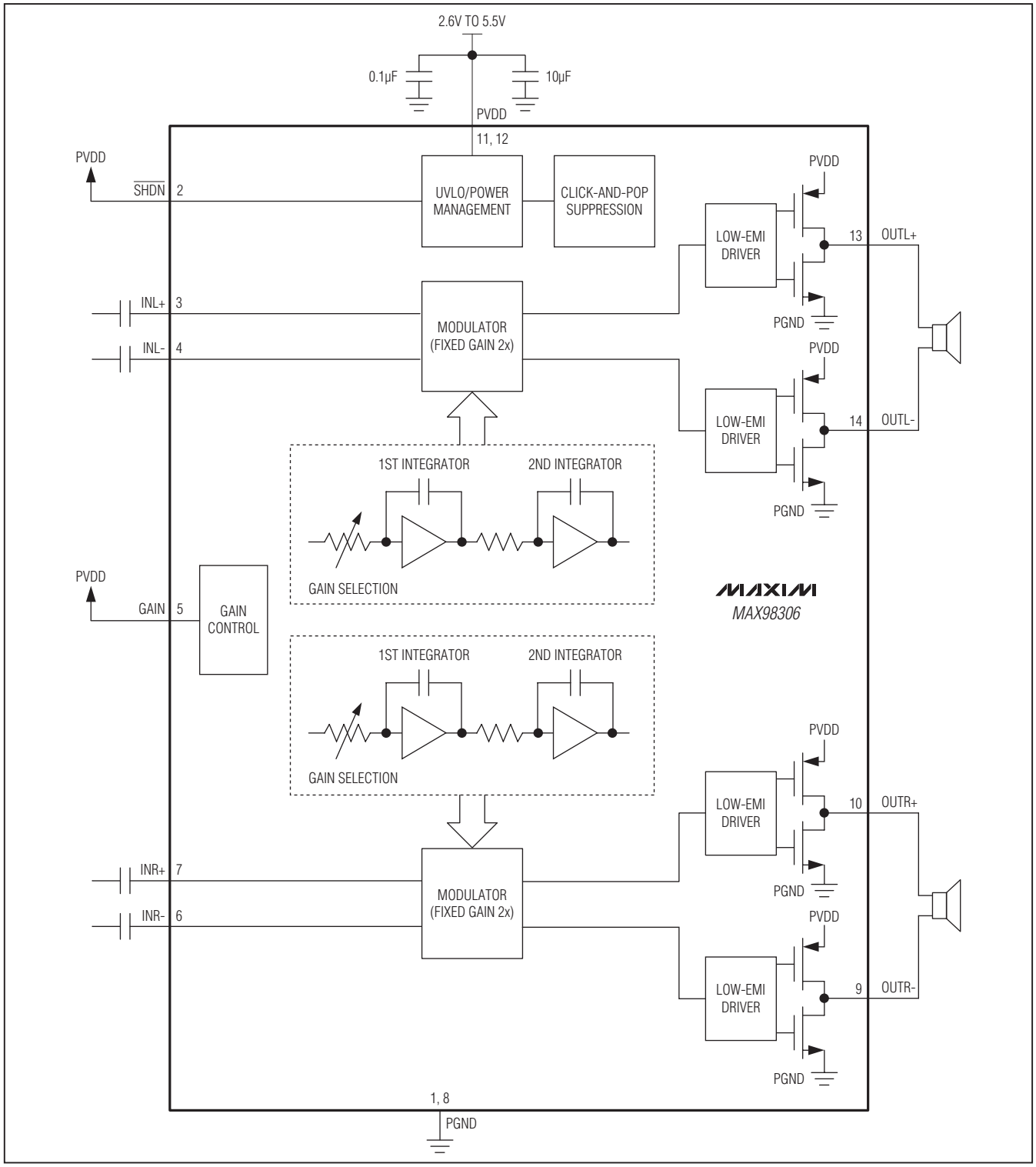
Use wide, low-resistance output traces. As the load impedance decreases, the current drawn from the device increases. At higher current, the resistance of the output traces decrease the power delivered to the load. For example, if 2W is delivered from the device output to a 4Ω load through 100mΩ of total speaker trace, 1.904W is delivered to the speaker. If power is delivered through 10mΩ of total speaker trace, 1.99W is delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the device.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

Chip Information

PROCESS: CMOS

Block Diagram

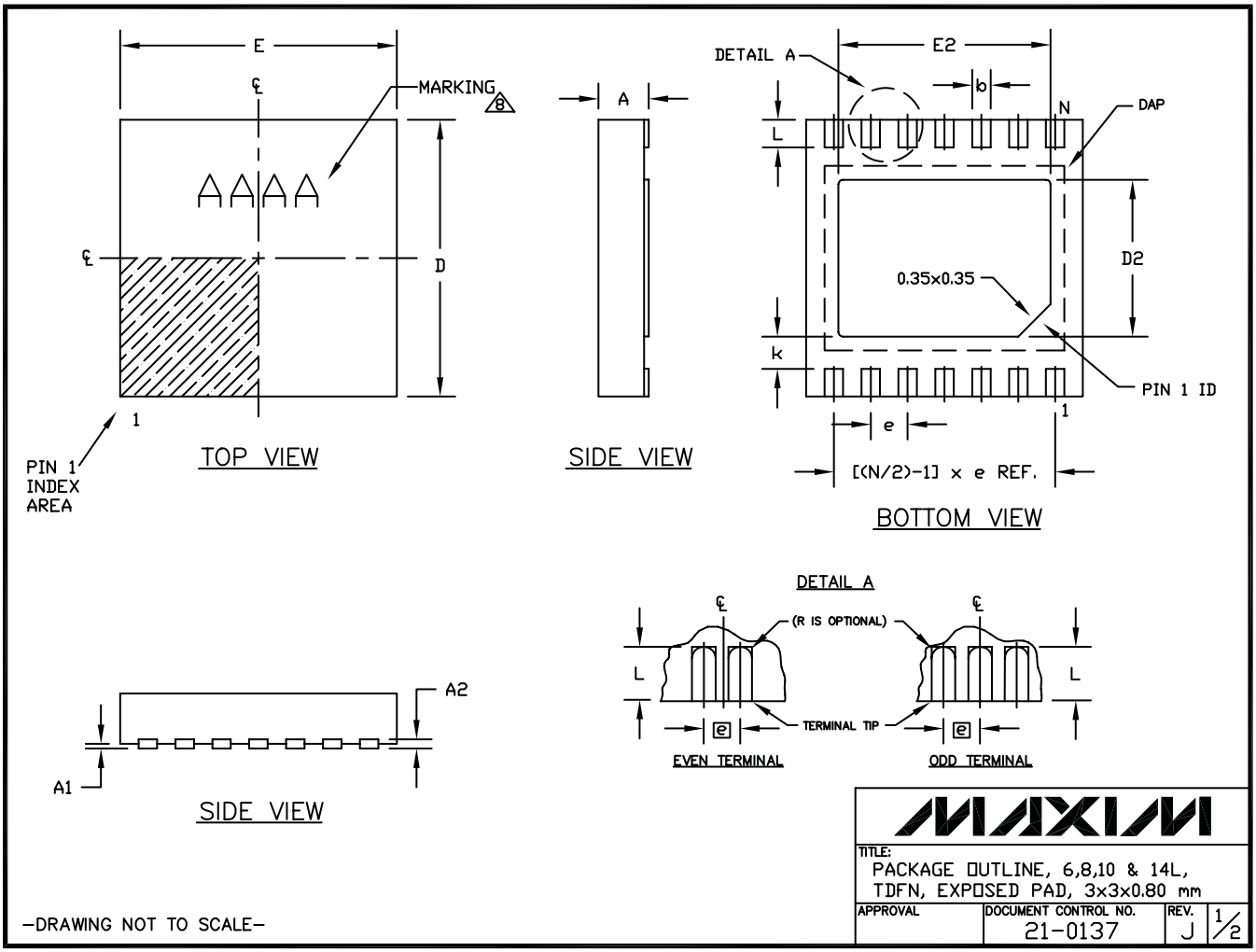


Stereo 3.7W Class D Amplifier

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TDFN	T1433+2	21-0137	90-0063



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	J	2/2

Stereo 3.7W Class D Amplifier

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/11	Initial release	—
1	8/11	Updated output power in *Electrical Characteristics*	3