Quad-SPDT, Clickless Audio Switches with Negative Signal Handling

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, CB_, $\overline{EN}$ .....-0.3V to +6.0V
COM_, NC_, NO_ .....(V_{CC} - 6V) to (V_{CC} + 0.3V)
Continuous Current NO_, NC_, COM_ .....±300mA
Peak Current NO_, NC_, COM_ (pulsed at 1ms, 50% duty cycle).....±400mA
Peak Current NO_, NC_, COM_ (pulsed at 1ms, 10% duty cycle).....±500mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin TQFN, Single-Layer Board (derate 15.6mW/°C above +70°C).....1250mW
16-Pin TQFN, Multilayer Board (derate 20.8mW/°C above +70°C).....1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, $\overline{EN}$ = low (MAX4911 only), unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{CC}			1.8		5.5	V
Supply Current	I_{CC}	V_{CC} = +5.5V, $V_{CB\_}$ = $V_{\overline{EN}}$ = 0V or V_{CC}			0.15	2	µA
		V_{CC} = +2.7V, $V_{CB\_}$ = $V_{\overline{EN}}$ = +0.5V or +1.4V				4	
		V_{CC} = +5.5V, $V_{CB\_}$ = $V_{\overline{EN}}$ = +0.5V or +1.4V				8	
ANALOG SWITCH							
Analog Signal Range	$V_{NC\_}$, $V_{NO\_}$, $V_{COM\_}$,	(Note 2)		V_{CC} - 5.5V		V_{CC}	V
On-Resistance (Note 3)	R_{ON}	Channels 1 and 3, V_{CC} = +3.3V, $V_{NC\_}$ or $V_{NO\_}$ = V_{CC} - 5.5V, -1V, 0V, +1V, +2V, V_{CC}, I_{COM1} = I_{COM3} = 100mA	T_A = +25°C		0.37	0.75	Ω
			T_A = T_{MIN} to T_{MAX}			0.8	
		Channels 2 and 4, V_{CC} = +3.3V, $V_{NC\_}$ or $V_{NO\_}$ = V_{CC} - 5.5V, -1V, 0V, +1V, +2V, V_{CC}, I_{COM2} = I_{COM4} = 100mA	T_A = +25°C		0.72	1.45	Ω
			T_A = T_{MIN} to T_{MAX}			1.6	
On-Resistance Match Between Channels (Notes 3, 4)	ΔR_{ON}	Channels 1 and 3, V_{CC} = +3.3V, $V_{NC\_}$ or $V_{NO\_}$ = 0, $I_{COM\_}$ = 100mA				0.1	Ω
		Channels 2 and 4, V_{CC} = +3.3V, $V_{NC\_}$ or $V_{NO\_}$ = 0, $I_{COM\_}$ = 100mA				0.1	
On-Resistance Flatness (Note 5)	R_{FLAT}	Channels 1 and 3, V_{CC} = +3.3V, $V_{NC\_}$ = $V_{NO\_}$ = V_{CC} - 5.5V, -1V, 0V, +1V, +2V, V_{CC}, $I_{COM\_}$ = 100mA				0.35	Ω
		Channels 2 and 4, V_{CC} = +3.3V, $V_{NC\_}$ = $V_{NO\_}$ = V_{CC} - 5.5V, -1V, 0V, +1V, +2V, V_{CC}, $I_{COM\_}$ = 100mA				0.6	
Shunt Switch Resistance	R_{SH}			2	3.8	6	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, $\overline{EN}$ = low (MAX4911 only), unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
NC_ Off-Leakage Current	$I_{NC\_(OFF)}$	MAX4912 (NC2 and NC4) only: V_{CC} = +2.7V, switch open, $V_{NC\_}$ = -2.5V or +2.5V, $V_{COM\_}$ = +2.5V or -2.5V	T_A = +25°C	-10		+10	nA
			T_A = T_{MIN} to T_{MAX}	-50		+50	
COM_ On-Leakage Current	$I_{COM\_(ON)}$	V_{CC} = +2.7V, switch closed; $V_{NC\_}$ or $V_{NO\_}$ = -2.5V, +2.5V, or floating; $V_{COM\_}$ = -2.5V, +2.5V, or floating	T_A = +25°C	-10		+10	nA
			T_A = T_{MIN} to T_{MAX}	-100		+100	
DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	V_{CC} = +2.7V, CB_ = low to high, R_L = 50Ω, C_L = 5pF, $V_{NO\_}$ = +1.5V, Figure 2			0.055	0.15	µs
Turn-Off Time	t_{OFF}	V_{CC} = +2.7V, CB_ = high to low, R_L = 50Ω, C_L = 5pF, $V_{NO\_}$ = +1.5V, Figure 2			0.3	1.0	µs
Break-Before-Make Delay Time	t_D	V_{CC} = +2.7V, CB_ = low to high or high to low, R_L = 50Ω, C_L = 5pF, $V_{NC\_}$ = $V_{NO\_}$ = +1.5V, Figure 3		1	25		ns
Charge Injection	Q	$V_{GEN\_}$ = 0, R_{GEN} = 0, C_L = 1nF, Figure 4			300		pC
Power-Supply Rejection Ratio	PSRR	f = 20kHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF			60		dB
Off-Isolation	V_{ISO}	f = 20kHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, Figure 5 (Note 6)			-90		dB
Crosstalk	V_{CT}	f = 20kHz, $V_{COM\_}$ = $1V_{RMS}$, R_L = 50Ω, Figure 5			-80		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, $V_{COM\_}$ = $0.5V_{P-P}$, R_L = 50Ω, DC bias = 0			0.05		%
NO_, NC_ Off-Capacitance	$C_{NO\_(OFF)}$	f = 1MHz, $V_{COM\_}$ = $0.5V_{P-P}$, DC bias = 0, Figure 6			100		pF
COM On-Capacitance	$C_{COM\_(ON)}$	f = 1MHz, $V_{COM\_}$ = $0.5V_{P-P}$, DC bias = 0, Figure 6			200		pF
DIGITAL INPUTS (CB_, $\overline{EN}$)							
Input Logic High	V_{IH}			1.4			V
Input Logic Low	V_{IL}					0.5	V
Input Leakage Current	I_{CB}, $I_{\overline{EN}}$	$V_{CB\_}$ = $V_{\overline{EN}}$ = 0V or V_{CC}		-1		+1	µA

Note 1: All parameters are production tested at T_A = +85°C and guaranteed by design over the specified temperature range.

Note 2: Signals on COM_, NO_, or NC_ exceeding V_{CC} are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 3: Guaranteed by design; not production tested.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

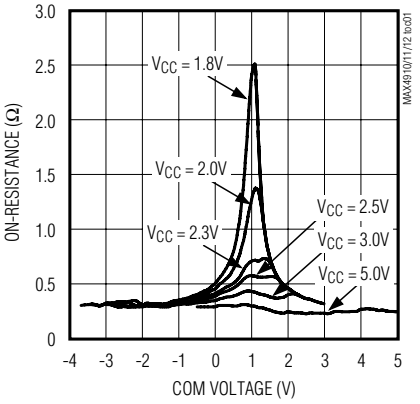
Note 6: Off-isolation = $20\log_{10}$ [$V_{COM\_}$/ $V_{NO\_}$], $V_{COM\_}$ = output, $V_{NO\_}$ = input to off switch.

Quad-SPDT, Clickless Audio Switches with Negative Signal Handling

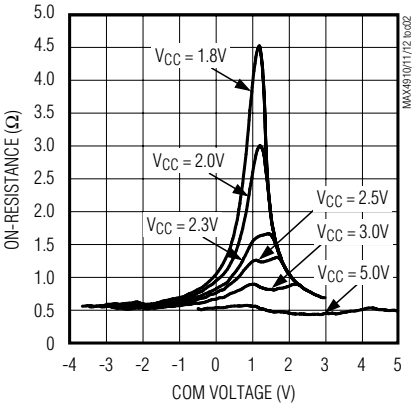
Typical Operating Characteristics

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

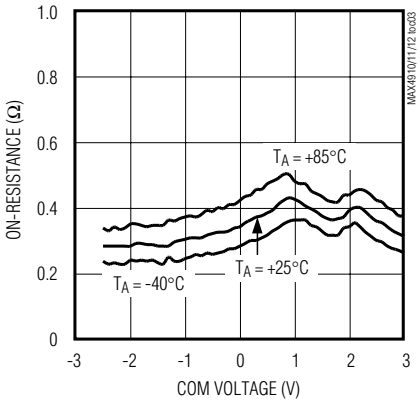
CHANNEL 1/3 ON-RESISTANCE vs. COM 1/3 VOLTAGE



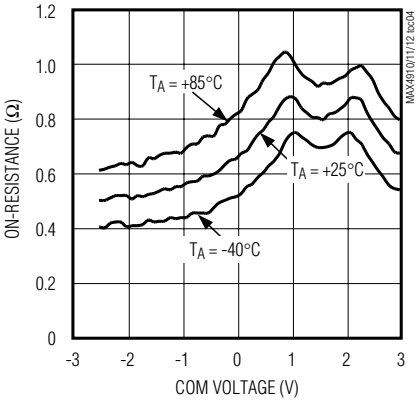
CHANNEL 2/4 ON-RESISTANCE vs. COM 2/4 VOLTAGE



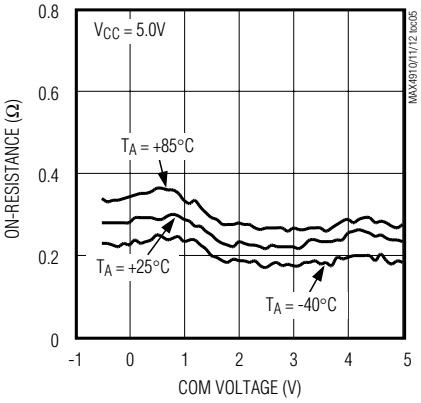
CHANNEL 1/3 ON-RESISTANCE vs. COM 1/3 VOLTAGE



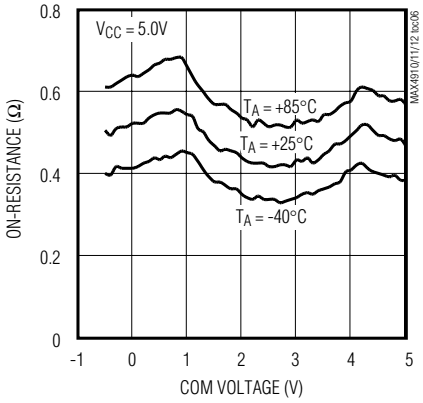
CHANNEL 2/4 ON-RESISTANCE vs. COM 2/4 VOLTAGE



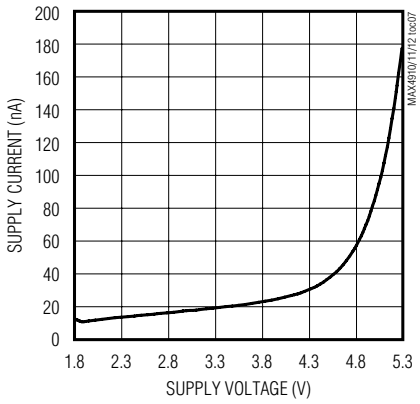
CHANNEL 1/3 ON-RESISTANCE vs. COM 1/3 VOLTAGE



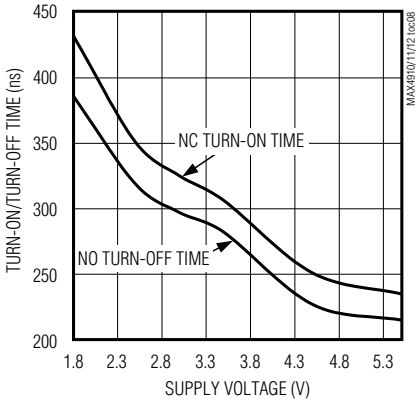
CHANNEL 2/4 ON-RESISTANCE vs. COM 2/4 VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



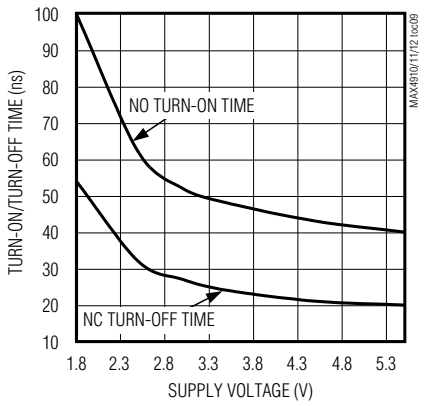
NC TURN-ON / NO TURN-OFF TIME vs. SUPPLY VOLTAGE



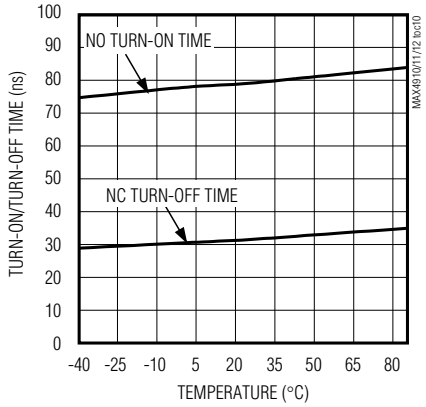
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

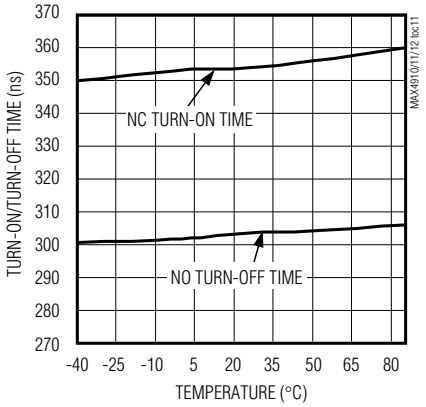
NO TURN-ON/NC TURN-OFF TIME vs. SUPPLY VOLTAGE



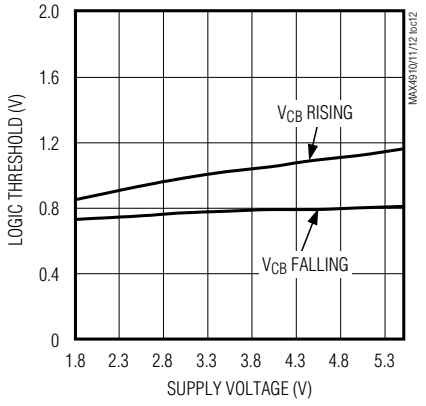
NO TURN-ON/NC TURN-OFF TIME vs. TEMPERATURE



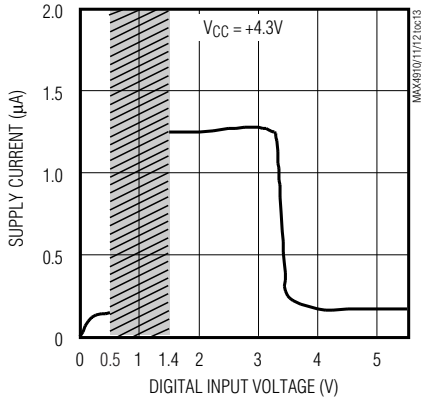
NC TURN-ON/NO TURN-OFF TIME vs. TEMPERATURE



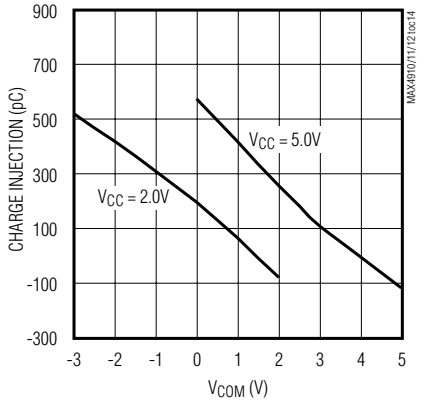
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



CHARGE INJECTION vs. COMMON VOLTAGE

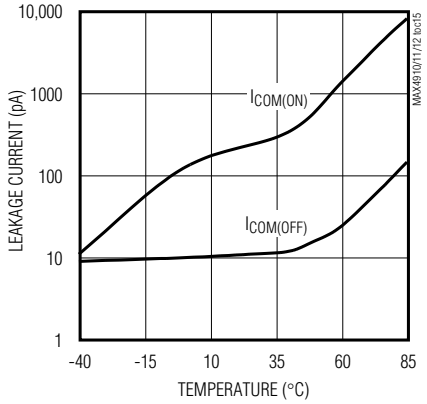


Quad-SPDT, Clickless Audio Switches with Negative Signal Handling

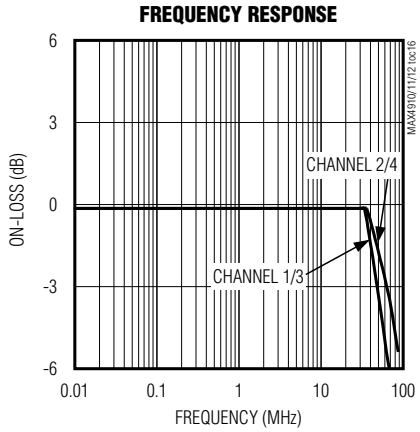
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

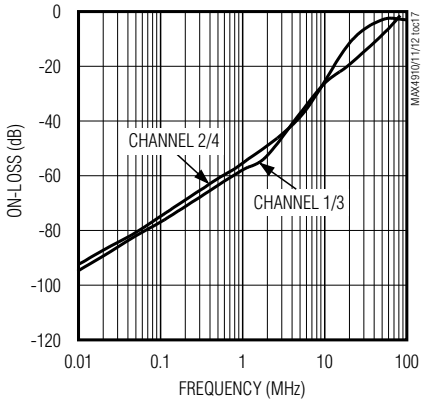
LEAKAGE CURRENT vs. TEMPERATURE



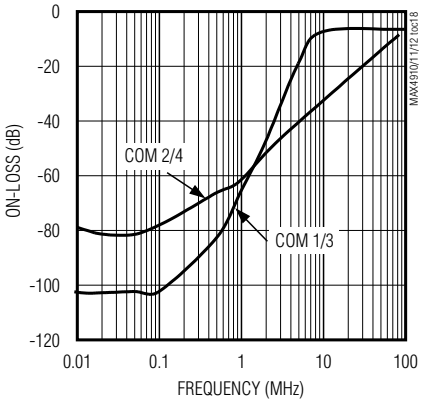
FREQUENCY RESPONSE



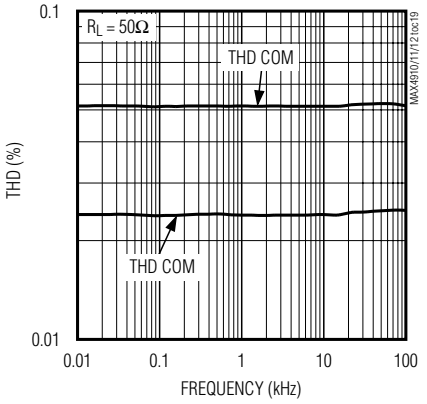
OFF-ISOLATION vs. FREQUENCY



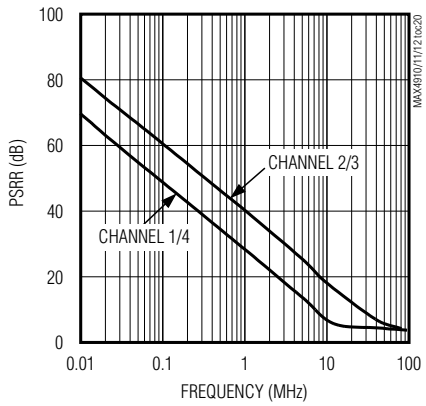
CROSSTALK vs. FREQUENCY



TOTAL HARMONIC DISTORTION vs. FREQUENCY



CHANNEL 2/3 POWER SUPPLY REJECTION RATIO vs. FREQUENCY



Pin Description

PIN		NAME	FUNCTION
MAX4910/ MAX4912	MAX4911		
1	1	NC1	Analog Switch 1—Normally Closed Terminal
2	—	CB1	Digital Control Input for Analog Switch 1 and Analog Switch 3
—	2	CB	Digital Control Input for All Analog Switches
3	3	NO2	Analog Switch 2—Normally Open Terminal
4	4	COM2	Analog Switch 2—Common Terminal
5	5	NC2	Analog Switch 2—Normally Closed Terminal
6	6	GND	Ground
7	7	NO3	Analog Switch 3—Normally Open Terminal
8	8	COM3	Analog Switch 3—Common Terminal
9	9	NC3	Analog Switch 3—Normally Closed Terminal
10	—	CB2	Digital Control Input for Analog Switch 2 and Analog Switch 4.
—	10	$\overline{EN}$	Enable Input. Driving $\overline{EN}$ high causes all switches to be high impedance. Pull $\overline{EN}$ low for normal operation.
11	11	NO4	Analog Switch 4—Normally Open Terminal
12	12	COM4	Analog Switch 4—Common Terminal
13	13	NC4	Analog Switch 4—Normally Closed Terminal
14	14	V_{CC}	Positive Supply Voltage Input
15	15	NO1	Analog Switch 1—Normally Open Terminal
16	16	COM1	Analog Switch 1—Common Terminal
—	—	EP	Exposed Pad. Connect to Ground

Detailed Description

The MAX4910/MAX4911/MAX4912 quad SPDT audio switches are low on-resistance, low supply current, high power-supply rejection ratio (PSRR) devices that operate from a +1.8V to +5.5V single supply. These devices feature a negative signal capability that allows signals below GND to pass through without distortion and break-before-make switching.

The MAX4910/MAX4912 have two digital control inputs CB1 and CB2 where each bit controls a pair of switches (see Table 1). The MAX4911 has an active-low enable $\overline{EN}$ and a digital control bit CB. Driving $\overline{EN}$ low takes the switches out of high impedance and CB controls all four switches (see Table 2). The MAX4910/MAX4911 have shunt resistors on all their NO and NC terminals to suppress click-and-pop sounds that may occur from switching to a precharged terminal. The MAX4912 does not have click-and-pop suppression resistors on NC2 and NC4 for applications that do not require predischarge switching.

Table 1. MAX4910/MAX4912 Truth Tables

CB1	NC1	NO1	NC3	NO3
0	On	Off	On	Off
1	Off	On	Off	On
CB2	**NC2**	**NO2**	**NC4**	**NO4**
0	On	Off	On	Off
1	Off	On	Off	On

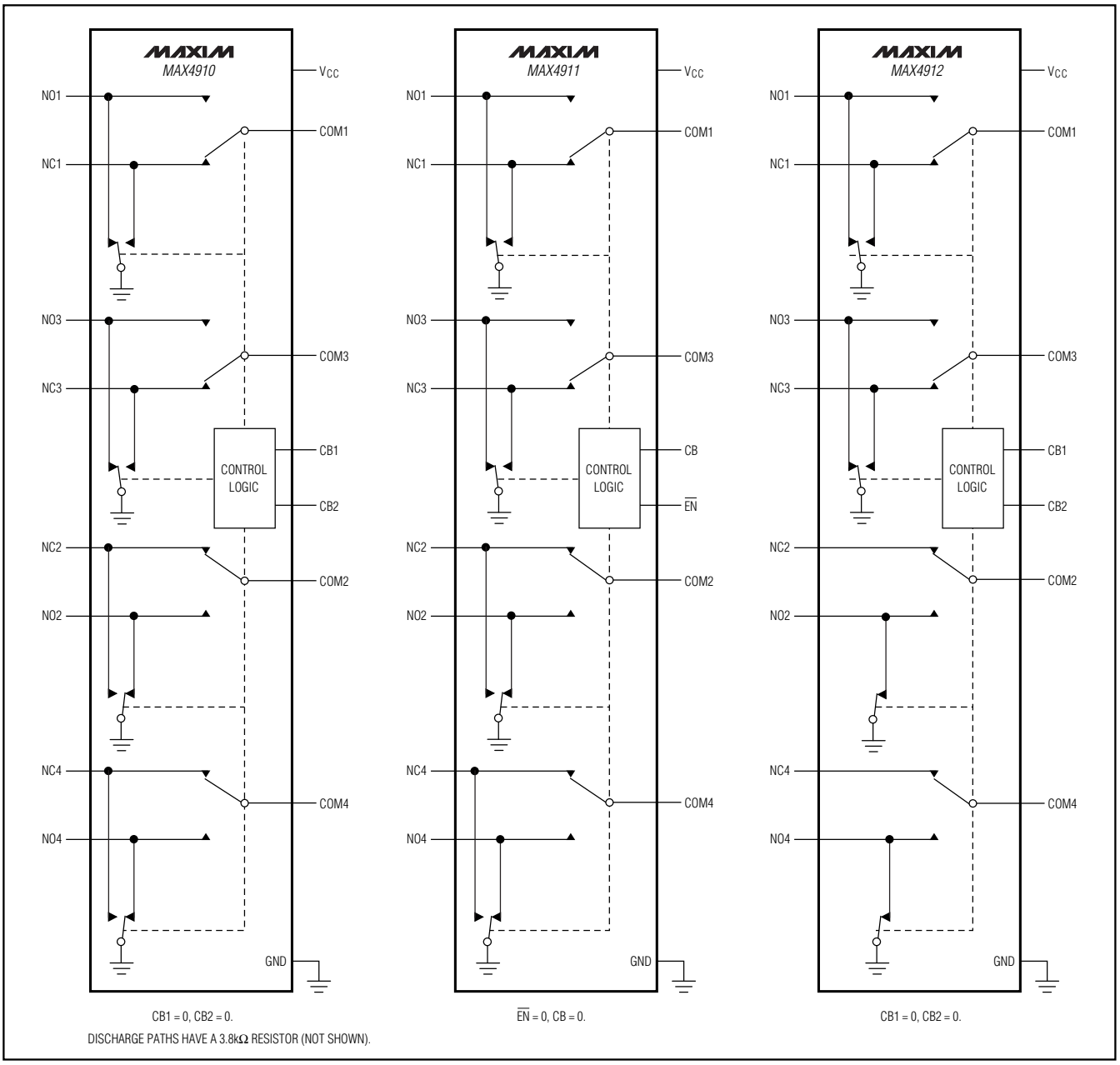
Table 2. MAX4911 Truth Table

$\overline{EN}$	CB	NC_	NO_
1	X	Off	Off
0	1	Off	On
0	0	On	Off

X = *Don't care.*

Quad-SPDT, Clickless Audio Switches with Negative Signal Handling

Functional Diagrams



Applications Information

Digital Control Inputs

The MAX4910/MAX4911/MAX4912 logic inputs accept up to +5.5V, regardless of supply voltage. For example, with a +3.3V supply, CB1, CB2, CB, and $\overline{EN}$ can be driven low to GND and high to +5.5V, allowing for mixed logic levels in a system. Driving CB, CB1, CB2, and $\overline{EN}$ rail-to-rail minimizes power consumption. For a +3.3V supply voltage, the logic thresholds are +0.5V (low) and +1.4V (high).

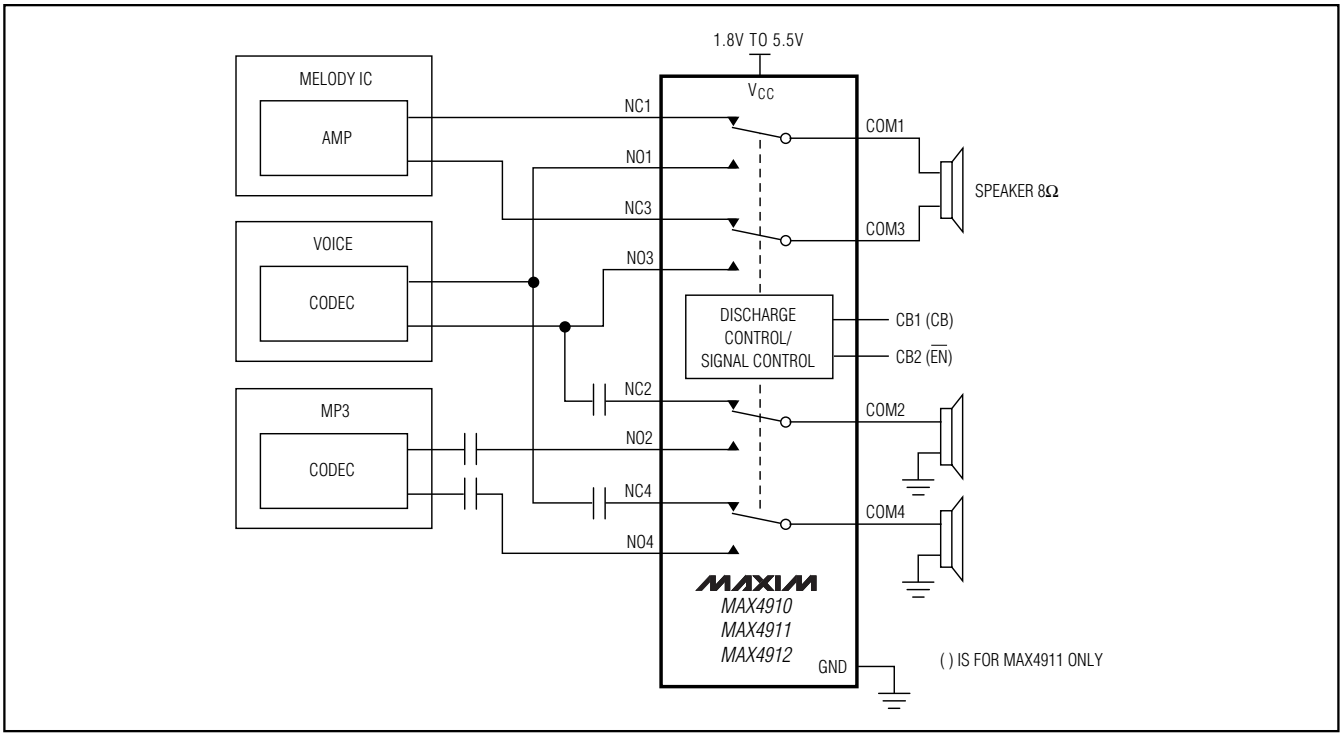


Figure 1. Typical Application Circuit

Analog Signal Levels

The MAX4910/MAX4911/MAX4912 on-resistance is channel dependant. Channels 1 and 3 have an on-resistance of 0.37Ω (typ), and channels 2 and 4 have an on-resistance of 0.72Ω (typ). The on-resistance flatness is guaranteed over temperature and shows minimal variation over the entire voltage supply range (see the *Typical Operating Characteristics*). The on-resistance flatness and low-leakage features make it ideal for bidirectional operation. The switches are bidirectional, so the NO_, NC_, and COM_ pins can be either inputs or outputs.

These devices pass signals as low as V_{CC} - 5.5V, including signals below ground with minimal distortion.

Click-and-Pop Suppression

The MAX4910/MAX4911 have a 3.8kΩ (typ) shunt resistor on all their NO and NC terminals to automatically discharge any capacitance when they are not connected to COM. The MAX4912 has shunt resistors on all NO, NC1, and NC3 terminals. The shunt resistors reduce audible click-and-pop sounds that occur when switching between audio sources.

Audible clicks and pops are caused when a step DC voltage is switched into the speaker. The DC step transients can be reduced by automatically discharging the side that is not connected to the COM terminal, reducing any residual DC voltage and reducing clicks and pops.

Break-Before-Make Switching

The MAX4910/MAX4911/MAX4912 feature break-before-make switching, which is configured to break (open) the first set of contacts before engaging (closing) the new contacts. This prevents the momentary connection of the old and new signal paths to the output, reducing click-and-pop sounds.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the Absolute Maximum Ratings since stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all CMOS devices. Improper supply sequencing can force the switch into latchup causing it to draw excessive supply current. The only way out of latchup is to recycle the power and properly reapply it. Connect all ground pins first, then apply power to V_{CC}, and finally apply signals to NO_, NC_, and COM_. Follow the reverse order upon power-down.

Quad-SPDT, Clickless Audio Switches with Negative Signal Handling

Test Circuits/Timing Diagrams

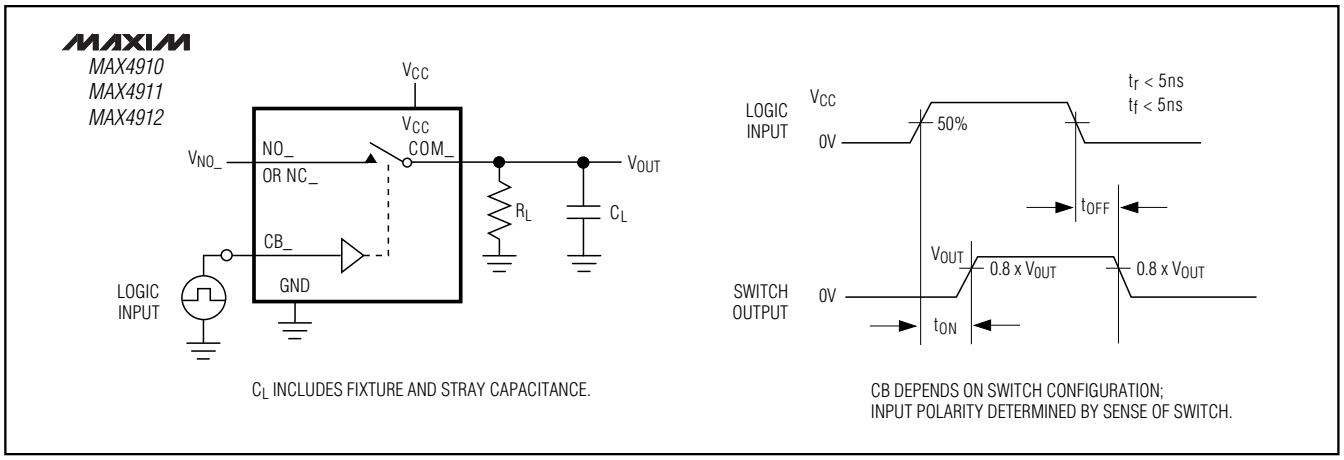


Figure 2. Switching Time

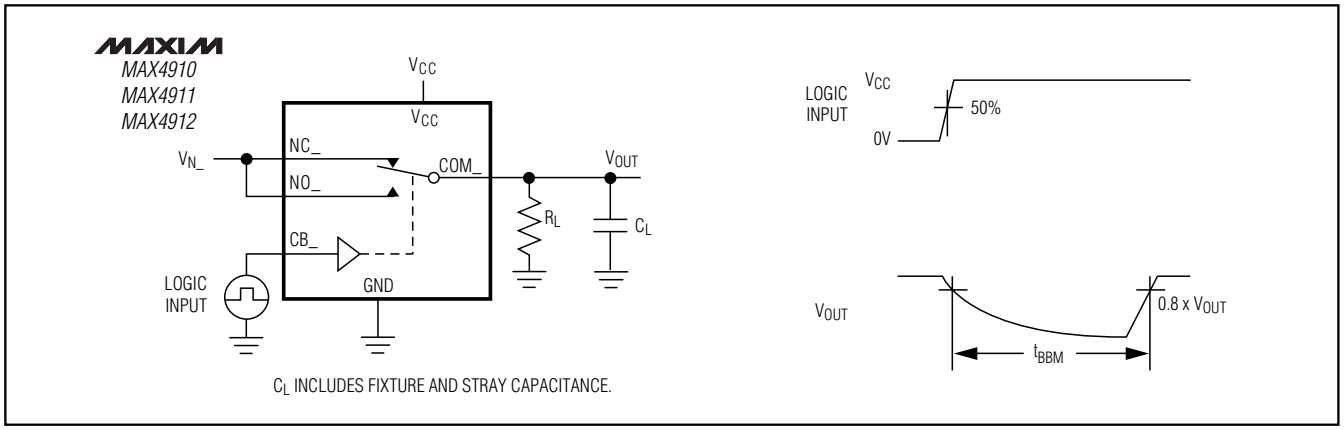


Figure 3. Break-Before-Make Interval

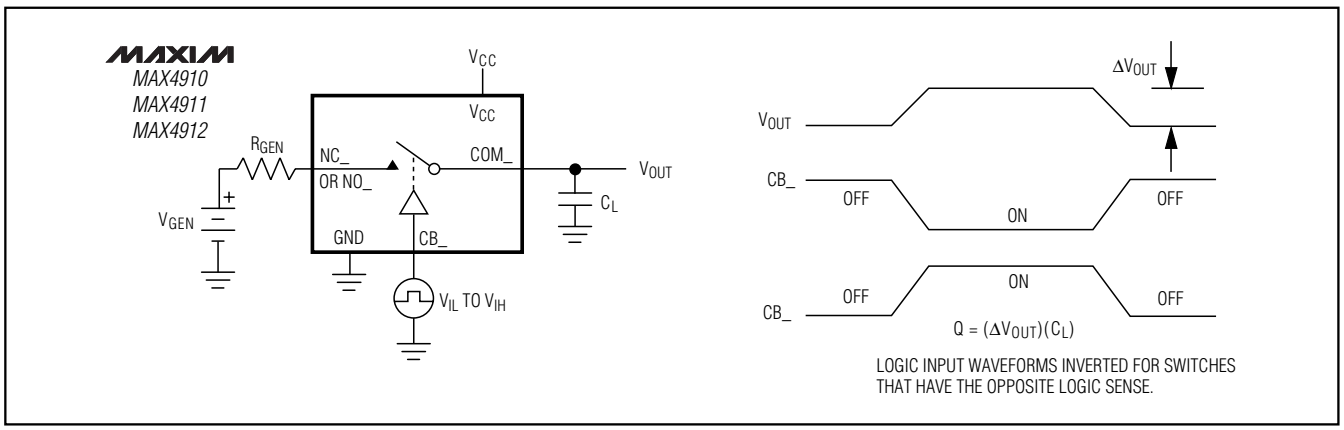


Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

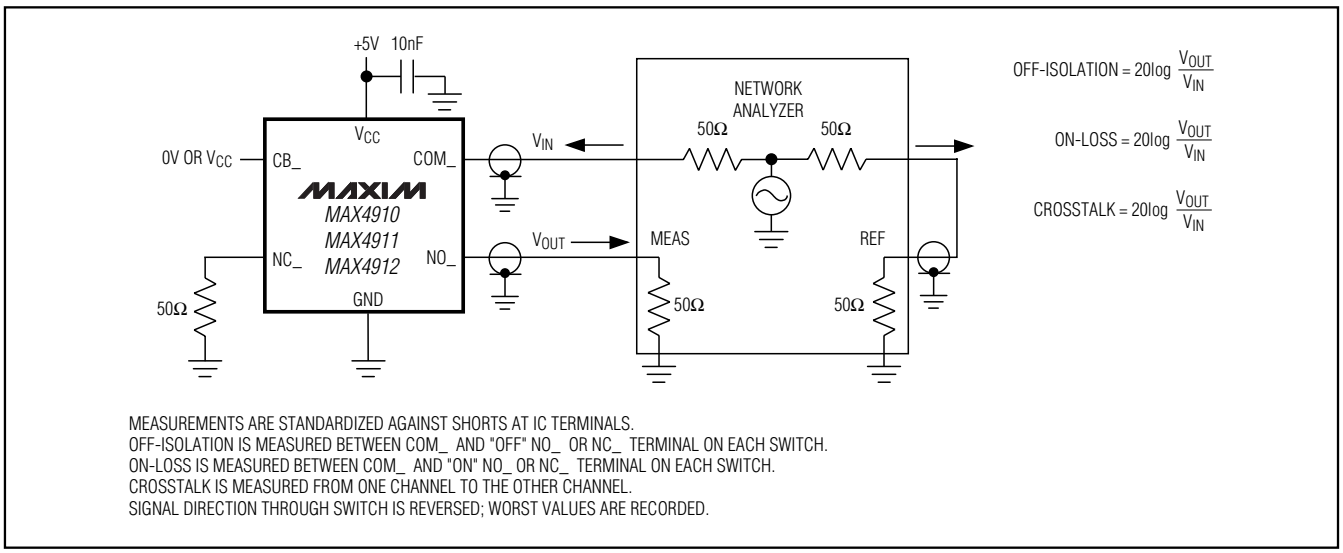


Figure 5. On-Loss, Off-Isolation, and Crosstalk

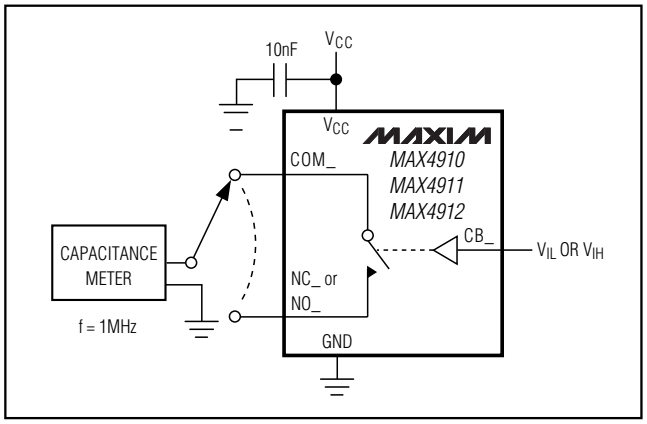
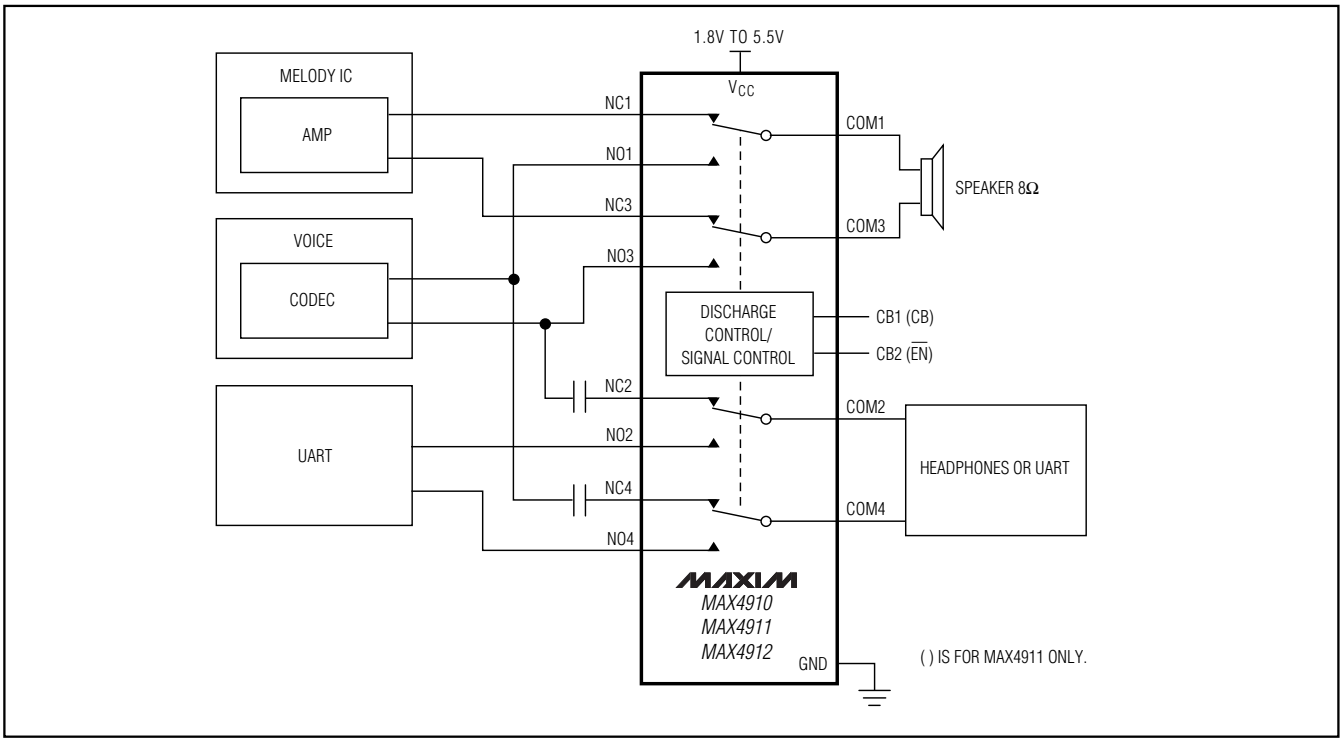


Figure 6. Channel Off-/On-Capacitance

Quad-SPDT, Clickless Audio Switches with Negative Signal Handling

Typical Operating Circuit



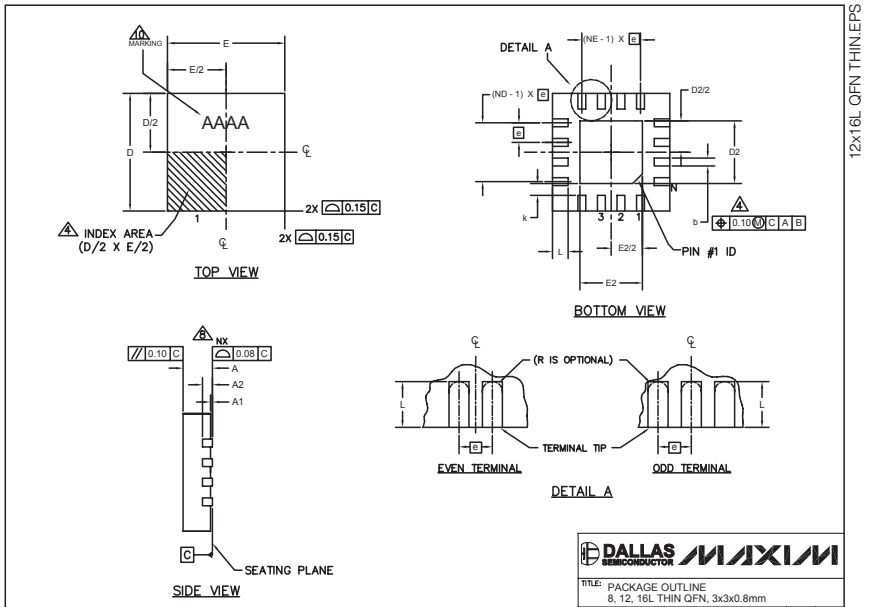
Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC	NO
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.8mm
APPROVAL
DOCUMENT CONTROL NO. 21-0136
REV. G
2/2

–DRAWING NOT TO SCALE–