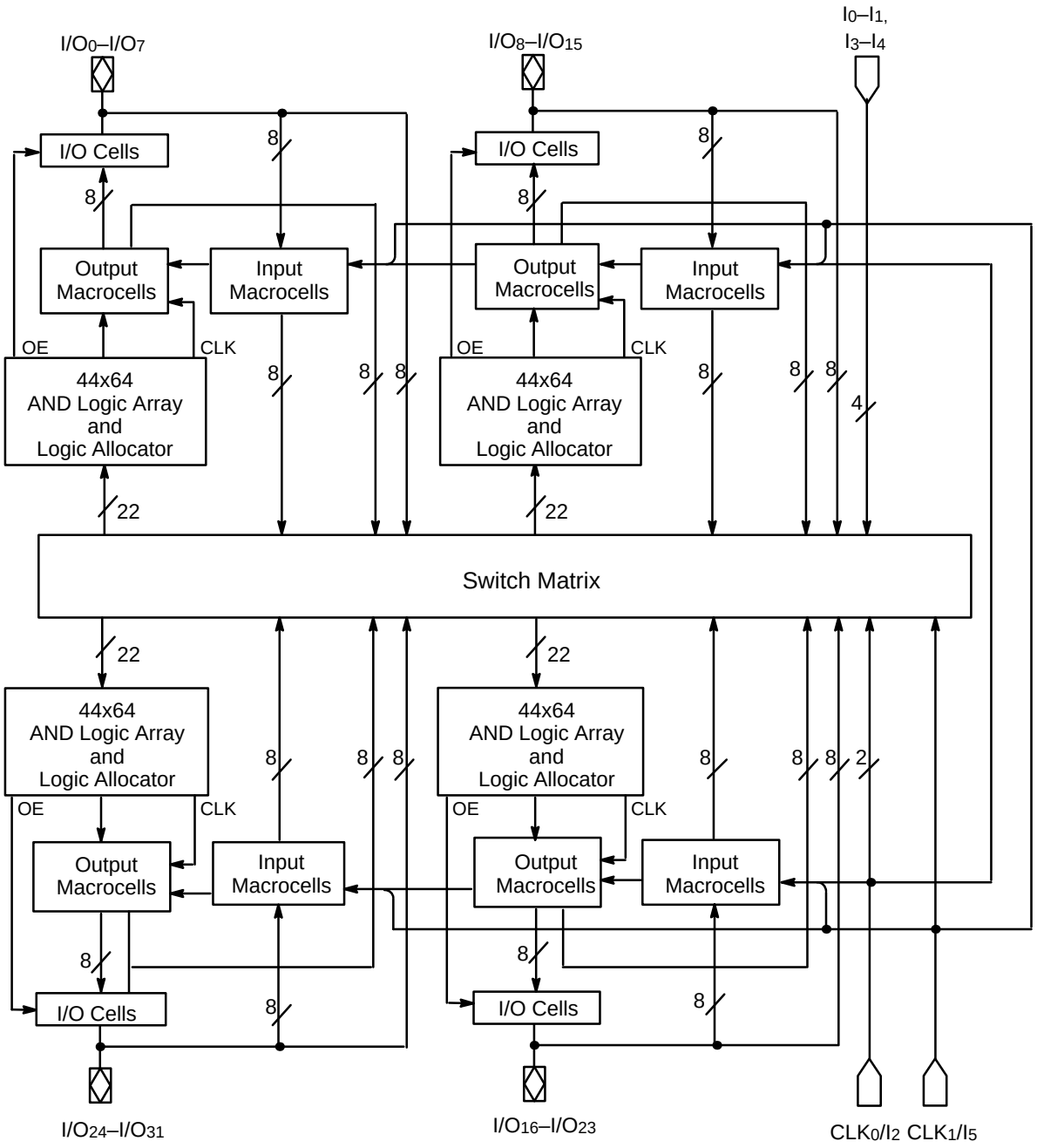
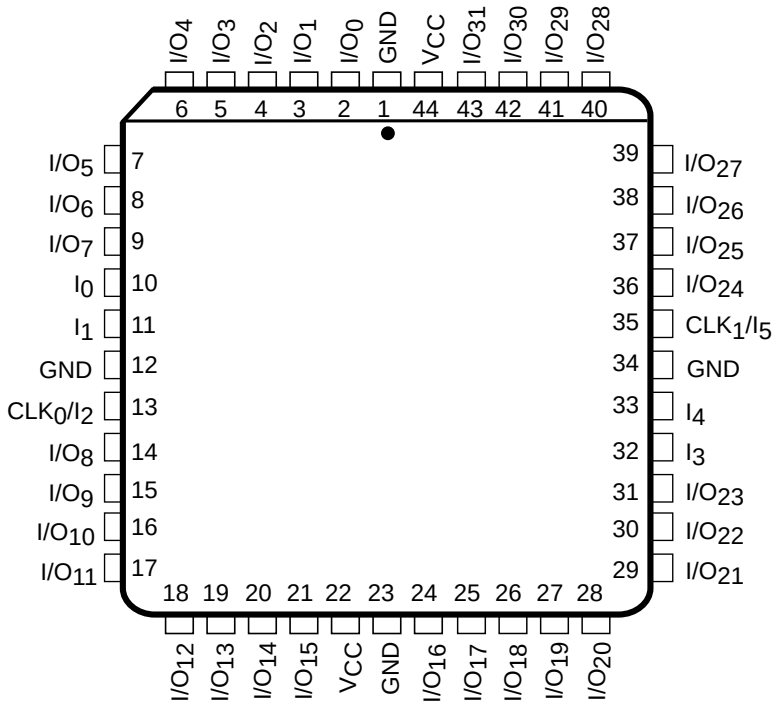
BLOCK DIAGRAM



16751E-1

CONNECTION DIAGRAM
Top View

PLCC



16751E-2

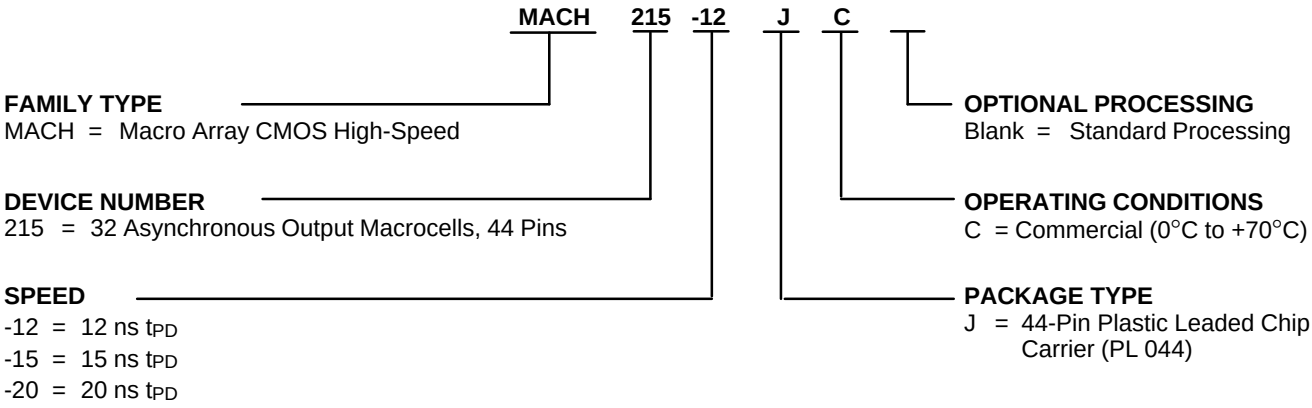
Note:
Pin-compatible with MACH110, MACH111, MACH210, and MACH211.

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

Programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



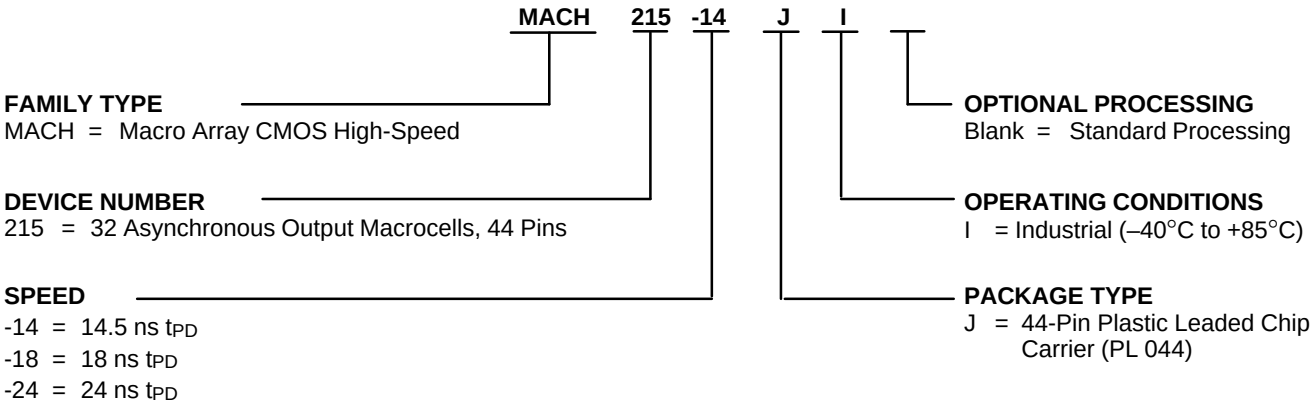
Valid Combinations	
MACH215-12	JC
MACH215-15	
MACH215-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
Industrial Products

Programmable logic products for industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH215-14	JI
MACH215-18	
MACH215-24	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH215 consists of four asynchronous PAL blocks connected by a switch matrix. There are 32 I/O pins and 4 dedicated input pins feeding the switch matrix. These signals are distributed to the four PAL blocks for efficient design implementation. There are also two additional global clock pins that can be used as dedicated inputs. This device provides two kinds of macrocell: output macrocells and input macrocells. This adds greater logic density without affecting the number of pins.

The PAL Blocks

Each PAL block in the MACH215 (Figure 1) contains a 64-product-term array, a logic allocator, 8 output macrocells, 8 input macrocells, and 8 I/O cells. The switch matrix feeds each PAL block with 22 inputs. This makes the PAL block look effectively like an independent "PAL22RA8" with 8 input macrocells. All flip-flops within the device can operate independently.

The Switch Matrix

The MACH215 switch matrix is fed by the inputs and feedback signals from the PAL blocks. Each PAL block provides 16 internal feedback signals and 8 I/O feedback signals. The switch matrix distributes these signals back to the PAL blocks in an efficient manner that also provides for high performance. The design software automatically configures the switch matrix when fitting a design into the device.

The Product-term Array

The MACH215 product-term array consists of 32 product terms for logic use and 32 product terms for generating macrocell control signals.

The Logic Allocator

The logic allocator in the MACH215 (Figure 2) takes the 32 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 12 product terms. The design software automatically configures the logic allocator when fitting the design into the device.

Table 1 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 1 for cluster and macrocell numbers.

Table 1. Logic Allocation

Output Macrocell	Available Clusters
M_0	C_0, C_1
M_1	C_0, C_1, C_2
M_2	C_1, C_2, C_3
M_3	C_2, C_3, C_4
M_4	C_3, C_4, C_5
M_5	C_4, C_5, C_6
M_6	C_5, C_6, C_7
M_7	C_6, C_7

The Macrocell

There are two types of macrocell in the MACH215: output macrocells and input macrocells. The output macrocell takes the logic of the device and provides it to I/O pins and/or provides feedback for additional logic generation. The input macrocell allows I/O pins to be configured as registered or latched inputs.

The output macrocell (Figure 3) can generate registered or combinatorial outputs. In addition, a transparent-low latched configuration is provided. If used, the register can be configured as a T-type or a D-type flip-flop. Register and latch functionality is defined in Table 2. Programmable polarity and the T-type flip-flop both give the software a way to minimize the number of product terms needed. These choices can be made automatically by the software when it fits the design into the device.

Table 2. Register/Latch Operation

Configuration	D/T	CLK/LE*	Q+
D-Register	X 0 1	0, 1, ↓ (↑) ↑ (↓) ↑ (↓)	Q 0 1
T-Register	X 0 1	0, 1, ↓ (↑) ↑ (↓) ↑ (↓)	Q $\overline{Q}$ $\overline{Q}$
Latch	X 0 1	1 (0) 0 (1) 0 (1)	Q 0 1

**Polarity of CLK/LE can be programmed.*

The output macrocell sends its output back to the switch matrix, via internal feedback, and to the I/O cell. The feedback is always available regardless of the configuration of the I/O cell. This allows for buried combinatorial or registered functions, freeing up the I/O pins for use as inputs if not needed as outputs. The basic output macrocell configurations are shown in Figure 4.

The clock/latch-enable for each individual output macrocell can be driven by one of four signals. Two of the signals are provided by the global clock pin CLK_0/LE_0; either polarity may be chosen. The other two signals come from a product term provided for each output macrocell. Either polarity of the logic generated by the product term can be chosen. The global clock pin is also available as an input, although care must be taken when a signal acts as both clock and input to the same device.

Each individual output macrocell also has a product term for asynchronous reset and a product term for asynchronous preset. This means that any register or latch may be reset or preset without affecting any other register or latch in the device. The functionality of the flip-flops with respect to initialization is illustrated in Table 3.

Table 3. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE	Q+
0	0	X	See Table 12
0	1	X	1
1	0	X	0
1	1	X	0

The input macrocell (Figure 5) consists of a flip-flop that can be used to provide registered or latched inputs. The flip-flop can be clocked by either polarity of one of the two global clock/latch-enable pins.

Reset or preset are not provided for these flip-flops. If combinatorial inputs are desired, this macrocell is not used, and the feedback from the I/O pin is used directly. Both the I/O pin feedback and the output of the input register or latch are always available to the switch matrix.

Possible input macrocell configurations are shown in Figure 6.

The I/O Cell

The I/O cell (Figure 7) provides a three-state output buffer. The three-state control is provided by an individual product term for each I/O cell. Depending on the logic programmed onto this product term, the I/O pin can be configured as an output, an input, or a bidirectional pin. The feedback from the I/O pin is always available to the switch matrix, regardless of the state of the output buffer or the output macrocell.

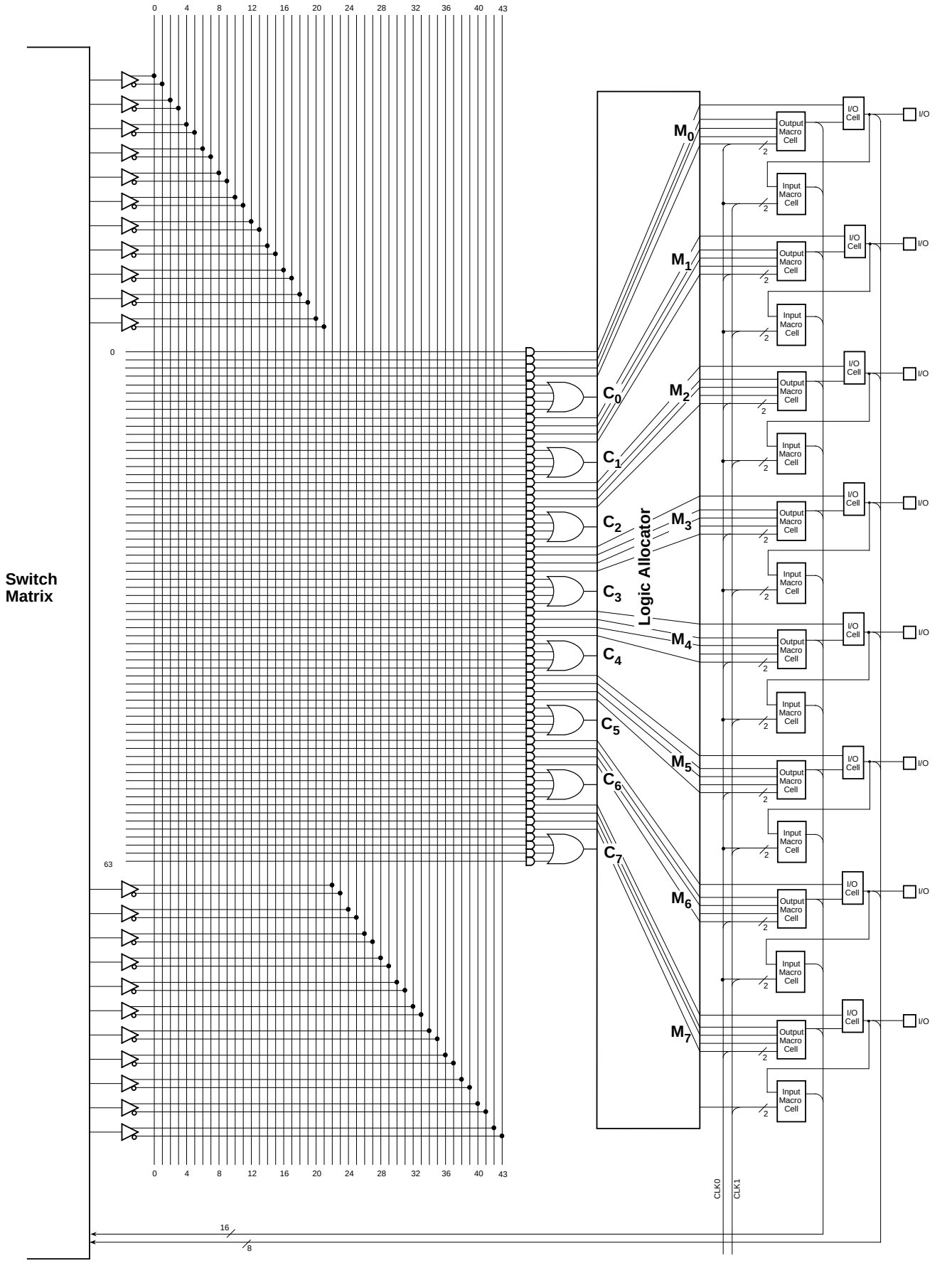


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Figure 1. MACH215 PAL Block

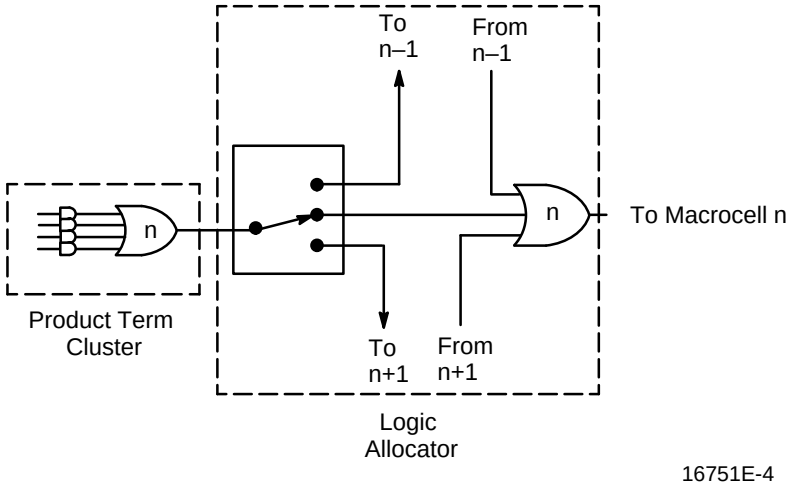


Figure 2. Product Term Clusters and the Logic Allocator

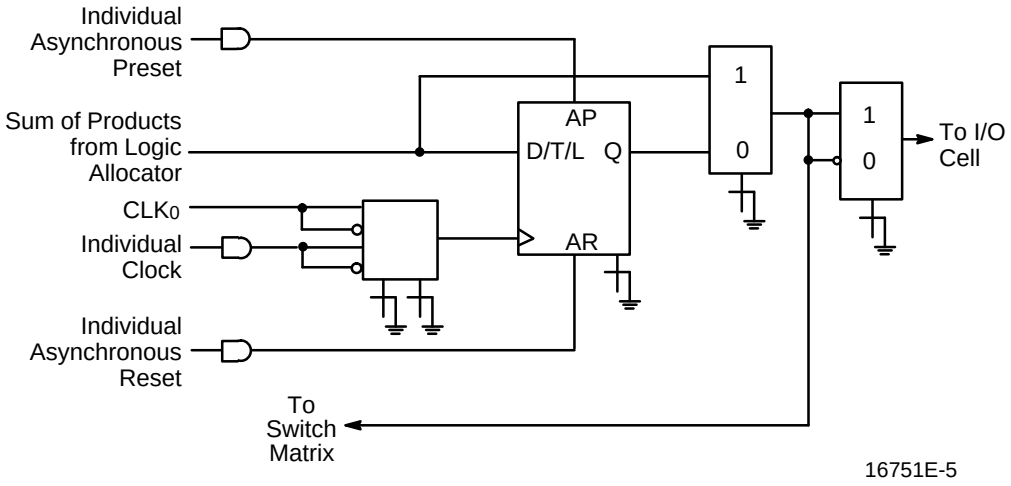


Figure 3. Output Macrocell

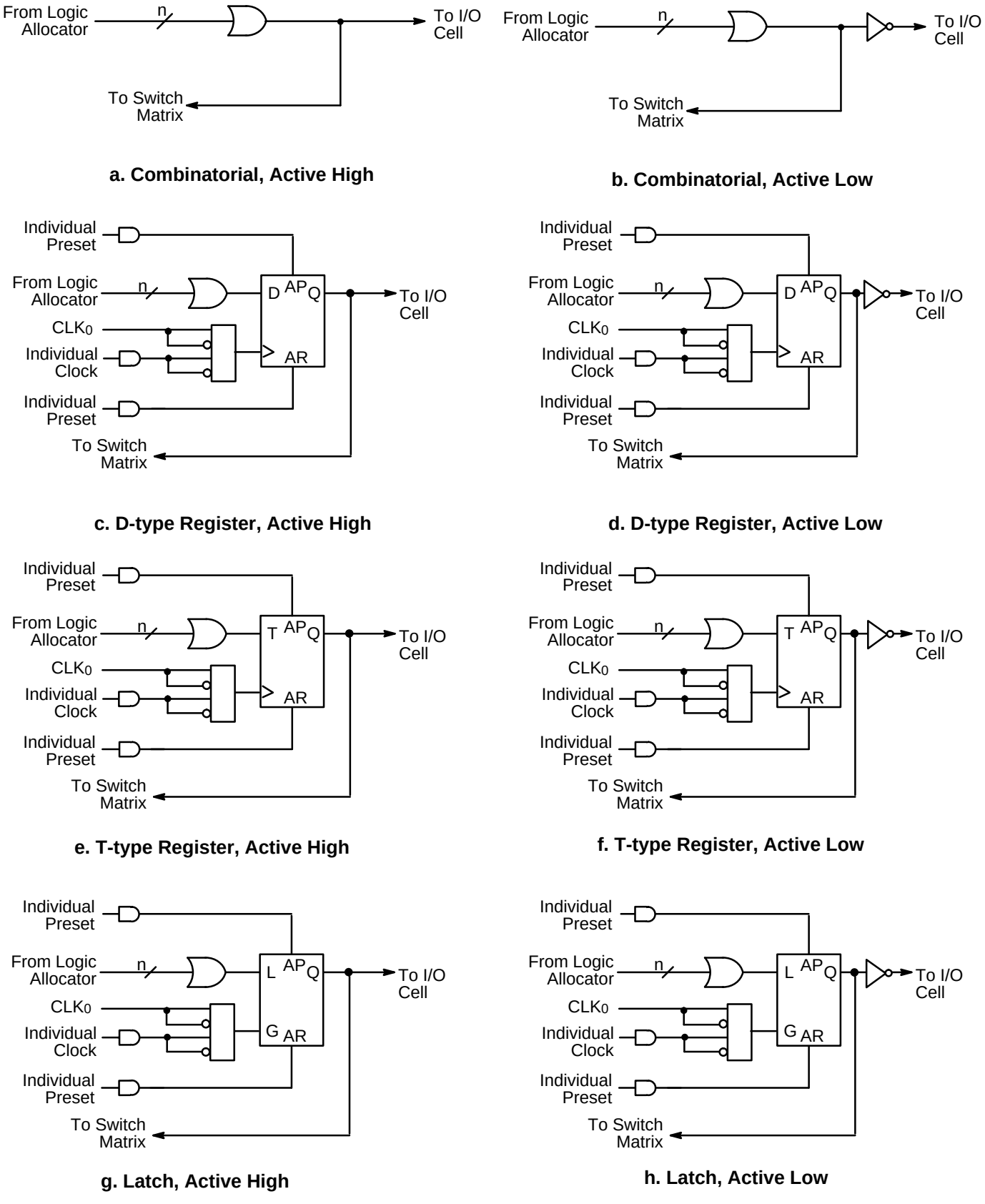


Figure 4. Output Macrocell Configurations

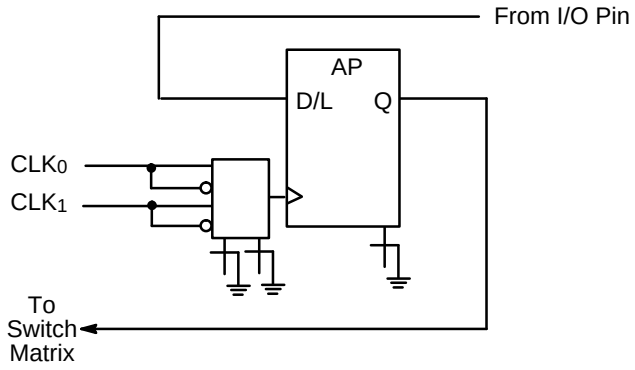
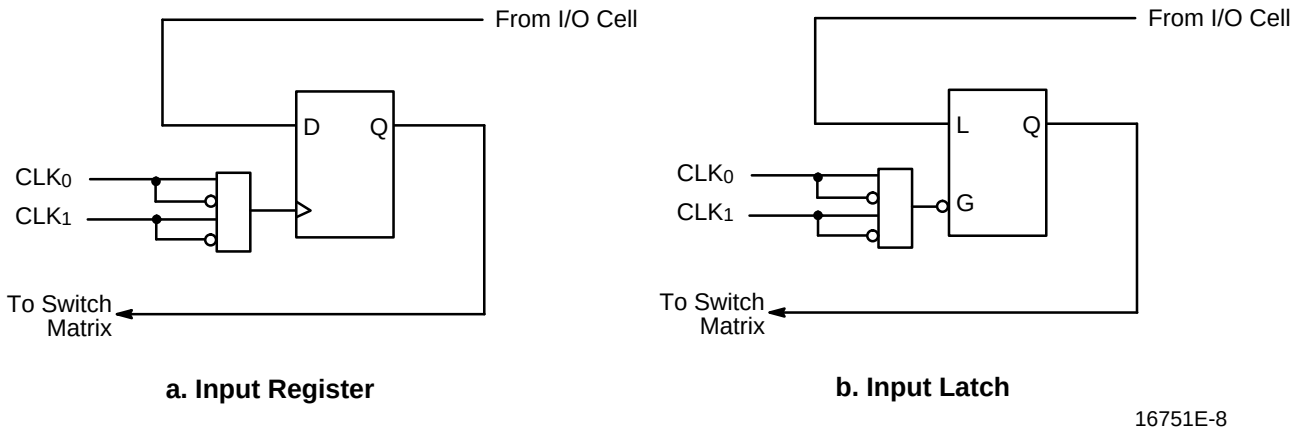


Figure 5. Input Macrocell



a. Input Register

b. Input Latch

Figure 6. Input Macrocell Configurations

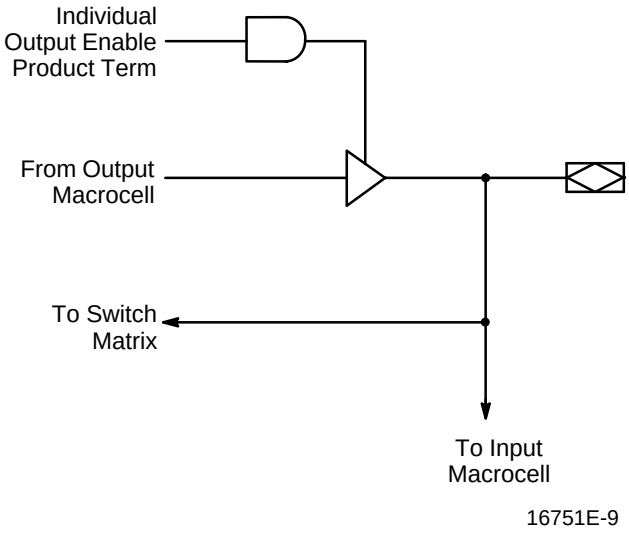


Figure 7. I/O Cell

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = 0°C to +70°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 5)		95		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-12		-15		-20		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)				3	12	3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	5		6		8		ns
				T-type	6		7		9		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				5		6		8		ns
t_{COA}	Product Term Clock to Output (Note 3)				4	14	4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	8		9		12		ns
t_{WHA}				HIGH	8		9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 1)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	52.6		41.7		33.3		MHz
				T-type	50		40		32.2		MHz
		Internal Feedback (f_{CNTA})		D-type	58.8		45.5		35.7		MHz
				T-type	55.6		43.5		34.5		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$		62.5		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	7		10		13		ns
				T-type	8		11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		ns
t_{COS}	Global Clock to Output (Note 3)				2	8	2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		6		8		ns
t_{WHS}				HIGH	6		6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 1)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	66.7		50		40		MHz
				T-type	62.5		47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	83.3		66.6		50		MHz
				T-type	76.9		62.5		47.6		MHz
		No Feedback	$1/(t_{WLS} + t_{WHS})$		83.3		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Gate				5		6		8		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				5		6		8		ns
t_{GOA}	Product Term Gate to Output (Note 3)					16		19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				8		9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				7		10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		0		ns
t_{GOS}	Gate to Output (Note 3)					10		11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		6		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2) (continued)

Parameter Symbol	Parameter Description		-12 Min	-12 Max	-15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch			14		17		22	ns
t_{SIR}	Input Register Setup Time		2		2		2		ns
t_{HIR}	Input Register Hold Time		2		2.5		3		ns
t_{ICO}	Input Register Clock to Combinatorial Output			15		18		23	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	12		15		20		ns
		T-type	13		16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		6		8		ns
t_{WICH}		HIGH	6		6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		2		2		ns
t_{HIL}	Input Latch Hold Time		2		2.5		3		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			17		20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			19		22		27	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		7		8		10		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		7		8		10		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		9		12		15		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		13		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			16		19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			16		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 1)		12		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)		8		10		15		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			16		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 1)		12		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)		8		10		15		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)		2	12	2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)		2	12	2	15	2	20	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions. Switching waveforms illustrate true clocks only. Switching waveforms can be used to illustrate both synchronous and asynchronous clock timing. For example, t_{SS} is the t_S parameter for synchronous clocks and t_{SA} is the t_S parameter for asynchronous clocks.*
3. *Parameters measured with 16 outputs switching.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current (T_A = –40°C to +85°C) . . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

INDUSTRIAL OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air . . . . . –40°C to +85°C

Supply Voltage (V_{CC}) with Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current (Typical)	V_{CC} = 5 V, T_A = 25°C, f = 25 MHz (Note 5)		95		mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				-14		-18		-24		Unit
					Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 3)					14.5		18		24	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	6		7.5		10		ns
				T-type	7.5		8.5		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				6		7.5		10		ns
t_{COA}	Product Term Clock to Output (Note 3)					17		22		26.5	ns
t_{WLA}	Product Term, Clock Width			LOW	10		11		15		ns
t_{WHA}				HIGH	10		11		15		ns
f_{MAXS}	Maximum Frequency Using Product Term Clock (Note 1)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	42		33		26.5		MHz
				T-type	40		32		25.5		MHz
		Internal Feedback (f_{CNTA})		D-type	47		36		28.5		MHz
				T-type	44		34.5		27.5		MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$		50		44.5		33		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	8.5		12		16		ns
				T-type	10		13.5		17		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		0		ns
t_{COS}	Global Clock to Output (Note 3)					10		12		14.5	ns
t_{WLS}	Global Clock Width			LOW	7.5		7.5		10		ns
t_{WHS}				HIGH	7.5		7.5		10		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 1)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	53		40		32		MHz
				T-type	50		38		30.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.5		53		40		MHz
				T-type	61.5		50		38		MHz
		No Feedback	$1/(t_{WLS} + t_{WHS})$		66.5		66.5		50		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Gate				6		7.5		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				6		7.5		10		ns
t_{GOA}	Product Term Gate to Output (Note 3)					19.5		23		26.5	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				10		11		14.5		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				8.5		12		16		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		0		ns
t_{GOS}	Gate to Output (Note 3)					12		13.5		14.5	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				7.5		7.5		10		ns

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2) (continued)

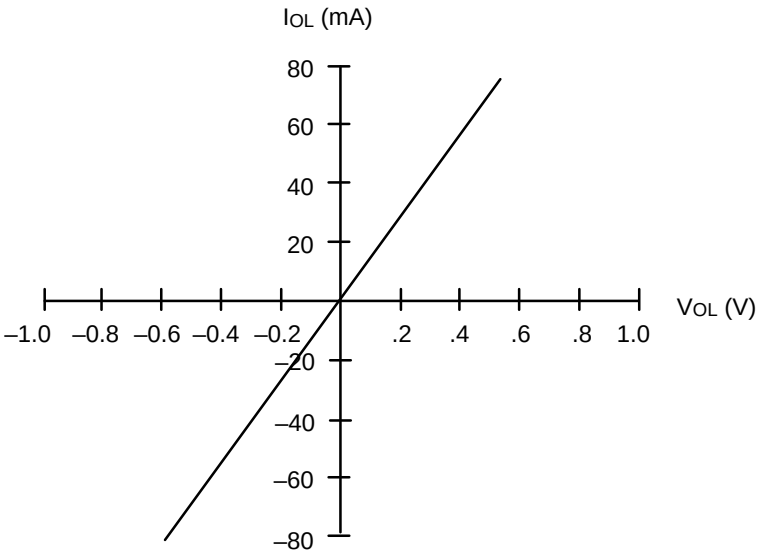
Parameter Symbol	Parameter Description		-14		-18		-24		Unit
			Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch			17		20.5		26.5	ns
t_{SIR}	Input Register Setup Time		2.4		2.4		2.4		ns
t_{HIR}	Input Register Hold Time		3		3.5		4		ns
t_{ICO}	Input Register Clock to Combinatorial Output			18		22		28	ns
t_{ICS}	Input Register Clock to Output Register Setup	D-type	14.5		18		24		ns
		T-type	16		19.5		25.5		ns
t_{WICL}	Input Register Clock Width	LOW	7.5		7.5		10		ns
t_{WICH}		HIGH	7.5		7.5		10		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL}+t_{WICH})$	66.5		66.5		50		MHz
t_{SIL}	Input Latch Setup Time		2.5		2.5		2.5		ns
t_{HIL}	Input Latch Hold Time		3		3.5		4		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			20.5		24		30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			23		26.5		32.5	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		8.5		10		12		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		8.5		10		12		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		11		14.5		18		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		19.5		25.5		ns
t_{WIGL}	Input Latch Gate Width LOW		7.5		7.5		10		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19.5		23		29	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			19.5		24		30	ns
t_{ARW}	Asynchronous Reset Width (Note 1)		14.5		18		24		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 1)		10		12		18		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			19.5		24		30	ns
t_{APW}	Asynchronous Preset Width (Note 1)		14.5		18		24		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 1)		10		12		18		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 3)			14.5		18		24	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 3)			14.5		18		24	ns

Notes:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
2. *See Switching Test Circuit for test conditions. Switching waveforms illustrate true clocks only. Switching waveforms can be used to illustrate both synchronous and asynchronous clock timing. For example, t_{SS} is the t_S parameter for synchronous clocks and t_{SA} is the t_S parameter for asynchronous clocks.*
3. *Parameters measured with 16 outputs switching.*

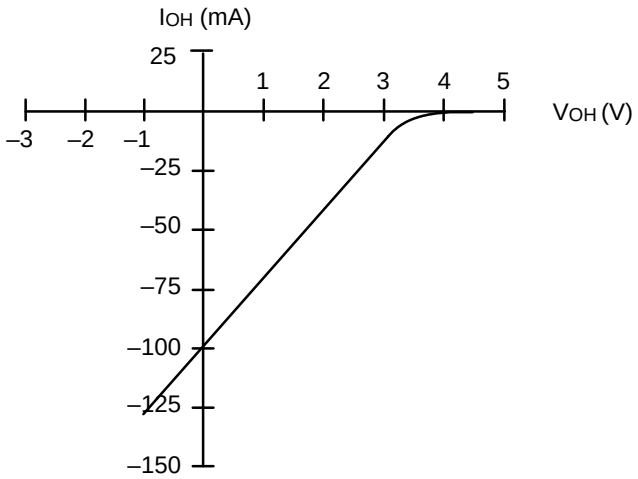
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



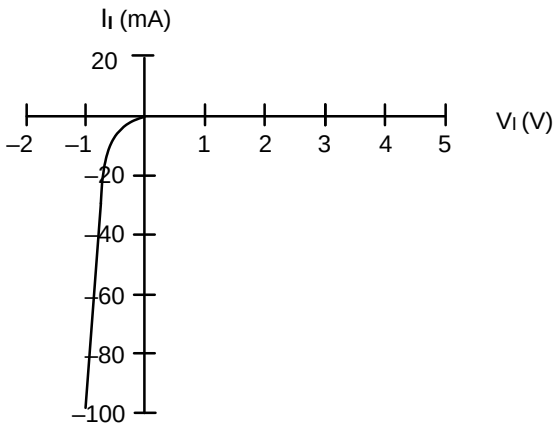
Output, LOW

16751E-10



Output, HIGH

16751E-11

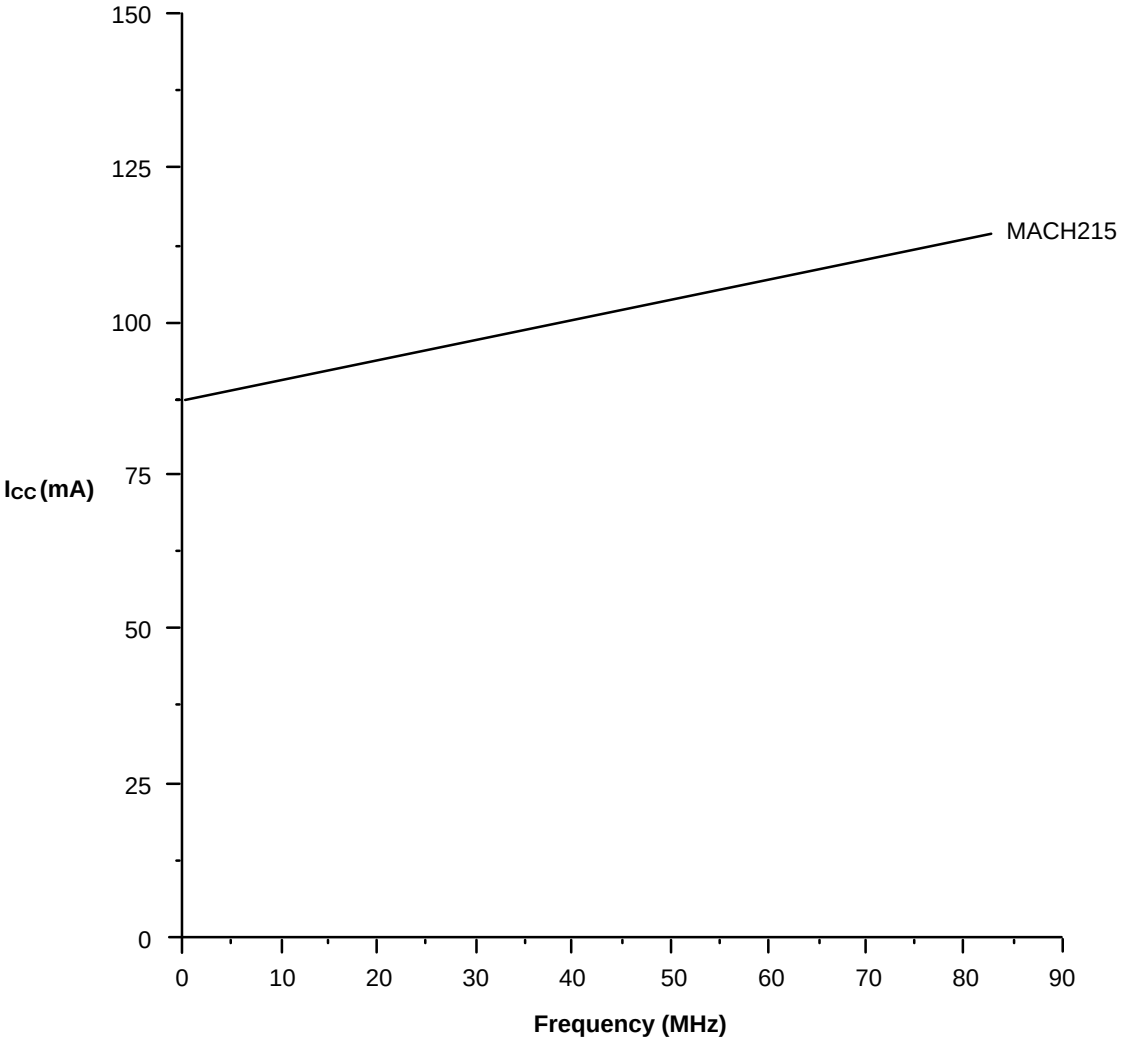


16751E-12

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



16751E-13

The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL THERMAL CHARACTERISTICS

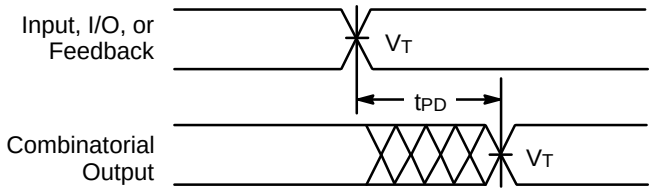
Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Units
θ_{jc}	Thermal impedance, junction to case		15	°C/W
θ_{ja}	Thermal impedance, junction to ambient		40	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	36	°C/W
		400 lfpm air	33	°C/W
		600 lfpm air	31	°C/W
		800 lfpm air	29	°C/W

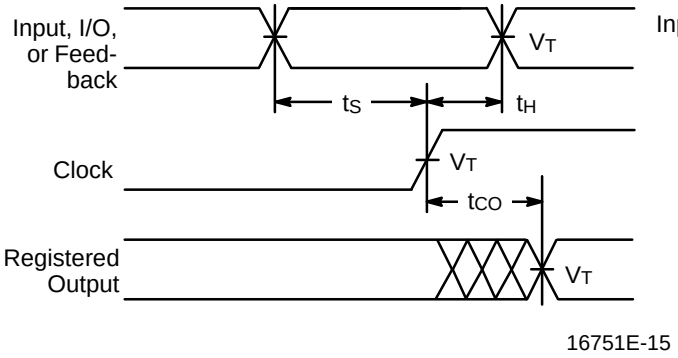
Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

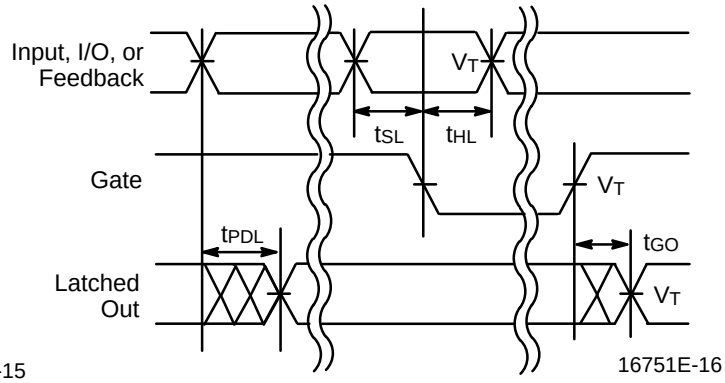
SWITCHING WAVEFORMS



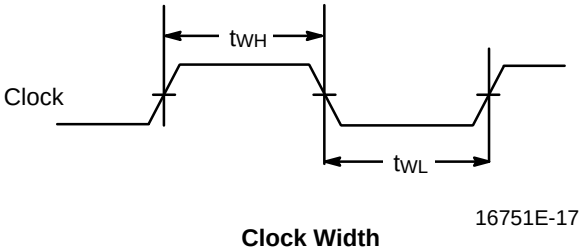
Combinatorial Output



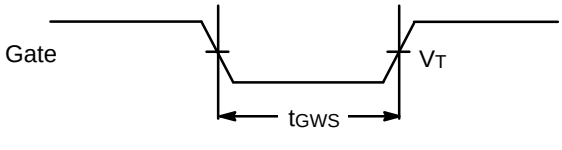
Registered Output



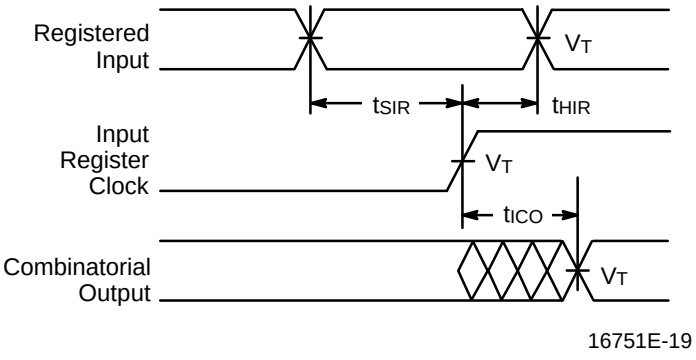
Latched Output (MACH 2, 3, and 4)



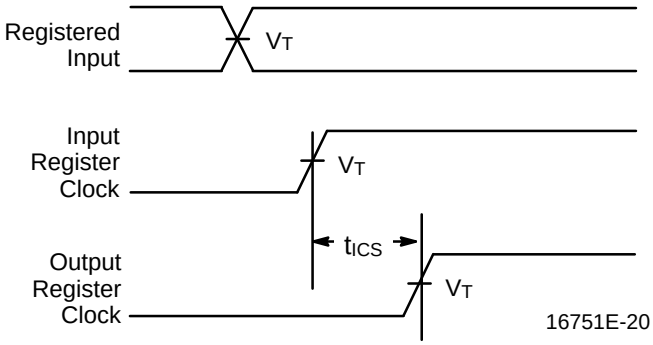
Clock Width



Gate Width (MACH 2, 3, and 4)



Registered Input (MACH 2 and 4)

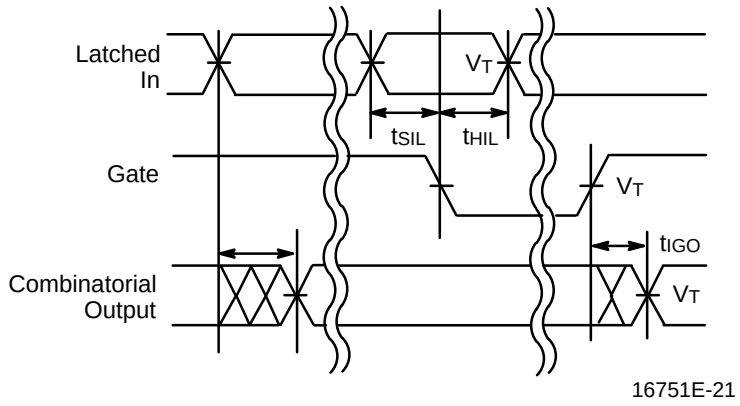


Input Register to Output Register Setup (MACH 2 and 4)

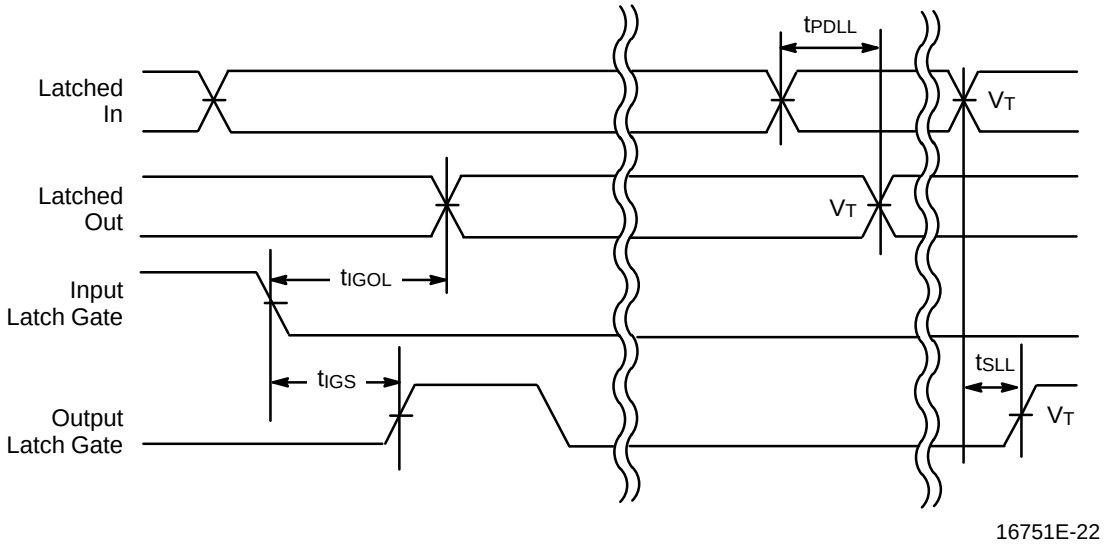
Notes:

1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



Latched Input (MACH 2 and 4)

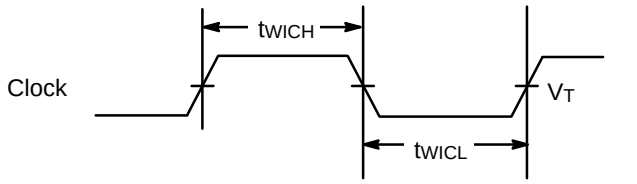


Latched Input and Output (MACH 2, 3, and 4)

Notes:

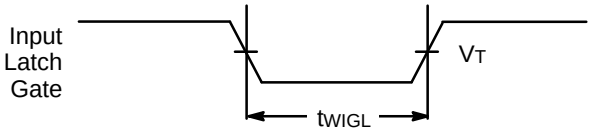
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



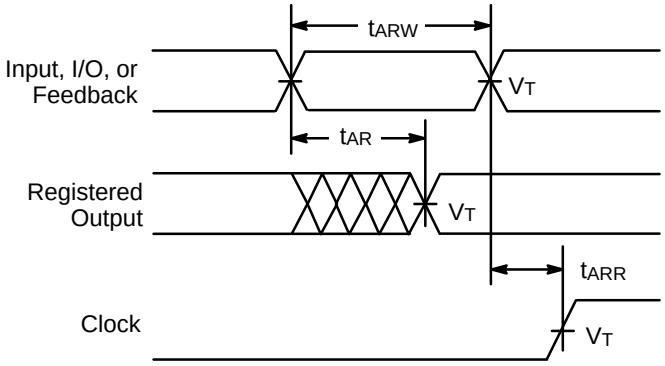
16751E-23

Input Register Clock Width (MACH 2 and 4)



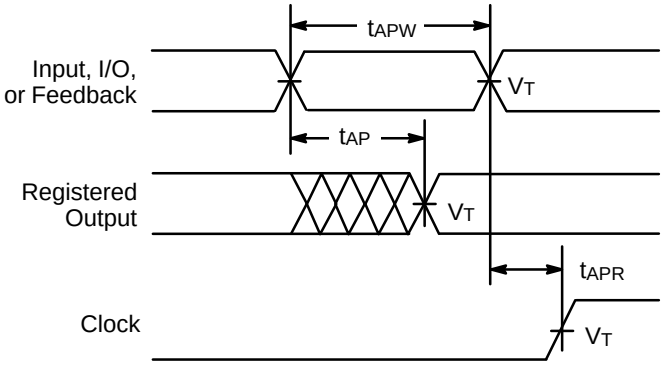
16751E-24

Input Latch Gate Width (MACH 2 and 4)



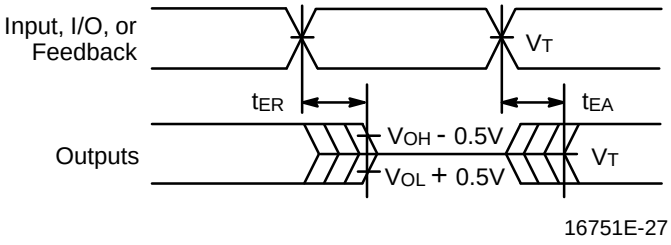
16751E-25

Asynchronous Reset



16751E-26

Asynchronous Preset



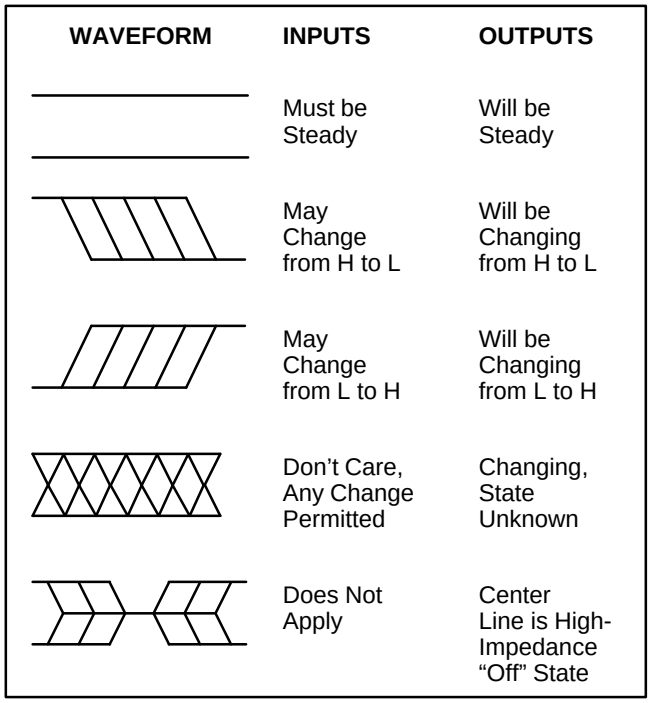
16751E-27

Output Disable/Enable

Notes:

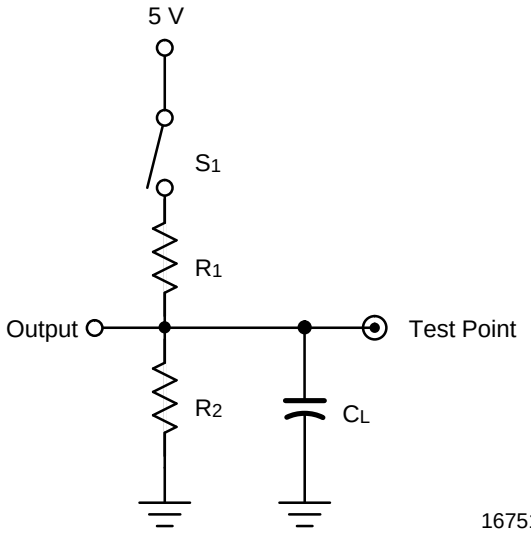
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS



KS000010-PAL

SWITCHING TEST CIRCUIT



16751E-28

Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} – 0.5 V L → Z: V_{OL} + 0.5 V

**Switching several outputs simultaneously should be avoided for accurate measurement.*

f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

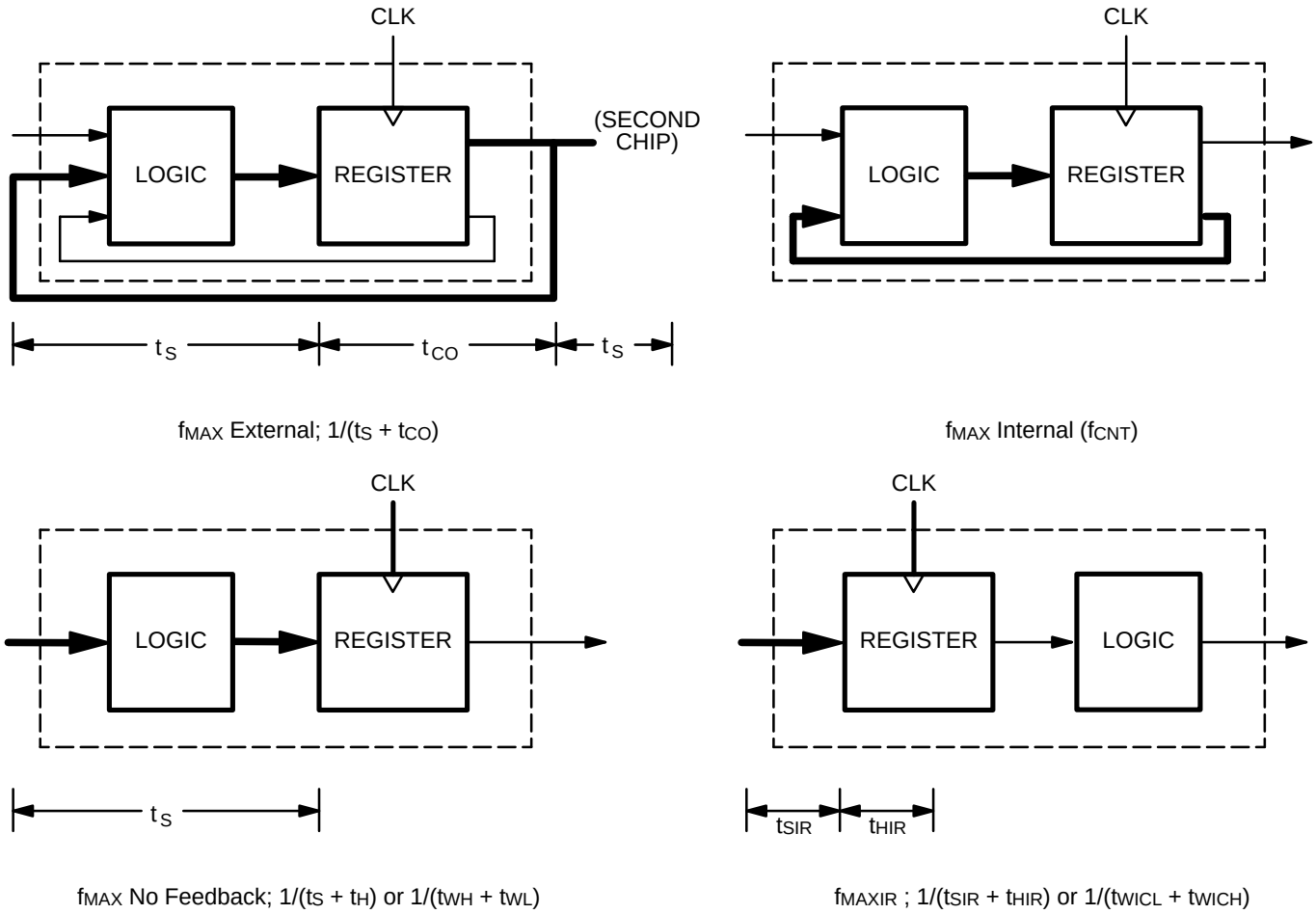
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "$f_{CNT.}$"

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are use in the same path, the overall frequency will be limited by t_{ICS}.

All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



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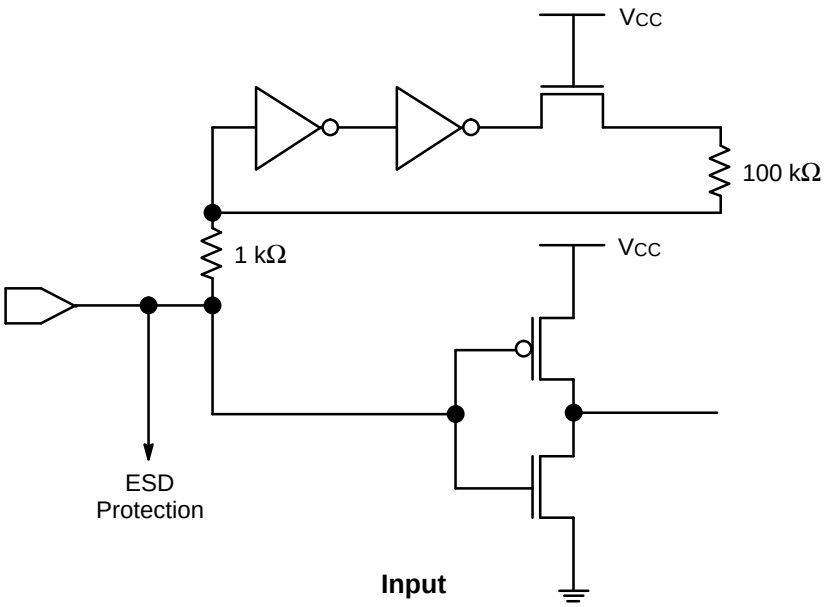
ENDURANCE CHARACTERISTICS

The MACH families are manufactured using our advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

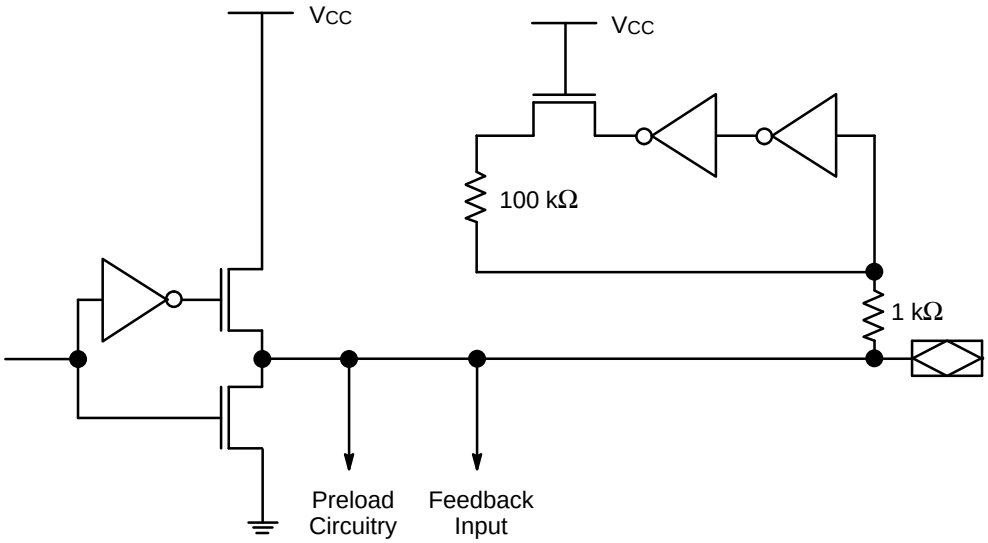
Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



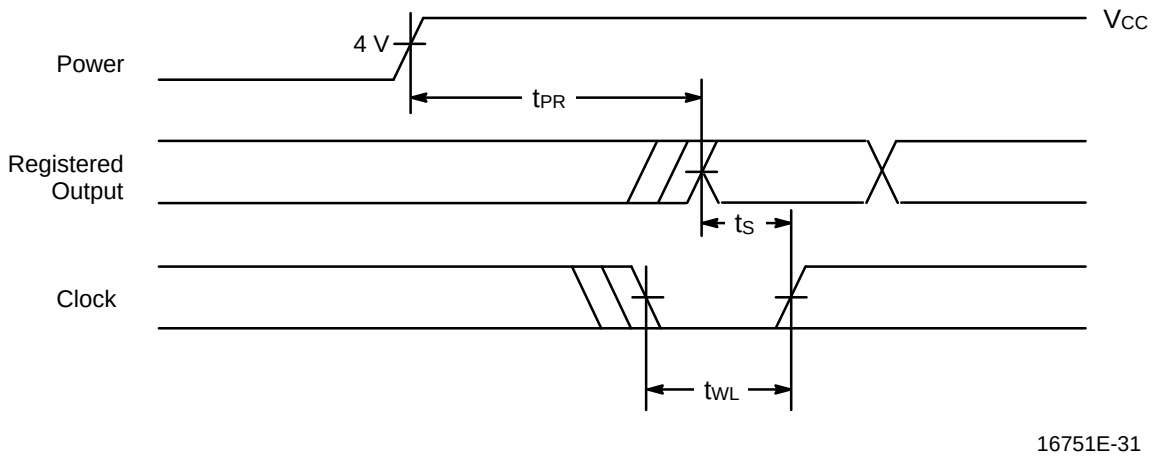
I/O

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

USING PRELOAD AND OBSERVABILITY

In order to be testable, a circuit must be both controllable and observable. To achieve this, the MACH devices incorporate register preload and observability.

In preload mode, each flip-flop in the MACH device can be loaded from the I/O pins, in order to perform functional testing of complex state machines. Register preload makes it possible to run a series of tests from a known starting state, or to load illegal states and test for proper recovery. This ability to control the MACH device's internal state can shorten test sequences, since it is easier to reach the state of interest.

The observability function makes it possible to see the internal state of the buried registers during test by overriding each register's output enable and activating the output buffer. The values stored in output and buried registers can then be observed on the I/O pins. Without this feature, a thorough functional test would be impossible for any designs with buried registers.

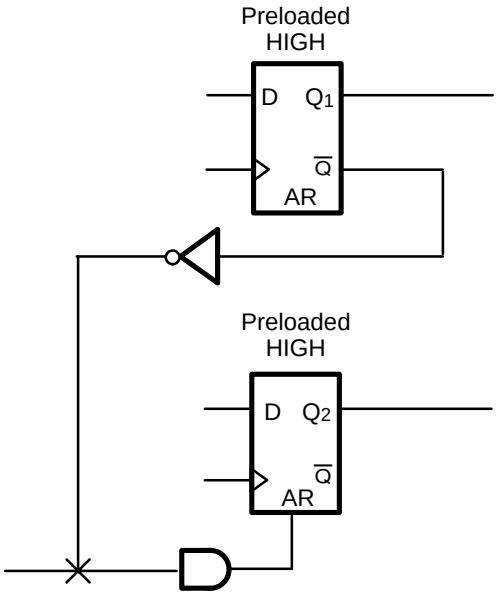
While the implementation of the testability features is fairly straightforward, care must be taken in certain instances to insure valid testing.

One case involves asynchronous reset and preset. If the MACH registers drive asynchronous reset or preset lines and are preloaded in such a way that reset or preset are asserted, the reset or preset may remove the preloaded data. This is illustrated in Figure 8. Care should be taken when planning functional tests, so that states that will cause unexpected resets and presets are not preloaded.

Another case to be aware of arises in testing combinatorial logic. When an output is configured as combinatorial, the observability feature forces the output into registered mode. When this happens, all product terms are forced to zero, which eliminates all combinatorial data. For a straight combinatorial output, the correct value will be restored after the preload or observe function, and there will be no problem. If the function implements a combinatorial latch, however, it relies on feedback to hold the correct value, as shown in Figure 9. As this value may change during the preload or observe operation, you cannot count on the data being correct after the operation. To insure valid testing in these cases, outputs that are combinatorial latches should not be tested immediately following a preload or observe sequence, but should first be restored to a known state.

All MACH 2 devices support both preload and observability.

Contact individual programming vendors in order to verify programmer support.



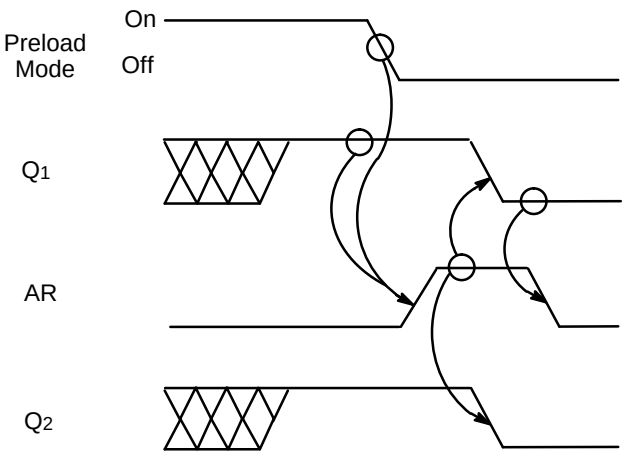


Figure 8. Preload/Reset Conflict

16751E-32

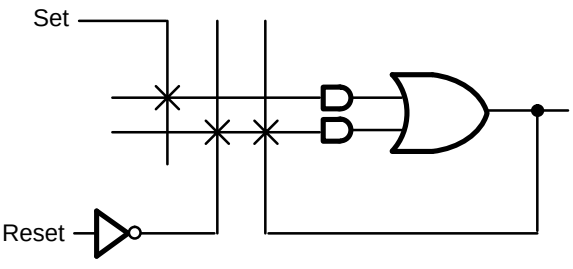


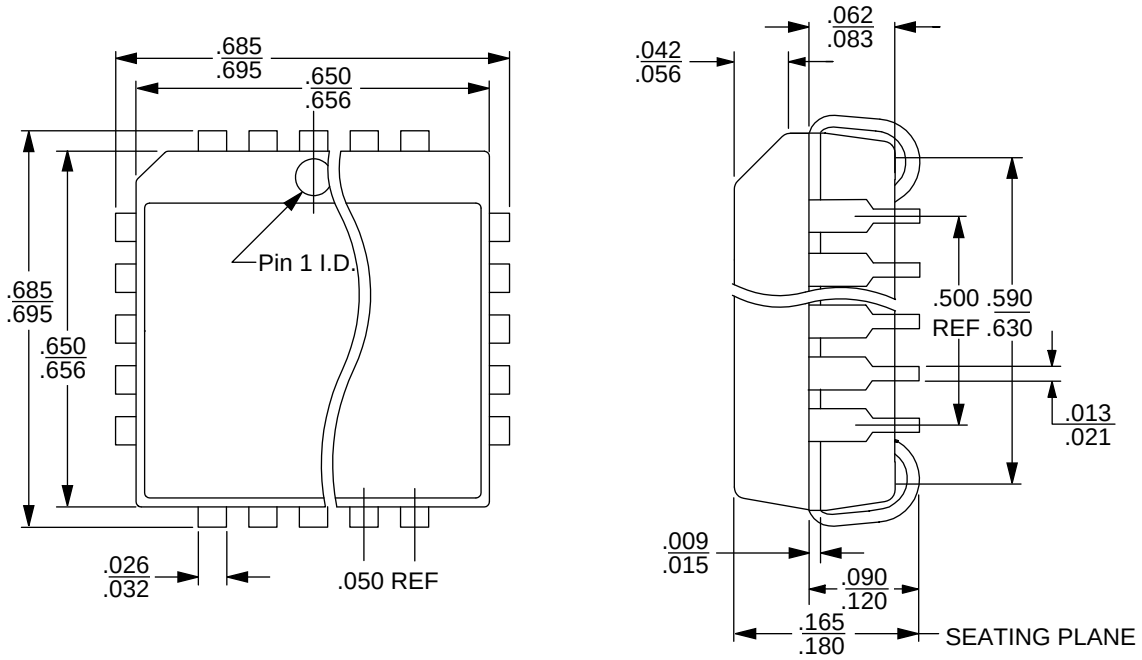
Figure 9. Combinatorial Latch

16751E-33

PHYSICAL DIMENSIONS*

PL 044

44-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW

SIDE VIEW

16-038-SQ
PL 044
DA78
6-28-94 ae

**For reference only. BSC is an ANSI standard for Basic Space Centering.*