Recommended Operating Range at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V_{BB}		10 to 28	V
Logic system supply voltage	V_{CC}		4.75 to 5.25	V
Reference voltage	VREF		1.5 to 5.0	V

Electrical Characteristics at Ta = 25°C, V_{BB} = 24V, V_{CC} = 5V, VREF = 5V

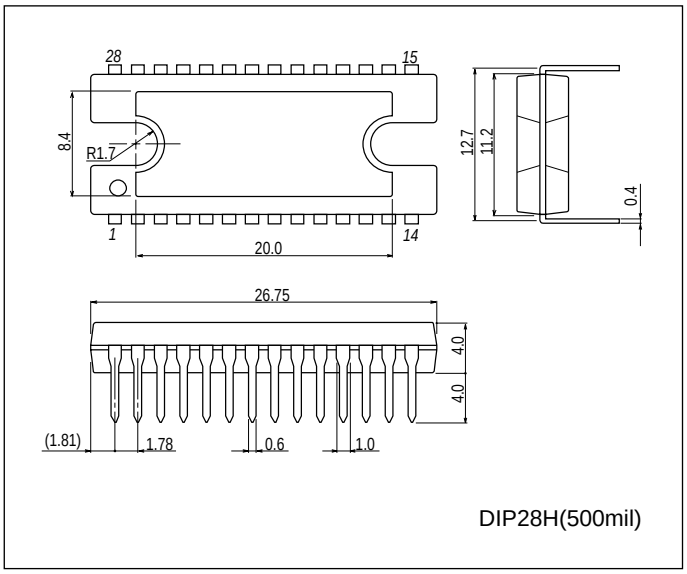
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output block						
Output stage supply current	I_{BB} ON I_{BB} OFF	I_1 = 0.8V, I_2 = 0.8V, ENABLE = 0.8V ENABLE = 3.2V	0.5	1.0	2.0 0.2	mA
Output saturation voltage 1	V_O sat1	I_O = +0.5A, sink side		0.3	0.5	V
Output saturation voltage 2	V_O sat2	I_O = +0.8A, sink side		0.5	0.7	V
Output saturation voltage 3	V_O sat3	I_O = -0.5A, source side		1.6	1.8	V
Output saturation voltage 4	V_O sat4	I_O = -0.8A, source side		1.8	2.0	V
Output leakage current	V_O1(leak) V_O2(leak)	V_O = V_{BB}, sink side V_O = 0V, source side	-50		50	µA
Output sustain voltage	VSUS	L = 3.9mH, I_O = 1.0A*	30			V
Logic block						
Logic supply current	I_{CC} ON I_{CC} OFF	I_1 = 0.8V, I_2 = 0.8V, ENABLE = 0.8V ENABLE = 3.2V	50 7	70.0 10.0	92 13	mA
Input voltage	V_{IH} V_{IL}		3.2		 1.8	V
Input current	I_{IH} I_{IL}	V_{IH} = 3.2V V_{IL} = 0.8V	35 7	50 10	65 13	µA
Set current control threshold value	VREF/ VSEN	I_1 = 0.8V, I_2 = 0.8V I_1 = 3.2V, I_2 = 0.8V I_1 = 0.8V, I_2 = 3.2V	9.5 13.5 25.5	10 15 30	10.5 16.5 34.5	
Reference current	IREF	VREF = 5.0V, I_1 = 0.8V, I_2 = 0.8V	17.5	25	32.5	µA
CR pin current	ICR	CR = 1.0V	-1.0			µA
Thermal shutdown temperature	TS			170		°C
Thermal shutdown hysteresis	TSHY			40		°C

*: The design specification items are design guarantees and are not measured.

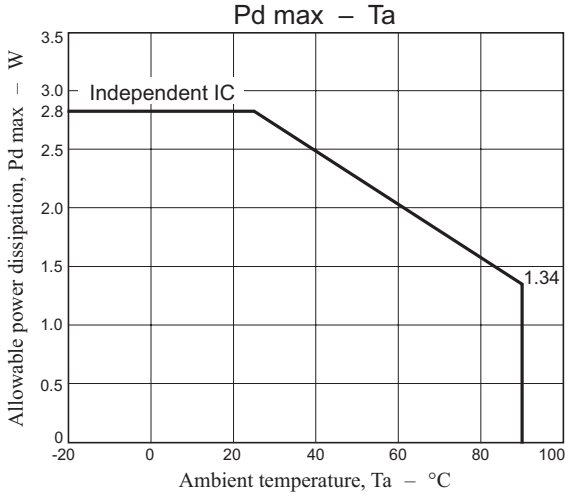
Package Dimensions

unit:mm (typ)

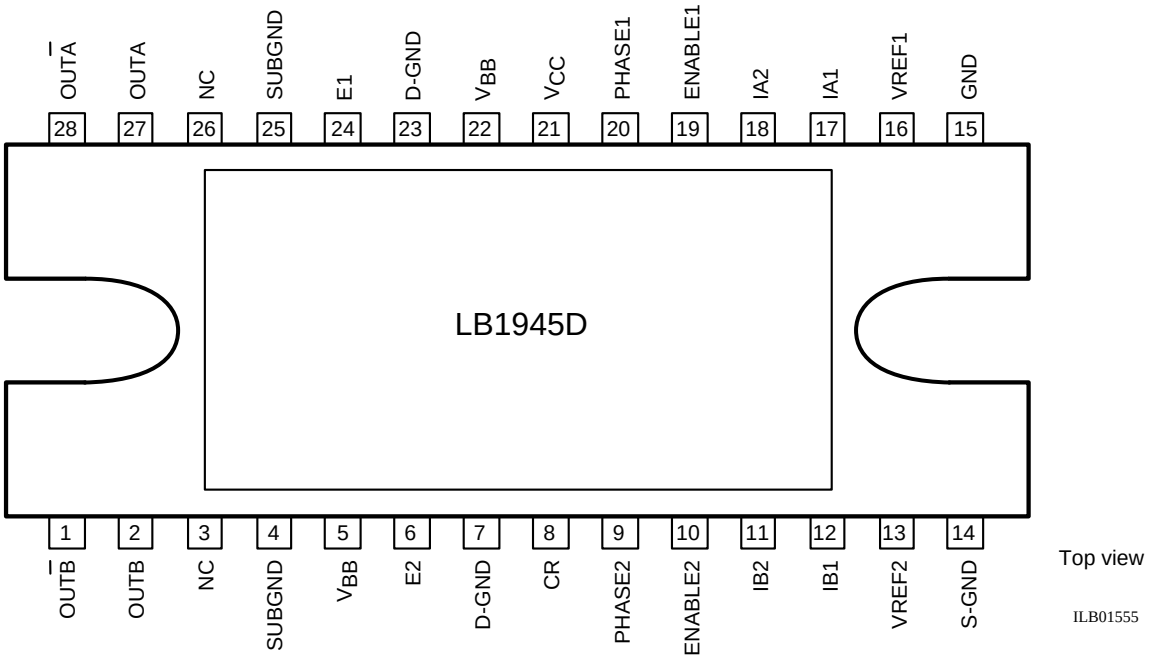
3147C



DIP28H(500mil)



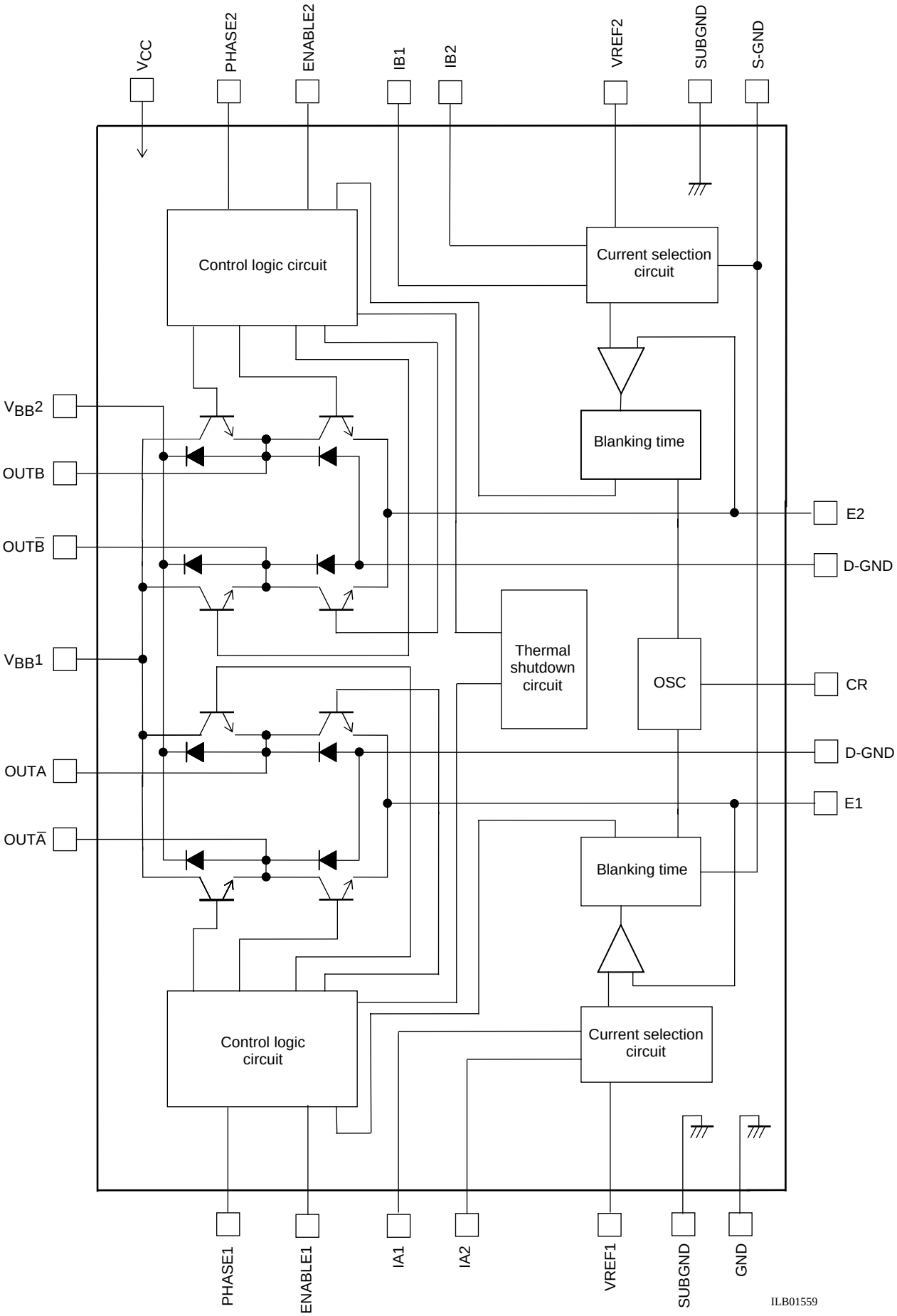
Pin Assignment



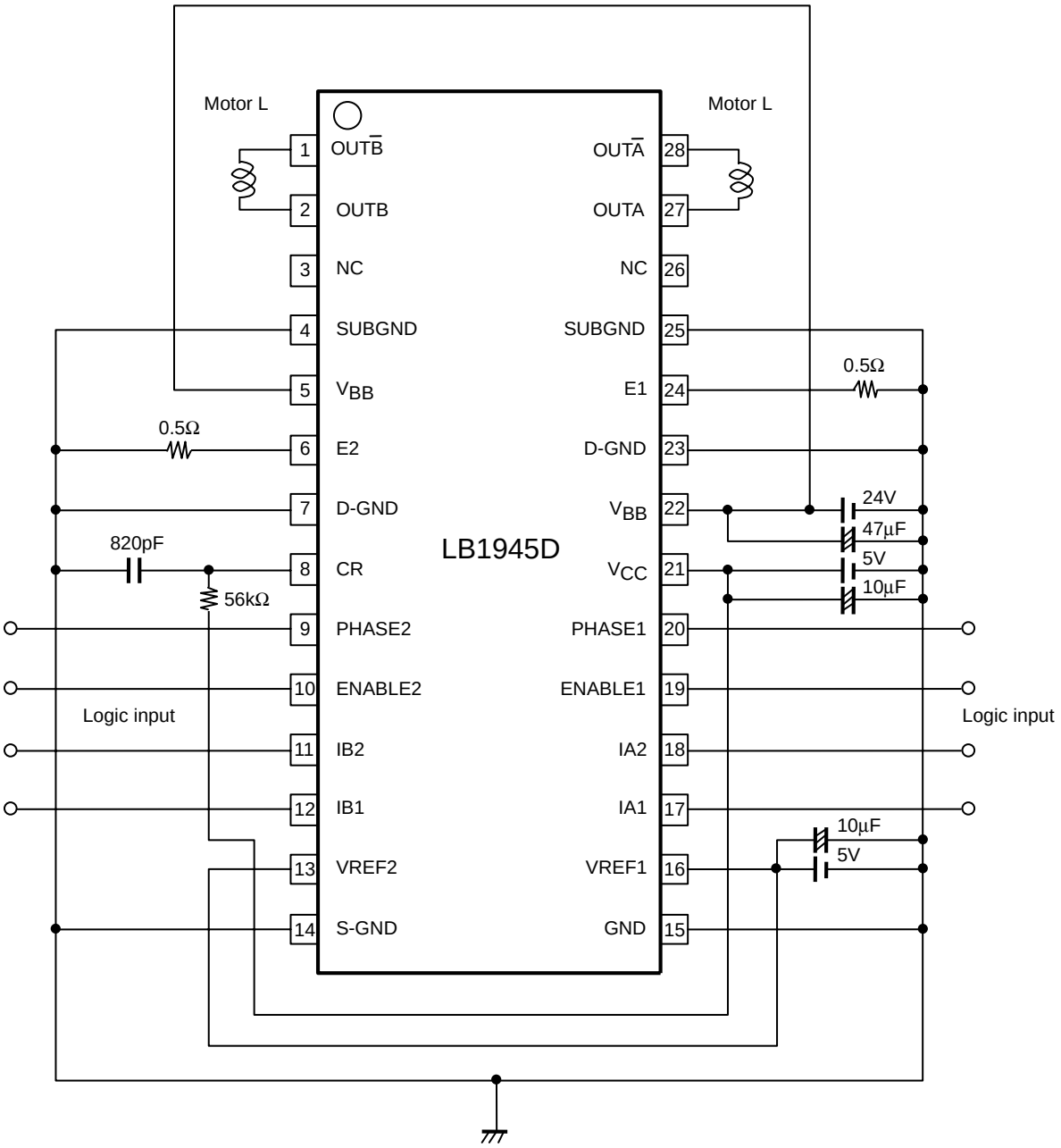
Pin Functions

Pin No.	Pin	Description
22	$V_{BB}1$	Output stage power supply voltage
5	$V_{BB}2$	High side diode cathode connection
24 6	E1 E2	The set current is controlled by inserting resistors RE between these pins and ground.
27 28 2 1	OUTA $\overline{OUTA}$ OUTB $\overline{OUTB}$	Output pins
15	GND	Ground
14	S-GND	Sense ground
4, 25	SUBGND	IC sub-ground
23 7	D-GND	Low side built-in diode ground (anode side)
8	CR	Chopping is performed at the period of a triangle wave set by the RC circuit connected to this pin. The triangle wave off time is the noise cancellation time.
16 13	VREF1 VREF2	Output current settings. (The output current is determined by providing an input in the range 1.5V to 5V.)
20 9	PHASE1 PHASE2	Output phase switching inputs High-level input: OUTA = high, $\overline{OUTA}$ = low Low-level input: OUTA = low, $\overline{OUTA}$ = high
19 10	ENABLE1 ENABLE2	Output on/off control inputs High-level input: Output off Low-level input: Output on
17, 18 12, 11	IA1, IA2 IB1, IB2	Output current setting digital inputs. The output current is set to 1/3, 2/3 or 1 by input high/low levels to these pins.
21	V_{CC}	Logic block power supply voltage

Block Diagram



Application circuit



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Truth Table

ENABLE	PHASE	OUTA	$\overline{OUTA}$
Low	High	High	Low
Low	Low	Low	High
High	-	OFF	OFF

I_1	I_2	Output current
Low	Low	$Vref/(10 \times R_E) = I_{OUT}$
High	Low	$Vref/(15 \times R_E) = I_{OUT} \times 2/3$
Low	High	$Vref/(30 \times R_E) = I_{OUT} \times 1/3$
High	High	0

Note: The output is turned off when ENABLE is high or in the $I_1 = I_2$ = high state.

Clockwise/counterclockwise Operating Sequence

2-phase excitation drive

Clockwise rotation — IA1 = IA2 = IB1 = IB2 = 0

No.	PHASE1	OUTA	$\overline{OUTA}$	PHASE2	OUTB	$\overline{OUTB}$
0	0	0	1	0	0	1
1	1	1	0	0	0	1
2	1	1	0	1	1	0
3	0	0	1	1	1	0

Counterclockwise rotation — IA1 = IA2 = IB1 = IB2 = 0

No.	PHASE1	OUTA	$\overline{OUTA}$	PHASE2	OUTB	$\overline{OUTB}$
0	0	0	1	1	1	0
1	1	1	0	1	1	0
2	1	1	0	0	0	1
3	0	0	1	0	0	1

Control Sequence

2-phase excitation

Table 1 — ENABLE1 = ENABLE2 = 0

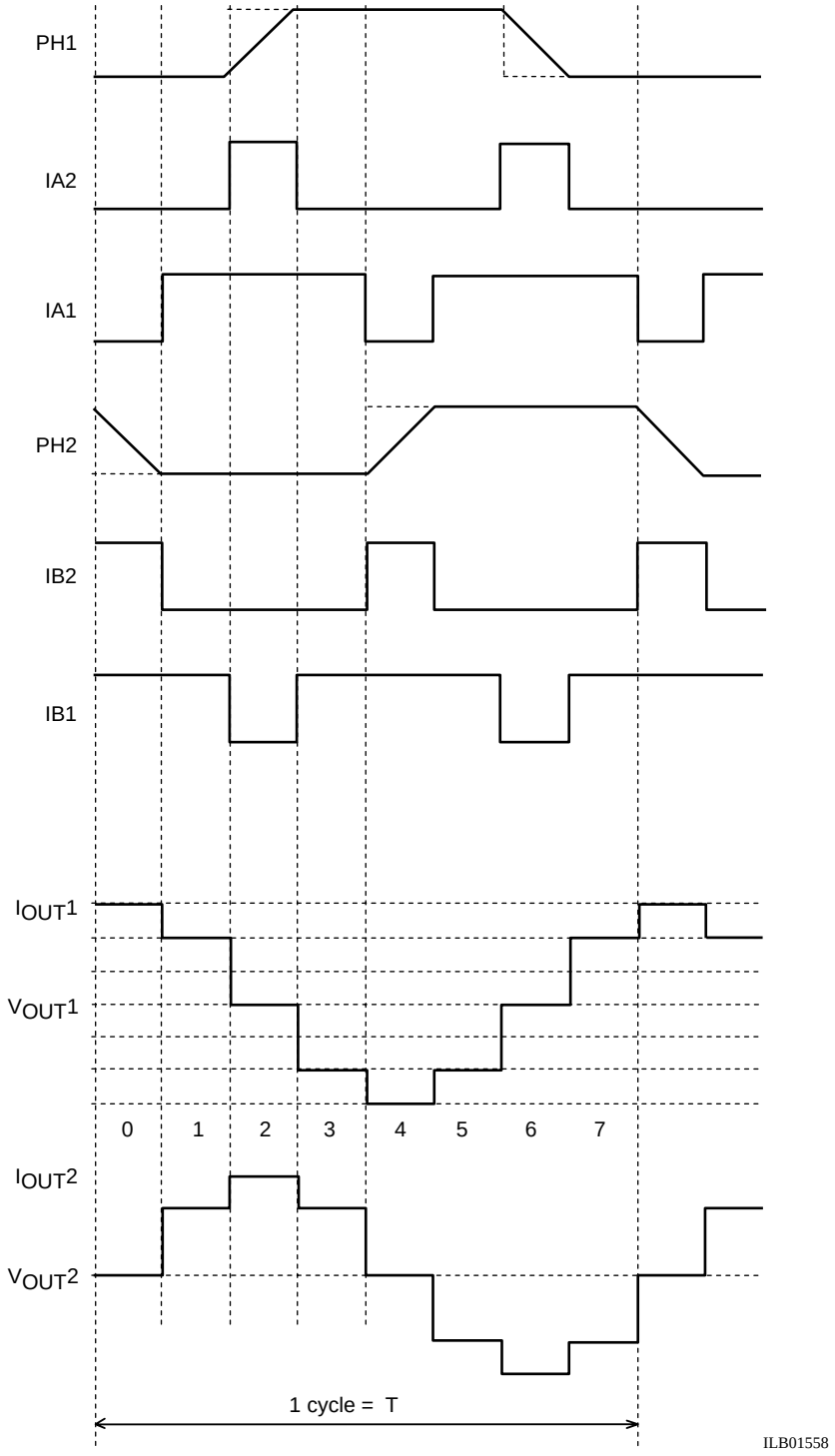
NO	Phase A				Phase B			
	PH1	IA2	IA1	Current value	PH2	IB2	IB1	Current value
0	0	0	0	1	0	0	0	1
1	1	0	0	1	0	0	0	1
2	1	0	0	1	1	0	0	1
3	0	0	0	1	1	0	0	1

1-2 phase excitation - 1/2 step

Table 2 — ENABLE1 = ENABLE2 = 0

No.	Phase A				Phase B			
	PH1	IA2	IA1	Current value	PH2	IB2	IB1	Current value
0	0	0	0	1	*	1	1	0
1	0	0	1	2/3	0	0	1	2/3
2	*	1	1	0	0	0	0	1
3	1	0	1	2/3	0	0	1	2/3
4	1	0	0	1	*	1	1	0
5	1	0	1	2/3	1	0	1	2/3
6	*	1	1	0	1	0	0	1
7	0	0	1	2/3	1	0	1	2/3

1-2 phase Excitation Timing Chart

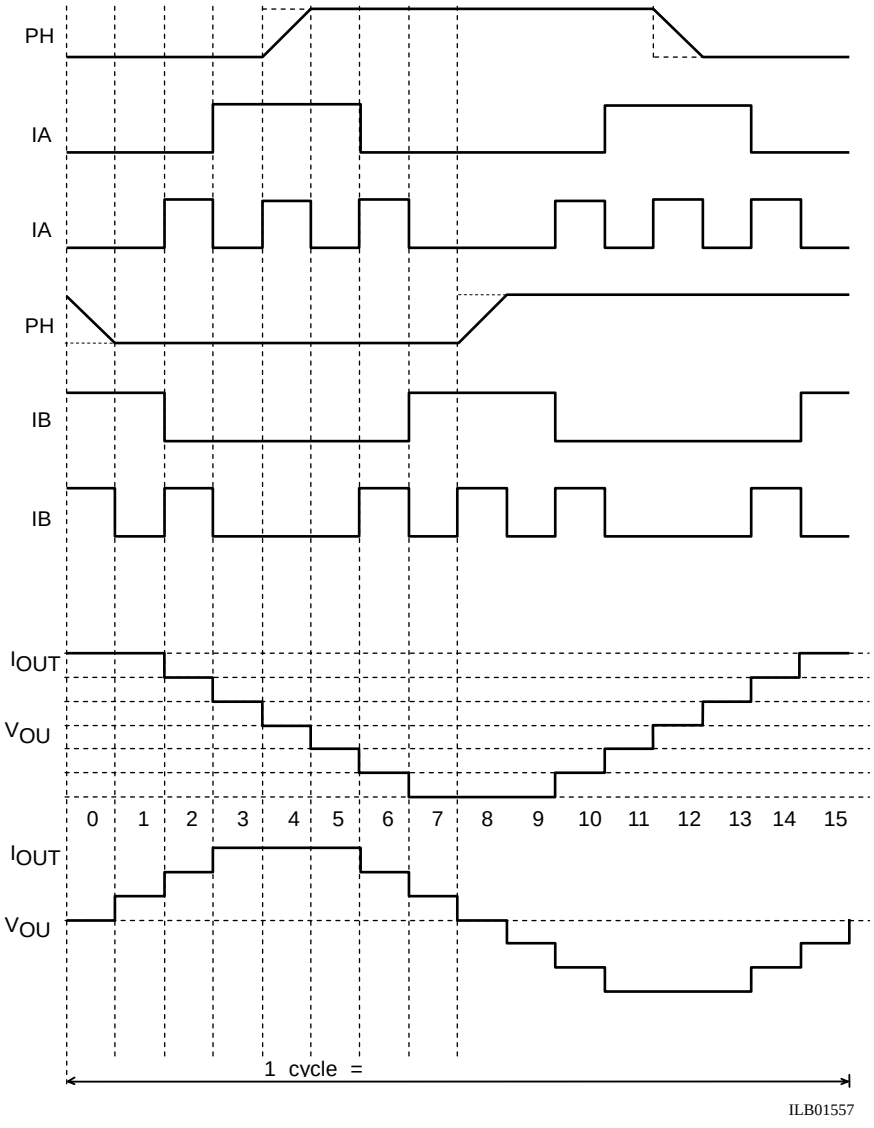


W1-2 phase excitation - about 1/4 step

Table 3 ENABLE1 = ENABLE2 = 0

NO	Phase A				Phase B			
	PH1	IA2	IA1	Current value	PH2	IB2	IB1	Current value
0	0	0	0	1	*	1	1	0
1	0	0	0	1	0	1	0	1/3
2	0	0	1	2/3	0	0	1	2/3
3	0	1	0	1/3	0	0	0	1
4	*	1	1	0	0	0	0	1
5	1	1	0	1/3	0	0	0	1
6	1	0	1	2/3	0	0	1	2/3
7	1	0	0	1	0	1	0	1/3
8	1	0	0	1	*	1	1	0
9	1	0	0	1	1	1	0	1/3
10	1	0	1	2/3	1	0	1	2/3
11	1	1	0	1/3	1	0	0	1
12	*	1	1	0	1	0	0	1
13	0	1	0	1/3	1	0	0	1
14	0	0	1	2/3	1	0	1	2/3
15	0	0	0	1	1	1	0	1/3

W1-2 phase Excitation Timing Chart



Simplified Equations for Determining RC Component Values

The equations for setting the RC oscillator circuit rise time (T1) and fall time (T2) are shown below.

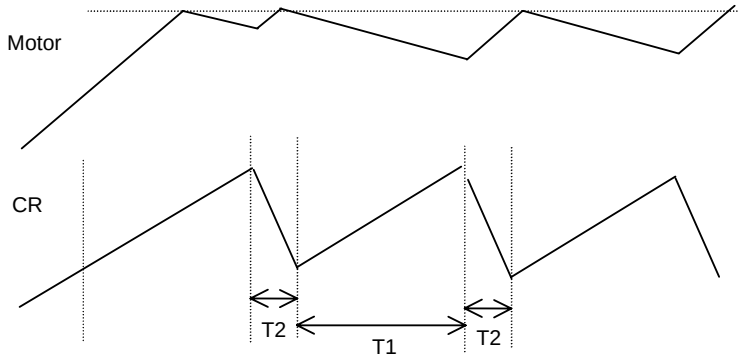
$T1 \approx 0.44C \times R$ (s)

$T2 \approx 0.72 \times (C \times R \times 1000)/(R + 1000)$ (s)

(C:220 to 4700pF, R = 10 to 150kΩ)

The oscillator frequency must be set using the simplified equations shown above.

Note that the triangle wave fall time (T2) is also used as the noise canceller time.



Usage Notes

1. VREF

   Since the VREF pin is the input pin for the reference voltage that sets the current, applications must be designed so that noise does not appear on this pin.

2. Ground pins

   Since this IC switches high currents, the following points concerning grounding must be observed.

   - The fins on the package rear surface, pins 7 and 8, and pins 21 and 22 must all be grounded.
   - Sections of the circuit that carry large currents must be implemented with wide lines in the printed circuit pattern, and must be physically separated from the small signal system.
   - The E pin sense resistor (RE) must be position as close as possible to the IC ground (pin 14).
   - The capacitors between V_{CC} and ground and between V_{BB} and ground must be positioned as close as possible to the V_{CC} and V_{BB} pins on the printed circuit pattern.