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REVISION HISTORY

1/2020—Rev. A to Rev. B

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This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

3/2017—Rev. 02.0317 to Rev. A

Updated Format ... Universal
Changes to Features Section, Figure 1, and General Description Section ... 1
Changed V_{SS} = −5 V to V_{SS} = −5 V to −3 V, Table 1 ... 3
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SPECIFICATIONS

Control voltage (V_{CTL}) = −5 V/0 V, die temperature (T_{DIE}) = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
BROADBAND FREQUENCY RANGE	f		0.1		20	GHz
INSERTION LOSS		0.1 GHz to 10 GHz		1.6	2.2	dB
		0.1 GHz to 20 GHz		2.0	2.7	dB
ISOLATION						
Between RFC and RF1 to RF2		0.1 GHz to 10 GHz	47	52		dB
		0.1 GHz to 20 GHz	35	40		dB
RETURN LOSS		0.1 GHz to 20 GHz				
RFC			9	12		dB
RF1 and RF2						
On State			13	18		dB
Off State			8	11		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		3		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		10		ns
INPUT LINEARITY		0.5 GHz to 20 GHz				
Input 1 dB Compression	P1dB	V_{CTL} = −5 V/0 V	22	29		dBm
		V_{CTL} = −3 V/0 V		24		dBm
Input 0.1 dB Compression	P0.1dB	V_{CTL} = −5 V/0 V		27		dBm
		V_{CTL} = −3 V/0 V		21		dBm
Input Third-Order Intercept	IP3	10 dBm per tone, 1 MHz spacing				
		V_{CTL} = −5 V/0 V	40	45		dBm
		V_{CTL} = −3 V/0 V		44		dBm
DIGITAL CONTROL INPUTS						
Voltage						
Low	V_{INL}		−0.2		0	V
High	V_{INH}		−5		−3	V
Current	I_{CTL}					
Low	I_{INL}	V_{CTL} = 0 V		3		µA
High	I_{INH}	V_{CTL} = −5 V to −3 V		10		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{CTL}	−7.5 V dc to +0.5 V
RF Input Power (f = 0.5 GHz to 20 GHz, T_{DIE} = 85°C)	
V_{CTL} = −5 V/0 V	
Through Path	27 dBm
Terminated Path	25 dBm
Hot Switching	23 dBm
V_{CTL} = −3 V/0 V	
Through Path	21 dBm
Terminated Path	19 dBm
Hot Switching	17 dBm
Temperature	
Channel	150°C
Storage	−65°C to +150°C
Operating	−55°C to +85°C
ESD (Electrostatic Discharge) Sensitivity	
Human Body Model (HBM)	Class 0, passed 150 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3.

Package Option	θ_{JC}	Unit
C-10-9		
Through Path	118	°C/W
Terminated Path	200	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

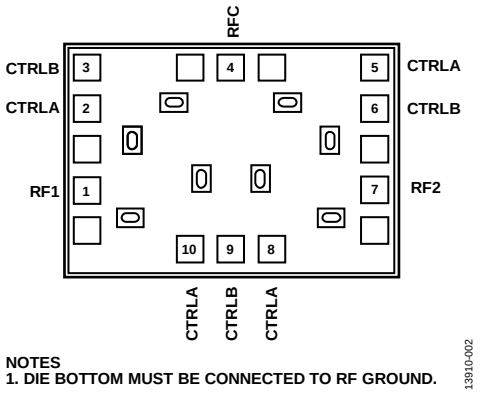

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
1	RF1	RF Throw Pad 1. This pad is dc-coupled and matched to 50 Ω. Blocking capacitors are required if the RF line potential ≠ 0 V.
2, 5, 8, 10	CTRLA	Control Input A. See Figure 4 for the interface schematic.
3, 6, 9	CTRLB	Control Input B. See Figure 4 for the interface schematic.
4	RFC	RF Common Pad. This pad is dc-coupled and matched to 50 Ω. Blocking capacitors are required if the RF line potential ≠ 0 V.
7	RF2	RF Throw Pad 2. This pad is dc-coupled and matched to 50 Ω. Blocking capacitors are required if the RF line potential ≠ to 0 V.
Die Bottom	GND	Die bottom must be connected to RF ground.

[1] No connection is required for the unlabeled grounds.

INTERFACE SCHEMATICS

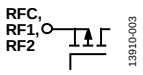

Figure 3. RFC, RF1, and RF2 Interface Schematic

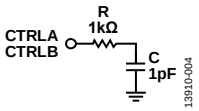

Figure 4. CTRLA, CTRLB Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

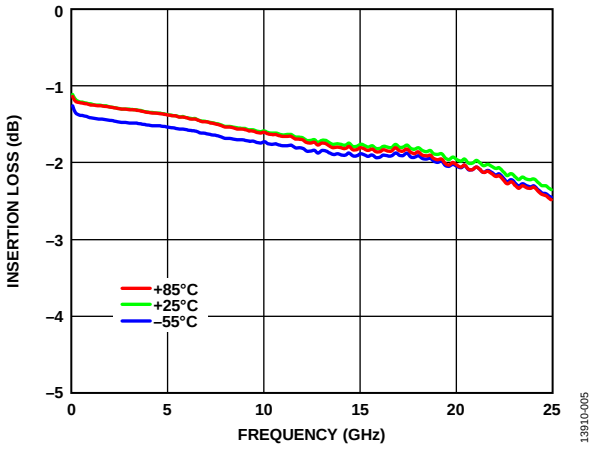

Figure 5. Insertion Loss vs. Frequency over Temperature

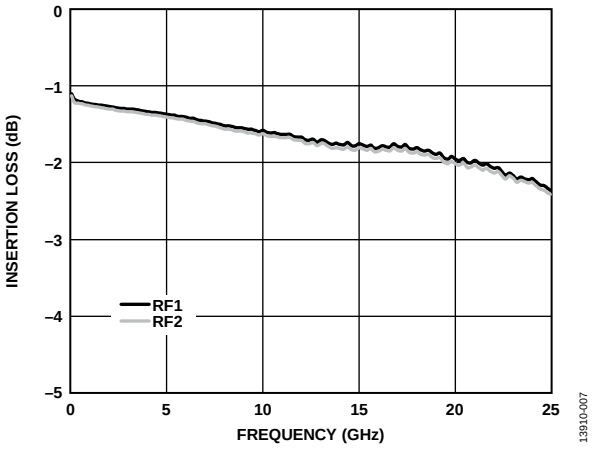

Figure 7. Insertion Loss Between RFC and RF1/RF2 vs. Frequency

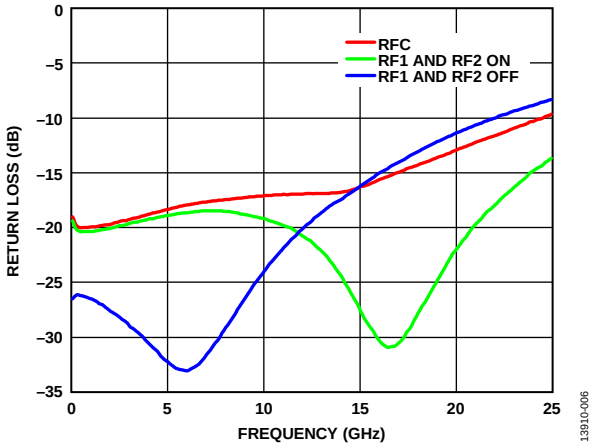

Figure 6. Return Loss vs. Frequency

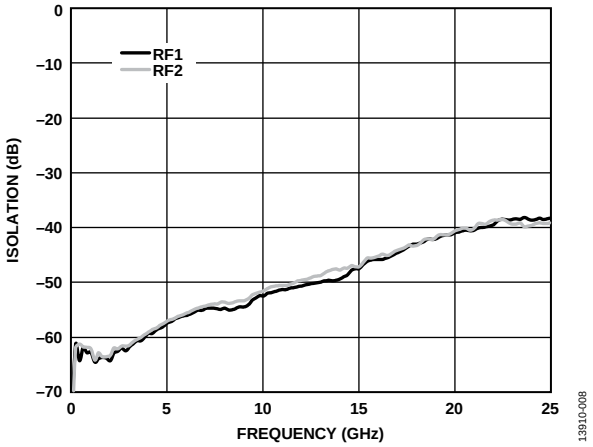

Figure 8. Isolation Between RFC and RF1/RF2 vs. Frequency

INPUT P1dB, INPUT P0.1dB, AND INPUT IP3

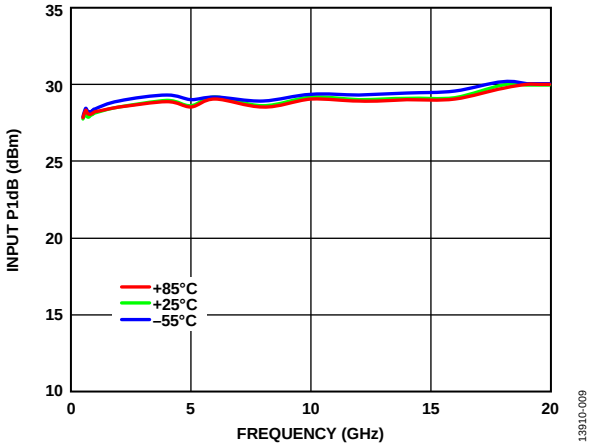

Figure 9. Input P1dB vs. Frequency over Temperature, V_{CTL} = –5 V

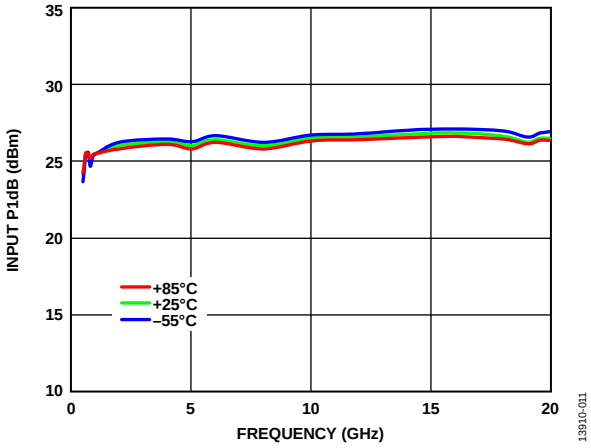

Figure 10. Input P1dB vs. Frequency over Temperature, V_{CTL} = –3 V

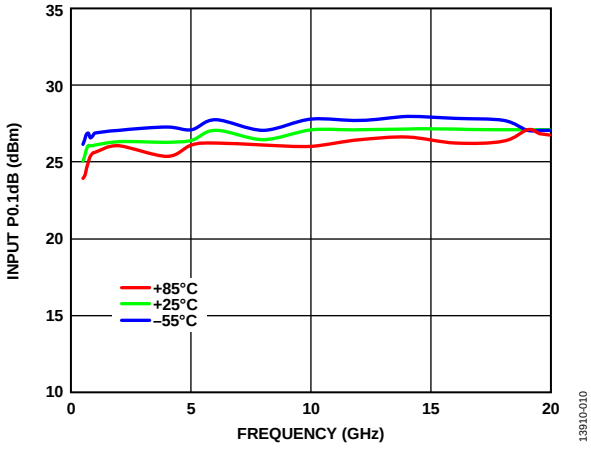

Figure 10. Input Power 0.1 dB vs. Frequency over Temperature, V_{CTL} = –5 V

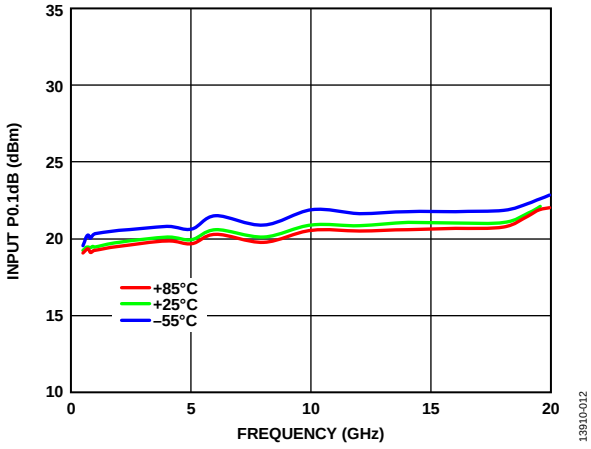

Figure 11. Input P0.1dB vs. Frequency over Temperature, V_{CTL} = –3 V

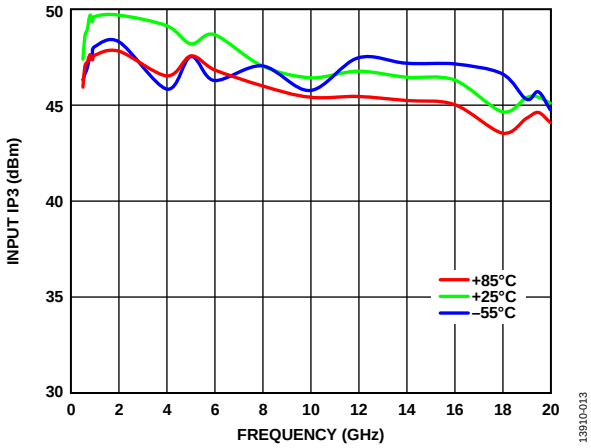

Figure 11. Input IP3 vs. Frequency over Temperature, V_{CTL} = –5 V

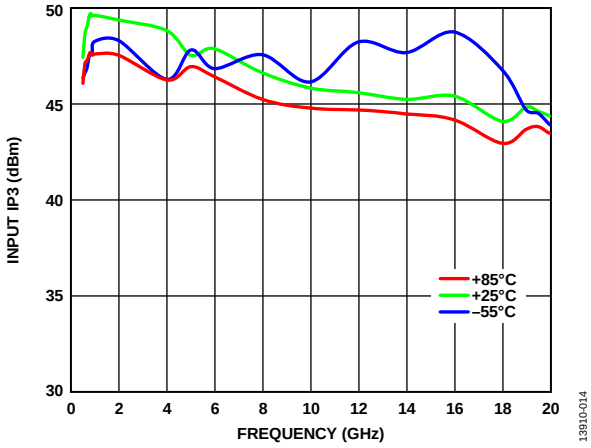

Figure 12. Input IP3 vs. Frequency over Temperature, V_{CTL} = –3 V

THEORY OF OPERATION

The HMC347A requires two negative control voltages at the CTRLx pads to control the state of the RF paths and requires no supply.

Depending on the logic level applied to the CTRLx pads, one RF path is in the insertion loss state and the other path is in isolation state (see Table 5). The insertion loss path conducts the RF signal between the RF1 pad or RF2 pad and the RFC pad. The isolation path provides high loss between the selected insertion loss path and the unselected RF1 pad or RF2 pad that is terminated to an internal 50 Ω resistor.

The ideal power-up sequence is as follows:

1. Ground to the die bottom.
2. Power up the digital control inputs. The relative order of the logic control inputs is not important.
3. Apply an RF input signal. The design is bidirectional and the RF input signal can be applied to the RFC pad when the RF1 and RF2 throw pads are outputs, or the RF input signal can be applied to the RF1 and RF2 throw pads when the RFC pad is the output. The RFx pads are dc-coupled to 0 V, and no dc blocking is required at the RFx pads when the RF line potential is equal to 0 V.

The power-down sequence is the reverse of the power-up sequence.

Table 5. Control Voltage Truth Table

Digital Control Input		RF Paths	
CTRLA	**CTRLB**	**RF1 to RFC**	**RF2 to RFC**
High	Low	Insertion loss (on)	Isolation (off)
Low	High	Isolation (off)	Insertion loss (on)

APPLICATIONS INFORMATION

MOUNTING AND BONDING TECHNIQUES

The HMC347A is back metallized and must be attached directly to the ground plane with gold tin (AuSn) eutectic preforms or with electrically conductive epoxy.

The die thickness is 0.102 mm (4 mil). The 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick, alumina thin film substrates are recommended to bring the RF signal to and from the HMC347A (see Figure 13).

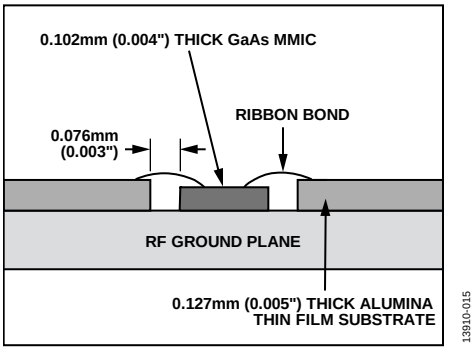

Figure 13. Bonding RF Pads to 5 mil Substrate

When using 0.254 mm (10 mil) thick, alumina thin film substrates, the HMC347A must be raised 0.150 mm (6 mil) so that the surface of the HMC347A is coplanar with the surface of the substrate. The device can be raised by attaching the 0.102 mm (4 mil) thick die to a 0.150 mm (6 mil) thick molybdenum (Mo) heat spreader (moly tab), which is then attached to the ground plane (see Figure 14).

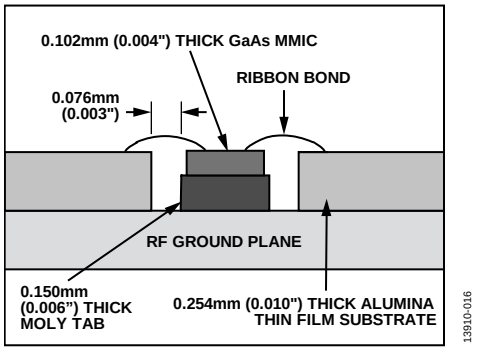

Figure 14. Bonding RF Pads to 10 mil Substrate

Microstrip substrates are placed as close to the HMC347A as possible to minimize bond length. Typical die to substrate spacing is 0.076 mm (3 mil).

RF bonds with 3 mil × 0.5 mil ribbon and dc bonds with 1 mil diameter wire are recommended. All bonds must be as short as possible.

ASSEMBLY DIAGRAM

An assembly diagram of the HMC347A is shown in Figure 15.

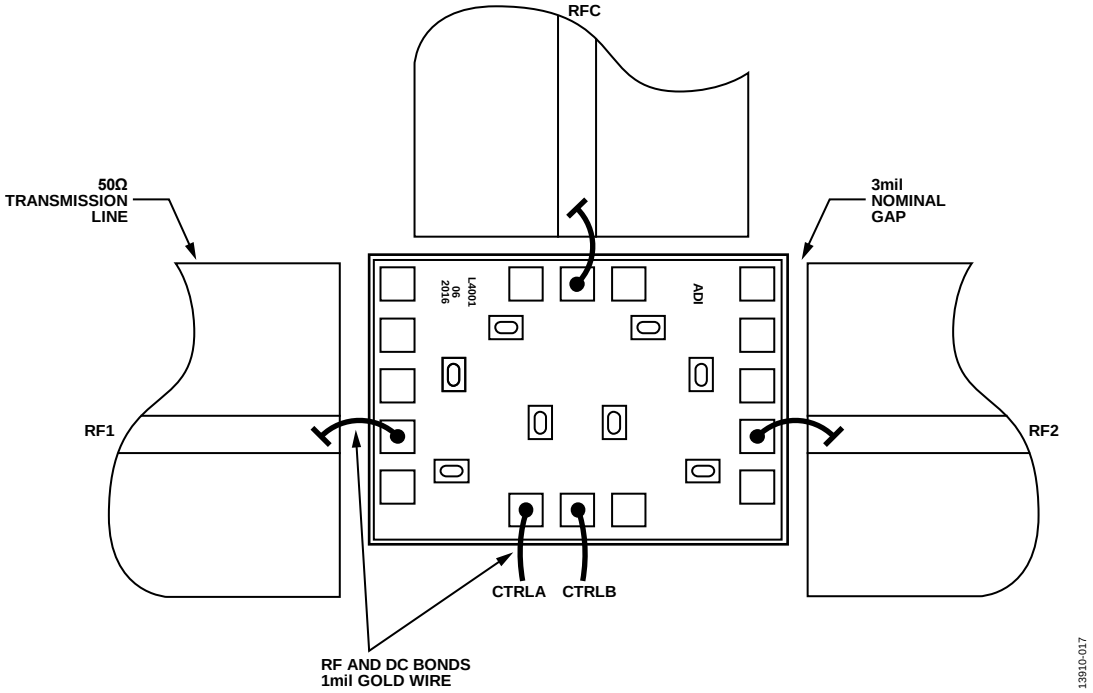

Figure 15. Die Assembly Diagram

OUTLINE DIMENSIONS

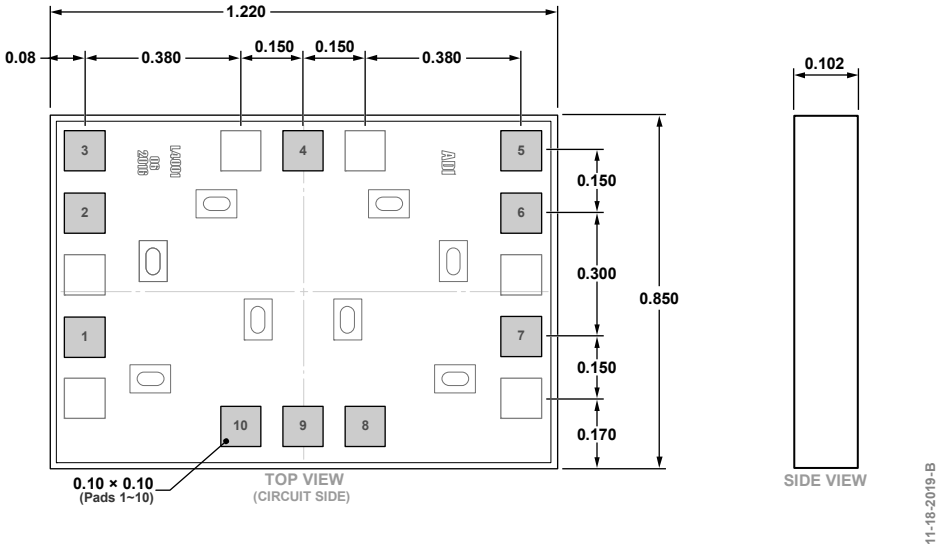

Figure 16. 10-Pad Bare Die [CHIP]
(C-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
HMC347A	−55°C to +85°C	10-Pad Bare Die [CHIP]	C-10-9
HMC347A-SX	−55°C to +85°C	10-Pad Bare Die [CHIP]	C-10-9

[1] The HMC347A is a RoHS Compliant Part.
[2] The HMC347A-SX is a sample order model.

D13910-0-1/20(B)