PIN DESCRIPTION

SIGNAL	FUNCTION	DESCRIPTION
Vcc	POWER	+5V ±5%
V+	POWER	+9.5V to +10.5V
V-	POWER	-9.5V to -10.5V
429DI1 (A)	INPUT	ARINC receiver 1 positive input
429DI1 (B)	INPUT	ARINC receiver 1 negative input
429DI2 (A)	INPUT	ARINC receiver 2 positive input
429DI2 (B)	INPUT	ARINC receiver 2 negative input
$\overline{D/R1}$	OUTPUT	Receiver 1 data ready flag
$\overline{D/R2}$	OUTPUT	Receiver 2 data ready flag
SEL	INPUT	Receiver data byte selection (0 = BYTE 1) (1 = BYTE 2)
$\overline{EN1}$	INPUT	Data Bus control, enables receiver 1 data to outputs
$\overline{EN2}$	INPUT	Data Bus control, enables receiver 2 data to outputs if $\overline{EN1}$ is high
BD15	I/O	Data Bus
BD14	I/O	Data Bus
BD13	I/O	Data Bus
BD12	I/O	Data Bus
BD11	I/O	Data Bus
BD10	I/O	Data Bus
BD09	I/O	Data Bus
BD08	I/O	Data Bus
BD07	I/O	Data Bus
BD06	I/O	Data Bus
GND	POWER	0 V
BD05	I/O	Data Bus
BD04	I/O	Data Bus
BD03	I/O	Data Bus
BD02	I/O	Data Bus
BD01	I/O	Data Bus
BD00	I/O	Data Bus
TX/R	OUTPUT	Transmitter ready flag. Goes low when ARINC word loaded into FIFO. Goes high after transmission and FIFO empty.
$\overline{PL1}$	INPUT	Latch enable for byte 1 entered from data bus to transmitter FIFO.
$\overline{PL2}$	INPUT	Latch enable for byte 2 entered from data bus to transmitter FIFO. Must follow $\overline{PL1}$.
TXA(OUT)	OUTPUT	Line driver output - A side
TXB(OUT)	OUTPUT	Line driver output - B side
ENTX	INPUT	Enable Transmission
$\overline{CWSTR}$	INPUT	Clock for control word register
CLK	INPUT	Master Clock input
TX CLK	OUTPUT	Transmitter Clock equal to Master Clock (CLK), divided by either 10 or 80.
$\overline{MR}$	INPUT	Master Reset, active low

FUNCTIONAL DESCRIPTION

CONTROL WORD REGISTER

Both the HI-8581and HI-8589 contain 10 data flip flops whose D inputs are connected to the data bus and clocks connected to $\overline{\text{CWSTR}}$. Each flip flop provides options to the user as follows:

DATA BUS PIN	FUNCTION	CONTROL	DESCRIPTION
BDO5	SELF TEST	0 = ENABLE	If enabled, the transmitter's digital outputs are internally connected to the receiver logic inputs
BDO6	RECEIVER 1 DECODER	1 = ENABLE	If enabled, ARINC bits 9 and, 10 must match the next two control word bits
BDO7	-	-	If Receiver 1 Decoder is enabled, the ARINC bit 9 must match this bit
BDO8	-	-	If Receiver 1 Decoder is enabled, the ARINC bit 10 must match this bit
BDO9	RECEIVER 2 DECODER	1 = ENABLE	If enabled, ARINC bits 9 and 10 must match the next two Control word bits
BD10	-	-	If Receiver 2 Decoder is enabled, then ARINC bit 9 must match this bit
BD11	-	-	If Receiver 2 Decoder is enabled, then ARINC bit 10 must match this bit
BD12	INVERT XMTR PARITY	1 = ENABLE	Logic 0 enables normal odd parity and Logic 1 enables even parity output in transmitter 32nd bit
BD13	XMTR DATA CLK SELECT	0 = ÷10 1 = ÷80	CLK is divided either by 10 or 80 to obtain XMTR data clock
BD14	RCVR DTA CLK SELECT	0 = ÷10 1 = ÷80	CLK is divided either by 10 or 80 to obtain RCVR data clock

ARINC 429 DATA FORMAT

The following table shows the bit positions in exchanging data with the receiver or the transmitter. ARINC bit 1 is the first bit transmitted or received.

BYTE 1																
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01	BD 00
ARINC BIT	13	12	11	10	9	31	30	32	1	2	3	4	5	6	7	8

BYTE 2																
DATA BUS	BD 15	BD 14	BD 13	BD 12	BD 11	BD 10	BD 09	BD 08	BD 07	BD 06	BD 05	BD 04	BD 03	BD 02	BD 01	BD 00
ARINC BIT	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14

THE RECEIVERS

ARINC BUS INTERFACE

Figure 1 shows the input circuit for each receiver. The ARINC 429 specification requires the following detection levels:

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

The HI-8581 and HI-8589 guarantee recognition of these levels with a common mode Voltage with respect to GND less than ±4V for the worst case condition (4.75V supply and 13V signal level).

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

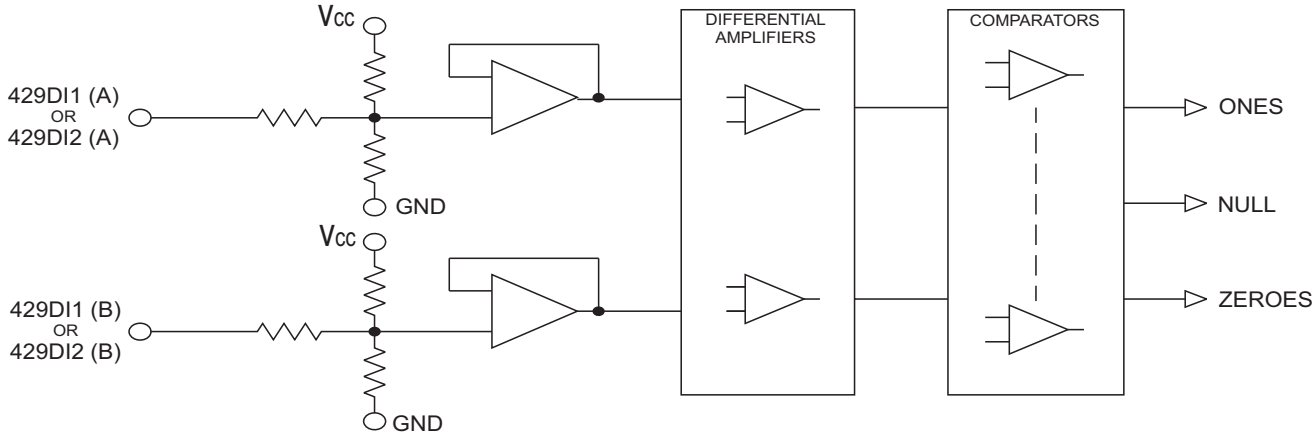


FIGURE 1. **ARINC RECEIVER INPUT**

FUNCTIONAL DESCRIPTION (cont.)

RECEIVER LOGIC OPERATION

Figure 2 is a block diagram showing each receiver's logic.

BIT TIMING

ARINC 429 specifies the following timing for received data:

	HIGH SPEED	LOW SPEED
BIT RATE	100K BPS ± 1%	12K -14.5K BPS
PULSE RISE TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE FALL TIME	1.5 ± 0.5 µsec	10 ± 5 µsec
PULSE WIDTH	5 µsec ± 5%	34.5 - 41.7 µsec

The HI-8581 and HI-8589 accepts signals meeting these specifications and rejects signals outside these tolerances using the method described here:

1. The timing logic requires an accurate 1.0 MHz clock source. Less than 0.1% error is recommended.

2. The sampling shift registers are 10 bits long and must show three consecutive Ones, Zeros or Nulls to be considered valid data. To qualify data bits, One or Zero in the upper bits of the sampling shift register must be followed by Null in the lower bits within the data bit time. A word gap Null requires three consecutive Nulls in both the upper and lower bits of the sampling shift register. This guarantees the minimum pulse width.

3. Each data bit must follow its predecessor by not less than 8 samples and not more than 12 samples. In this manner the bit rate is checked. With exactly 1 MHz input clock frequency, the acceptable data bit rates are as follows:

	HIGH SPEED	LOW SPEED
DATA BIT RATE MIN	83K BPS	10.4K BPS
DATA BIT RATE MAX	125K BPS	15.6K BPS

4. The Word Gap timer samples the Null shift register every 10 input clocks (80 for low speed) after the last data bit of a valid reception. If the Null is present, the Word Gap counter is incremented. A count of 3 enables the next reception.

RECEIVER PARITY

The 32nd bit of received ARINC words stored in the receive FIFO is used as a Parity Flag indicating whether good Odd parity is received from the incoming ARINC word.

Odd Parity Received
The parity bit is reset to indicate correct parity was received and the resulting word is then written to the receive FIFO.

Even Parity Received
The receiver sets the 32nd bit to a "1", indicating a parity error and the resulting word is then written to the receive FIFO.

Therefore, the 32nd bit retrieved from the receiver FIFO will always be a "0" when valid (odd parity) ARINC 429 words are received.

RETRIEVING DATA

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). If the receiver decoder is enabled and the 9th and 10th ARINC bits match the control word program bits or if the receiver decoder is disabled, then EOS clocks the data ready flag flip flop to a "1", $\overline{D/R1}$ or $\overline{D/R2}$ (or both) will go low. The data flag for a receiver remains low until after both ARINC bytes from that receiver are retrieved. This is accomplished by first activating $\overline{EN}$ with SEL, the byte selector, low to retrieve the first byte and then activating $\overline{EN}$ with SEL high to retrieve the second byte. $\overline{EN1}$ retrieves data from receiver 1 and $\overline{EN2}$ retrieves data from receiver 2.

If another ARINC word is received and a new EOS occurs before the two bytes are retrieved, the data is overwritten by the new word.

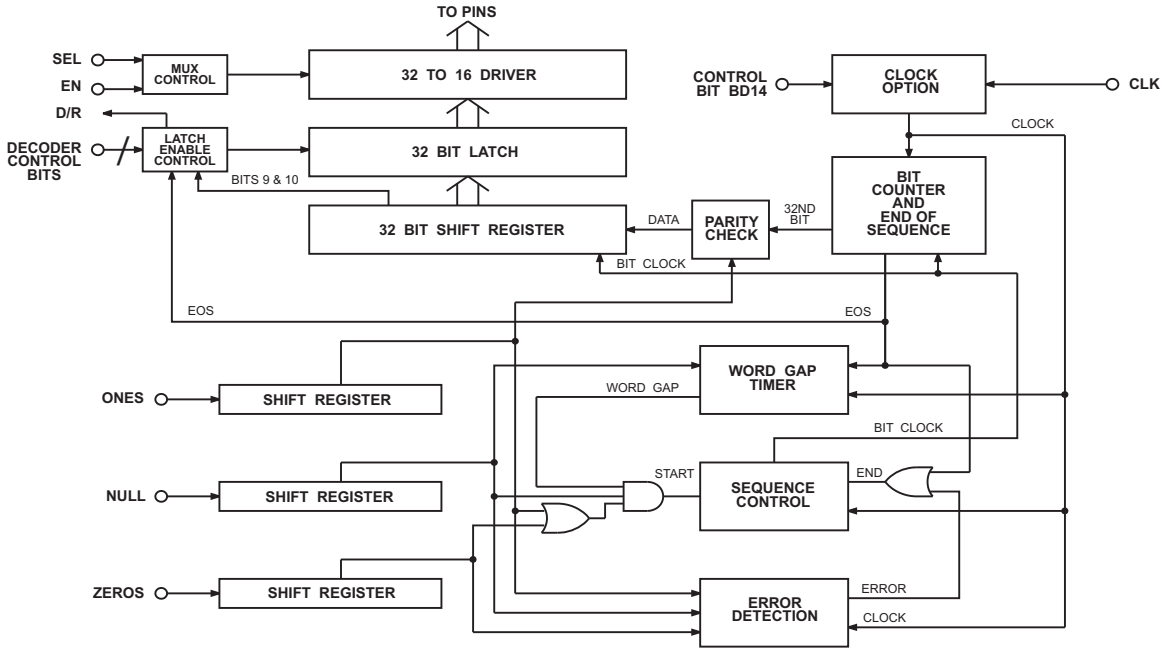


FIGURE 2. **RECEIVER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (cont.)

TRANSMITTER

A block diagram of the transmitter section is shown in Figure 3.

FIFO OPERATION

The FIFO is loaded sequentially by first pulsing $\overline{PL1}$ to load byte 1 and then $\overline{PL2}$ to load byte 2. The control logic automatically loads the 31 bit word in the next available position of the FIFO. If TX/R, the transmitter ready flag is high (FIFO empty), then 8 words, each 31 bits long, may be loaded. If TX/R is low, then only the available positions may be loaded. If all 8 positions are full, the FIFO ignores further attempts to load data.

DATA TRANSMISSION

When ENTX goes high, enabling transmission, the FIFO positions are incremented with the top register loading into the data transmission shift register. Within 2.5 data clocks the first data bit appears at either TXA(OUT) or TXB(OUT). The 31 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	HIGH SPEED	LOW SPEED
ARINC DATA BIT TIME	10 Clocks	80 Clocks
DATA BIT TIME	5 Clocks	40 Clocks
NULL BIT TIME	5 Clocks	40 Clocks
WORD GAP TIME	40 Clocks	320 Clocks

The word counter detects when all loaded positions are transmitted and sets the transmitter ready flag, TX/R, high.

TRANSMITTER PARITY

The parity generator counts the ONES in the 31-bit word. If the BD12 control word bit is set low, the 32nd bit transmitted will make parity odd. If the control bit is high, the parity is even.

SELF TEST

If the BD05 control word bit is set low, the digital outputs of the transmitter are internally connected to the logic inputs of the receivers, bypassing the analog bus interface circuitry. Data to Receiver 1 is as transmitted and data to Receiver 2 is the complement. All data transmitted during self test is also present on the TXA(OUT) and TXB(OUT) line driver outputs.

SYSTEM OPERATION

The two receivers are independent of the transmitter. Therefore, control of data exchanges is strictly at the option of the user. The only restrictions are:

1. The received data may be overwritten if not retrieved within one ARINC word cycle.

2. The FIFO can store 8 words maximum and ignores attempts to load addition data if full.

3. Byte 1 of the transmitter data must be loaded first.

4. Either byte of the received data may be retrieved first. Both bytes must be retrieved to clear the data ready flag.

5. After ENTX, transmission enable, goes high it cannot go low until TX/R, transmitter ready flag, goes high. Otherwise, one ARINC word is lost during transmission.

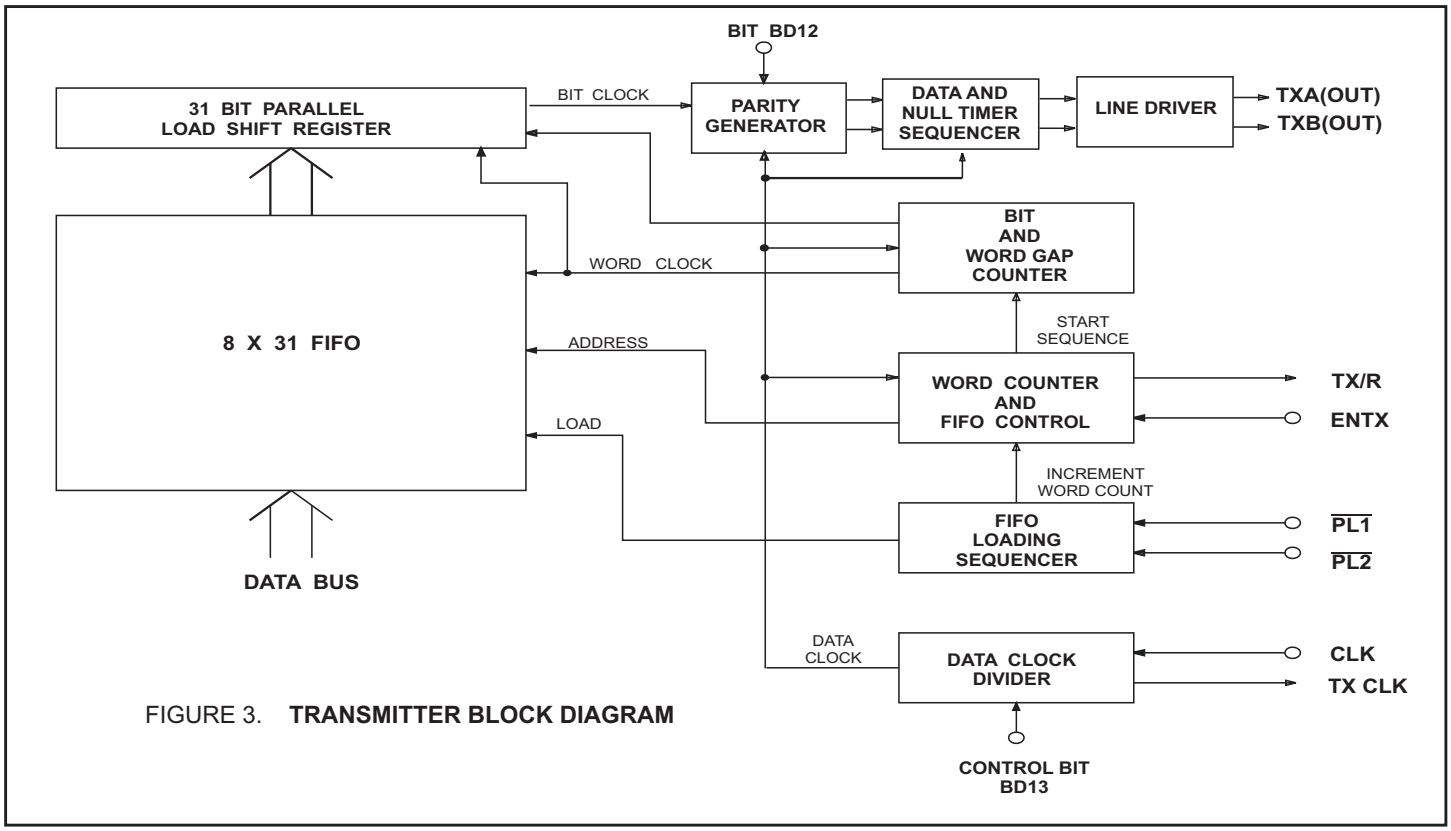


FIGURE 3. **TRANSMITTER BLOCK DIAGRAM**

FUNCTIONAL DESCRIPTION (cont.)

LINE DRIVER OPERATION

The line driver in the HI-8581 and HI-8589 is designed to directly drive the ARINC 429 bus. The two ARINC outputs (TXA(OUT) and TXB(OUT)) provide a differential voltage to produce a +10 volt One, a -10 volt Zero, and a 0 volt Null. Setting Control Register bit 13 to zero causes a slope of 1.5 μs on the ARINC outputs. A one in Control Register bit 13 causes a slope of 10 μs. Timing is set by on-chip resistor and capacitor and tested to be within ARINC requirements. No additional hardware is required to control the slope. The HI-8581 has 37.5 ohms whereas the HI-8589 has 10 ohms in series with each line driver output. The HI-8589 is for applications where additional external series resistance is required, such as lightning protection.

REPEATER OPERATION

Repeater mode of operation allows a data word that has been received by the HI-8581 or HI-8589 to be placed directly into its FIFO for transmission. Repeater operation is similar to normal receiver operation. In normal operation, either byte of a received data word may be read from the receiver latches first by use of SEL input. During repeater operation however, the lower byte of the data word must be read first. This is necessary because, as the data is being read, it is also being loaded into the FIFO and the transmitter FIFO is always loaded with the lower byte of the data word first. Signal flow for repeater operation is shown in the Timing Diagrams section.

HI-8581-10 and HI-8589-10

The "-10" versions of the HI-8581 and HI-8589 products require a 10 Kohm resistor to be placed in series with each ARINC input without affecting the ARINC input thresholds. This option is especially useful in applications where external lightning protection is required.

Each ARINC input pin must be connected to the ARINC bus through a 10 Kohm resistor in order for the chip to properly detect the correct ARINC levels. The typical 10 volt differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 10 Kohm resistors, they are just below the standard 6.5 volt minimum ARINC data threshold and just above the 2.5 volt maximum ARINC null threshold.

Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

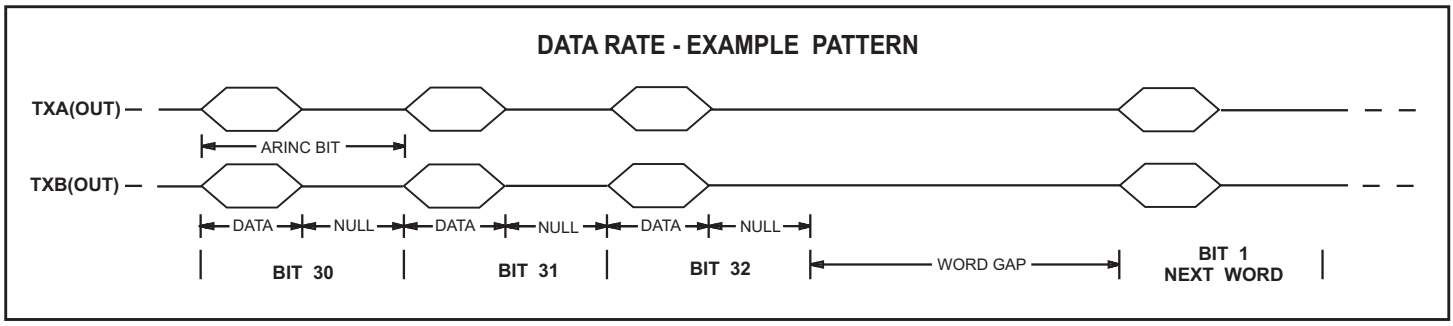
POWER SUPPLY SEQUENCING

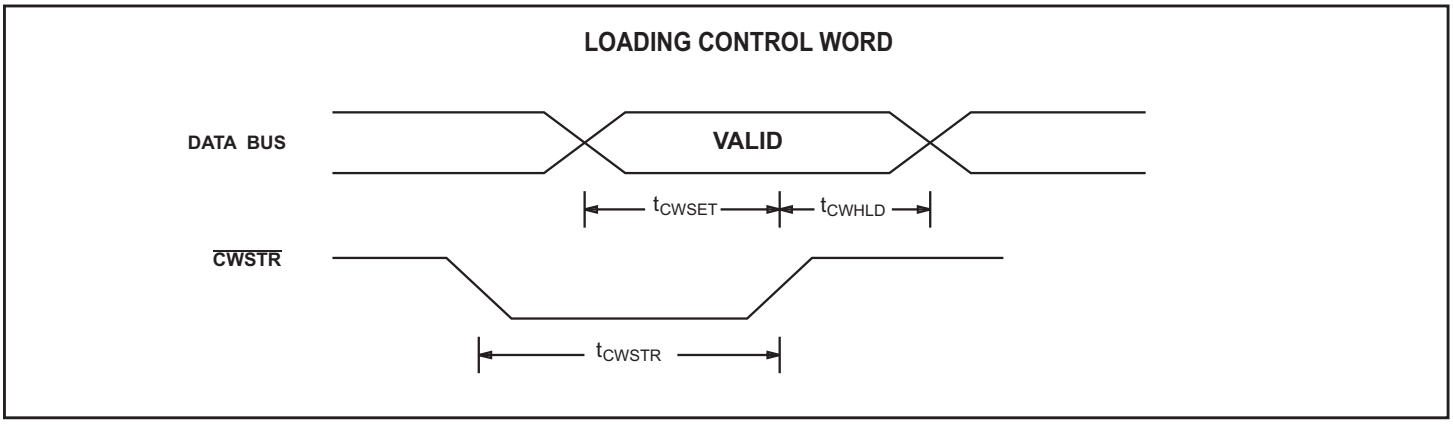
The power supplies should be controlled to prevent large currents during supply turn-on and turn-off. The recommended sequence is V+ followed by Vcc, always ensuring that V+ is the most positive supply. The V- supply is not critical and can be asserted at any time.

MASTER RESET ($\overline{MR}$)

On a Master Reset data transmission and reception are immediately terminated, all three FIFOs are cleared as are the FIFO flags at the device pins and in the Status Register. The Control Register is not affected by a Master Reset.

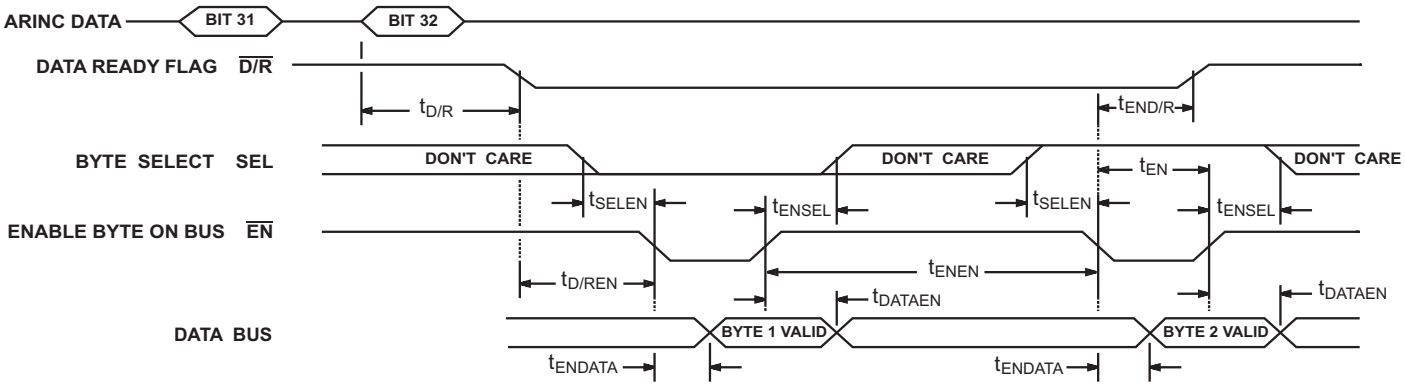
TIMING DIAGRAMS



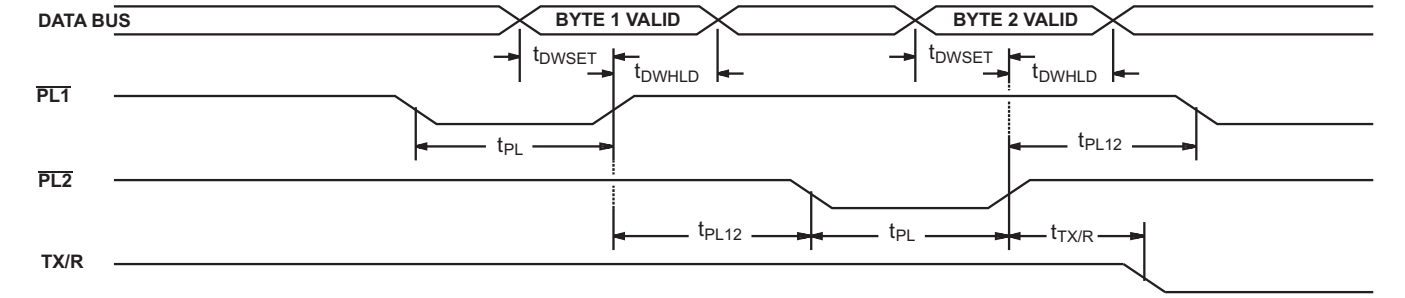


TIMING DIAGRAMS (cont.)

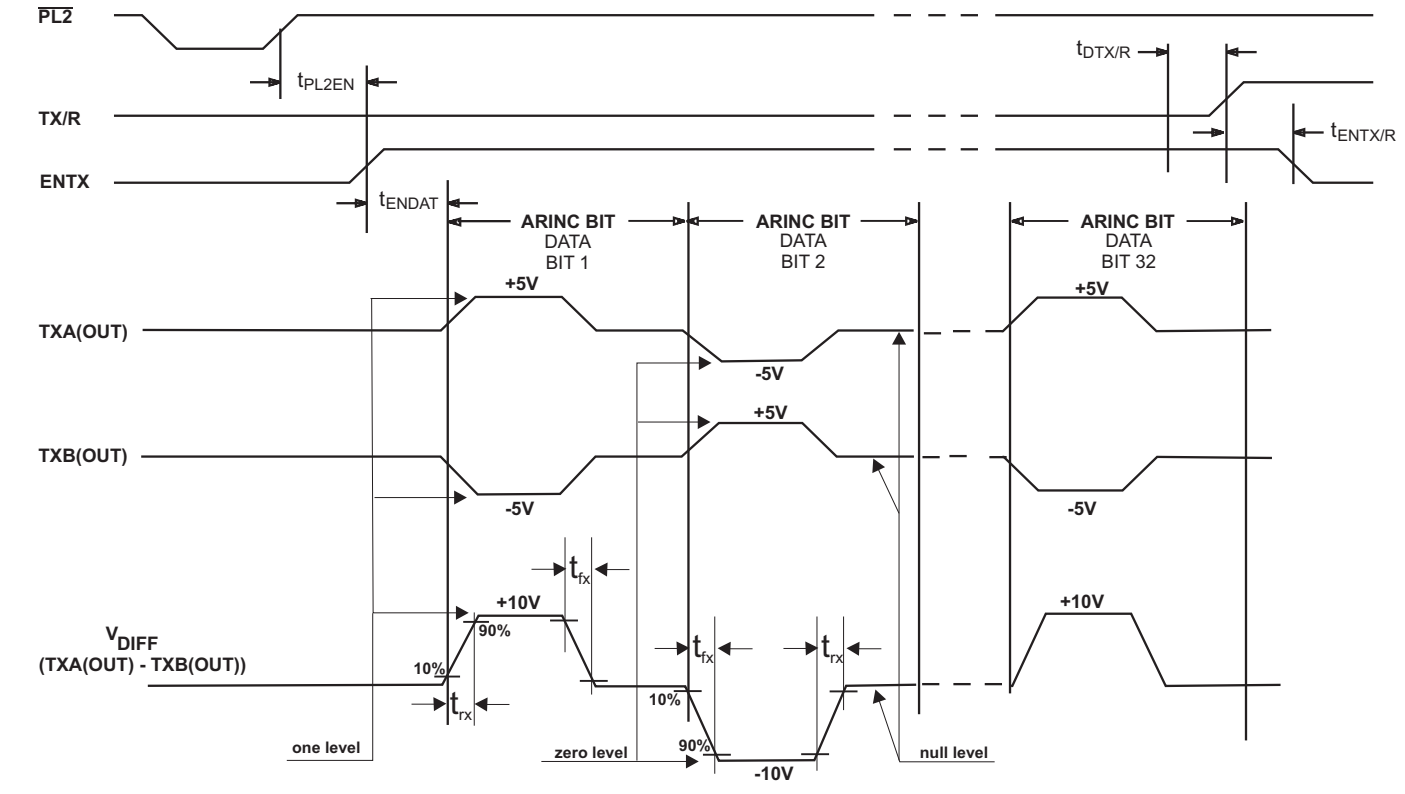
RECEIVER OPERATON



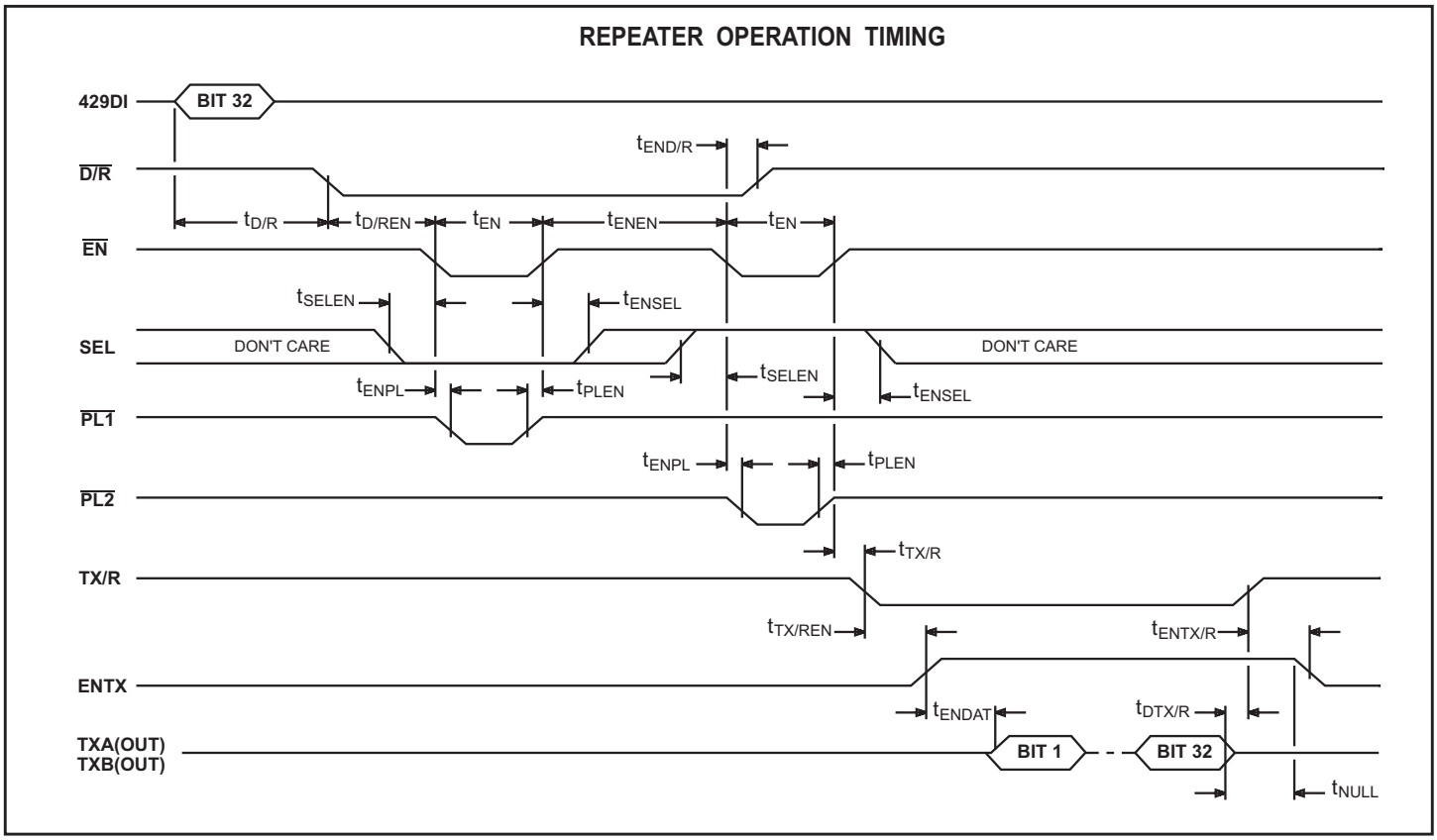
TRANSMITTER OPERATION



TRANSMITTING DATA



TIMING DIAGRAMS (cont.)



ABSOLUTE MAXIMUM RATINGS

Supply Voltages Vcc . . . . . -0.3V to +7V V+ . . . . . +12.5V V- . . . . . -12.5V	Power Dissipation at 25°C Plastic PLCC/PQFP . . . . . 1.5 W, derate 10mW/°C Ceramic J-LEAD CERQUAD . . . . . 1.0 W, derate 7mW/°C
Voltage at ARINC inputs . . . . . -120V to +120V	DC Current Drain per pin . . . . . ±10mA
Voltage at any other pin . . . . . -0.3V to Vcc +0.3V	Storage Temperature Range: . . . . . -65°C to +150°C
Soldering Temperature (Reflow) . . . . . 260°C	Operating Temperature Range: (Industrial) . . . . . -40°C to +85°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ±5%, V+ = 10V , V- = -10V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER		SYMBOL	CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
ARINC INPUTS							
Differential Input Voltage: (429DI1(A) to 429DI1(B); 429DI2(A) to 429DI2(B))	ONE ZERO NULL	V_{IH} V_{IL} V_{NUL}	Common mode voltage less than ±4V with respect to GND	6.5 -13.0 -2.5	10.0 -10.0 0	13.0 -6.5 2.5	V V V
Input Resistance:	Differential To GND To Vcc	R_I R_G R_H		12 12 12	 27 27		KΩ KΩ KΩ
Input Current:	Input Sink Input Source	I_{IH} I_{IL}		 -450		200	µA µA
Input Capacitance:(Guaranteed but not tested) (429DI1(A), 429DI1(B), 429DI2(A) & 429DI2(B))	Differential To GND To Vcc	C_I C_G C_H				20 20 20	pF pF pF
BI-DIRECTIONAL INPUTS							
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}		2.1		 0.7	V V
Input Current:	Input Sink Input Source	I_{IH} I_{IL}		 -1.5		1.5	µA µA
OTHER INPUTS							
Input Voltage:	Input Voltage HI Input Voltage LO	V_{IH} V_{IL}		3.5		 0.7	V V
Input Current:	Input Sink Input Source	I_{IH} I_{IL}		 -20		10	µA

DC ELECTRICAL CHARACTERISTICS (cont.)

Vcc = 5V ±5%, V+ = 10V, V- = -10V, GND = 0V, TA = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
ARINC OUTPUTS						
ARINC output voltage One or zero Null	 V_{DOUT} V_{NOUT}	 no load and magnitude at pin " " " " " "	 4.50 -0.25	 5.00	 5.50 0.25	 V V
ARINC output current	I_{OUT}		80			mA
OTHER OUTPUTS						
Output Voltage: Logic "1" Output Voltage Logic "0" Output Voltage	V_{OH} V_{OL}	I_{OH} = -1.5mA I_{OL} = 2.6mA	2.7		 0.4	V V
Output Current: Output Sink (Bi-directional Pins) Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{CC} - 0.4V	3.0 1.1			mA mA
Output Current: Output Sink (All Other Outputs) Output Source	I_{OL} I_{OH}	V_{OUT} = 0.4V V_{OUT} = V_{CC} - 0.4V	2.6 1.1			mA mA
Output Capacitance:	C_O			15		pF
Operating Voltage Range						
	V_{CC}		4.75		5.25	V
	V+		9.5		10.5	V
	V-		-9.5		-10.5	V
Operating Supply Current						
V_{CC}	I_{CC1}				20	mA
V+	I_{DD1}				16	mA
V-	I_{EE1}				16	mA

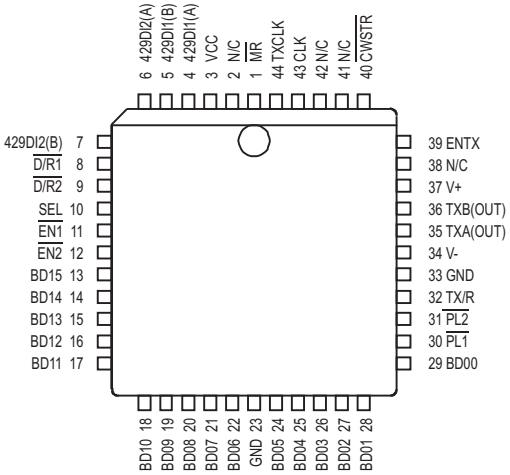
AC ELECTRICAL CHARACTERISTICS

Vcc = 5V, V+=10V, V- = -10V, GND = 0V, TA = Oper. Temp. Range and fclk = 1MHz ±0.1% with 60/40 duty cycle

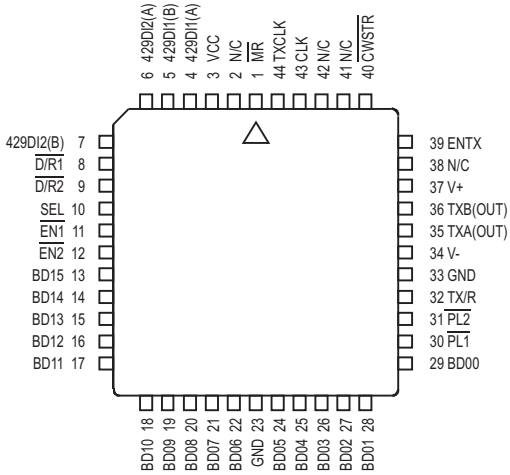
PARAMETER	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
CONTROL WORD TIMING					
Pulse Width - $\overline{\text{CWSTR}}$	t_{CWSTR}	80			ns
Setup - DATA BUS Valid to $\overline{\text{CWSTR}}$ HIGH	t_{CWSET}	50			ns
Hold - $\overline{\text{CWSTR}}$ HIGH to DATA BUS Hi-Z	t_{CWHLD}	10			ns
RECEIVER TIMING					
Delay - Start ARINC 32nd Bit to $\overline{\text{D/R}}$ LOW: High Speed	$t_{D/R}$			16	µs
Low Speed	$t_{D/R}$			128	µs
Delay - $\overline{\text{D/R}}$ LOW to $\overline{\text{EN}}$ LOW	$t_{D/REN}$	0			ns
Delay - $\overline{\text{EN}}$ LOW to $\overline{\text{D/R}}$ HIGH	$t_{END/R}$			200	ns
Setup - SEL to $\overline{\text{EN}}$ LOW	t_{SELEN}	10			ns
Hold - SEL to $\overline{\text{EN}}$ HIGH	t_{ENSEL}	10			ns
Delay - $\overline{\text{EN}}$ LOW to DATA BUS Valid	t_{ENDATA}		50	100	ns
Delay - $\overline{\text{EN}}$ HIGH to DATA BUS Hi-Z	t_{DATAEN}			30	ns
Pulse Width - $\overline{\text{EN1}}$ or $\overline{\text{EN2}}$	t_{EN}	80			ns
Spacing - $\overline{\text{EN}}$ HIGH to next $\overline{\text{EN}}$ LOW	t_{ENEN}	50			ns
FIFO TIMING					
Pulse Width - $\overline{\text{PL1}}$ or $\overline{\text{PL2}}$	t_{PL}	80			ns
Setup - DATA BUS Valid to $\overline{\text{PL}}$ HIGH	t_{DWSET}	50			ns
Hold - $\overline{\text{PL}}$ HIGH to DATA BUS Hi-Z	t_{DWHLD}	10			ns
Spacing - $\overline{\text{PL1}}$ or $\overline{\text{PL2}}$	t_{PL12}	0			ns
Delay - $\overline{\text{PL2}}$ HIGH to TX/R LOW	$t_{TX/R}$			840	ns
TRANSMISSION TIMING					
Spacing - $\overline{\text{PL2}}$ HIGH to ENTX HIGH	t_{PL2EN}	0			µs
Delay - 32nd ARINC Bit to TX/R HIGH	$t_{DTX/R}$			50	ns
Spacing - TX/R HIGH to ENTX LOW	$t_{ENTX/R}$	0			ns
LINE DRIVER OUTPUT TIMING					
Delay - ENTX HIGH to TXA(OUT) or TXB(OUT): High Speed	t_{ENDAT}			25	µs
Delay - ENTX HIGH to TXA(OUT) or TXB(OUT): Low Speed	t_{ENDAT}			200	µs
Line driver transition differential times:					
(High Speed) high to low	t_{fx}	1.0	1.5	2.0	µs
low to high	t_{rx}	1.0	1.5	2.0	µs
(Low Speed) high to low	t_{fx}	5.0	10	15	µs
low to high	t_{rx}	5.0	10	15	µs
REPEATER OPERATION TIMING					
Delay - $\overline{\text{EN}}$ LOW to $\overline{\text{PL}}$ LOW	t_{ENPL}	0			ns
Hold - $\overline{\text{PL}}$ HIGH to $\overline{\text{EN}}$ HIGH	t_{PLEN}	0			ns
Delay - TX/R LOW to ENTX HIGH	$t_{TX/REN}$	0			ns
MASTER RESET PULSE WIDTH	t_{MR}	400			ns
ARINC DATA RATE AND BIT TIMING				± 1%	

ADDITIONAL HI-8581 / HI-8589 PIN CONFIGURATIONS

(See page 1 for the 44-Pin Plastic Quad Flat Pack (PQFP) pin configuration)



HI-8581PJI / HI-8589PJI
HI-8581PJT / HI-8589PJT
44-Pin Plastic J-Lead PLCC



HI-8581CJI / HI-8589CJI
HI-8581CJT / HI-8589CJT
44-Pin J-Lead CERQUAD

ORDERING INFORMATION

HI - 8581 xx x x - xx

PART NUMBER	INPUT SERIES RESISTANCE	
	BUILT-IN	REQUIRED EXTERNALLY
No dash number	35 Kohm	0
-10	25 Kohm	10 Kohm

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	No
T	-55°C TO +125°C	T	No

PART NUMBER	PACKAGE DESCRIPTION
CJ	44 PIN CERQUAD J LEAD (44U) not available Pb-free
PJ	44 PIN PLASTIC J LEAD PLCC (44J)
PQ	44 PIN PLASTIC QUAD FLAT PACK, PQFP (44PQS)

PART NUMBER	OUTPUT SERIES RESISTANCE	
	BUILT-IN	REQUIRED EXTERNALLY
8581	37.5 Ohms	0
8589	10 Ohms	27.5 Ohms

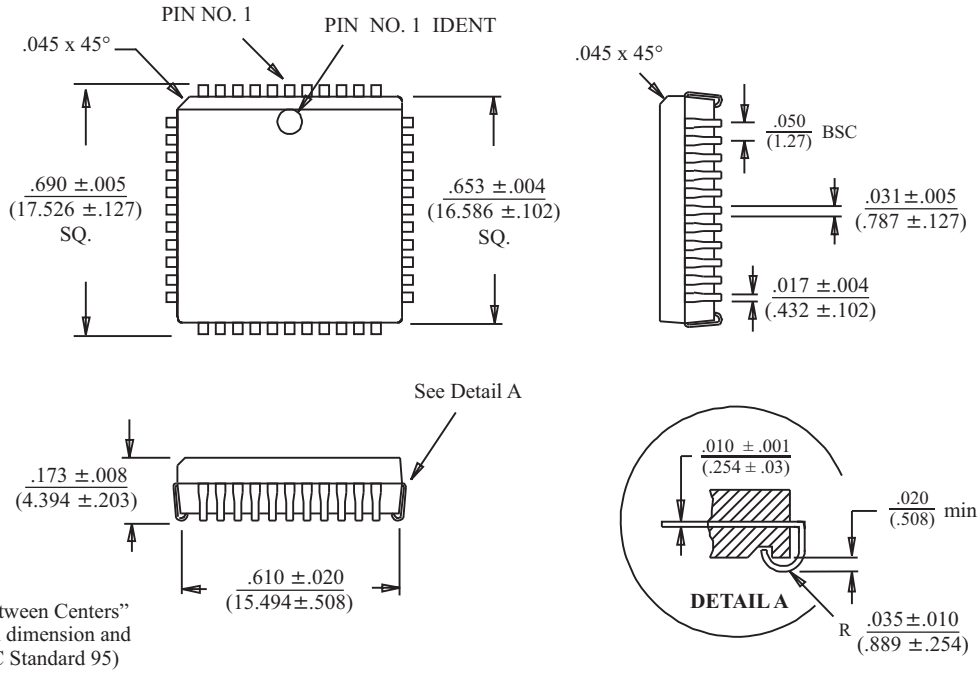
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8581	J	08/06/13	Clarified description of receiver parity. Updated solder temp to reflow 260 only. Updated PQFP package. Update Voltage at ARINC input pins from +/-29V to +/-120V. Updated last paragraph under Retrieving Data (not visible in previous version).

44-PIN PLASTIC PLCC

inches (millimeters)

Package Type: 44J

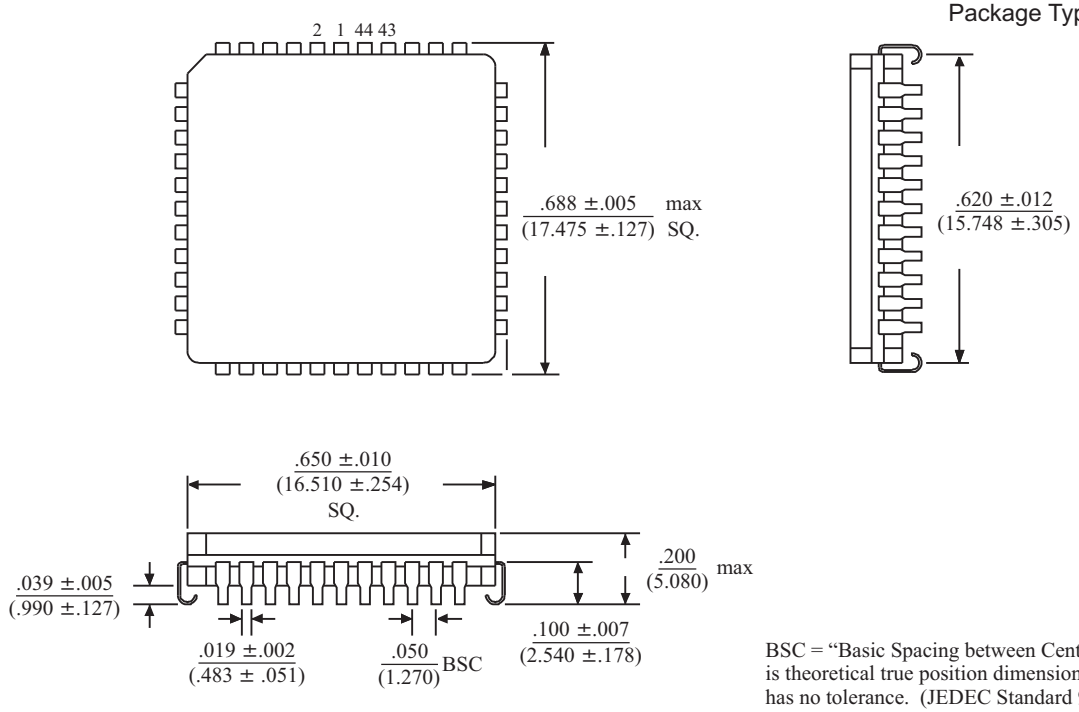


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN J-LEAD CERQUAD

inches (millimeters)

Package Type: 44U

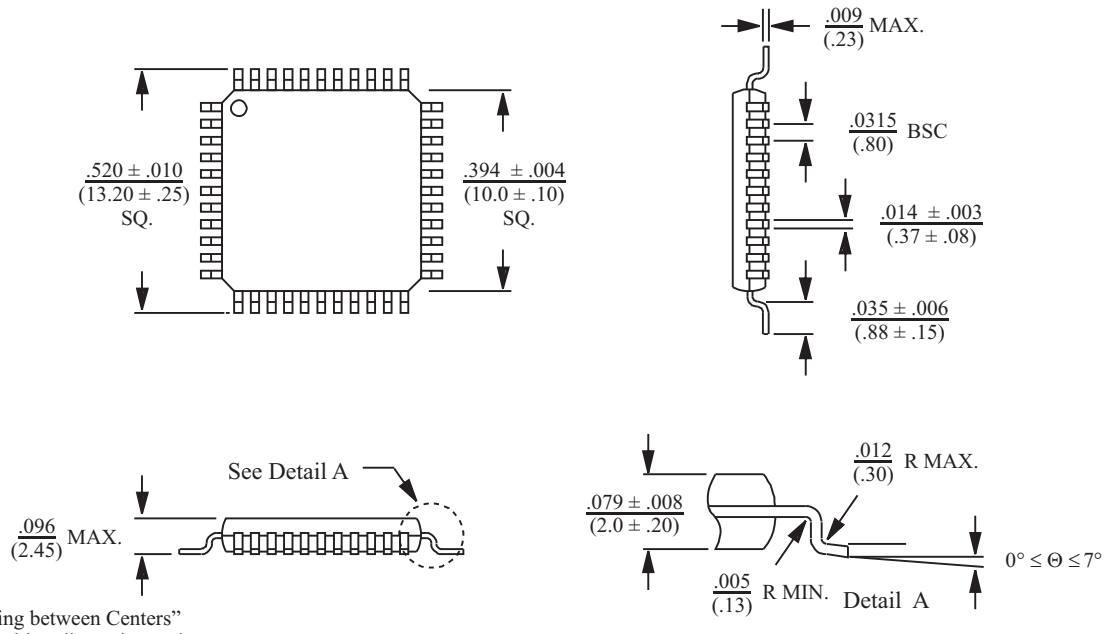


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

inches (millimeters)

Package Type: 44PMQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)