Absolute Maximum Ratings

Voltage Range on V_{CC} Pin Relative to Ground ... -0.3V to +6.0V
Voltage Range on Inputs Relative to Ground ... -0.3V to (V_{CC} + 0.3V)
Operating Temperature Range ... -40°C to +85°C
Storage Temperature Range ... -55°C to +125°C
Soldering Temperature ... Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at nominal supply voltage and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Note 2)	V_{CC}	DS139x-33	2.97	3.3	5.50	V
		DS139x-3	2.7	3.0	3.3	
		DS139x-18	1.71	1.8	1.89	
Logic 1	V_{IH}	(Note 2)	0.7 x V_{CC}		V_{CC} + 0.5	V
Logic 0	V_{IL}	(Note 2)	-0.3		+0.3 x V_{CC}	V
Supply Voltage, Pullup SQW/$\overline{INT}$, SQW, $\overline{INT}$, V_{CC} = 0V	V_{PU}	(Note 2)			5.5	V
V_{BACKUP} Voltage (Note 2)	V_{BACKUP}	-33	1.3	3.0	$V_{CC(MAX)}$	V
		-3	1.3	3.0	3.7	
		-18	1.3	3.0	3.7	
Power-Fail Voltage (Note 2)	V_{PF}	-33	2.70	2.88	2.97	V
		-3	2.45	2.6	2.70	
		-18	1.51	1.6	1.71	
Trickle-Charge Current-Limiting Resistors	R1	(Notes 3, 4)		250		Ω
	R2	(Notes 3, 5)		2000		
	R3	(Notes 3, 6)		4000		
Input Leakage	I_{LI}	(Note 7)	-1		+1	µA
I/O Leakage	I_{LO}	(Note 8)	-1		+1	µA
$\overline{RST}$ Pin I/O Leakage	I_{LORST}	(Note 9)	-200		+10	µA
DOUT Logic 1 Output	I_{OHDOUT}	-33, -3 (V_{OH} = 0.85 x V_{CC})			-1	mA
		-18 (V_{OH} = 0.80 x V_{CC})			0.750	
DOUT Logic 0 Output	I_{OHDOUT}	-33, -3 (V_{OL} = 0.15 x V_{CC})			3	mA
		-18 (V_{OL} = 0.20 x V_{CC})			2	
Logic 0 Output (DS1390/DS1393/DS1394 SQW/$\overline{INT}$; DS1392 SQW, $\overline{INT}$; DS1391/DS1393 $\overline{RST}$)	I_{OLSIR}	V_{CC} > 1.71V; V_{OL} = 0.4V			3.0	mA
		1.3V < V_{CC} < 1.71V; V_{OL} = 0.4V			250	µA
V_{CC} Active Supply Current (Note 10)	I_{CCA}	-33			2	mA
		-3			2	
		-18			500	µA

Recommended DC Operating Conditions (continued)

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at nominal supply voltage and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Standby Current (Note 11)	I_{CCS}	-33		115	175	µA
		-3		80	125	
		-18		60	100	
V_{BACKUP} Leakage Current (V_{BACKUP} = 3.7V, V_{CC} = $V_{CC(MAX)}$)	$I_{BACKUPLKG}$			15	100	nA

DC Electrical Characteristics

(V_{CC} = 0V, V_{BACKUP} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{BACKUP} Current OSC On, SQW Off	$I_{BACKUP1}$	(Note 12)		500	1000	nA
V_{BACKUP} Current OSC On, SQW On (32kHz)	$I_{BACKUP2}$	(Note 12)		600	1150	nA
V_{BACKUP} Current OSC On, SQW On, V_{BACKUP} = 3.0V, T_A = +25°C	$I_{BACKUP3}$	(Note 12)		600	1000	nA
V_{BACKUP} Current, OSC Off (Data Retention)	$I_{BACKUPDR}$	(Note 12)		25	100	nA

AC Electrical Characteristics—SPI Interface

(V_{CC} = 0V, V_{BACKUP} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SCLK Frequency (Note 13)	f_{SCLK}	2.7V ≤ V_{CC} ≤ 5.5V	0		4	MHz
		1.71V ≤ V_{CC} ≤ 1.89V	0		1	
Data to SCLK Setup	t_{DC}	(Notes 13, 14)	30			ns
SCLK to Data Hold	t_{CDH}	(Notes 13, 14)	30			ns
SCLK to Data Valid (Notes 13, 14, 15)	t_{CDD}	2.7V ≤ V_{CC} ≤ 5.5V			80	ns
		1.71V ≤ V_{CC} ≤ 1.89V			160	
SCLK Low Time (Note 13)	t_{CL}	2.7V ≤ V_{CC} ≤ 5.5V	110			ns
		1.71V ≤ V_{CC} ≤ 1.89V	400			
SCLK High Time (Note 13)	t_{CH}	2.7V ≤ V_{CC} ≤ 5.5V	110			ns
		1.71V ≤ V_{CC} ≤ 1.89V	400			
SCLK Rise and Fall	t_R, t_F				200	ns
$\overline{CS}$ to SCLK Setup (Note 13)	t_{CC}		400			ns
SCLK to CS Hold (Note 13)	t_{CCH}		100			ns
$\overline{CS}$ Inactive Time (Note 13)	t_{CWH}	2.7V ≤ V_{CC} ≤ 5.5V	400			ns
		1.71V ≤ V_{CC} ≤ 1.89V	500			
$\overline{CS}$ to Output High Impedance	t_{CDZ}	(Notes 13, 14)			40	ns

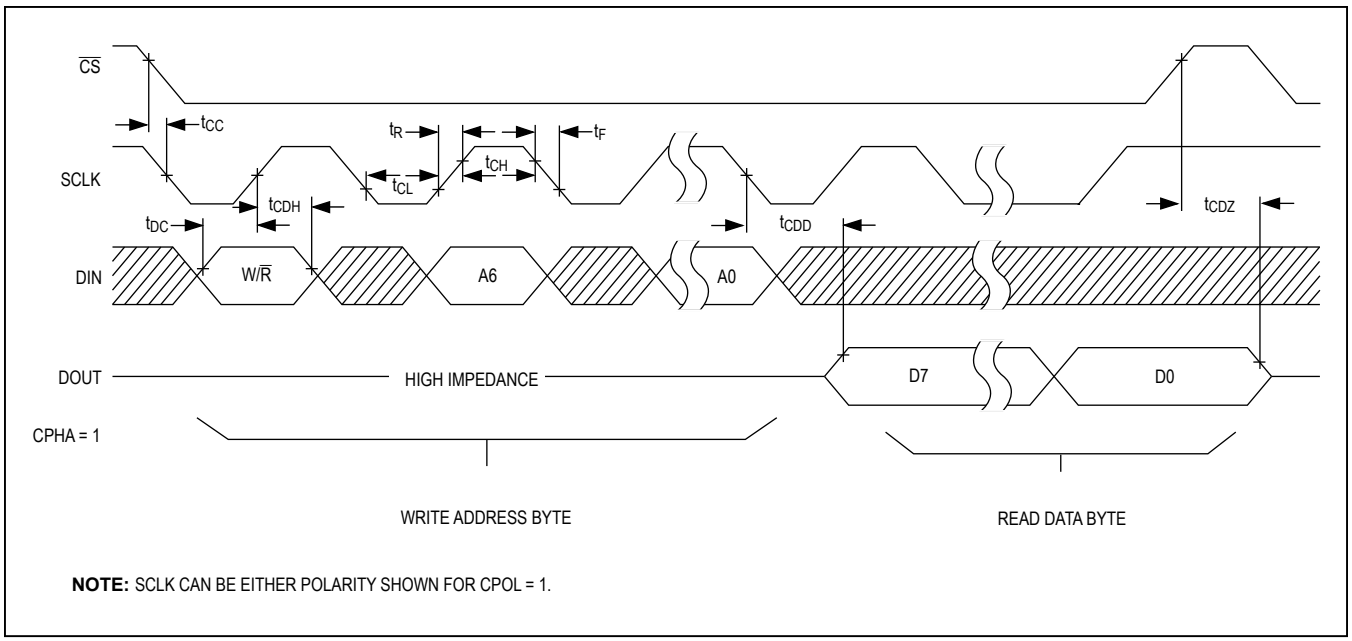


Figure 1a. Timing Diagram—SPI Read Transfer (Mode 3)

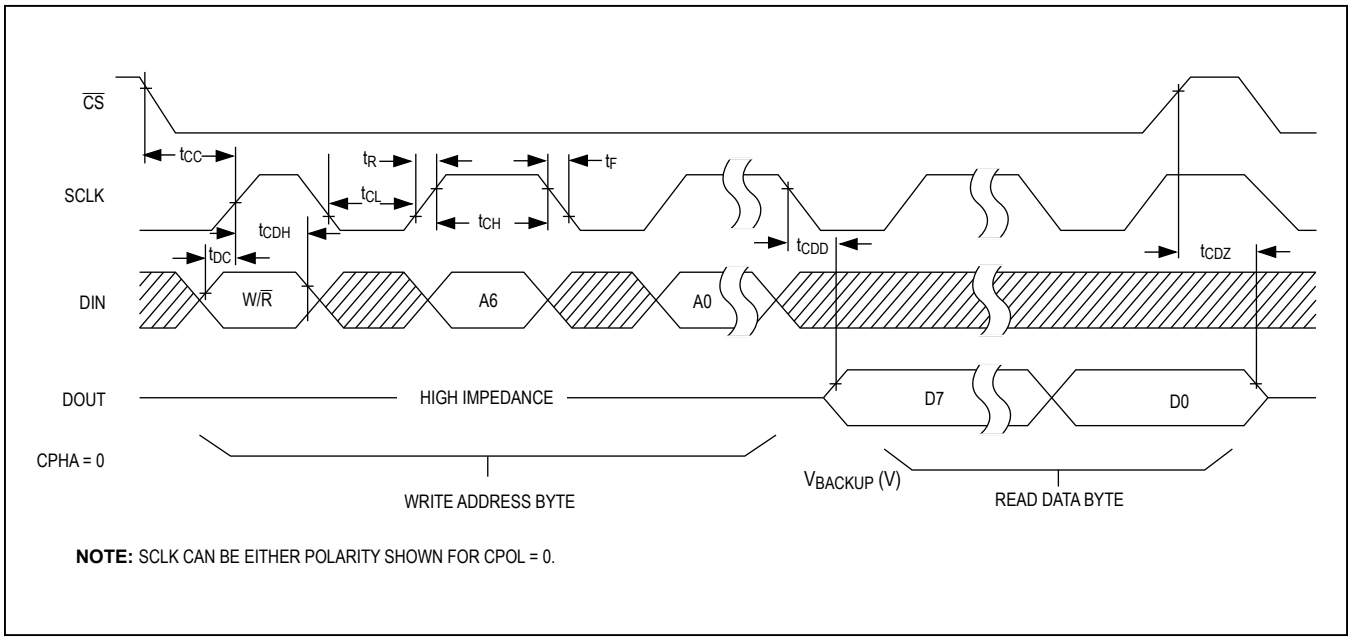


Figure 1b. Timing Diagram—SPI Read Transfer (Mode 0)

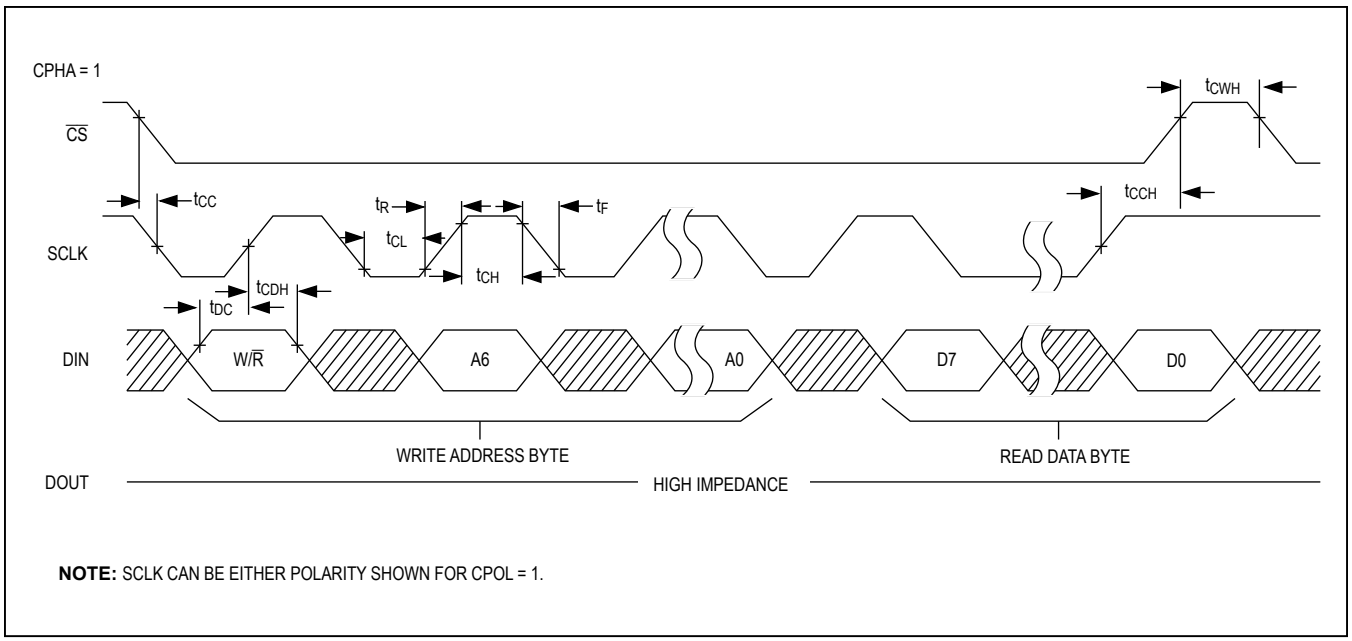


Figure 2a. Timing Diagram—SPI Write Transfer (Mode 3)

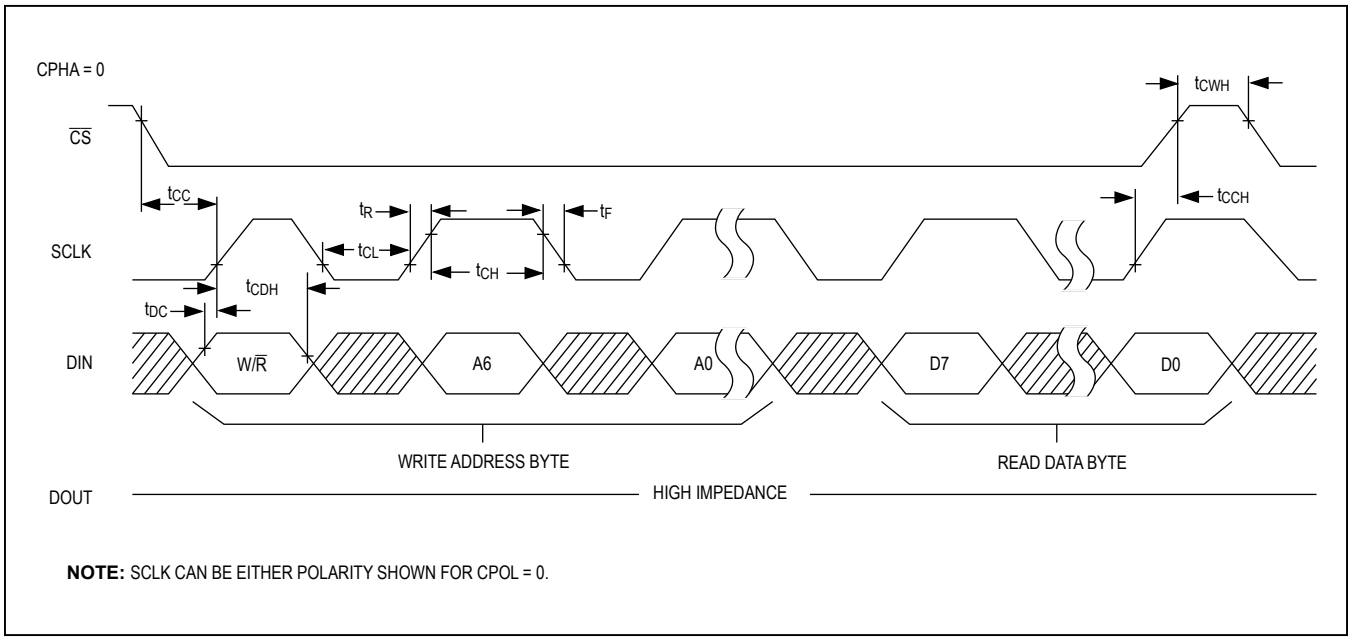


Figure 2b. Timing Diagram—SPI Write Transfer (Mode 0)

AC Electrical Characteristics—3-Wire Interface

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C.) (Note 1) (Figures 3, 4)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SCLK Frequency (Note 13)	f_{SCLK}	2.7V ≤ V_{CC} ≤ 5.5V	0		4	MHz
		1.71V ≤ V_{CC} ≤ 1.89V	0		1	
Data to SCLK Setup	t_{DC}	(Notes 13, 14)	30			ns
SCLK to Data Hold	t_{CDH}	(Notes 13, 14)	30			ns
SCLK to Data Valid (Notes 13, 14, 15)	t_{CDD}	2.7V ≤ V_{CC} ≤ 5.5V			80	ns
		1.71V ≤ V_{CC} ≤ 1.89V			160	
SCLK Low Time (Note 13)	t_{CL}	2.7V ≤ V_{CC} ≤ 5.5V	110			ns
		1.71V ≤ V_{CC} ≤ 1.89V	400			
SCLK High Time (Note 13)	t_{CH}	2.7V ≤ V_{CC} ≤ 5.5V	110			ns
		1.71V ≤ V_{CC} ≤ 1.89V	400			
SCLK Rise and Fall	t_R, t_F				200	ns
$\overline{CS}$ to SCLK Setup	t_{CC}	(Note 13)	400			ns
SCLK to $\overline{CS}$ Hold	t_{CCH}	(Note 13)	100			ns
$\overline{CS}$ Inactive Time (Note 13)	t_{CWH}	2.7V ≤ V_{CC} ≤ 5.5V	400			ns
		1.71V ≤ V_{CC} ≤ 1.89V	500			
$\overline{CS}$ to Output High Impedance	t_{CDZ}	(Note 13, 14)			40	ns

AC Electrical Characteristics

(V_{CC} = $V_{CC(MIN)}$ to $V_{CC(MAX)}$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Pushbutton Debounce	PB_{DB}			160	200	ms
Reset Active Time	t_{RST}			160	200	ms
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(Note 16)		100		ms

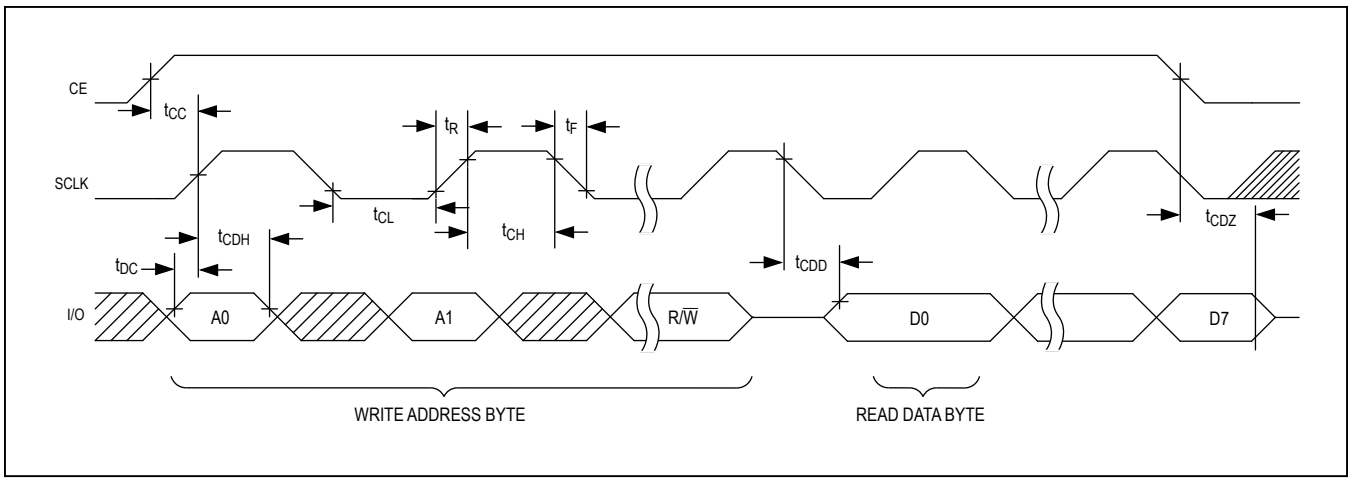


Figure 3. Timing Diagram—3-Wire Read Transfer

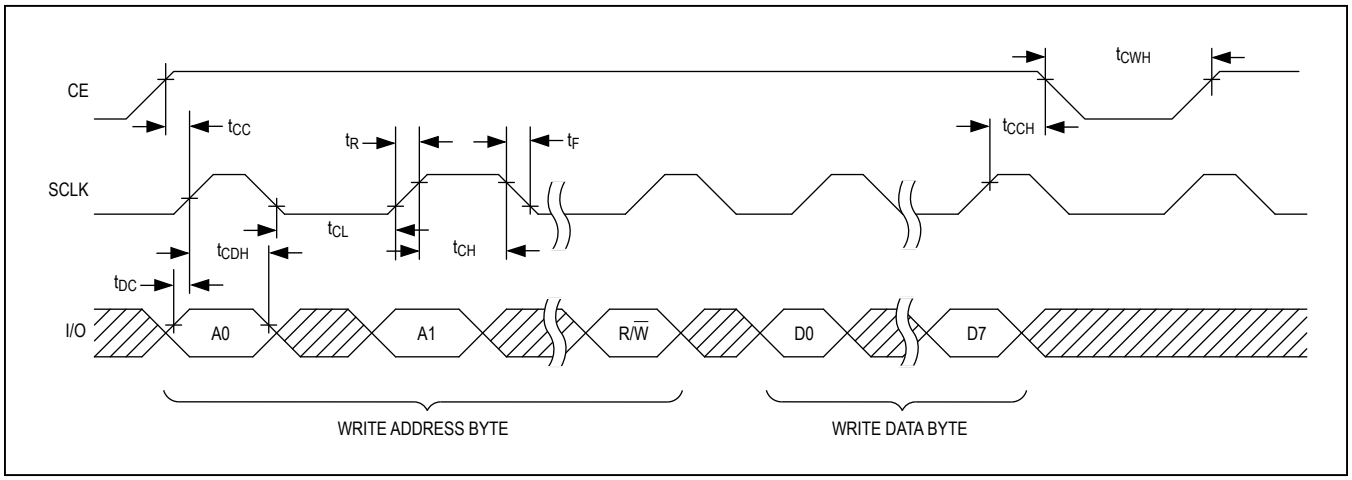


Figure 4. Timing Diagram—3-Wire Write Transfer

Power-Up/Power-Down Characteristics

(T_A = -40°C to +85°C) (Figures 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Detect to Recognize Inputs (V_{CC} Rising)	t_{RST}	(Note 17)		160	200	ms
V_{CC} Fall Time; $V_{PF(MAX)}$ to $V_{PF(MIN)}$	t_F		300			µs
V_{CC} Rise Time; $V_{PF(MIN)}$ to $V_{PF(MAX)}$	t_R		0			µs

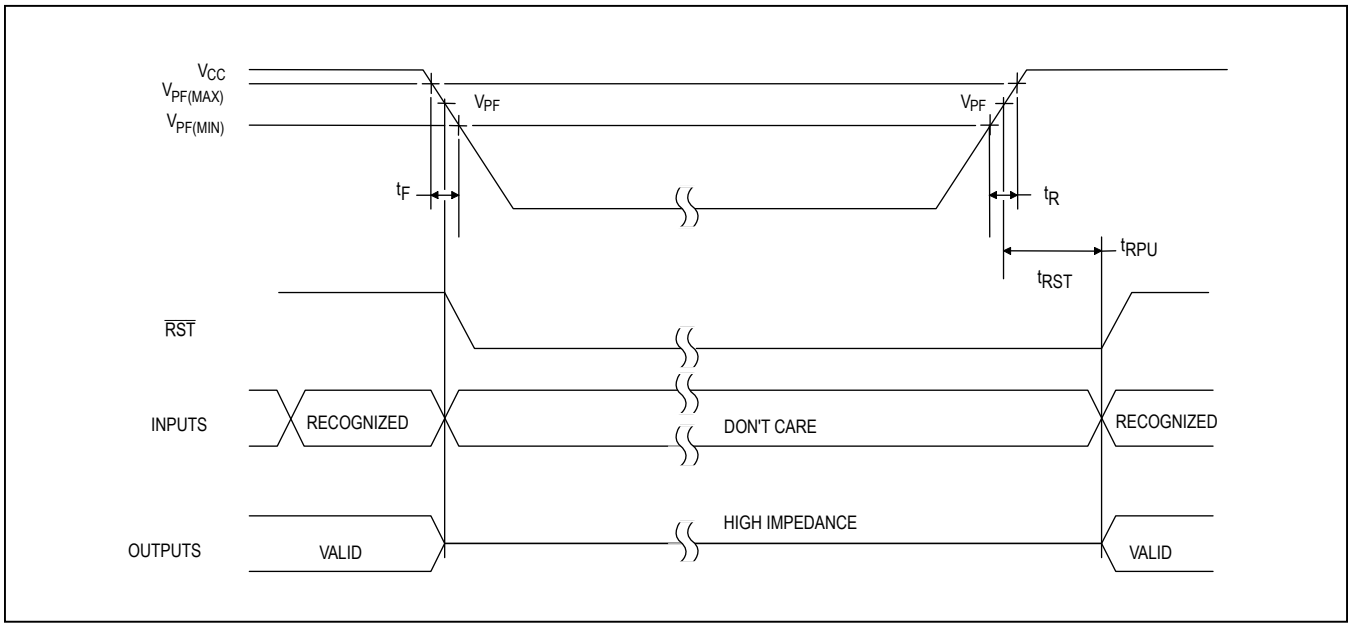


Figure 5. Power-Up/Down Timing

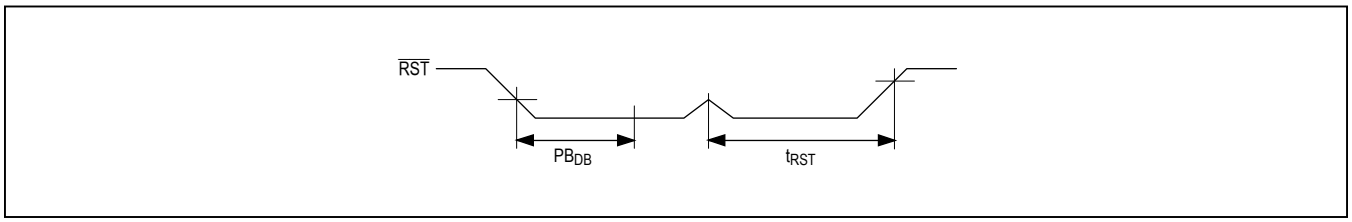


Figure 6. Pushbutton Reset Timing

Capacitance

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitance on All Input Pins	C_{IN}				10	pF
Capacitance on All Output Pins (High Impedance)	C_{IO}				10	pF

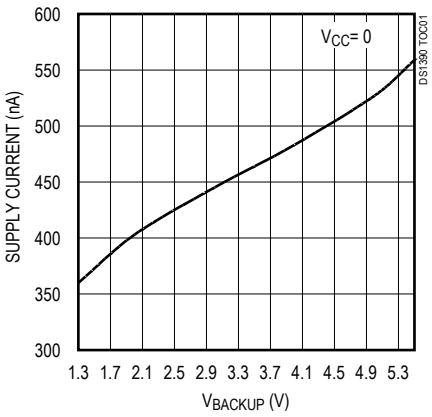
WARNING: Negative undershoots below -0.3V while the part is in battery-backed mode can cause loss of data.

Note 1: Limits at -40°C are guaranteed by design and not production tested.
Note 2: All voltages are referenced to ground.
Note 3: The use of the 250Ω trickle-charge resistor is not allowed at V_{CC} > 3.63V and should not be enabled. Use of the diode is not recommended for V_{CC} < 3.0V.
Note 4: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 0Fh = A5h.
Note 5: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 0Fh = A6h.
Note 6: Measured at V_{CC} = typ, V_{BACKUP} = 0V, register 0Fh = A7h.
Note 7: SCLK, DIN, $\overline{CS}$ on DS1390/DS1391/DS1394; SCLK, and CE on DS1392/DS1393.
Note 8: DOUT, SQW/$\overline{INT}$ (DS1390/DS1393/DS1394), SQW, and $\overline{INT}$ (DS1392).
Note 9: The RST pin has an internal 50kΩ (typ) pullup resistor to V_{CC}.
Note 10: I_{CCA}—SCLK clocking at max frequency = 4MHz for 3V and 3.3V versions; 1MHz for 1.8V version; RST (DS1391/DS1393) inactive. Outputs are open.
Note 11: Specified with bus inactive.
Note 12: Measured with a 32.768kHz crystal attached to X1 and X2. Typical values measured at +25°C and 3.0V_{BACKUP}.
Note 13: With 50pF load.
Note 14: Measured at V_{IH} = 0.7 x V_{DD} or V_{IL} = 0.2 x V_{DD}, 10ns rise/fall times.
Note 15: Measured at V_{OH} = 0.7 x V_{DD} or V_{OL} = 0.2 x V_{DD}. Measured from the 50% point of SCLK to the V_{OH} minimum of SDO.
Note 16: The parameter t_{OSF} is the time that the oscillator must be stopped for the OSF flag to be set over the voltage range of 0 ≤ V_{CC} ≤ $V_{CC(MAX)}$ and 1.3V ≤ V_{BACKUP} ≤ 5.5V.
Note 17: This delay applies only if the oscillator is enabled and running. If the $\overline{EOSC}$ bit is 1, the startup time of the oscillator is added to this delay.

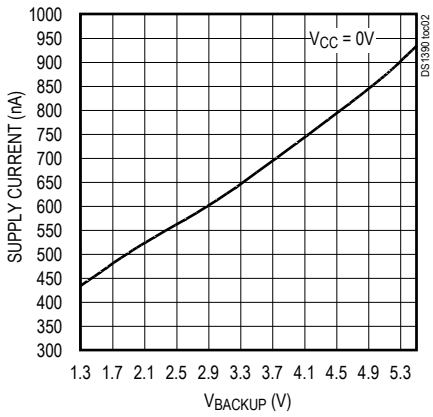
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

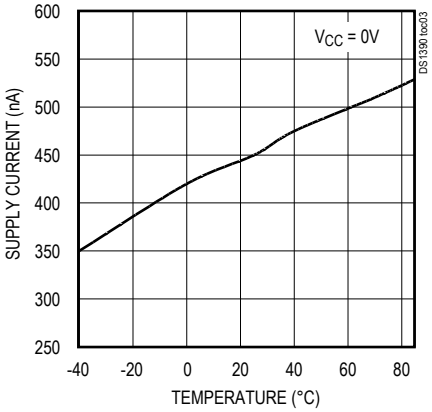
I_{BACKUP} vs. V_{BACKUP}, BBSQ1 = 0



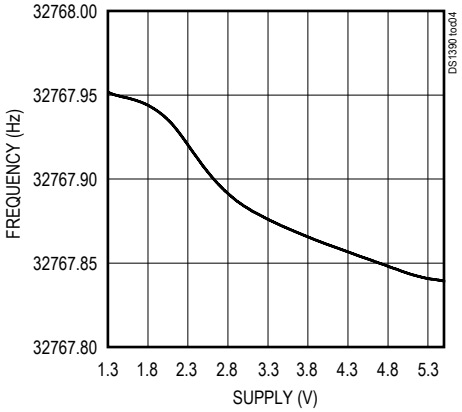
I_{BACKUP} vs. V_{BACKUP}, BBSQ1 = 1



I_{BACKUP} vs. TEMPERATURE
V_{BACKUP} = 3.0V

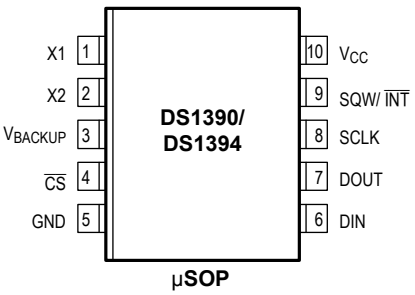


OSCILLATOR FREQUENCY
vs. SUPPLY VOLTAGE

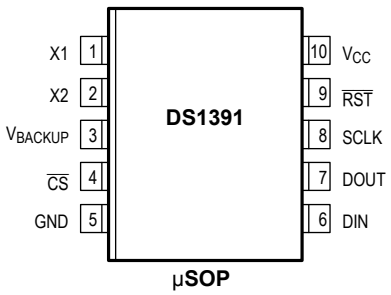


Pin Configurations

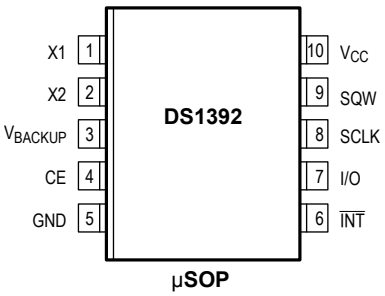
TOP VIEW



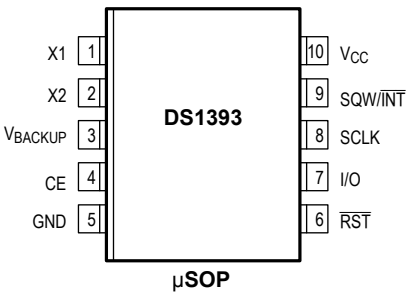
µSOP



µSOP



µSOP

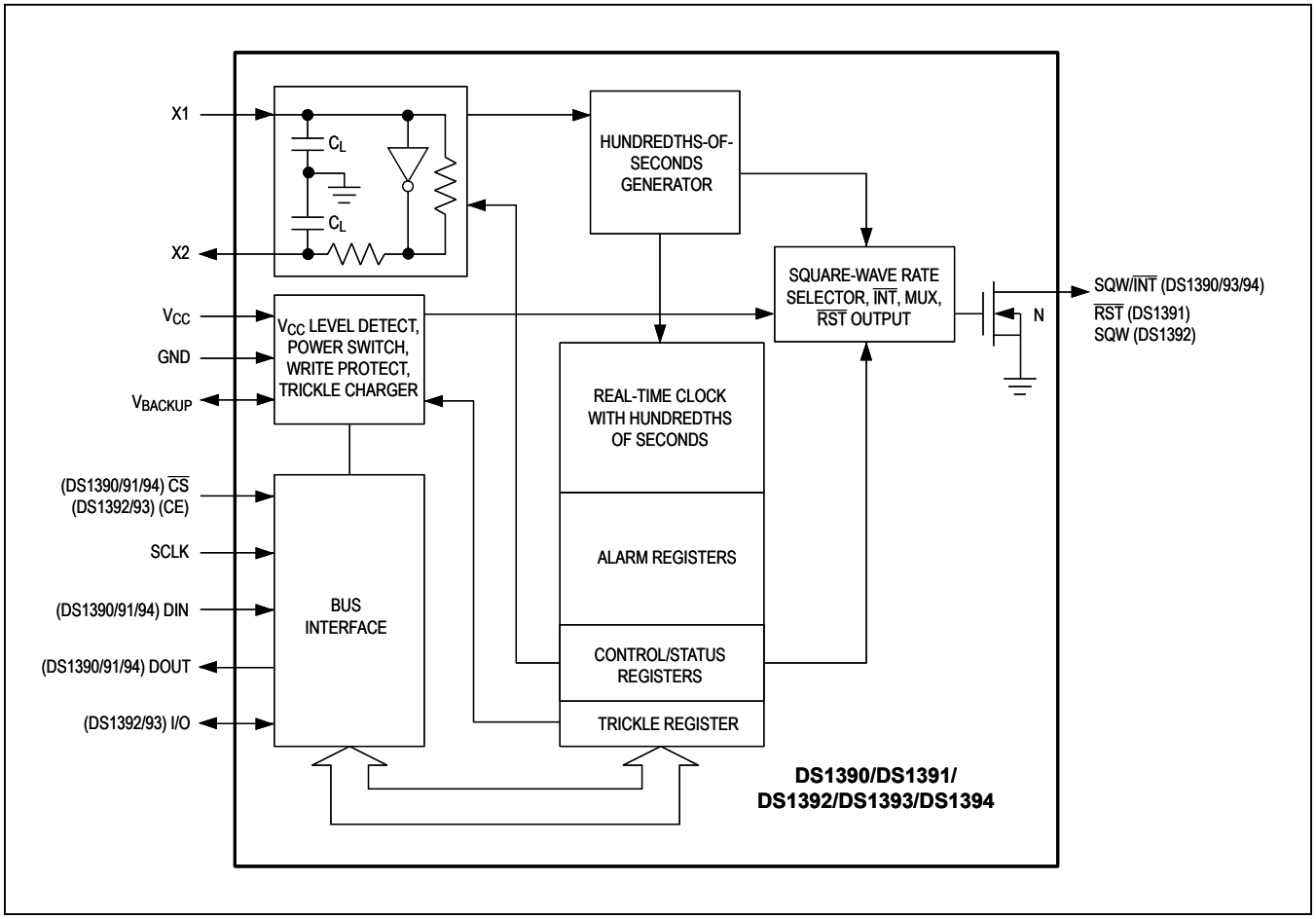


µSOP

Pin Description

PIN				NAME	FUNCTION
DS1390/ DS1394	DS1391	DS1392	DS1393		
1	1	1	1	X1	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator circuitry is designed for operation with a crystal having a 6pF specified load capacitance (C_L). Pin X1 is the input to the oscillator and can optionally be connected to an external 32.768kHz oscillator. The output of the internal oscillator, pin X2, is floated if an external oscillator is connected to pin X1.
2	2	2	2	X2	
3	3	3	3	V_{BACKUP}	DC Backup Power Input for Primary Cell. This pin is a rechargeable battery/ super cap or a secondary supply. UL recognized to ensure against reverse charging current when used with a lithium battery (http://www.maximintegrated.com/qa/info/w/). This pin must be grounded if not used. Diodes in series between the battery and the V_{BACKUP} pin may prevent proper operation.
4	4	—	—	$\overline{CS}$	SPI Chip-Select Input. This pin is used to select or deselect the part.
—	—	4	4	CE	Chip Enable for 3-Wire Interface
5	5	5	5	GND	Ground
6	6	—	—	DIN	SPI Data Input. This pin is used to shift address and data into the part.
—	—	6	—	$\overline{INT}$	Interrupt Output. This pin is used to output the interrupt signal, if enabled by the control register. The maximum voltage on this pin is 5.5V, independent of V_{CC} or V_{BACKUP}. If enabled, $\overline{INT}$ functions when the device is powered by either V_{CC} or V_{BACKUP}.
—	9	—	6	$\overline{RST}$	Reset. This active-low, open-drain output indicates the status of V_{CC} relative to the V_{PF} specification. As V_{CC} falls below V_{PF}, the $\overline{RST}$ pin is driven low. When V_{CC} exceeds V_{PF}, for t_{RST}, the $\overline{RST}$ pin is driven high impedance. This pin is combined with a debounced pushbutton input function. This pin can be activated by a pushbutton reset request. This pin has an internal, 50kΩ (typ) pullup resistor to V_{CC}. No external pullup resistors should be connected. If the crystal oscillator is disabled, the startup time of the oscillator is added to the t_{RST} delay.
7	7	—	—	DOUT	SPI Data Output. Data is output on this pin when the part is in read mode. CMOS push-pull driver.
—	—	7	7	I/O	Input/Output for 3-Wire Interface. CMOS push-pull driver.
8	8	8	8	SCLK	Serial Clock Input. This pin is used to control the timing of data into and out of the part.
9	—	—	9	SQW/$\overline{INT}$	Square-Wave/Interrupt Output. This pin is used to output the programmable square wave or interrupt signal. When enabled by setting the $\overline{ESQW}$ bit to logic 1, the SQW/$\overline{INT}$ pin outputs one of four frequencies: 32.768kHz, 8.192kHz, 4.096kHz, or 1Hz. This pin is open drain and requires an external pullup resistor. The maximum voltage on this pin is 5.5V, independent of V_{CC} or V_{BACKUP}. If enabled, SQW/$\overline{INT}$ functions when the device is powered by either V_{CC} or V_{BACKUP}. If not used, this pin can be left open.
—	—	9	—	SQW	Square-Wave Output. This pin is open drain and requires an external pullup resistor. The maximum voltage on this pin is 5.5V, independent of V_{CC} or V_{BACKUP}. If enabled, SQW functions when the device is powered by either V_{CC} or V_{BACKUP}. If not used, this pin can be left open.
10	10	10	10	V_{CC}	DC Power Pin for Primary Power Supply

Functional Diagram



Detailed Description

The DS1390–DS1394 RTCs are low-power clocks/calendars with alarms. Address and data are transferred serially through a 4-wire SPI interface for the DS1390 and DS1391 and through a 3-wire interface for the DS1392, DS1393, and DS1394. The DS1390/DS1391 operate as a slave device on the SPI serial bus. The DS1392/DS1393 operate using a 3-wire synchronous serial bus. Access is obtained by selecting the part by the $\overline{CS}$ pin (CE on DS1392/DS1393) and clocking data into/out of the part using the SCLK and DIN/DOUT pins (I/O on DS1392/DS1393). Multiple-byte transfers are supported within one $\overline{CS}$ low period (see the *SPI Serial-Data Bus* section).

The clocks/calendars provide hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The alarm functions are performed off all timekeeping registers, allowing the user to set high resolution alarms. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clocks operate in either the 24-hour or 12-hour format with an AM/PM indicator. All five devices have a built-in temperature-compensated voltage reference that detects power failures and automatically switches to the battery supply. Additionally, the devices can provide trickle charging of the backup voltage source, with selectable charging resistance and diode voltage drops.

Power Control

The power-control function is provided by a precise, temperature-compensated voltage reference and a comparator circuit that monitors the V_{CC} level. The device is fully accessible and data can be written and read when V_{CC} is greater than V_{PF}. However, when V_{CC} falls below V_{PF}, the internal clock registers are blocked from any access. If V_{PF} is less than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{PF}. If V_{PF} is greater than V_{BACKUP}, the device power is switched from V_{CC} to V_{BACKUP} when V_{CC} drops below V_{BACKUP}. Timekeeping operation and register data are maintained from the V_{BACKUP} source until V_{CC} is returned to nominal levels (Table 1). After V_{CC} returns above V_{PF}, read and write access is allowed after $\overline{RST}$ goes high (Figure 5).

Table 1. Power Control

SUPPLY CONDITION	READ/WRITE ACCESS)	POWERED BY
$V_{CC} < V_{PF}$, $V_{CC} < V_{BACKUP}$	No	V_{BACKUP}
$V_{CC} < V_{PF}$, $V_{CC} > V_{BACKUP}$	No	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} < V_{BACKUP}$	Yes	V_{CC}
$V_{CC} > V_{PF}$, $V_{CC} > V_{BACKUP}$	Yes	V_{CC}

Oscillator Circuit

All five devices use an external 32.768kHz crystal. The oscillator circuit does not require any external resistors or capacitors to operate. Table 2 specifies several crystal parameters for the external crystal. If a crystal is used with the specified characteristics, the startup time is usually less than one second.

Table 2. Crystal Specifications*

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Nominal Frequency	f_O		32.768		kHz
Series Resistance	ESR			55	kΩ
Load Capacitance	C_L		6		pF

**The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58: Crystal Considerations for Maxim Real-Time Clocks for additional specifications.*

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Figure 7 shows a typical PC board layout for isolation of the crystal and oscillator from noise. Refer to Application Note 58: *Crystal Considerations with Maxim Real-Time Clocks* for detailed information.

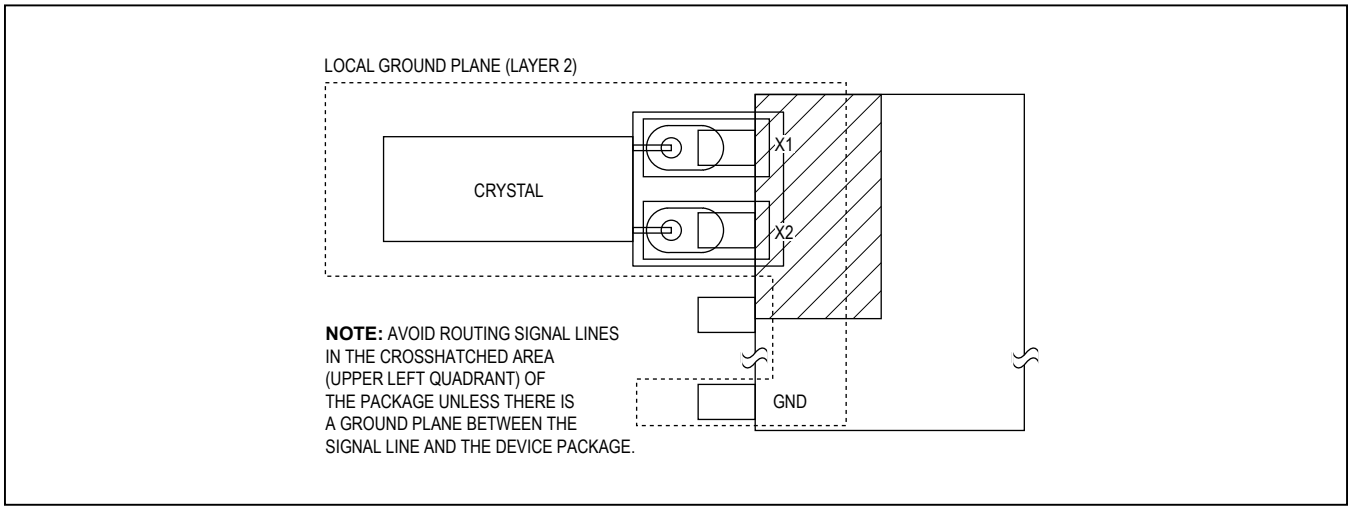


Figure 7. Layout Example

Address Map

Table 3 shows the address map for the DS1390–DS1393 RTC and RAM registers. The RTC registers are located in address locations 00h to 0Fh in read mode, and 80h to 8Fh in write mode. During a multibyte access, when the address pointer reaches 0Fh, it wraps around to location 00h. On the falling edge of the $\overline{CS}$ pin (DS1390/DS1391/DS1394) or the rising edge of CE (DS1392/DS1393), the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers if the main registers update during a read. To avoid rollover issues when writing to the time and date registers, all registers should be written before the hundredths-of-seconds registers reaches 99 (BCD).

When reading from the hundredths of seconds register, there is a possibility that the data transfer happens at the same time as an increment of the register. If this occurs, the data in the buffer may be incorrect. The chances of this happening is approximately 170ppb. There are two ways to deal with this.

The first method is to synchronize enabling the device (CE or $\overline{CS}$) with the square wave or interrupt output (DS1390–DS1394). Enabling the device, either after detecting the falling edge of the interrupt output or the rising edge of the square-wave output, ensures that the two events are not simultaneous.

The second method is to read the hundredths of seconds register until the data for two consecutive reads match. With this method, the master must be able to read the register at least twice within the 10ms update period of the hundredths of seconds register.

Either of the described methods ensures that the data in all the registers is correct. If the hundredths of seconds register is not used, it is also possible for the same problem to occur when reading the seconds register. The probability of an error is inversely proportional to the rate of the register's update frequency in relation to the hundredth of seconds register, so the error rate for the seconds register would be approximately 1.7ppb. The same methods used for the hundredth of seconds register would be used for the seconds register.

Table 3. Address Map

WRITE ADDRESS	READ ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
80h	00h	Tenths of Seconds				Hundredths of Seconds				Hundredths of Seconds	0–99 BCD
81h	01h	0	10 Seconds			Seconds				Seconds	00–59 BCD
82h	02h	0	10 Minutes			Minutes				Minutes	00–59 BCD
83h	03h	0	12/$\overline{24}$	$\overline{AM}$/PM 10 Hour	10 Hour	Hour				Hours	1–12 +AM/PM 00–23 BCD
84h	04h	0	0	0	0	0	Day			Day	1–7 BCD
85h	05h	0	0	10 Date		Date				Date	01–31 BCD
86h	06h	Century	0	0	10 Month	Month				Month/ Century	01–12 + Century BCD
87h	07h	10 Year				Year				Year	00–99 BCD
88h	08h	Tenths of Seconds				Hundredths of Seconds				Alarm Hundredths of Seconds	0–99 BCD
89h	09h	AM1	10 Seconds			Seconds				Alarm Seconds	00–59 BCD
8Ah	0Ah	AM2	10 Minutes			Minutes				Alarm Minutes	00–59 BCD

Table 3. Address Map (continued)

WRITE ADDRESS	READ ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FUNCTION	RANGE
8Bh	0Bh	AM3	12/$\overline{24}$	$\overline{AM}$/PM	10 Hour	Hour				Alarm Hours	1–12 + AM/PM 00–23 BCD
				10 Hour							
8Ch	0Ch	AM4	DY/$\overline{DT}$	10 Date		Day				Alarm Day	1–7 BCD
						Date				Alarm Date	01–31 BCD
8Dh	0Dh	$\overline{EOSC}$	0	BBSQI	RS2	RS1	INTCN	0	AIE	Control	DS1390/93/94
			0	X	X	X	X	0	X		DS1391
			0	BBSQI	RS2	RS1	$\overline{ESQW}$	0	AIE		DS1392
8Eh	0Eh	OSF	0	0	0	0	0	0	AF	Status	—
8Fh	0Fh	TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	Trickle Charger	—

Note: *Unless otherwise specified, the state of the registers is not defined when power (V_{CC} and V_{BACKUP}) is first applied.*
X = General-purpose read/write bit.
0 = Always reads as zero.

Hundredths-of-Seconds Generator

The hundredths-of-seconds generator circuit shown in the functional diagram is a state machine that divides the incoming frequency (4096Hz) by 41 for 24 cycles and 40 for one cycle. This produces a 100Hz output that is slightly off during the short term, and is exactly correct every 250ms. The divide ratio is given by:

Ratio = [41 x 24 + 40 x 1] / 25 = 40.96

Thus, the long-term average frequency output is exactly the desired 100Hz.

Clock and Calendar

The time and calendar information is obtained by reading the appropriate register bytes. See Table 3 for the RTC registers. The time and calendar are set or initialized by writing the appropriate register bytes. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The day-of-week register increments at midnight. Values that correspond to the day-of-week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. The DS1390–DS1393 can run in either 12-hour or 24-hour mode. Bit 6 of the hours register is defined as the 12- or 24-hour mode-select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the $\overline{AM}$/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20 to 23 hours). Changing the 12/$\overline{24}$-hour mode-select bit requires that the hours data be re-entered, including the alarm register (if used). The century bit (bit 7 of the month register) is toggled when the years register overflows from 99 to 00.

Alarms

All five devices contain one time-of-day/date alarm. Writing to registers 88h through 8Ch sets the alarm. The alarm can be programmed (by the alarm enable and INTCN bits of the control register) to activate the SQW/$\overline{INT}$ or $\overline{INT}$ output on an alarm-match condition. The alarm can activate the SQW/$\overline{INT}$ or $\overline{INT}$ output while the device is running from V_{BACKUP} if BBSQI is enabled. Bit 7 of each of the time-of-day/date alarm registers are mask bits (Table 4). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers 00h to 06h match the values stored in the time-of-day/date alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. Table 4 shows the possible settings. Configurations not listed in the table result in illogical operation.

The DY/$\overline{DT}$ bits (bit 6 of the alarm day/date registers) control whether the alarm value stored in bits 0 to 5 of that register reflects the day of the week or the date of the month. If DY/$\overline{DT}$ is written to logic 0, the alarm is the result of a match with date of the month. If DY/$\overline{DT}$ is written to a logic 1, the alarm is the result of a match with day of the week.

When the RTC register values match alarm register settings, the alarm-flag (AF) bit is set to logic 1. If the alarm-interrupt enable (AIE) is also set to logic 1 and the INTCN bit is set to logic 1, the alarm condition activates the SQW/$\overline{INT}$ signal.

Since the contents of register 08h are expected to normally contain a match value of 00–99 decimal, the codes F[0–9], and FF have been used to tell the part to mask the tenths or hundredths of seconds accordingly.

Power-Up/Down, Reset, and Pushbutton Reset Functions

A precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power-fail signal is generated that blocks read/write access to the device and forces the $\overline{RST}$ pin (DS1391/DS1393 only) low. When V_{CC} returns to an in-tolerance condition, the internal power-fail signal is held active for t_{RST} to allow the power supply to stabilize, and the $\overline{RST}$ (DS1391/DS1393 only) pin is held low. If the $\overline{EOSC}$ bit is set to logic 1 (to disable the oscillator in battery-backup mode), the internal power-fail signal and the $\overline{RST}$ pin is kept active for t_{RST} plus the startup time of the oscillator.

The DS1391/DS1393 provide for a pushbutton switch to be connected to the $\overline{RST}$ output pin. When the DS1391/DS1393 are not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low-going edge. If an edge is detected, the part debounces the switch by pulling the $\overline{RST}$ pin low and inhibits read/write access. After PB_{DB} has expired, the part continues to monitor the $\overline{RST}$ line. If the line is still low, it continues to monitor the line looking for a rising edge. Upon detecting release, the part forces the $\overline{RST}$ pin low and holds it low for an additional PB_{DB}.

Table 4. Alarm Mask Bits

REGISTER 08H	DY/$\overline{DT}$	ALARM REGISTER MASK BITS (BIT 7)				ALARM RATE
		AM4	AM3	AM2	AM1	
FFh	X	1	1	1	1	Alarm every 1/100th of a second
F[0–9]h	X	1	1	1	1	Alarm when hundredths of seconds match
[0–9][0–9]	X	1	1	1	1	Alarm when tenths, hundredths of seconds match
[0–9][0–9]	X	1	1	1	0	Alarm when seconds, tenths, and hundredths of seconds match
[0–9][0–9]	X	1	1	0	0	Alarm when minutes, seconds, tenths, and hundredths of seconds match
[0–9][0–9]	X	1	0	0	0	Alarm when hours, minutes, seconds, tenths, and hundredths of seconds match
[0–9][0–9]	0	0	0	0	0	Alarm when date, hours, minutes, seconds, tenths, and hundredths of seconds match
[0–9][0–9]	1	0	0	0	0	Alarm when day, hours, minutes, seconds, tenths, and hundredths of seconds match

Special-Purpose Registers

The DS1390–DS1394 have three additional registers (control, status, and trickle charger) that control the RTC, alarms, square-wave output, and trickle charger.

Control Register (0D/8Dh) (DS1390/DS1393/DS1394 Only)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{EOSC}$	0	BBSQI	RS2	RS1	INTCN	0	AIE

Bit 7: Enable Oscillator ($\overline{EOSC}$). When set to logic 0, this bit starts the oscillator. When this bit is set to logic 1, the oscillator is stopped whenever the device is powered by V_{BACKUP}. The oscillator is always enabled when V_{CC} is valid. This bit is enabled (logic 0) when V_{CC} is first applied.

Bit 5: Battery-Backed Square-Wave and Interrupt Enable (BBSQI). This bit when set to logic 1 enables the square wave or interrupt output when V_{CC} is absent and the DS1390/DS1392/DS1393/DS1394 are being powered by the V_{BACKUP} pin. When BBSQI is logic 0, the SQW/$\overline{INT}$ pin (or SQW and $\overline{INT}$ pins) goes high impedance when V_{CC} falls below the power-fail trip point. This bit is disabled (logic 0) when power is first applied.

Bits 4 and 3: Rate Select (RS2 and RS1). These bits control the frequency of the square-wave output when the square wave has been enabled. The table below shows the square-wave frequencies that can be selected with the RS bits. These bits are both set to logic 1 (32kHz) when power is first applied.

RS2	RS1	SQUARE-WAVE OUTPUT FREQUENCY
0	0	1Hz
0	1	4.096kHz
1	0	8.192kHz
1	1	32.768kHz

Bit 2: Interrupt Control (INTCN). This bit controls the SQW/$\overline{INT}$ signal. When the INTCN bit is set to logic 0, a square wave is output on the SQW/$\overline{INT}$ pin. The oscillator must also be enabled for the square wave to be out-put. When the INTCN bit is set to logic 1, a match between the timekeeping registers and either of the alarm registers then activates the SQW/$\overline{INT}$ (provided the alarm is also enabled). The corresponding alarm flag is always set, regardless of the state of the INTCN bit. The INTCN bit is set to logic 0 when power is first applied.

Bit 0: Alarm Interrupt Enable (AIE). When set to logic 1, this bit permits the alarm flag (AF) bit in the status register to assert SQW/$\overline{INT}$ (when INTCN = 1). When the AIE bit is set to logic 0 or INTCN is set to logic 0, the AF bit does not initiate the SQW/$\overline{INT}$ signal. The AIE bit is disabled (logic 0) when power is first applied.

Control Register (0D/8Dh) (DS1391 Only)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{EOSC}$	0	X	X	X	X	0	X

Control bits used in the DS1390 become general-purpose, battery-backed, nonvolatile SRAM bits in the DS1391.

Control Register (0D/8Dh) (DS1392 Only)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{EOSC}$	0	BBSQI	RS2	RS1	$\overline{ESQW}$	0	AIE

The INTCN bit used in the DS1390/DS1393/DS1394 becomes the SQW pin-enable bit in the DS1392. This bit powers up a zero, making SQW active.

Status Register (0E/8Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
OSF	0	0	0	0	0	0	AF

Bit 7: Oscillator Stop Flag (OSF). A logic 1 in this bit indicates that the oscillator has stopped or was stopped for some time and may be used to judge the validity of the clock and calendar data. This bit is edge-triggered and is set to logic 1 when the internal circuitry senses the oscillator has transitioned from a normal run state to a STOP condition. The following are examples of conditions that can cause the OSF bit to be set:

1) The first time power is applied.
2) The voltage present on V_{CC} and V_{BACKUP} is insufficient to support oscillation.
3) The $\overline{EOSC}$ bit is turned off.
4) External influences on the crystal (i.e., noise, leakage, etc.).

This bit remains at logic 1 until written to logic 0. This bit can only be written to logic 0. Attempting to write OSF to logic 1 leaves the value unchanged.

Bit 0: Alarm Flag (AF). A logic 1 in the AF bit indicates that the time matched the alarm registers. If the AIE bit is logic 1 and the INTCN bit is set to logic 1, the SQW/$\overline{INT}$ pin is also asserted. AF is cleared when written to logic 0. This bit can only be written to logic 0. Attempting to write to logic 1 leaves the value unchanged.

Trickle-Charge Register (0F/8Fh)

The simplified schematic in Figure 8 shows the basic components of the trickle charger. The trickle-charge select (TCS) bits (bits 4 to 7) control the selection of the trickle charger. To prevent accidental enabling, only a pattern on 1010 enables the trickle charger. All other patterns disable the trickle charger. The trickle charger is disabled when power is first applied. The diode-select (DS) bits (bits 2 and 3) select whether or not a diode is connected between V_{CC} and V_{BACKUP}. If DS is 01, no diode is selected or if DS is 10, a diode is selected. The ROUT bits (bits 0 and 1) select the value of the resistor connected between V_{CC} and V_{BACKUP}. Table 5 shows the resistor selected by the resistor-select (ROUT) bits and the diode selected by the diode-select (DS) bits.

Table 5. Trickle-Charge Register

TCS3	TCS2	TCS1	TCS0	DS1	DS0	ROUT1	ROUT0	FUNCTION
X	X	X	X	0	0	X	X	Disabled
X	X	X	X	1	1	X	X	Disabled
X	X	X	X	X	X	0	0	Disabled
1	0	1	0	0	1	0	1	No diode, 250Ω resistor
1	0	1	0	1	0	0	1	One diode, 250Ω resistor
1	0	1	0	0	1	1	0	No diode, 2kΩ resistor
1	0	1	0	1	0	1	0	One diode, 2kΩ resistor
1	0	1	0	0	1	1	1	No diode, 4kΩ resistor
1	0	1	0	1	0	1	1	One diode, 4kΩ resistor
0	0	0	0	0	0	0	0	Initial default value—disabled

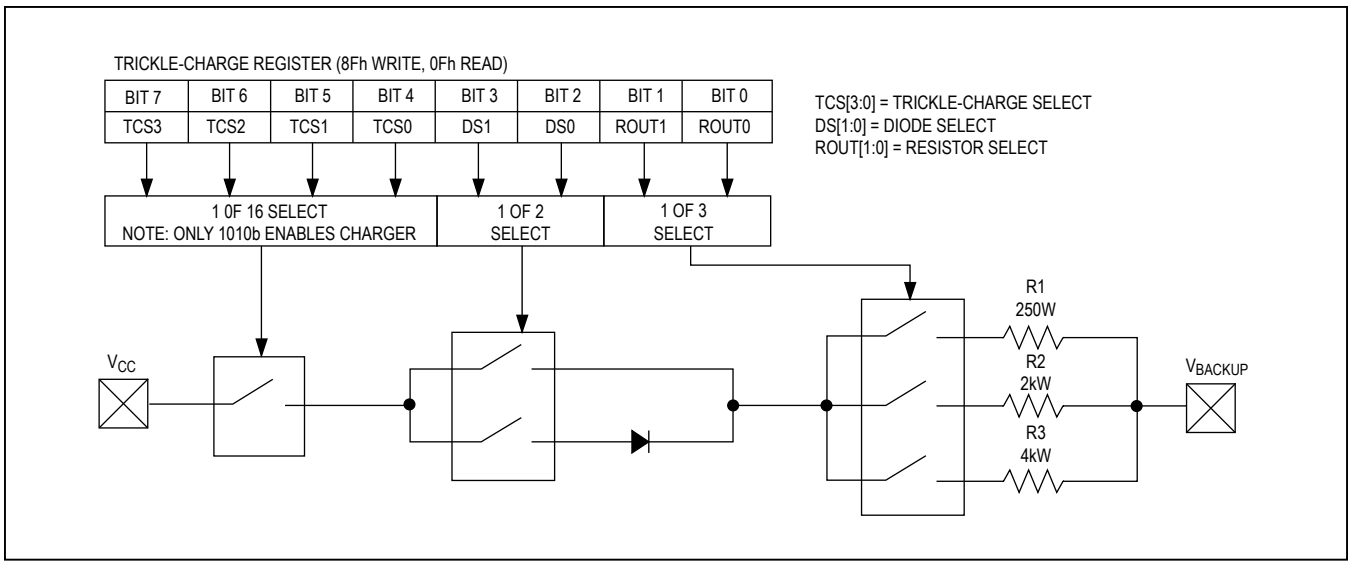


Figure 8. DS1390–DS1394 Programmable Trickle Charger

Table 6. SPI Pin Function

MODE	CPHA	CS	SCLK	SDI	SDO
Disable	X	High	Input Disabled	Input Disabled	High-Z
Write	0	Low	CPOL* = 0, SCLK Rising; CPOL = 1, SCLK Falling	Data Bit Latch	High-Z
Read	0	Low	CPOL = 0, SCLK Falling; CPOL = 1, SCLK Rising	X	Next Data Bit Shift**
Write	1	Low	CPOL* = 1, SCLK Rising; CPOL = 0, SCLK Falling	Data Bit Latch	High-Z
Read	1	Low	CPOL = 1, SCLK Falling; CPOL = 0, SCLK Rising	X	Next Data Bit Shift**

**CPOL is the clock-polarity bit set in the control register of the host microprocessor.*
***SDO remains at high-Z until 8 bits of data are ready to be shifted out during a read.*

The user determines diode and resistor selection according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 3.3V is applied to V_{CC} and a super cap is connected to V_{BACKUP}. Also, assume that the trickle charger has been enabled with a diode and resistor R2 between V_{CC} and V_{BACKUP}. The maximum current I_{MAX} would therefore be calculated as follows:

$$I_{MAX} = (3.3V - \text{diode drop}) / R2 \approx (3.3V - 0.7V) / 2k\Omega \approx 1.3mA$$

As the super cap changes, the voltage drop between V_{CC} and V_{BACKUP} decreases and therefore the charge current decreases.

SPI Serial-Data Bus

The DS1390/DS1391/DS1394 provide a 4-wire SPI serial-data bus to communicate in systems with an SPI host controller. The DS1390/DS1391 support SPI modes 1 and 3, while the DS1394 supports SPI modes 0 and 2. Both devices support single-byte and multiple-byte data transfers for maximum flexibility. The DIN and DOUT pins are the serial-data input and output pins, respectively. The $\overline{CS}$ input initiates and terminates a data transfer. The SCLK pin synchronizes data movement between the master (microcontroller) and the slave (DS1390/DS1391) devices. The shift clock (SCLK), which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus. Input data (DIN) is latched on the internal strobe edge and output data (DOUT) is shifted out on the shift edge (Figure 9). There is one clock for each bit transferred. Address and data bits are transferred in groups of eight.

Address and data bytes are shifted MSB first into the serial-data input (DIN) and out of the serial-data output (DOUT). Any transfer requires the address of the byte to specify a write or read, followed by one or more bytes of data. Data is transferred out of the DOUT pin for a read operation and into the DIN for a write operation (Figures 10 and 11).

The address byte is always the first byte entered after $\overline{CS}$ is driven low. The most significant bit (W/$\overline{R}$) of this byte determines if a read or write takes place. If W/$\overline{R}$ is 0, one or more read cycles occur. If W/$\overline{R}$ is 1, one or more write cycles occur.

Data transfers can occur one byte at a time or in multiple-byte burst mode. After $\overline{CS}$ is driven low, an address is written to the DS1390/DS1391/DS1394. After the address, one or more data bytes can be written or read. For a single-byte transfer, one byte is read or written and then $\overline{CS}$ is driven high. For a multiple-byte transfer, however, multiple bytes can be read or written after the address has been written. Each read or write cycle causes the RTC register address to automatically increment. Incrementing continues until the device is disabled. The address wraps to 00h after incrementing to 0Fh (during a read) and wraps to 80h after incrementing to 8Fh (during a write). Note, however, that an updated copy of the time is only loaded into the user-accessible copy upon the falling edge of $\overline{CS}$. Reading the RTC registers in a continuous loop does not show the time advancing.

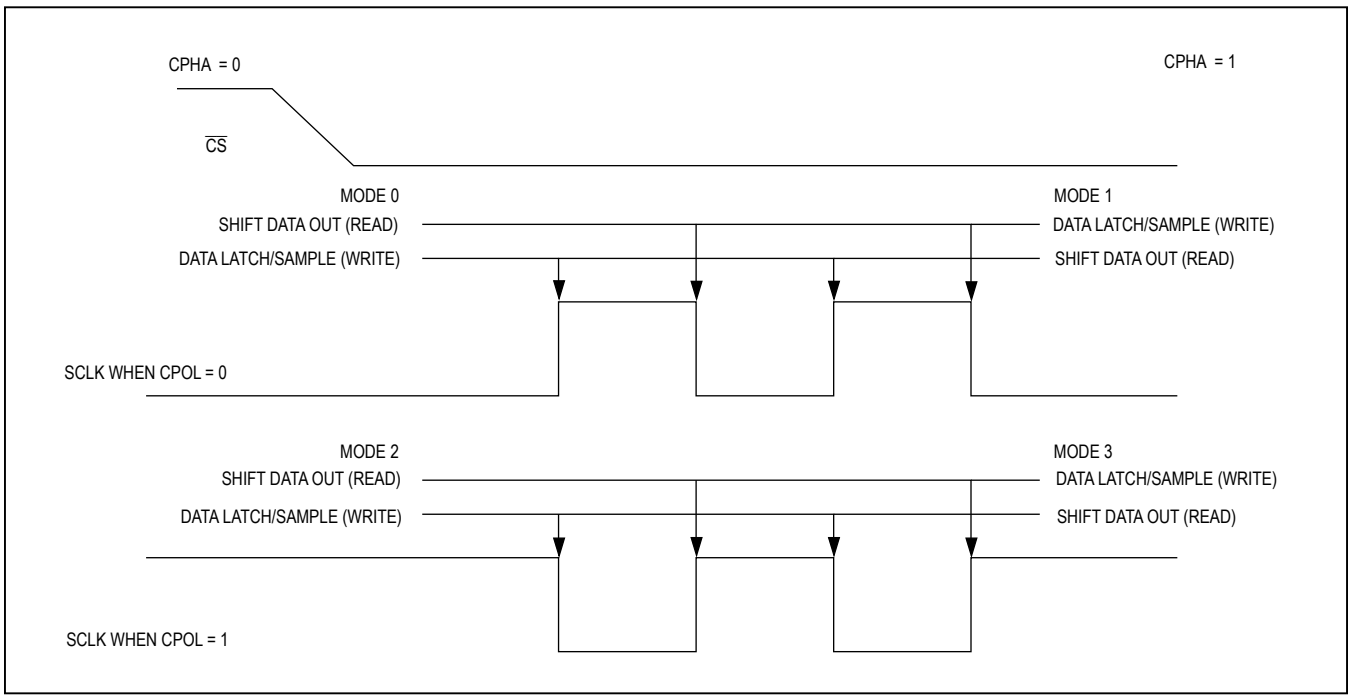


Figure 9. Serial Clock as a Function of Microcontroller Clock-Polarity Bit

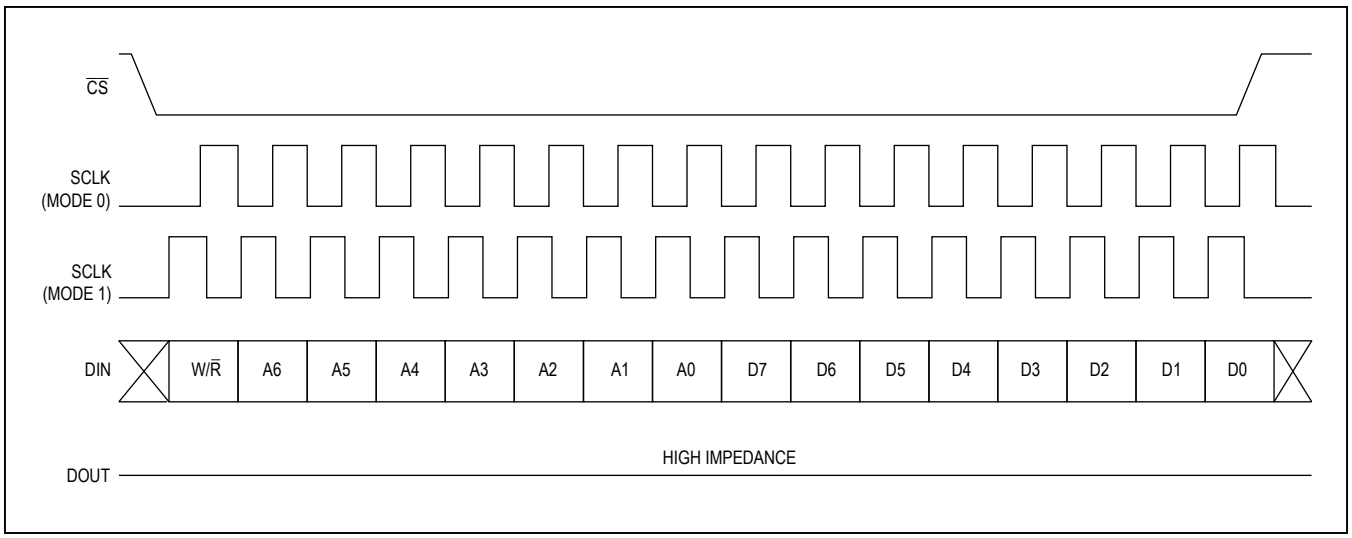


Figure 10. SPI Single-Byte Write

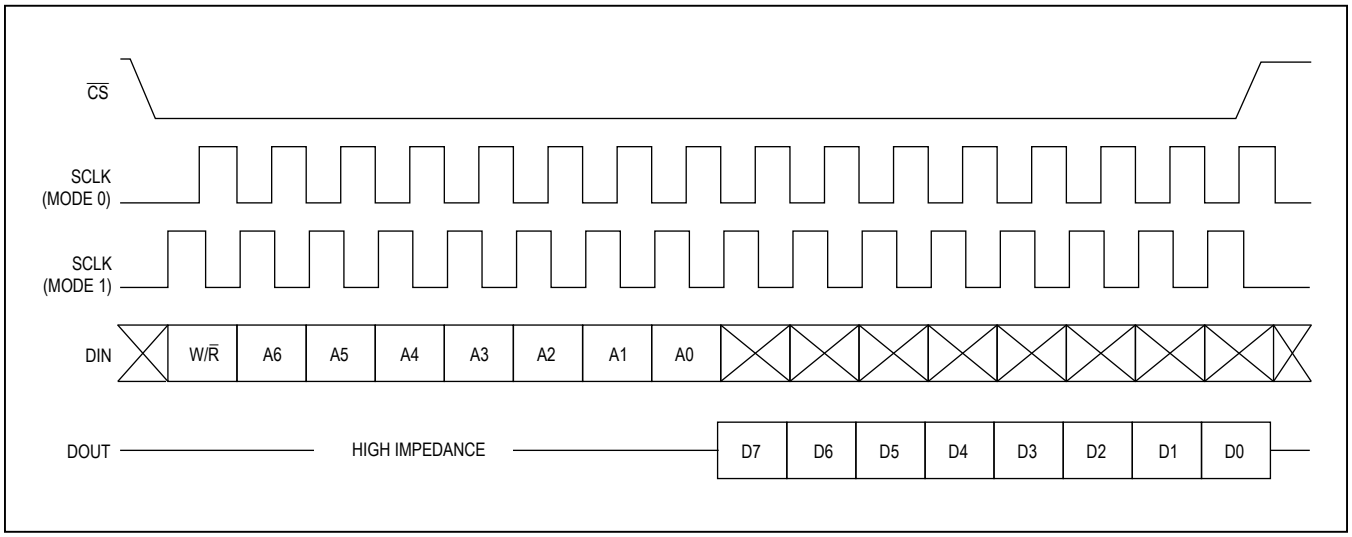


Figure 11. SPI Single-Byte Read

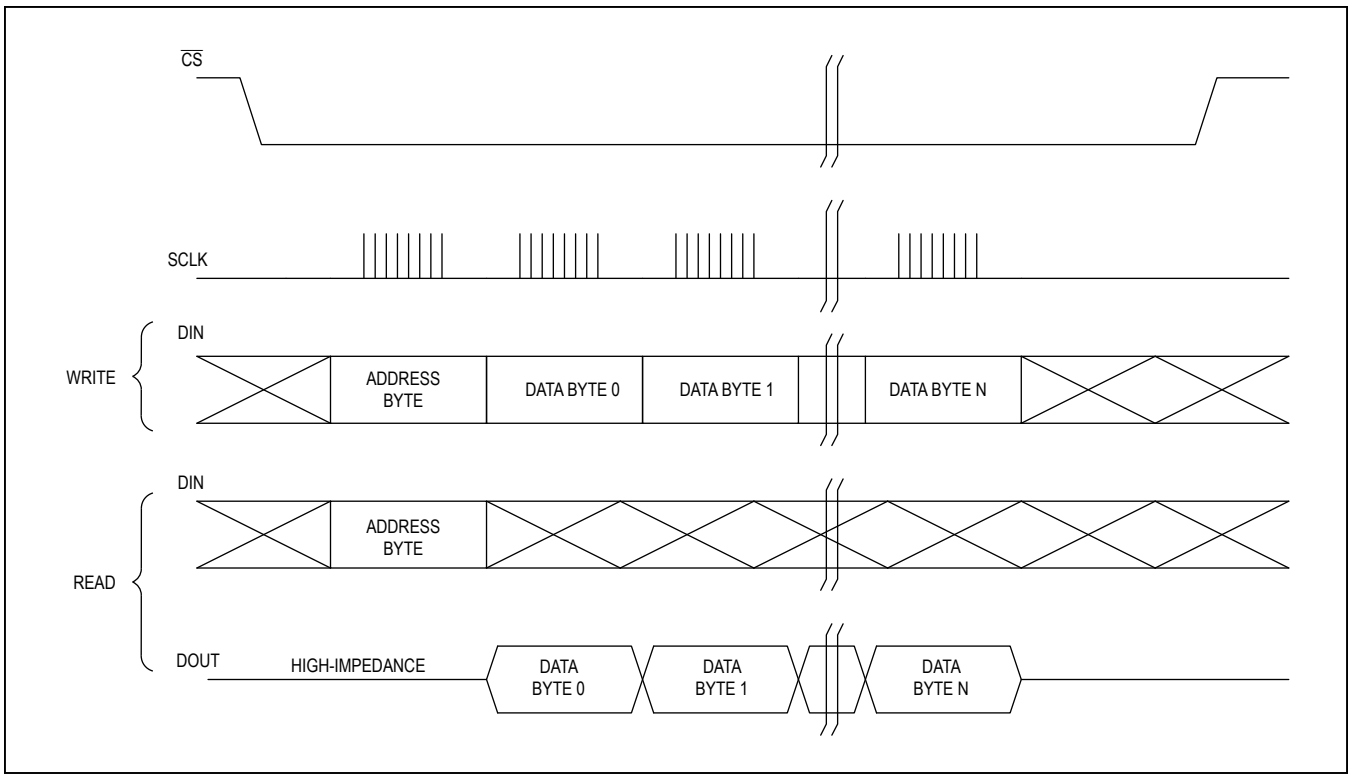


Figure 12. SPI Multiple-Byte Burst Transfer

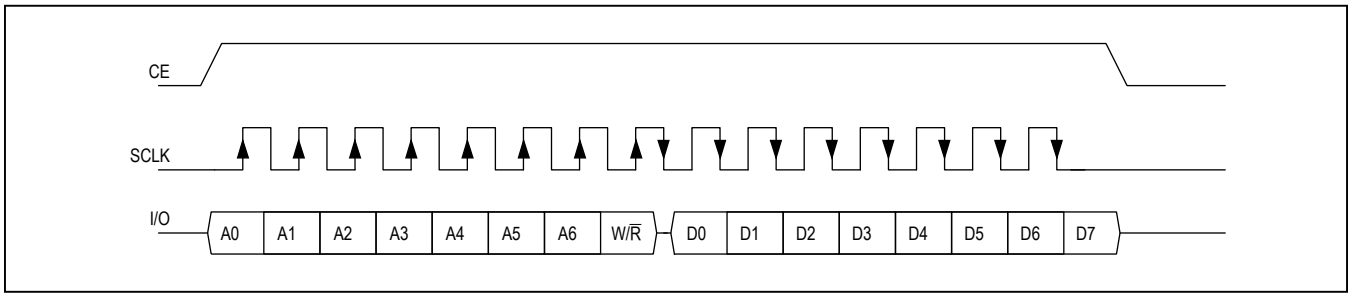


Figure 13. 3-Wire Single-Byte Read

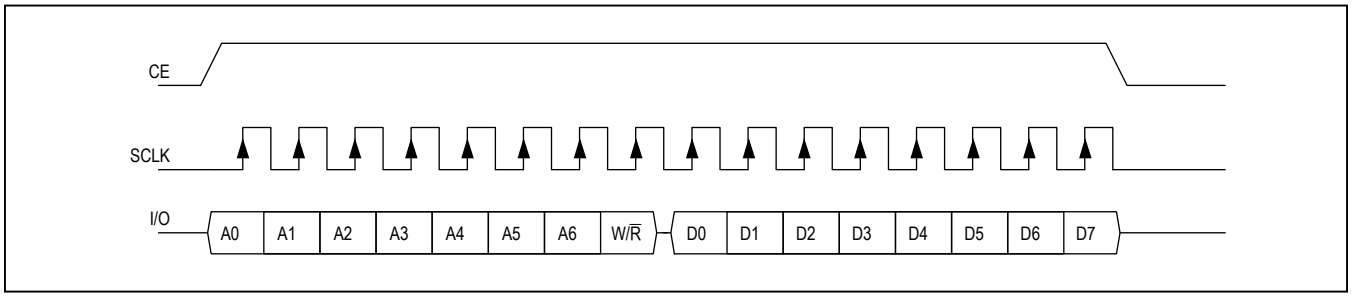


Figure 14. 3-Wire Single-Byte Write

3-Wire Serial-Data Bus

The DS1392/DS1393 provide a 3-wire serial-data bus, and support both single-byte and multiple-byte data transfers for maximum flexibility. The I/O pin is the serial-data input/output pin. The CE input is used to initiate and terminate a data transfer. The SCLK pin is used to synchronize data movement between the master (microcontroller) and the slave (DS1392/DS1393) devices. Input data is latched on the SCLK rising edge and output data is shifted out on the SCLK falling edge. There is one clock for each bit transferred. Address and data bits are transferred in groups of eight. Address and data bytes are shifted LSB first into the I/O pin. Data is transferred out LSB first on the I/O pin for a read operation.

The address byte is always the first byte entered after CE is driven high. The MSB (W/$\overline{R}$) of this byte determines if a read or write takes place. If W/$\overline{R}$ is 0, one or more read cycles occur. If W/$\overline{R}$ is 1, one or more write cycles occur.

Data transfers can be one byte at a time or in multiple-byte burst mode. After CE is driven high, an address is written to the DS1392/DS1393. After the address, one or more data bytes can be written or read. For a single-byte transfer, one byte is read or written and then CE is driven low (Figures 13 and 14). For a multiple-byte transfer, however, multiple bytes can be read or written after the address has been written (Figure 15). Each read or write cycle causes the RTC register address to automatically increment. Incrementing continues until the device is disabled. The address wraps to 00h after incrementing to 0Fh (during a read) and wraps to 80h after incrementing to 8Fh (during a write). Note, however, that an updated copy of the time is only loaded into the user-accessible copy upon the rising edge of CE. Reading the RTC registers in a continuous loop does not show the time advancing.

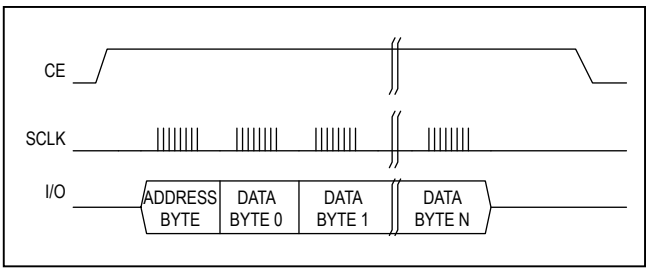


Figure 15. 3-Wire Multiple-Byte Burst Transfer

Chip Information

TRANSISTOR COUNT: 11,525

PROCESS: CMOS

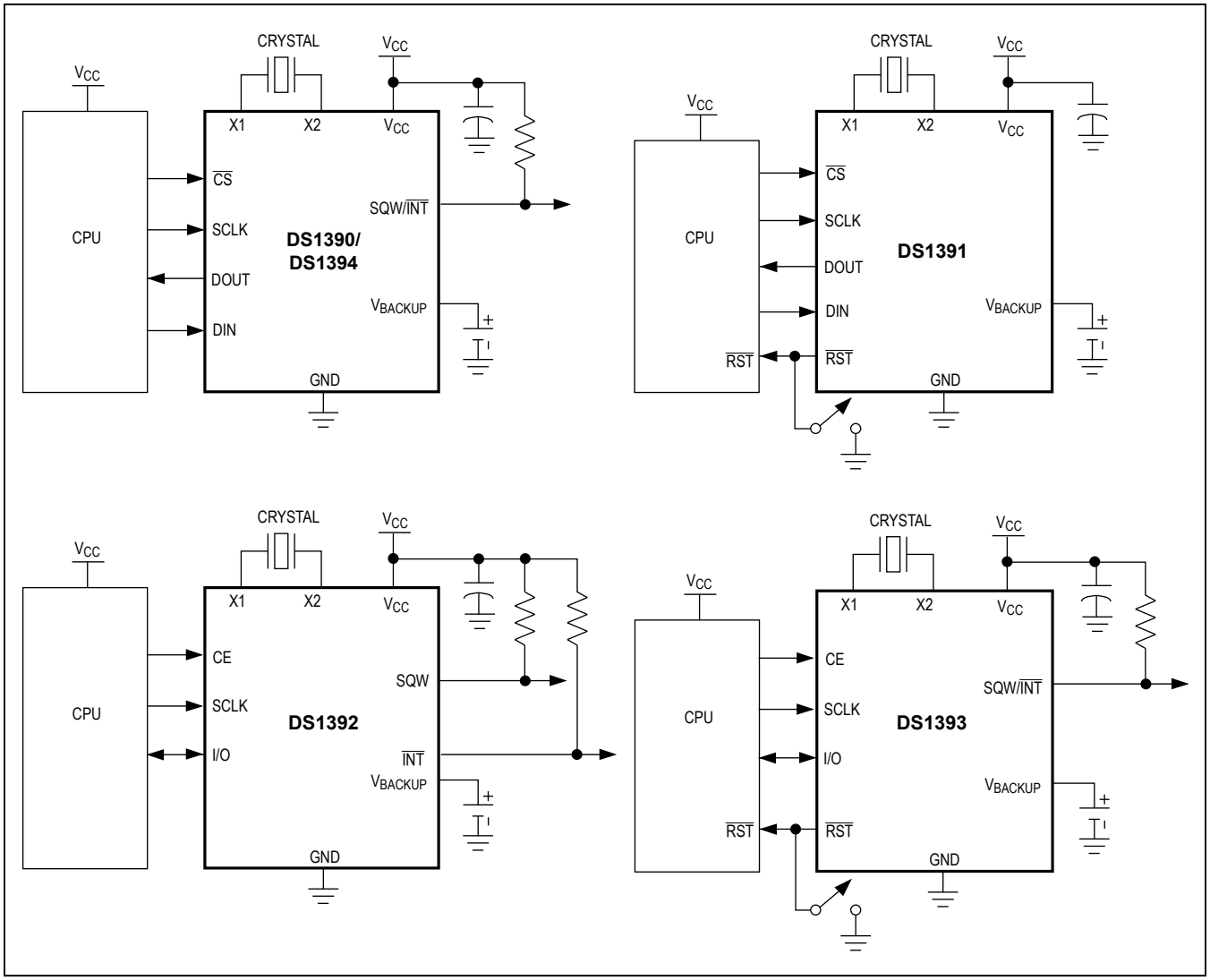
SUBSTRATE CONNECTED TO GROUND

Thermal Information

Theta-JA: 180°C/W

Theta-JC: 41.9°C/W

Typical Operating Circuits



Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µSOP	—	21-0061	90-0330

Ordering Information

PART	TYP OPERATING VOLTAGE (V)	PIN-PACKAGE	TOP MARK†
DS1390U-18+	1.8	10 µSOP	1390 rr-18
DS1390U-3+	3.0	10 µSOP	1390 rr-3
DS1390U-33+	3.3	10 µSOP	1390 rr-33
DS1391U-18+	1.8	10 µSOP	1391 rr-18
DS1391U-3+	3.0	10 µSOP	1391 rr-3
DS1391U-33+	3.3	10 µSOP	1391 rr-33
DS1392U-18+	1.8	10 µSOP	1393 rr-18
DS1392U-3+	3.0	10 µSOP	1392 rr-3
DS1392U-33+	3.3	10 µSOP	1392 rr-33
DS1393U-18+	1.8	10 µSOP	1393 rr-18
DS1393U-3+	3.0	10 µSOP	1393 rr-3
DS1393U-33+	3.3	10 µSOP	1393 rr-33
DS1394U-33+	3.3	10 µSOP	1394 rr-33

Note: *All devices are rated for the -40°C to +85°C operating temperature range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
†A "+" anywhere on the top mark denotes a lead(Pb)-free/RoHS-compliant package.
rr = Revision code on second line of top mark.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/04	Initial release.	—
1	1/07	Added text to the *General Description* section to indicate that the bus interface is disabled when the part switches to V_{BACKUP}; replaced *Ordering Information* table with lead-free packages.	1
		Added 0MHz (min) spec for SCLK frequency for SPI, 3-wire AC timing.	3, 5
		Added the “High Impedance” label for DOUT to Figure 1 and added DOUT trace to Figure 2.	4
		Changed all references of V_{BAT} to V_{BACKUP}.	8, 10
		Replaced the *Operation* section with the *Power Control* section and added new Table 1.	11, 12
2	8/08	Added the DS1394.	All
		In the *Address Map* section, added the description on how to avoid misreads of the time registers.	15
3	8/09	Added DS1390U-33/V+ to the *Ordering Information* table.	1
4	10/12	Updated *Ordering Information*	1
5	7/19	Updated *Special Purpose Registers* section	18

For pricing, delivery, and ordering information, please visit Maxim Integrated’s online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

