

TABLE OF CONTENTS

Features	1
Applications	1
Functional Block Diagrams	1
General Description	1
Revision History	2
Specifications	3
Absolute Maximum Ratings	5
ESD Caution	5
Pin Configurations and Function Descriptions	6
Typical Performance Characteristics	7
Circuit Description	9
Reset Output	9

REVISION HISTORY

7/2018—Rev. I to Rev. J

Deleted ADM6317	Throughout
Deleted Figure 4, Renumbered Sequentially	6
Changes to Table 4	6
Changes to Ordering Guide	13

3/2018—Rev. H to Rev. I

Changes to General Description Section	1
Added Note 1, Table 2	3
Changed Model Options Section to Device Model Options Section	11
Changes to Device Model Options Section and Table 5	11
Deleted Table 8; Renumbered Sequentially	12
Changes to Ordering Guide	13

12/2015—Rev. G to Rev. H

Added Endnote 1 and Endnote 2, Table 2	3
Change to Model Options Section Title	11
Added Endnote 1, Table 5	11
Changes to Table 8	12
Changes to Ordering Guide	14

1/2015—Rev. F to Rev. G

Changes to Table 8	12
--------------------------	----

5/2013—Rev. E to Rev. F

Changes to Table 8	12
Changes to Ordering Guide	13

Open-Drain $\overline{\text{RESET}}$ Output	9
Manual Reset Input	9
Watchdog Input	9
Applications Information	10
Watchdog Input Current	10
Negative Going V_{CC} Transients	10
Ensuring Reset Valid to $V_{CC} = 0\text{ V}$	10
Watchdog Software Considerations	10
Device Model Options	11
Outline Dimensions	13
Ordering Guide	13

10/2010—Rev. D to Rev. E

Changes to Table 8	12
Updated Outline Dimensions	13

8/2008—Rev. C to Rev. D

Change to Figure 18	9
---------------------------	---

4/2007—Rev. B to Rev. C

Added Figure 2	1
Changes to Figure 23	13
Changes to Ordering Guide	13

1/2007—Rev. A to Rev. B

Changes to Functional Block Diagram	1
Changes to Figure 18	10

5/2006—Rev. 0 to Rev. A

Updated Format	Universal
Changes to Functional Block Diagram	1
Changes to Table 8	12
Changes to Figure 22	13
Changes to Ordering Guide	13

10/2004—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = full operating range, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range	1		5.5	V	$V_{CC} = 5.5\text{ V}$
Supply Current		10	20	μA	$V_{CC} = 5.5\text{ V}$
		5	12	μA	$V_{CC} = 3.6\text{ V}$
RESET THRESHOLD VOLTAGE ¹	$V_{TH} - 1.5\%$ $V_{TH} - 2.5\%$	V_{TH}	$V_{TH} + 1.5\%$ $V_{TH} + 2.5\%$	V V	$T_A = 25^\circ\text{C}$ $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
RESET THRESHOLD TEMPERATURE COEFFICIENT		40		ppm/ $^\circ\text{C}$	
RESET THRESHOLD HYSTERESIS		3		mV	
RESET TIMEOUT PERIOD ¹					
ADM63xxA ²	1	1.4	2	ms	
ADM63xxB ²	20	28	40	ms	
ADM63xxC ²	140	200	280	ms	
ADM63xxD ²	1120	1600	2240	ms	
V_{CC} TO RESET DELAY		40		μs	V_{CC} falling at 1 mV/ μs
PUSH-PULL OUTPUT (ADM6316, ADM6318, ADM6319, ADM6321, ADM6322)					
RESET Output Voltage			0.3	V	$V_{CC} \geq 1.0\text{ V}$, $I_{SINK} = 50\text{ }\mu\text{A}$
			0.3	V	$V_{CC} \geq 1.2\text{ V}$, $I_{SINK} = 100\text{ }\mu\text{A}$
			0.3	V	$V_{CC} \geq 2.7\text{ V}$, $I_{SINK} = 1.2\text{ mA}$
			0.4	V	$V_{CC} \geq 4.5\text{ V}$, $I_{SINK} = 3.2\text{ mA}$
	$0.8 \times V_{CC}$			V	$V_{CC} \geq 2.7\text{ V}$, $I_{SOURCE} = 500\text{ }\mu\text{A}$
	$V_{CC} - 1.5$			V	$V_{CC} \geq 4.5\text{ V}$, $I_{SOURCE} = 800\text{ }\mu\text{A}$
RESET Rise Time		5	25	ns	From 10% to 90% V_{CC} , $C_L = 5\text{ pF}$, $V_{CC} = 3.3\text{ V}$
RESET Output Voltage			0.3	V	$V_{CC} \geq 2.7\text{ V}$, $I_{SINK} = 1.2\text{ mA}$
			0.4	V	$V_{CC} \geq 4.5\text{ V}$, $I_{SINK} = 3.2\text{ mA}$
	$0.8 \times V_{CC}$			V	$V_{CC} \geq 1.8\text{ V}$, $I_{SOURCE} = 150\text{ }\mu\text{A}$
	$0.8 \times V_{CC}$			V	$V_{CC} \geq 2.7\text{ V}$, $I_{SOURCE} = 500\text{ }\mu\text{A}$
	$V_{CC} - 1.5$			V	$V_{CC} \geq 4.5\text{ V}$, $I_{SOURCE} = 800\text{ }\mu\text{A}$
OPEN-DRAIN OUTPUT (ADM6320, ADM6321, ADM6322)					
RESET Output Voltage			0.3	V	$V_{CC} \geq 1.0\text{ V}$, $I_{SINK} = 50\text{ }\mu\text{A}$
			0.3	V	$V_{CC} \geq 1.2\text{ V}$, $I_{SINK} = 100\text{ }\mu\text{A}$
			0.3	V	$V_{CC} \geq 2.7\text{ V}$, $I_{SINK} = 1.2\text{ mA}$
			0.4	V	$V_{CC} \geq 4.5\text{ V}$, $I_{SINK} = 3.2\text{ mA}$
Open-Drain Reset Output Leakage Current			1	μA	
WATCHDOG INPUT (ADM6316, ADM6318, ADM6320, ADM6321)					
Watchdog Timeout Period ¹					
ADM63xxxW ³	4.3	6.3	9.3	ms	
ADM63xxxX ³	71	102	153	ms	
ADM63xxxY ³	1.12	1.6	2.4	sec	
ADM63xxxZ ³	17.9	25.6	38.4	sec	
WDI Pulse Width	50			ns	$V_{IL} = 0.3 \times V_{CC}$, $V_{IH} = 0.7 \times V_{CC}$
WDI Input Threshold	$0.3 \times V_{CC}$		$0.7 \times V_{CC}$	V	
WDI Input Current		120	160	μA	$V_{WDI} = V_{CC}$, time average
	-20	-15		μA	$V_{WDI} = 0$, time average

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MANUAL RESET INPUT (ADM6316, ADM6319, ADM6320, ADM6322)					
$\overline{\text{MR}}$ Input Threshold	0.8		2.0	V	$V_{\text{TH}} > 4.0 \text{ V}$
	$0.3 \times V_{\text{CC}}$		$0.7 \times V_{\text{CC}}$	V	$V_{\text{TH}} < 4.0 \text{ V}$
$\overline{\text{MR}}$ Input Pulse Width	1			μs	
$\overline{\text{MR}}$ Glitch Rejection		100		ns	
$\overline{\text{MR}}$ Pull-Up Resistance	35	52	75	k Ω	
$\overline{\text{MR}}$ to Reset Delay		230		ns	$V_{\text{CC}} = 5 \text{ V}$

¹ Not all device options are released for sale as standard models. See the Ordering Guide for full details.

² Complete the model code by replacing xx with a device generic number.

³ Complete the model code by replacing xxx with a device generic number and code for the reset timeout period.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
V_{CC}	–0.3 V to +6 V
$\overline{\text{RESET}}$ (ADM6320, ADM6321, ADM6322)	–0.3 V to +6 V
All Other Pins	–0.3 V to ($V_{CC} + 0.3$ V)
Output Current ($\overline{\text{RESET}}$, $\overline{\text{RESET}}$)	20 mA
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
θ_{JA} Thermal Impedance, SOT-23	270°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

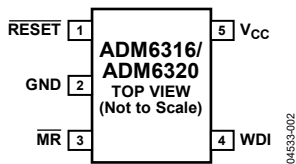


Figure 3. ADM6316/ADM6320 Pin Configuration

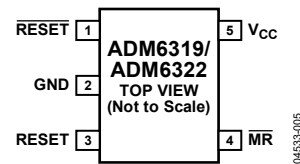


Figure 5. ADM6319/ADM6322 Pin Configuration

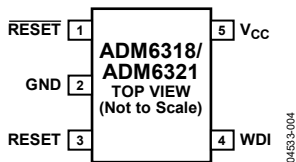


Figure 4. ADM6318/ADM6321 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RESET	Active Low Reset Output. Asserted whenever V_{CC} is below the reset threshold, V_{TH} . Push-Pull Output Stage for the ADM6316/ADM6318/ADM6319. Open-Drain Output Stage for the ADM6320/ADM6321/ADM6322.
2	GND	Ground.
3	MR (ADM6316/ADM6320)	Manual Reset Input. This is an active low input that when forced low for at least 1 μs , generates a reset. It features a 52 k Ω internal pull-up.
4	RESET (ADM6318/ADM6319/ADM6321/ADM6322) WDI (ADM6316/ADM6318/ADM6320/ADM6321)	Active High Push-Pull Reset Output. Watchdog Input. Generates a reset if the logic level on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated. Leave this pin floating to disable the watchdog timer.
5	MR (ADM6319/ADM6322) VCC (all models)	Manual Reset Input. Power Supply Voltage Being Monitored.

TYPICAL PERFORMANCE CHARACTERISTICS

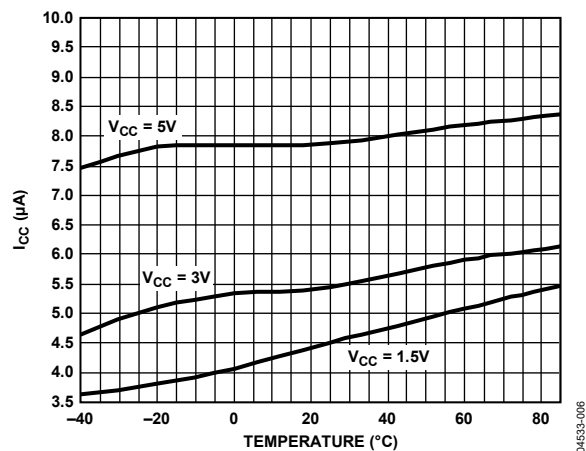


Figure 6. Supply Current vs. Temperature
(ADM6316/ADM6318/ADM6320/ADM6321)

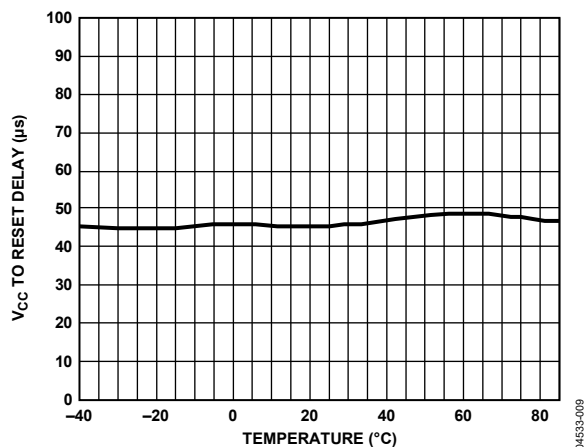


Figure 9. V_{CC} Falling to Reset Propagation Delay vs. Temperature

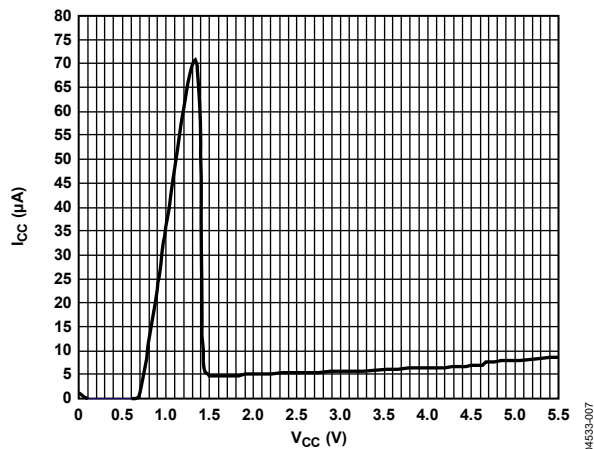


Figure 7. Supply Current vs. Supply Voltage

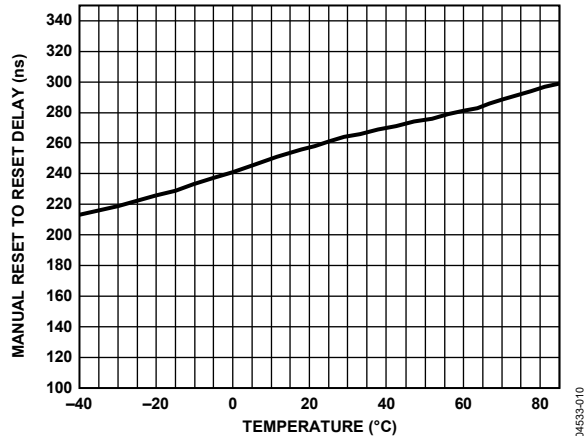


Figure 10. Manual Reset to Reset Propagation Delay vs. Temperature
(ADM6316/ADM6319/ADM6320/ADM6322)

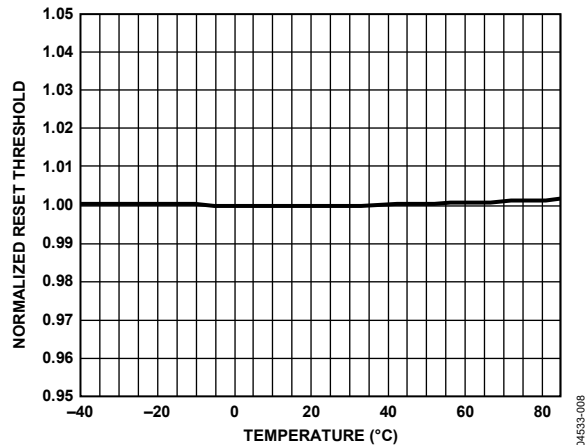


Figure 8. Normalized Reset Threshold vs. Temperature

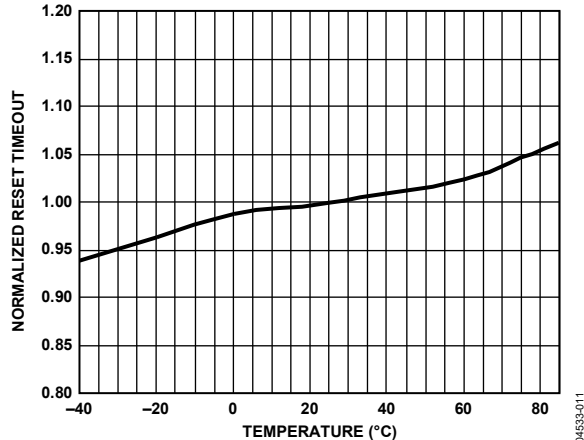


Figure 11. Normalized Reset Timeout Period vs. Temperature

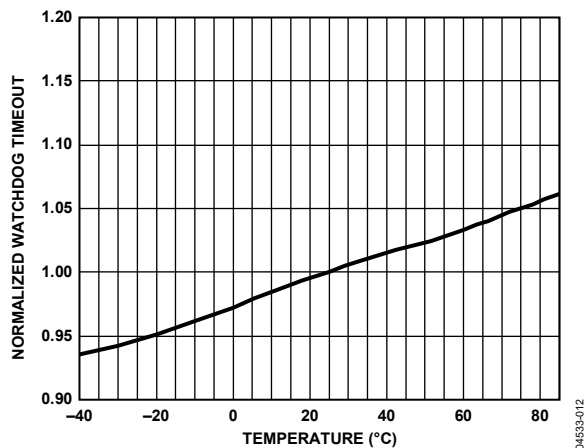


Figure 12. Normalized Watchdog Timeout Period vs. Temperature (ADM6316/ADM6318/ADM6320/ADM6321)

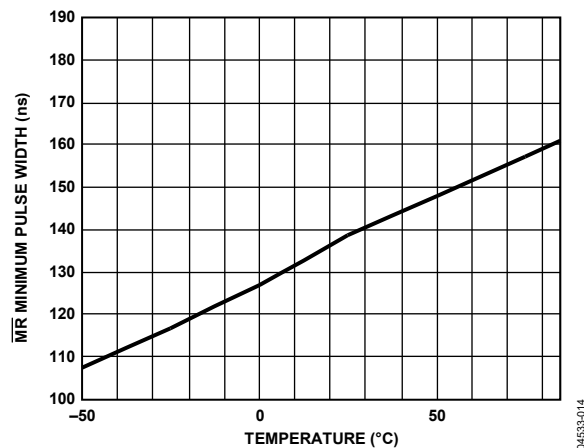


Figure 14. Manual Reset Minimum Pulse Width vs. Temperature (ADM6316/ADM6319/ADM6320/ADM6322)

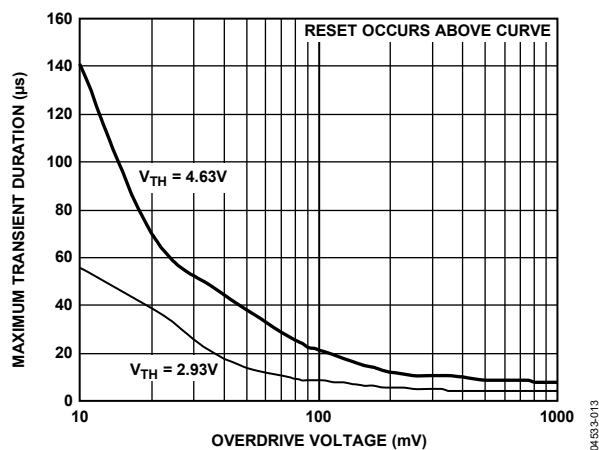


Figure 13. Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive

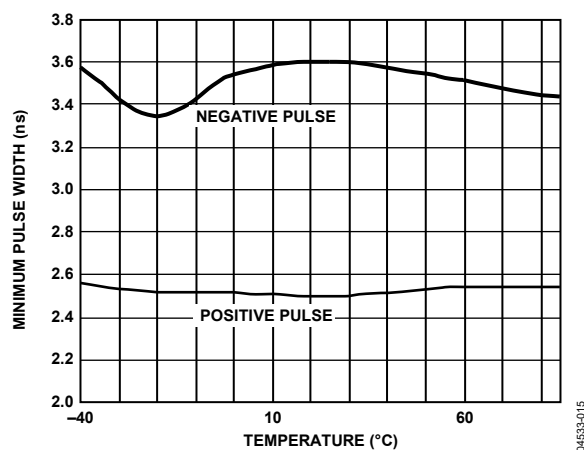


Figure 15. Watchdog Input Minimum Pulse Width vs. Temperature (ADM6316/ADM6318/ADM6320/ADM6321)

CIRCUIT DESCRIPTION

The ADM6316/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322 provide microprocessor supply voltage supervision by controlling the reset input of the microprocessor. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout reset pulse after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a watchdog timer (ADM6316/ADM6318/ADM6320/ADM6321). If the user detects a problem with the system's operation, a manual reset input is available (ADM6316/ADM6319/ADM6320/ADM6322) to reset the microprocessor, for example, by means of an external push button.

RESET OUTPUT

The ADM6316 features an active low push-pull reset output, while the ADM6321/ADM6322 have active high push-pull reset outputs. The ADM6318/ADM6319 feature dual active low and active high push-pull reset outputs. For active low and active high outputs, the reset signal is guaranteed to be logic low and logic high, respectively, for V_{CC} down to 1 V.

The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}), when $\overline{MR}$ is driven low, or when WDI is not serviced within the watchdog timeout period (t_{WD}). Reset remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after $\overline{MR}$ transitions from low to high, or after the watchdog timer times out. Figure 16 illustrates the behavior of the reset outputs.

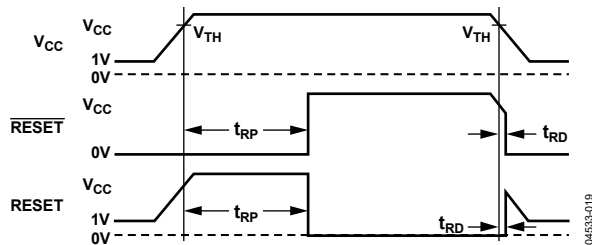


Figure 16. Reset Timing Diagram

OPEN-DRAIN RESET OUTPUT

The ADM6320/ADM6321/ADM6322 have an active low, open-drain reset output. This output structure requires an external pull-up resistor to connect the reset output to a voltage rail no higher than 6 V. The resistor must comply with the microprocessor's logic low and logic high voltage level requirements while supplying input current and leakage paths on the RESET line. A 10 k Ω resistor is adequate in most situations.

MANUAL RESET INPUT

The ADM6316/ADM6319/ADM6320/ADM6322 feature a manual reset input ($\overline{MR}$), which when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 52 k Ω , internal pull-up so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on chip. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative going transients of up to 100 ns (typical) are ignored. A 0.1 μ F capacitor between $\overline{MR}$ and ground provides additional noise immunity.

WATCHDOG INPUT

The ADM6316/ADM6318/ADM6320/ADM6321 feature a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI), which detects pulses as short as 50 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), reset is asserted. The microprocessor is required to toggle the WDI pin to avoid being reset. Failure of the microprocessor to toggle WDI within the timeout period, therefore, indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

As well as logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on V_{CC} or due to $\overline{MR}$ being pulled low. When reset is asserted, the watchdog timer is cleared and does not begin counting again until reset deasserts. The watchdog timer can be disabled by leaving WDI floating or by three-stating the WDI driver.

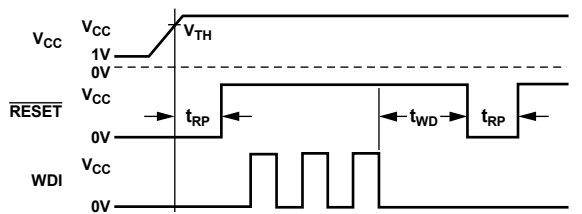


Figure 17. Watchdog Timing Diagram

APPLICATIONS INFORMATION

WATCHDOG INPUT CURRENT

To minimize watchdog input current (and minimize overall power consumption), leave WDI low for the majority of the watchdog timeout period. When driven high, WDI can draw as much as 160 μ A. Pulsing WDI low-to-high-to-low at a low duty cycle reduces the effect of the large input current. When WDI is unconnected, a window comparator disconnects the watchdog timer from the reset output circuitry so that reset is not asserted when the watchdog timer times out.

NEGATIVE GOING V_{CC} TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM6316/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322 are equipped with glitch rejection circuitry. The typical performance characteristic in Figure 13 plots V_{CC} transient duration vs. the transient magnitude. The curves show combinations of transient magnitude and duration for which a reset is not generated for 4.63 V and 2.93 V reset threshold parts. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 8 μ s typically does not cause a reset, but if the transient is any larger in magnitude or duration, a reset is generated. An optional 0.1 μ F bypass capacitor mounted close to V_{CC} provides additional glitch rejection.

ENSURING RESET VALID TO $V_{CC} = 0$ V

Both active low and active high reset outputs are guaranteed to be valid for V_{CC} as low as 1 V. However, by using an external resistor with push-pull configured reset outputs, valid outputs for V_{CC} as low as 0 V are possible. For an active low reset output, a resistor connected between $\overline{\text{RESET}}$ and ground pulls the output low when it is unable to sink current. For the active high case, a resistor connected between $\overline{\text{RESET}}$ and V_{CC} pulls the output high when it is unable to source current. A large resistance, such as 100 k Ω , must be used so that it does not overload the reset output when V_{CC} is above 1 V.

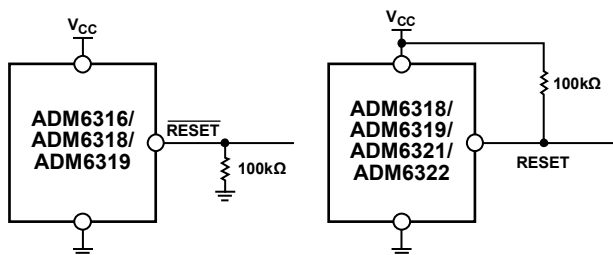


Figure 18. Ensuring Reset Valid to $V_{CC} = 0$ V

WATCHDOG SOFTWARE CONSIDERATIONS

In implementing the microprocessor's watchdog strobe code, quickly switching WDI low to high and then high to low (minimizing WDI high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low-to-high-to-low WDI pulse within a given subroutine prevents the watchdog from timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog cannot detect this because the subroutine continues to toggle WDI. A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI is set high. The subroutine sets WDI low when it is called. If the program executes without error, WDI is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI is kept low, the watchdog times out, and the microprocessor is reset (see Figure 19).

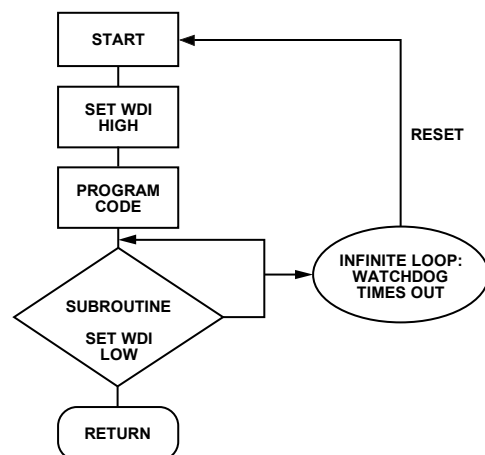


Figure 19. Watchdog Flow Diagram

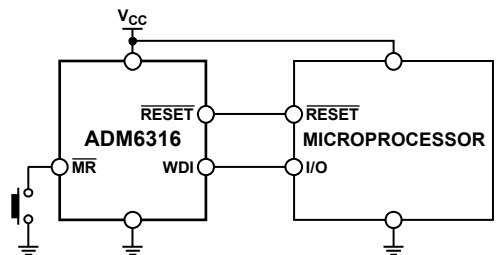


Figure 20. Typical Application Circuit

DEVICE MODEL OPTIONS

The ADM6316/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322 include many device options, however, not all options are released for sale. Released options called standard models and are listed in the Ordering Guide.

The [Watchdog Timers](#) page on the ADI website also shows a list of standard models. Contact a sales representative for information on nonstandard models and be aware that samples and production units have very long lead times.

Table 5. Reset Voltage Threshold Options

Reset Threshold Number	T _A = +25°C			T _A = –40°C to +85°C		Unit
	Min	Typ	Max	Min	Max	
50	4.925	5.000	5.075	4.875	5.125	V
49	4.827	4.900	4.974	4.778	5.023	V
48	4.728	4.800	4.872	4.680	4.920	V
47	4.630	4.700	4.771	4.583	4.818	V
46	4.561	4.630	4.699	4.514	4.746	V
45	4.433	4.500	4.568	4.388	4.613	V
44	4.314	4.390	4.446	4.270	4.490	V
43	4.236	4.300	4.365	4.193	4.408	V
42	4.137	4.200	4.263	4.095	4.305	V
41	4.039	4.100	4.162	3.998	4.203	V
40	3.940	4.00	4.060	3.900	4.100	V
39	3.842	3.900	3.959	3.803	3.998	V
38	3.743	3.800	3.857	3.705	3.895	V
37	3.645	3.700	3.756	3.608	3.793	V
36	3.546	3.600	3.654	3.510	3.690	V
35	3.448	3.500	3.553	3.413	3.588	V
34	3.349	3.400	3.451	3.315	3.485	V
33	3.251	3.300	3.350	3.218	3.383	V
32	3.152	3.200	3.248	3.120	3.280	V
31	3.034	3.080	3.126	3.003	3.157	V
30	2.955	3.000	3.045	2.925	3.075	V
29	2.886	2.930	2.974	2.857	3.000	V
28	2.758	2.800	2.842	2.730	2.870	V
27	2.660	2.700	2.741	2.633	2.768	V
26	2.591	2.630	2.669	2.564	2.696	V
25	2.463	2.500	2.538	2.438	2.563	V

Table 6. Reset Timeout Options

Suffix	Min	Typ	Max	Unit
A	1	1.6	2	ms
B	20	30	40	ms
C	140	200	280	ms
D	1.12	1.60	2.24	sec

Table 7. Watchdog Timer Options

Suffix	Min	Typ	Max	Unit
W	4.3	6.3	9.3	ms
X	71	102	153	ms
Y	1.12	1.6	2.24	sec
Z	17.9	25.6	38.4	sec

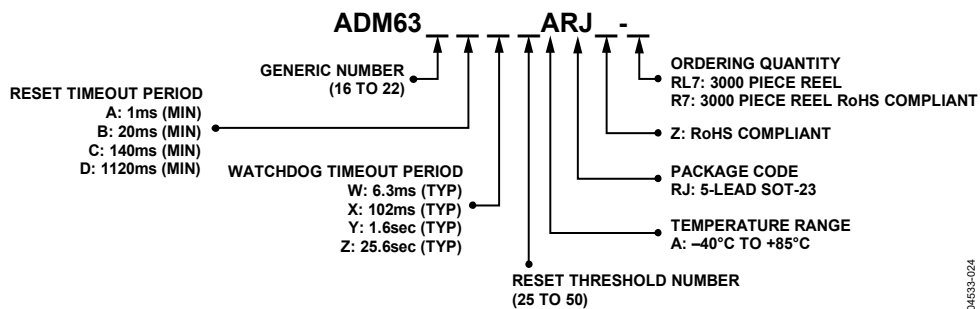
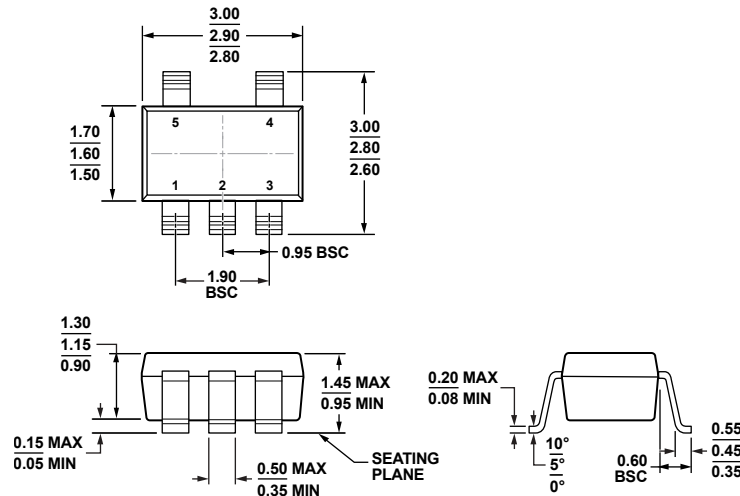


Figure 21. Ordering Code Structure (Modified Diagram)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AA

Figure 22. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)

Dimensions shown in millimeters

ORDERING GUIDE

Model ^{1,2,3}	Reset Voltage Threshold (V)	Minimum Reset Timeout (ms)	Typical Watchdog Timeout (sec) ⁴	Temperature Range	Package Description	Package Option	Ordering Quantity	Marking Code
ADM6316AY27ARJZ-R7	2.7	1	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316AY29ARJZ-R7	2.93	1	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316AZ29ARJZ-R7	2.93	1	25.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316BX30ARJZ-R7	3	20	0.102	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316BX46ARJZ-R7	4.63	20	0.102	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316CW25ARJZ-R7	2.5	140	0.0063	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316CY26ARJZ-R7	2.63	140	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316CY29ARJZ-R7	2.93	140	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316CY46ARJZ-R7	4.63	140	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316DZ26ARJ-RL7	2.63	1120	25.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N00
ADM6316DZ26ARJZ-R7	2.63	1120	25.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6316DZ31ARJZ-R7	3.08	1120	25.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M7Q
ADM6318BX49ARJZ-R7	4.9	20	0.102	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M9N
ADM6318CY29ARJZ-R7	2.93	140	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M4Q
ADM6318CY46ARJ-RL7	4.63	140	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M4Q
ADM6318CY46ARJZ-R7	4.63	140	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N02
ADM6318CZ28ARJZ-R7	2.8	140	25.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M4Q
ADM6319B25ARJZ-R7	2.5	20	N/A	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M4Q
ADM6319B31ARJZ-RL7	3.08	20	N/A	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0S
ADM6319C29ARJZ-RL7	2.93	140	N/A	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0S
ADM6319C46ARJZ-RL7	4.63	140	N/A	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0S
ADM6320BX33ARJZ-R7	3.3	20	0.102	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0S
ADM6320BX45ARJZ-R7	4.5	20	0.102	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0T
ADM6320CX29ARJZ-R7	2.93	140	0.102	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0T
ADM6320CY29ARJ-RL7	2.93	140	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0T
ADM6320CY29ARJZ-R7	2.93	140	1.6	-40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N04

Model ^{1,2,3}	Reset Voltage Threshold (V)	Minimum Reset Timeout (ms)	Typical Watchdog Timeout (sec) ⁴	Temperature Range	Package Description	Package Option	Ordering Quantity	Marking Code
ADM6320CY31ARJZ-R7	3.08	140	1.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0T
ADM6320CY46ARJZ-R7	4.63	140	1.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0T
ADM6320CZ27ARJZ-R7	2.7	140	25.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0T
ADM6320CZ29ARJ-RL7	2.93	140	25.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0T
ADM6320CZ29ARJZ-R7	2.93	140	25.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N04
ADM6321AX29ARJZ-R7	2.93	1	0.102	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	N0T
ADM6321AY30ARJZ-R7	3	1	1.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M8L
ADM6321AY31ARJZ-R7	3.08	1	1.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M8L
ADM6321AY43ARJZ-R7	4.3	1	1.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M8L
ADM6321BZ25ARJZ-R7	2.5	20	25.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M8L
ADM6321CY46ARJZ-R7	4.63	140	1.6	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M8L
ADM6322C29ARJZ-R7	2.93	140	N/A	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M8L
ADM6322C46ARJZ-RL7	4.63	140	N/A	−40°C to +85°C	5-Lead SOT-23	RJ-5	3,000	M8J
								M8J

¹ Z = RoHS Compliant Part.

² The ADM6316/ADM6318/ADM6319/ADM6320/ADM6321/ADM6322 include many device options, however, not all options are released for sale. Released options called standard models and are listed in the Ordering Guide. The [Watchdog Timers](#) page on the ADI website also shows a list of standard models. Contact a sales representative for information on nonstandard models and be aware that samples and production units have very long lead times.

³ If ordering nonstandard models, complete the ordering code (see Figure 21) by inserting the reset voltage threshold, reset timeout, and watchdog timer (ADM6316/ADM6318/ADM6320/ADM6321) suffixes from Table 5 to Table 7. No watchdog timeout is available for ADM6319/ADM6322.

⁴ N/A means not applicable.