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REVISION HISTORY

7/11—Rev. E to Rev. F

Deleted ADG528F ..... Universal
Changes to Features Section and General Description Section 1
Changes to Specifications Section 3
Deleted Timing Diagrams Section 4
Changes to Table 4 5
Added Table 5 6
Added Table 6 7
Replaced Typical Performance Characteristics Section 8
Changes to Terminology Section 10
Changes to Figure 27 and Figure 28 13
Changes to Figure 31 14
Changes to Theory of Operation Section 11
Updated Outline Dimensions 15
Changes to Ordering Guide 17

7/09—Rev. D: Rev. E

Updated Format ..... Universal
Added TSSOP ..... Universal
Updated Outline Dimensions 15
Changes to Ordering Guide 18

4/01—Data Sheet Changed from Rev. C to Rev. D.

Changes to Ordering Guide 1
Changes to Specifications Table 2
Max Ratings Changed 4
Deleted 16-Lead Cerdip from Outline Dimensions 11
Deleted 18-Lead Cerdip from Outline Dimensions 12

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range	V_{SS} + 1.4		V typ	Output open circuit
	V_{DD} − 1.4		V typ	
	V_{SS} + 2.2		V typ	Output loaded, 1 mA
	V_{DD} − 2.2		V typ	
R_{ON}	270	350	Ω typ	−10 V ≤ V_S ≤ +10 V, I_S = 1 mA;
		390	Ω max	V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10% See Figure 21
R_{ON} Drift	0.6		%/°C typ	V_S = 0 V, I_S = 1 mA
On-Resistance Match Between Channels, ΔR_{ON}	3		% max	V_S = ±10 V, I_S = −1 mA
LEAKAGE CURRENTS				
Source Off Leakage I_S (Off)	±0.02		nA typ	V_D = ±10 V, V_S = ∓10 V;
	±1	±50	nA max	See Figure 22
Drain Off Leakage I_D (Off)	±0.04		nA typ	V_D = ±10 V, V_S = ∓10 V;
ADG508F	±1	±60	nA max	See Figure 23
ADG509F	±1	±30	nA max	
Channel On Leakage I_D, I_S (On)	±0.04		nA typ	V_S = V_D = ± 10 V;
ADG508F	±1	±60	nA max	See Figure 24
ADG509F	±1	±30	nA max	
FAULT				
Source Leakage Current I_S (Fault)	±0.02		nA typ	V_S = +55 V or −40 V, V_D = 0 V, see Figure 25
(With Overvoltage)	±2	±2	µA max	
Drain Leakage Current I_D (Fault)	±5		nA typ	V_S = ±25 V, V_D = ∓10 V, see Figure 23
(With Overvoltage)	±2		µA max	
Source Leakage Current I_S (Fault) (Power Supplies Off)	±1		nA typ	V_S = ±25 V, V_D = V_{EN} = A0, A1, A2 = 0 V
	±2		µA max	See Figure 26
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}		±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	5		pF typ	
DYNAMIC CHARACTERISTICS[1]				
$t_{TRANSITION}$	175		ns typ	R_L = 1 MΩ, C_L = 35 pF;
	220	300	ns max	V_{S1} = ±10 V, V_{S8} = ∓10 V; see Figure 27
t_{OPEN}	90		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	60	40	ns min	V_S = 5 V; see Figure 28
t_{ON} (EN)	180		ns typ	R_L = 1 kΩ, C_L = 35 pF;
	230	300	ns max	V_S = 5 V; see Figure 29
t_{OFF} (EN)	100		ns typ	R_L = 1 kΩ, C_L = 35 pF
	130	150		
t_{SETT}, Settling Time			ns max	V_S = 5 V; see Figure 29
0.1%		1	µs typ	R_L = 1 kΩ, C_L = 35 pF;
0.01%		2.5	µs typ	V_S = 5 V

Parameter	B Version +25°C	B Version −40°C to +85°C	Unit	Test Conditions/Comments
Charge Injection	15		pC typ	V_S = 0 V, R_S = 0 Ω, C_L= 1 nF; see Figure 30
Off Isolation	93		dB typ	R_L = 1 kΩ, C_L = 15 pF, f = 100 kHz; V_S = 7 V rms; see Figure 31
C_S (Off)	3		pF typ	
C_D (Off)				
ADG508F	22		pF typ	
ADG509F	12		pF typ	
POWER REQUIREMENTS				
I_{DD}	0.05	0.2	mA max	V_{IN} = 0 V or 5 V
I_{SS}	0.1	1	µA max	

[1] Guaranteed by design, not subject to production test.

TRUTH TABLES

Table 2. ADG508F Truth Table[1]

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

[1] X = don't care.

Table 3. ADG509F Truth Table[1]

A1	A0	EN	On Switch Pair
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

[1] X = don't care.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Digital Input, EN, Ax	−0.3 V to V_{DD} + 0.3 V or 20 mA, whichever occurs first
V_S, Analog Input Overvoltage with Power On (V_{DD} = +15 V, V_{SS} = −15 V)	V_{SS} − 25 V to V_{DD} + 40 V
V_S, Analog Input Overvoltage with Power Off (V_{DD} = 0 V, V_{SS} = 0 V)	−40 V to +55 V
Continuous Current, S or D	20 mA
Peak Current, S or D	
(Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP	
θ_{JA}, Thermal Impedance	112°C/W
Plastic DIP Package	
θ_{JA}, Thermal Impedance	
16-Lead	117°C/W
SOIC Package	
θ_{JA}, Thermal Impedance	
Narrow Body	77°C/W
Wide Body	75°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

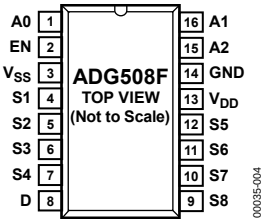


Figure 3. ADG508F Pin Configuration

Table 5. ADG508F Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1	Source Terminal 1. This pin can be an input or an output.
5	S2	Source Terminal 2. This pin can be an input or an output.
6	S3	Source Terminal 3. This pin can be an input or an output.
7	S4	Source Terminal 4. This pin can be an input or an output.
8	D	Drain Terminal. This pin can be an input or an output.
9	S8	Source Terminal 8. This pin can be an input or an output.
10	S7	Source Terminal 7. This pin can be an input or an output.
11	S6	Source Terminal 6. This pin can be an input or an output.
12	S5	Source Terminal 5. This pin can be an input or an output.
13	V_{DD}	Most Positive Power Supply Potential.
14	GND	Ground (0 V) Reference.
15	A2	Logic Control Input.
16	A1	Logic Control Input.

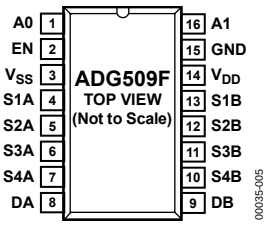


Figure 4. ADG509F Pin Configuration

Table 6. ADG509F Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Logic Control Input.
2	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
4	S1A	Source Terminal 1A. This pin can be an input or an output.
5	S2A	Source Terminal 2A. This pin can be an input or an output.
6	S3A	Source Terminal 3A. This pin can be an input or an output.
7	S4A	Source Terminal 4A. This pin can be an input or an output.
8	DA	Drain Terminal A. This pin can be an input or an output.
9	DB	Drain Terminal B. This pin can be an input or an output.
10	S4B	Source Terminal 4B. This pin can be an input or an output.
11	S3B	Source Terminal 3B. This pin can be an input or an output.
12	S2B	Source Terminal 2B. This pin can be an input or an output.
13	S1B	Source Terminal 1B. This pin can be an input or an output.
14	V_{DD}	Most Positive Power Supply Potential.
15	GND	Ground (0 V) Reference.
16	A1	Logic Control Input.

TYPICAL PERFORMANCE CHARACTERISTICS

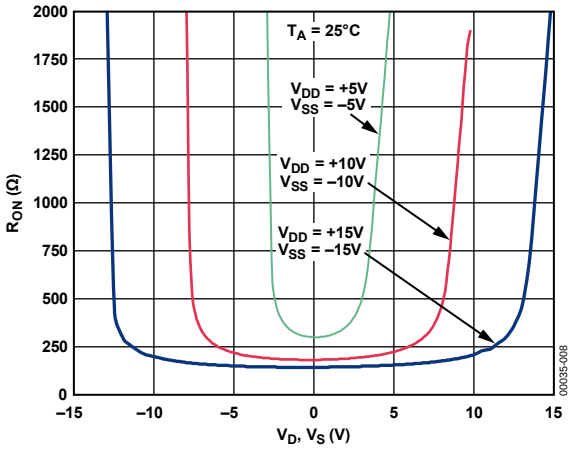


Figure 5. On Resistance as a Function of V_D (V_S)

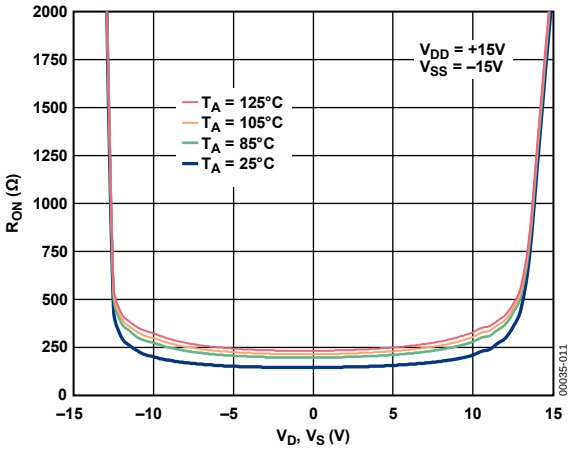


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures

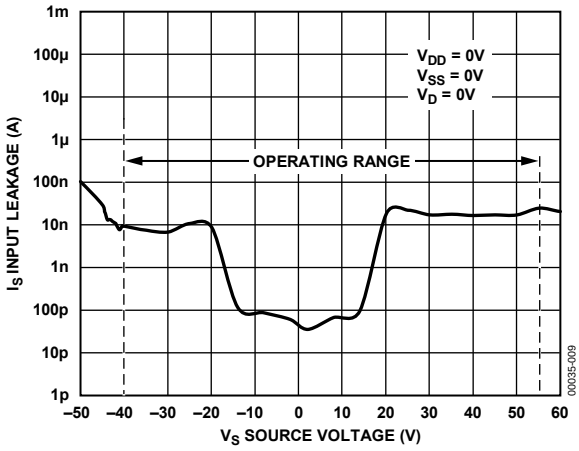


Figure 6. Source Input Leakage Current as a Function of V_S (Power Supplies Off) During Overvoltage Conditions

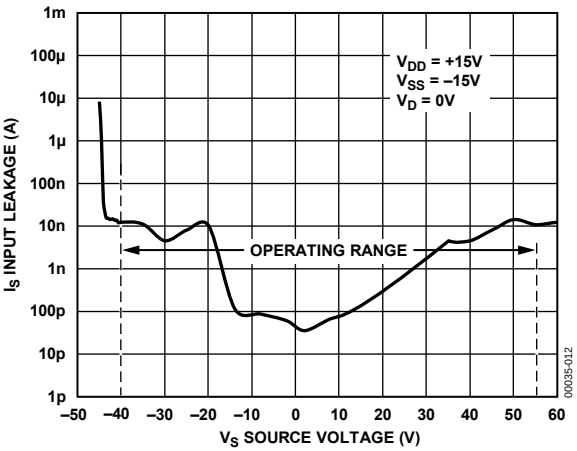


Figure 9. Source Input Leakage Current as a Function of V_S (Power Supplies On) During Overvoltage Conditions

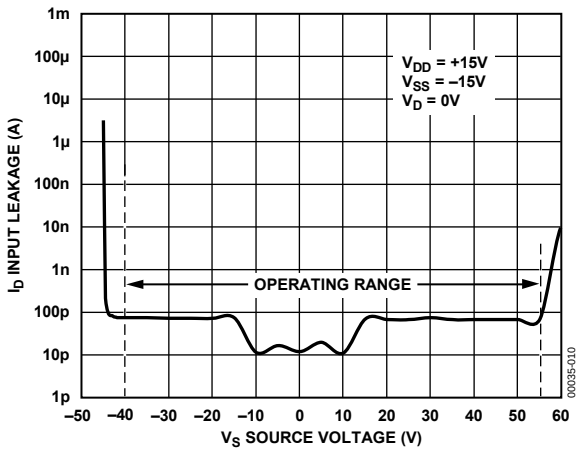


Figure 7. Drain Output Leakage Current as a Function of V_S (Power Supplies On) During Overvoltage Conditions

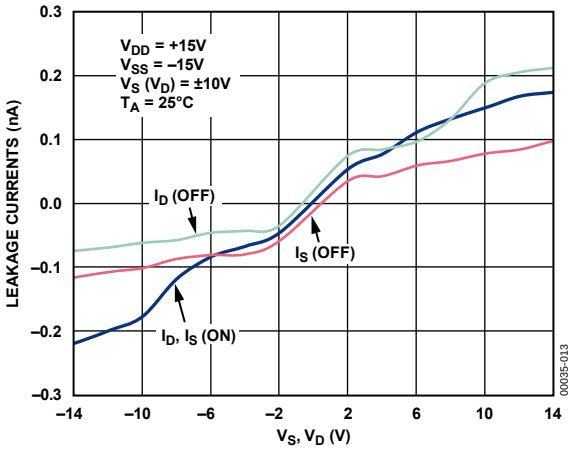


Figure 10. Leakage Currents as a Function of V_D (V_S)

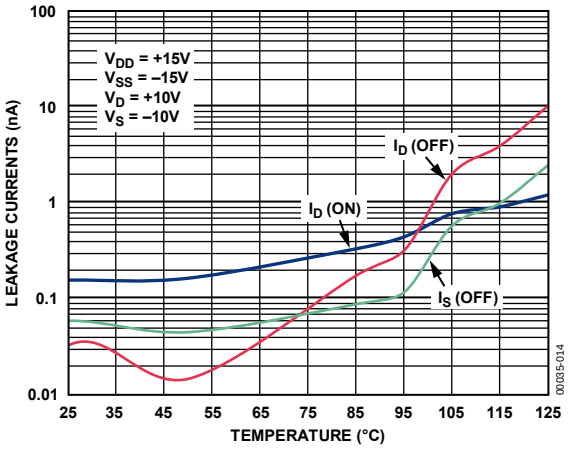


Figure 11. Leakage Currents as a Function of Temperature

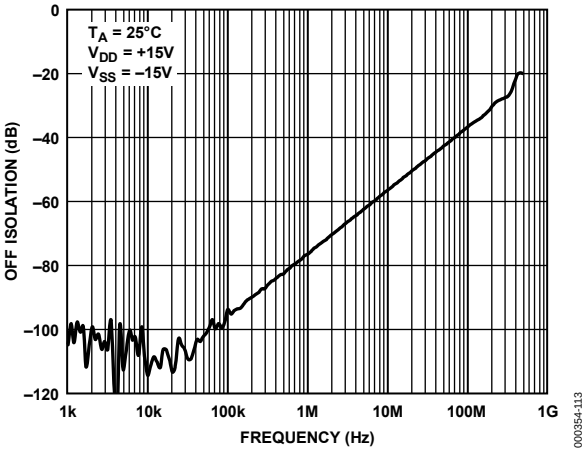


Figure 14. Off Isolation vs. Frequency, ±15 V Dual Supply

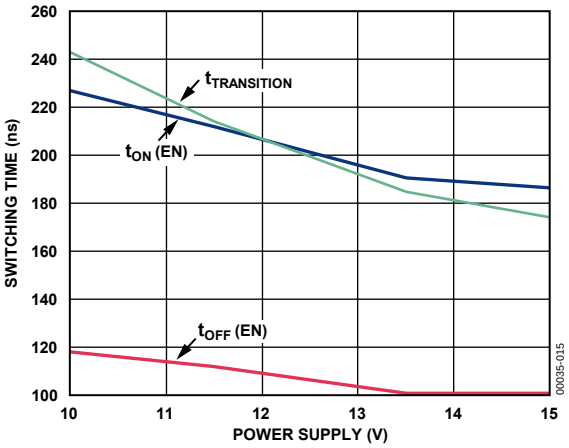


Figure 12. Switching Time vs. Dual Power Supply

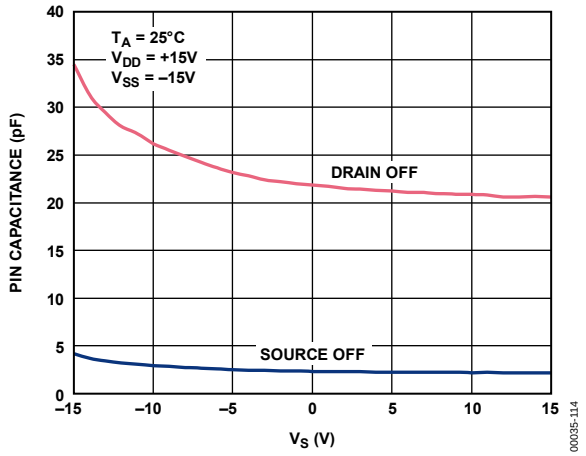


Figure 15. Capacitance vs. Source Voltage

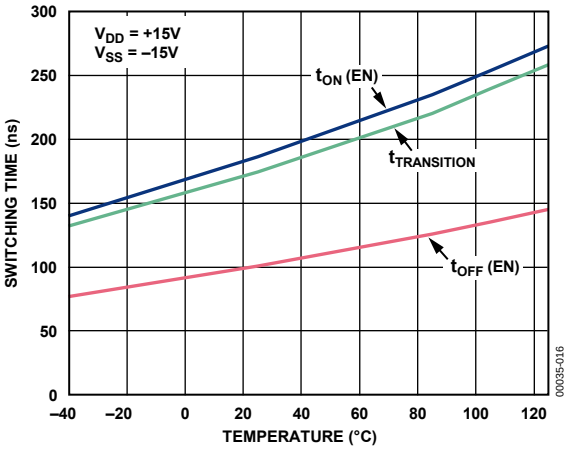


Figure 13. Switching Time vs. Temperature

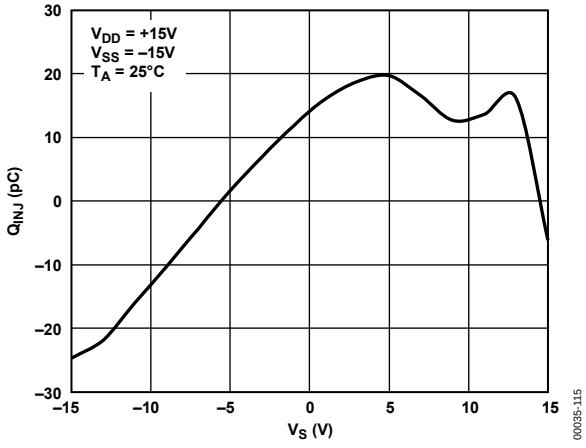


Figure 16. Charge Injection vs. Source Voltage

TERMINOLOGY

V_{DD}
Most positive power supply potential.

V_{SS}
Most negative power supply potential.

GND
Ground (0 V) reference.

R_{ON}
Ohmic resistance between D and S.

R_{ON} Drift
Percentage change in R_{ON} when temperature changes by one degree Celsius.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels as a percentage of the maximum R_{ON} of those two channels.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

I_S (Fault—Power Supplies On)
Source leakage current when exposed to an overvoltage condition.

I_D (Fault—Power Supplies On)
Drain leakage current when exposed to an overvoltage condition.

I_S (Fault—Power Supplies Off)
Source leakage current with power supplies off.

V_D (V_S)
Analog Voltage on Terminals D, S.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_{IN}
Digital input capacitance.

t_{ON} (EN)
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{OPEN}
Off time measured between 80% points of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

THEORY OF OPERATION

The ADG508F/ADG509F multiplexers are capable of withstanding overvoltages from −40 V to +55 V, irrespective of whether the power supplies are present or not. Each channel of the multiplexer consists of an n-channel MOSFET, a p-channel MOSFET, and an n-channel MOSFET, connected in series. When the analog input exceeds the power supplies, one of the MOSFETs will saturate limiting the current. The current during a fault condition is determined by the load on the output. Figure 17 illustrates the channel architecture that enables these multiplexers to withstand continuous overvoltages.

When an analog input of V_{SS} + 2.2 V to V_{DD} − 2.2 V (output loaded, 1 mA) is applied to the ADG508F/ADG509F, the multiplexer behaves as a standard multiplexer, with specifications similar to a standard multiplexer, for example, the on-resistance is 390 Ω maximum. However, when an overvoltage is applied to the device, one of the three MOSFETs saturate.

Figure 17 to Figure 20 show the conditions of the three MOSFETs for the various overvoltage situations. When the analog input applied to an on channel approaches the positive power supply line, the n-channel MOSFET saturates because the voltage on the analog input exceeds the difference between V_{DD} and the n-channel threshold voltage (V_{TN}). When a voltage more negative than V_{SS} is applied to the multiplexer, the p-channel MOSFET will saturate because the analog input is more negative than the difference between V_{SS} and the p-channel threshold voltage (V_{TP}). Because V_{TN} is nominally 1.4 V and V_{TP} −1.4 V, the analog input range to the multiplexer is limited to V_{SS} + 1.4 V to V_{DD} − 1.4 V (output open circuit) when a ±15 V power supply is used.

When the power supplies are present but the channel is off, again either the p-channel MOSFET or one of the n-channel MOSFETs will remain off when an overvoltage occurs.

Finally, when the power supplies are off, the gate of each MOSFET will be at ground. A negative overvoltage switches on the first n-channel MOSFET but the bias produced by the overvoltage causes the p-channel MOSFET to remain turned off. With a positive overvoltage, the first MOSFET in the series will remain off because the gate to source voltage applied to this MOSFET is negative.

During fault conditions (power supplies off), the leakage current into and out of the ADG508F/ADG509F is limited to a few microamps. This protects the multiplexer and succeeding circuitry from over stresses as well as protecting the signal sources which drive the multiplexer. Also, the other channels of the multiplexer will be undisturbed by the overvoltage and will continue to operate normally.

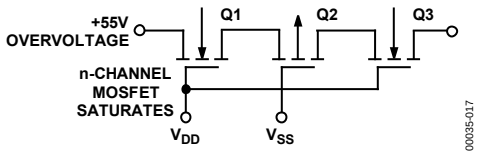


Figure 17. +55 V Overvoltage Input to the On Channel

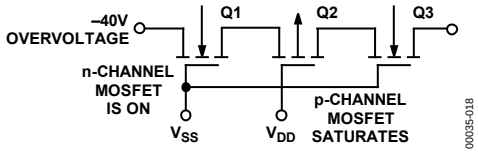


Figure 18. −40 V Overvoltage on an Off Channel with Multiplexer Power On

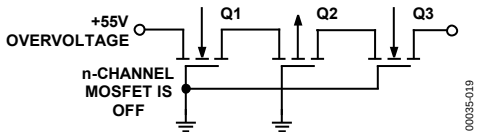


Figure 19. +55 V Overvoltage with Power Off

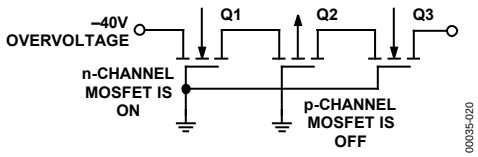


Figure 20. −40 V Overvoltage with Power Off

TEST CIRCUITS

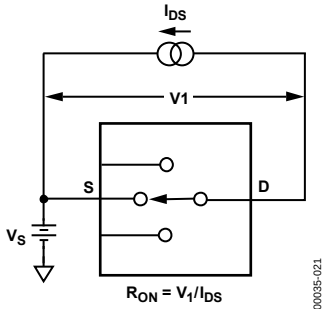


Figure 21. On Resistance

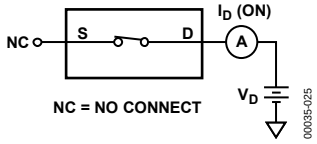


Figure 24. I_D (On)

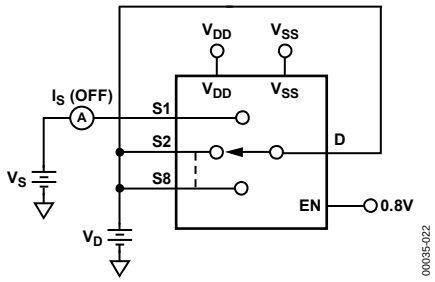


Figure 22. I_S (Off)

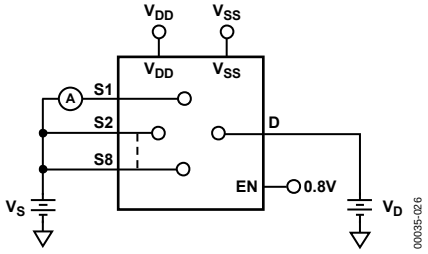


Figure 25. Input Leakage Current (with Overvoltage)

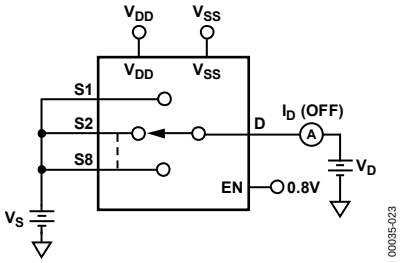


Figure 23. I_D (Off)

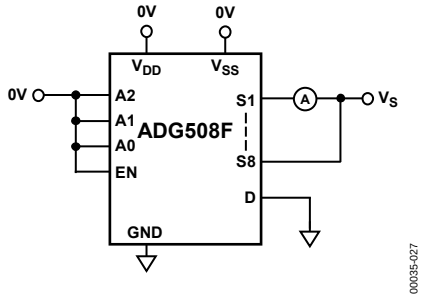


Figure 26. Input Leakage Current (with Power Supplies Off)

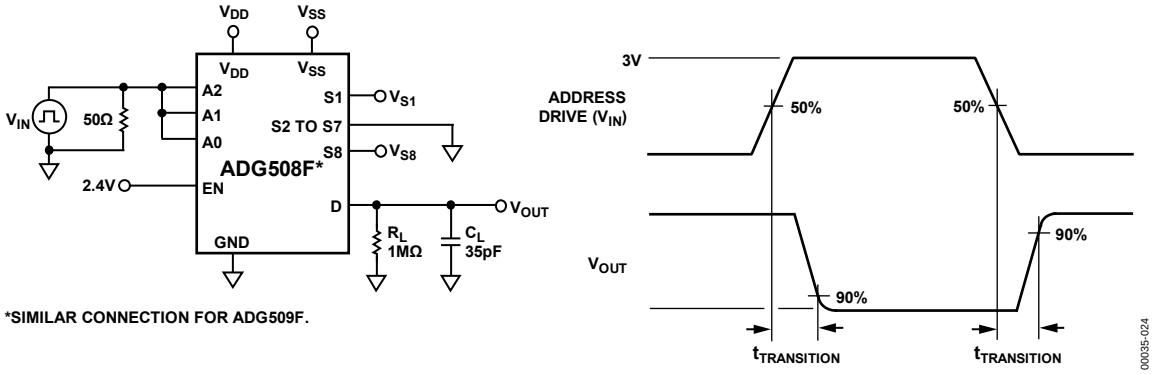


Figure 27. Switching Time of Multiplexer, $t_{TRANSITION}$

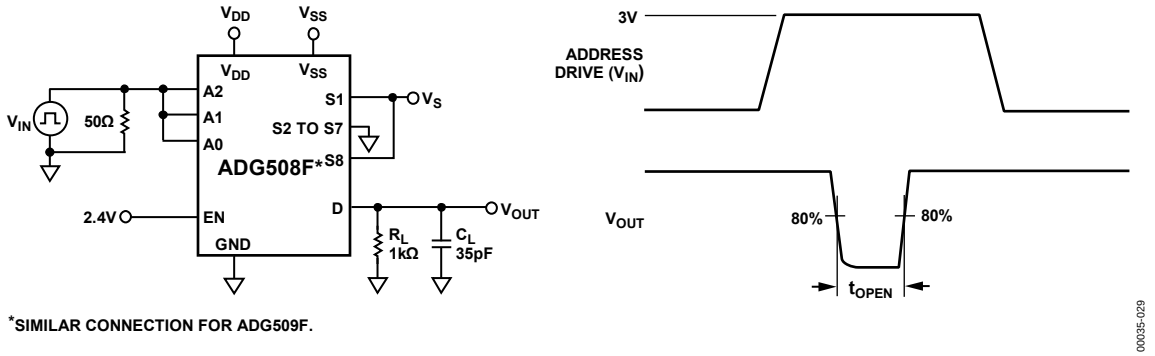


Figure 28. Break-Before-Make Delay, t_{OPEN}

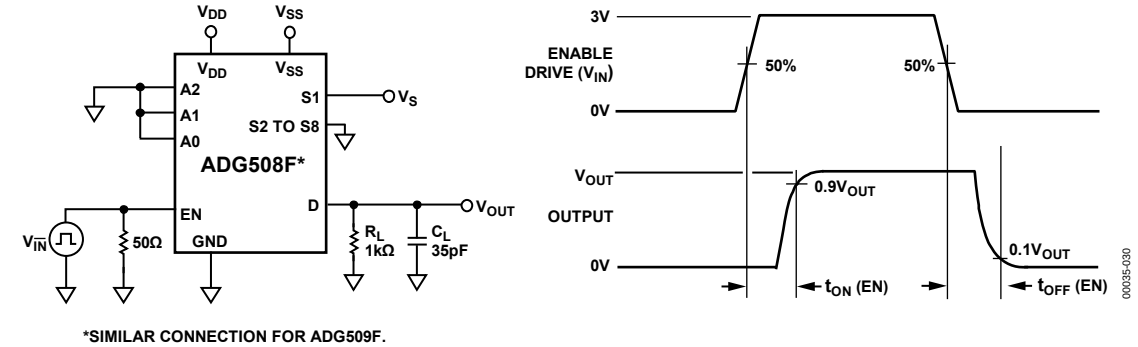


Figure 29. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

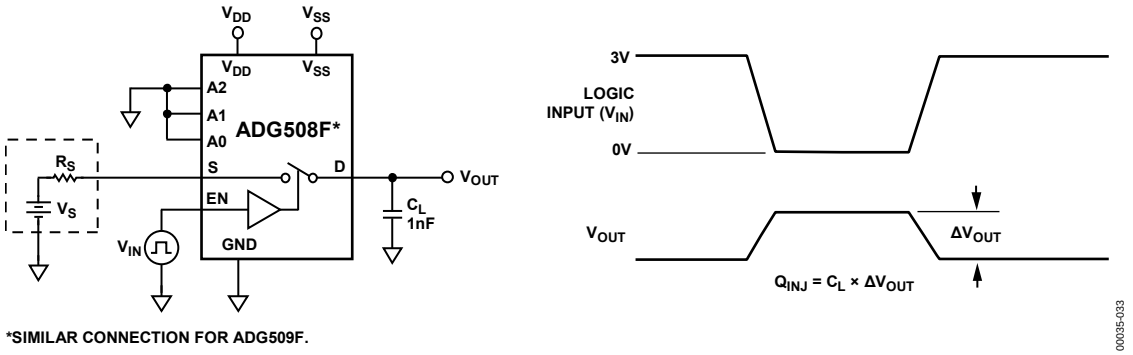


Figure 30. Charge Injection

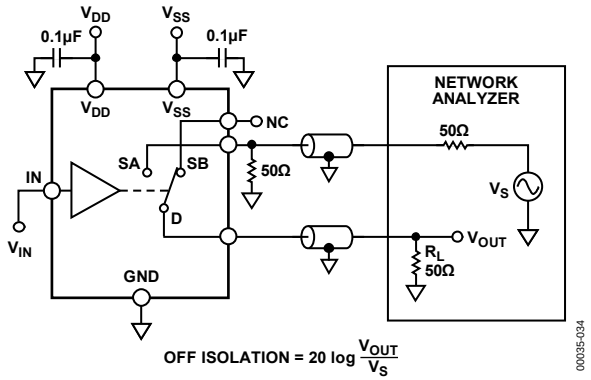
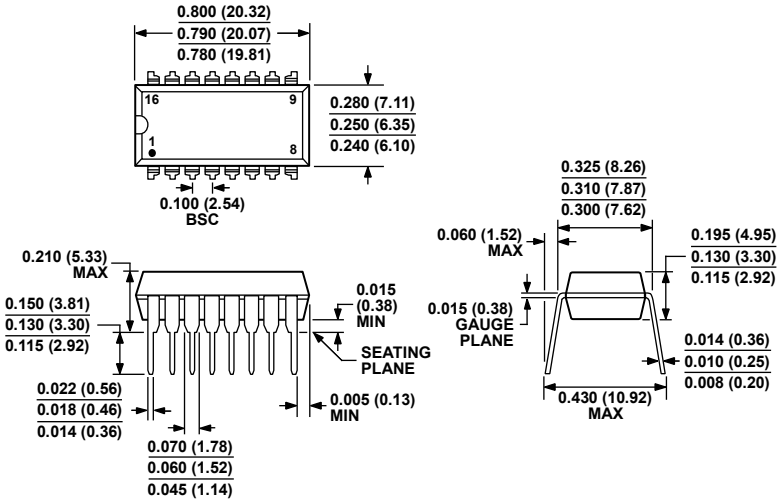


Figure 31. Off Isolation

OUTLINE DIMENSIONS

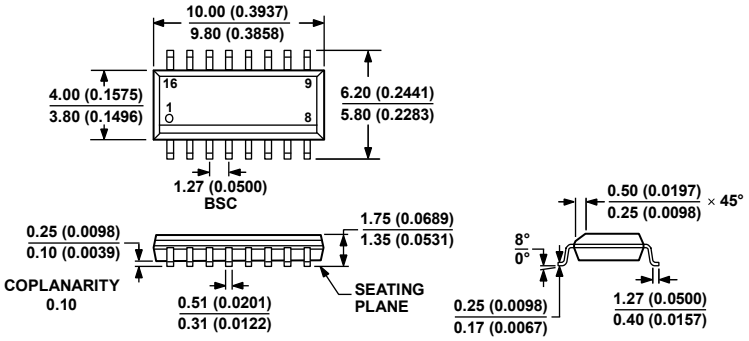


COMPLIANT TO JEDEC STANDARDS MS-001-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

073106-B

Figure 32. 16-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

060606-A

Figure 33. 16-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-16)
Dimensions shown in millimeters and (inches)

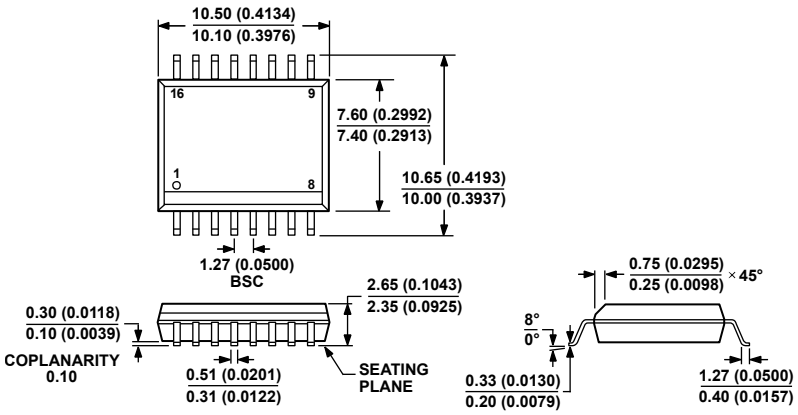


Figure 34. 16-Lead Standard Small Outline Package [SOIC_W] Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

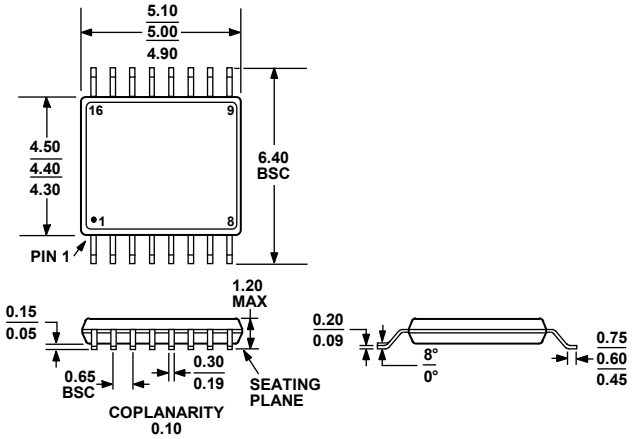


Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG508FBNZ	−40°C to +85°C	16-Lead PDIP	N-16
ADG508FBRN	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRNZ	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRNZ–REEL7	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG508FBRWZ	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADG508FBRWZ-REEL	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADG508FBRUZ	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG508FBRUZ-REEL7	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG509FBNZ	−40°C to +85°C	16-Lead PDIP	N-16
ADG509FBRN	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRNZ	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRNZ–REEL7	−40°C to +85°C	16-Lead SOIC_N	R-16
ADG509FBRWZ	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADG509FBRWZ-REEL	−40°C to +85°C	16-Lead SOIC_W	RW-16
ADG509FBRUZ	−40°C to +85°C	16-Lead TSSOP	RU-16
ADG509FBRUZ-REEL7	−40°C to +85°C	16-Lead TSSOP	RU-16

[1] Z = RoHS Compliant Part.

NOTES

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