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Data Sheet

- ADG1436: 1.5 Ω On Resistance, ± 15 V/12 V/ ± 5 V, iCMOS, Dual SPDT Switch Data Sheet

User Guides

- UG-945: Evaluation Board for 16-Lead TSSOP Devices in the Switches and Multiplexers Portfolio

Reference Materials

Informational

- iCMOS Technology Enabling the +/-10V World

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

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- PCN-PDN Information
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REVISION HISTORY

9/2016—Rev. A to Rev. B

Changes to Figure 4	8
Updated Outline Dimensions	16
Changes to Ordering Guide	16

3/2009—Rev. 0 to Rev. A

Change to I_{DD} Parameter, Table 1	3
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7/2008—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

$V_{DD} = 15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	1.5			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$; see Figure 23
	1.8	2.3	2.6	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
On-Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.18	0.19	0.21	Ω max	
On-Resistance Flatness ($R_{FLAT(ON)}$)	0.28			Ω typ	$V_S = \pm 10\text{ V}$, $I_S = -10\text{ mA}$
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	± 0.04			nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.55	± 2	± 12.5	nA max	$V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$; see Figure 24
Drain Off Leakage, I_D (Off)	± 0.04			nA typ	$V_S = \pm 10\text{ V}$, $V_D = \pm 10\text{ V}$; see Figure 24
	± 0.55	± 2	± 12.5	nA max	
Channel On Leakage, I_D , I_S (On)	± 0.1			nA typ	$V_S = V_D = \pm 10\text{ V}$; see Figure 25
	± 2	± 4	± 35	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		± 0.1	μA typ	$V_{IN} = V_{GND}$ or V_{DD}
				μA max	
Digital Input Capacitance, C_{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	125			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	170	215	245	ns max	$V_S = +10\text{ V}$; see Figure 30
t_{ON} (EN)	95			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	120	140	155	ns max	$V_S = 10\text{ V}$; see Figure 30
t_{OFF} (EN)	105			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	130	150	170	ns max	$V_S = 10\text{ V}$; see Figure 30
Break-Before-Make Time Delay, t_{BBM}	20			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			10	ns min	$V_{S1} = V_{S2} = +10\text{ V}$; see Figure 31
Charge Injection	−20			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 33
Off Isolation	−80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 26
Channel-to-Channel Crosstalk	−80			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$; see Figure 27
Total Harmonic Distortion + Noise	0.011			% typ	$R_L = 110\ \Omega$, 15 V p-p, $f = 20\text{ Hz}$ to 20 kHz; see Figure 29
−3 dB Bandwidth	110			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 28
Insertion Loss	−0.18			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28
C_S (Off)	23			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
C_D (Off)	50			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
C_D , C_S (On)	120			pF typ	$f = 1\text{ MHz}$, $V_S = 0\text{ V}$
POWER REQUIREMENTS					
I_{DD}	0.001			μA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
			1	μA max	Digital Inputs = 0 V or V_{DD}
I_{DD}	170			μA typ	Digital Input = 5 V
			285	μA max	
I_{SS}	0.001			μA typ	Digital Inputs = 0 V, 5 V, or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			$\pm 4.5/\pm 16.5$	V min/max	GND = 0 V

¹ Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

$V_{DD} = 12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V _{DD}	V	
On Resistance (R _{ON})	2.8 3.5	4.3	4.8	Ω typ Ω max	V _S = 0 V to 10 V, I _S = −10 mA; see Figure 23 V _{DD} = +10.8 V, V _{SS} = 0 V
On-Resistance Match Between Channels (ΔR _{ON})	0.13			Ω typ	V _S = 0 V to 10 V, I _S = −10 mA
	0.21	0.23	0.25	Ω max	
On-Resistance Flatness (R _{FLAT(ON)})	0.6 1.1			Ω typ Ω max	V _S = 0 V to 10 V, I _S = −10 mA
		1.2	1.3		
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.04 ±0.55	±2	±12.5	nA typ nA max	V _{DD} = 13.2 V, V _{SS} = 0 V V _S = 1 V/10 V, V _D = 10 V/1 V; see Figure 24
Drain Off Leakage, I _D (Off)	±0.04 ±0.55	±2	±12.5	nA typ nA max	V _S = 1 V/10 V, V _D = 10 V/1 V; see Figure 24
Channel On Leakage, I _D , I _S (On)	±0.1 ±1	±4	±35	nA typ nA max	V _S = V _D = 1 V or 10 V; see Figure 25
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.001		±0.1	μA typ μA max	V _{IN} = V _{GND} or V _{DD}
Digital Input Capacitance, C _{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, t _{TRANSITION}	200 270	320	350	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 8 V; see Figure 30
t _{ON} (EN)	175 235	280	310	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 8 V; see Figure 30
t _{OFF} (EN)	105 145	175	195	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 8 V; see Figure 30
Break-Before-Make Time Delay, t _{BBM}	70		10	ns typ ns min	R _L = 300 Ω, C _L = 35 pF V _{S1} = V _{S2} = 8 V; see Figure 31
Charge Injection	30			pC typ	V _S = 6 V, R _S = 0 Ω, C _L = 1 nF; see Figure 33
Off Isolation	−80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 26;
Channel-to-Channel Crosstalk	−80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 27
−3 dB Bandwidth	78			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 28
Insertion Loss	−0.3			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 28
C _S (Off)	40			pF typ	f = 1 MHz, V _S = 6 V
C _D (Off)	80			pF typ	f = 1 MHz, V _S = 6 V
C _D , C _S (On)	140			pF typ	f = 1 MHz, V _S = 6 V
POWER REQUIREMENTS					
I _{DD}	0.001		1.0	μA typ μA max	V _{DD} = 13.2 V Digital inputs = 0 V or V _{DD}
I _{DD}	170		285	μA typ μA max	Digital inputs = 5 V
V _{DD}			5/16.5	V min/max	GND = 0 V, V _{SS} = 0 V

¹ Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

$V_{DD} = 5\text{ V} \pm 10\%$, $V_{SS} = -5\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V _{DD} to V _{SS}	V	
On Resistance (R _{ON})	3.3			Ω typ	V _S = ±4.5 V, I _S = −10 mA; see Figure 23
	4	4.9	5.4	Ω max	V _{DD} = +4.5 V, V _{SS} = −4.5 V
On-Resistance Match Between Channels (ΔR _{ON})	0.13			Ω typ	V _S = ±4.5 V, I _S = −10 mA
	0.22	0.23	0.25	Ω max	
On-Resistance Flatness (R _{FLAT(ON)})	0.9			Ω typ	V _S = ±4.5 V, I _S = −10 mA
	1.1	1.24	1.31	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	±0.03			nA typ	V _{DD} = +5.5 V, V _{SS} = −5.5 V
	±0.2	±1	±12.5	nA max	V _S = ±4.5 V, V _D = ∓4.5 V; see Figure 24
Drain Off Leakage, I _D (Off)	±0.03			nA typ	
	±0.2	±1	±12.5	nA max	V _S = ±4.5 V, V _D = ∓4.5 V; see Figure 24
Channel On Leakage, I _D , I _S (On)	±0.05			nA typ	V _S = V _D = ±4.5V; see Figure 25
	±0.25	±1.5	±35	nA max	
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.001		±0.1	μA typ	V _{IN} = V _{GND} or V _{DD}
				μA max	
Digital Input Capacitance, C _{IN}	3.5			pF typ	
DYNAMIC CHARACTERISTICS ¹					
Transition Time, t _{TRANSITION}	310			ns typ	R _L = 300 Ω, C _L = 35 pF
	445	510	565	ns max	V _S = 3 V; see Figure 30
t _{ON} (EN)	255			ns typ	R _L = 300 Ω, C _L = 35 pF
	355	415	460	ns max	V _S = 3 V; see Figure 30
t _{OFF} (EN)	215			ns typ	R _L = 300 Ω, C _L = 35 pF
	305	355	400	ns max	V _S = 3 V; see Figure 30
Break-Before-Make Time Delay, t _{BBM}	80		10	ns typ	R _L = 300 Ω, C _L = 35 pF
				ns min	V _{S1} = V _{S2} = 3 V; see Figure 31
Charge Injection	30			pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 1 nF; see Figure 33
Off Isolation	−80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	−80			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 100 kHz; see Figure 27
Total Harmonic Distortion + Noise	0.03			% typ	R _L = 110 Ω, 2.5 V pp, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	85			MHz typ	R _L = 50 Ω, C _L = 5 pF; see Figure 28
Insertion Loss	−0.28			dB typ	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz; see Figure 28
C _S (Off)	33			pF typ	V _S = 0 V, f = 1 MHz
C _D (Off)	65			pF typ	V _S = 0 V, f = 1 MHz
C _D , C _S (On)	145			pF typ	V _S = 0 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	0.001		1.0	μA typ	V _{DD} = +5.5 V, V _{SS} = −5.5 V
				μA max	Digital inputs = 0 V or V _{DD}
I _{SS}	0.001		1.0	μA typ	Digital inputs = 0 V or V _{DD}
				μA max	
V _{DD} /V _{SS}			±4.5/±16.5	V min/max	GND = 0 V

¹ Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL

Table 4.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
CONTINUOUS CURRENT PER CHANNEL ¹					
15 V Dual Supply					$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
ADG1436 TSSOP	260	170	100	mA max	
ADG1436 LFCSP	400	250	120	mA max	
12 V Single Supply					$V_{DD} = 10.8\text{ V}$, $V_{SS} = 0\text{ V}$
ADG1436 TSSOP	240	160	100	mA max	
ADG1436 LFCSP	350	240	120	mA max	
5 V Dual Supply					$V_{DD} = +4.5\text{ V}$, $V_{SS} = -4.5\text{ V}$
ADG1436 TSSOP	240	160	100	mA max	
ADG1436 LFCSP	300	240	120	mA max	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 5.

Parameter	Ratings
V_{DD} to V_{SS}	35 V
V_{DD} to GND	$-0.3\text{ V to }+25\text{ V}$
V_{SS} to GND	$+0.3\text{ V to }-25\text{ V}$
Analog Inputs ¹	$V_{SS} - 0.3\text{ V to }V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	GND $- 0.3\text{ V to }V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, S or D	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel, S or D ²	Data + 15%
Operating Temperature Range Automotive (Y Version)	$-40^\circ\text{C to }+125^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance (4-Layer Board)	112°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	$260(+0/-5)^\circ\text{C}$

¹ Over voltages at IN, S, and D are clamped by internal diodes. Current must be limited to the maximum ratings given.

² See data given in Table 4.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

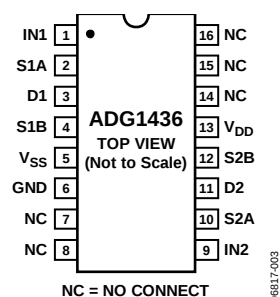
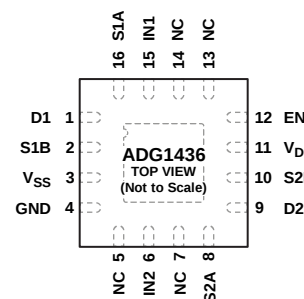


Figure 3. TSSOP Pin Configuration



NOTES
 1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS} .
 2. NC = NO CONNECT.

Figure 4. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.		Mnemonic	Function
TSSOP	LFCSP		
1	15	IN1	Logic Control Input.
2	16	S1A	Source Terminal. Can be an input or output.
3	1	D1	Drain Terminal. Can be an input or output.
4	2	S1B	Source Terminal. Can be an input or output.
5	3	V_{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14 to 16	5, 7, 13, 14	NC	No Connect.
9	6	IN2	Logic Control Input.
10	8	S2A	Source Terminal. Can be an input or output.
11	9	D2	Drain Terminal. Can be an input or output.
12	10	S2B	Source Terminal. Can be an input or output.
13	11	V_{DD}	Most Positive Power Supply Potential.
N/A	12	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, INx logic inputs determine the on switches.

TRUTH TABLE FOR SWITCHES

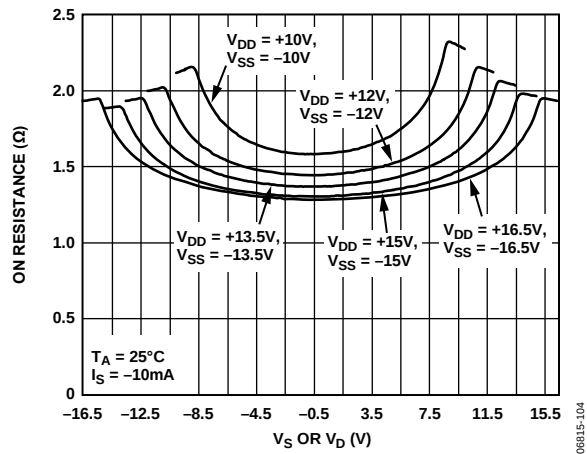
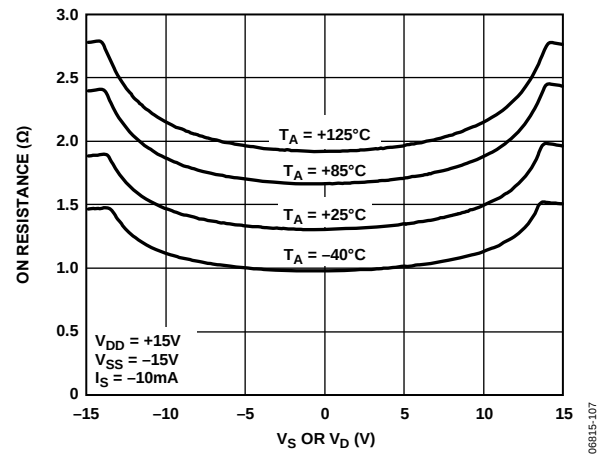
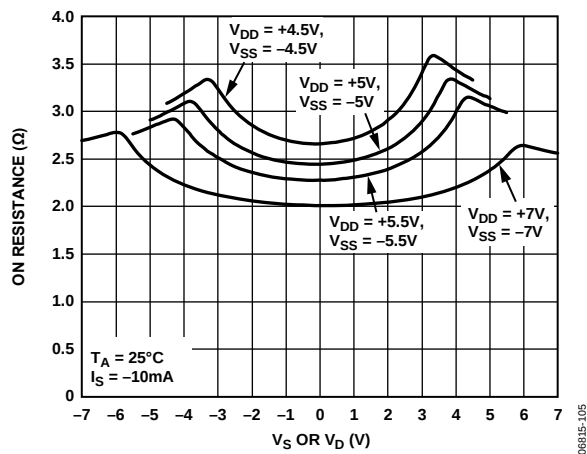
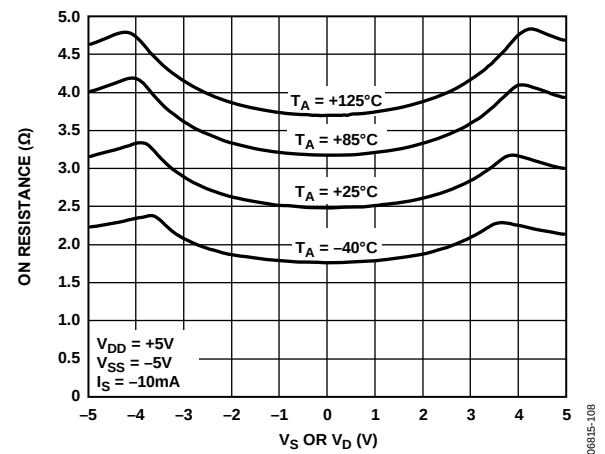
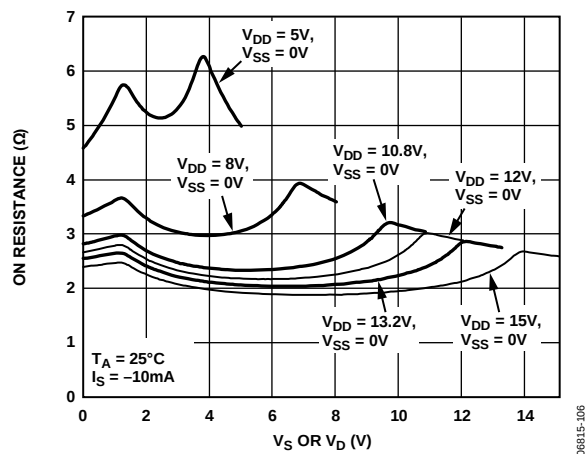
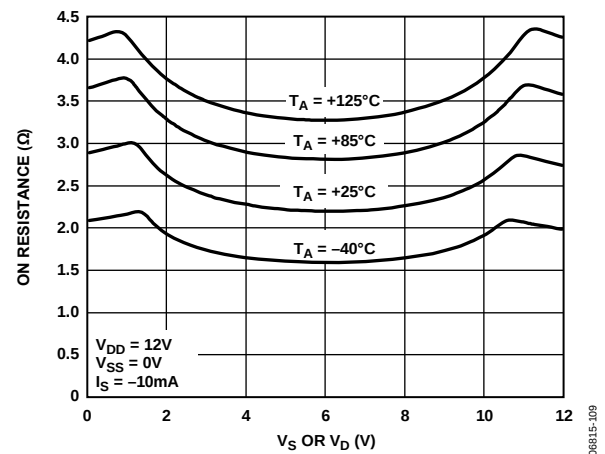
Table 7. ADG1436 TSSOP Truth Table

INx	SxA	SxB
0	Off	On
1	On	Off

Table 8. ADG1436 LFCSP Truth Table

EN	INx	SxA	SxB
0	X	Off	Off
1	0	Off	On
1	1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5. On Resistance vs. V_D or V_S , Dual SupplyFigure 8. On Resistance vs. V_D or V_S for Different Temperatures, 15 V Dual SupplyFigure 6. On Resistance vs. V_D or V_S , Dual SupplyFigure 9. On Resistance vs. V_D or V_S for Different Temperatures, 5 V Dual SupplyFigure 7. On Resistance vs. V_D or V_S , Single SupplyFigure 10. On Resistance vs. V_D or V_S for Different Temperatures, Single Supply

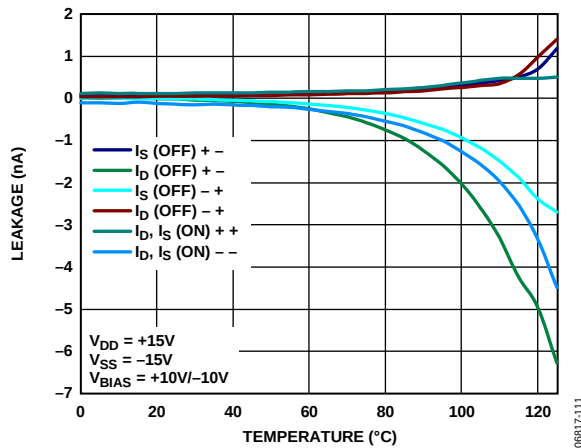


Figure 11. Leakage Currents vs. Temperature, 15 V Dual Supply

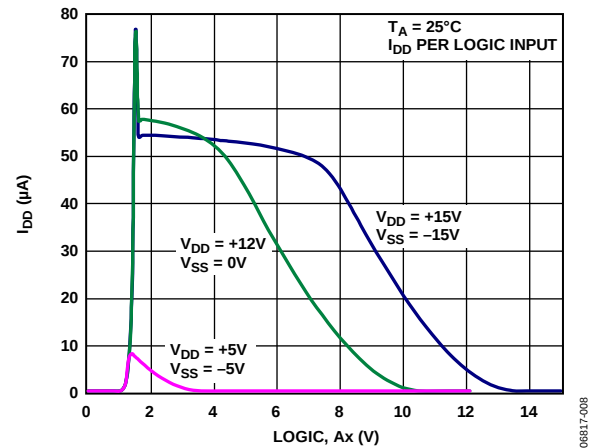
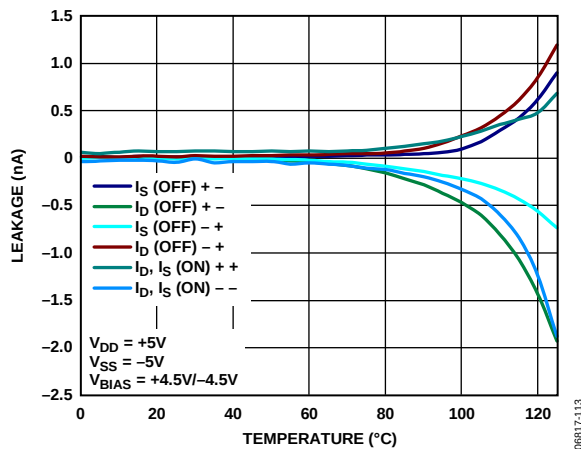
Figure 14. I_{DD} vs. Logic Level

Figure 12. Leakage Currents vs. Temperature, 5 V Dual Supply

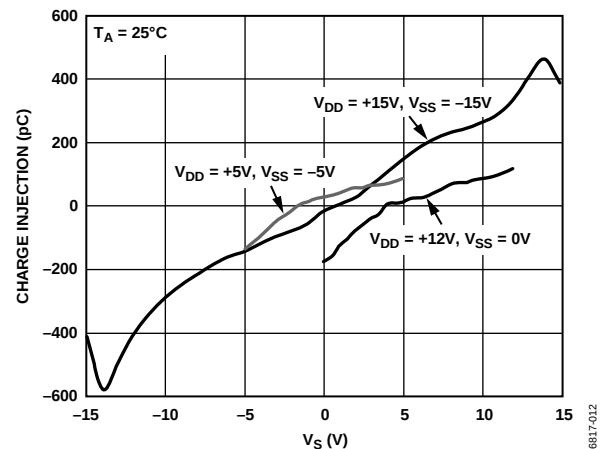


Figure 15. Charge Injection vs. Source Voltage

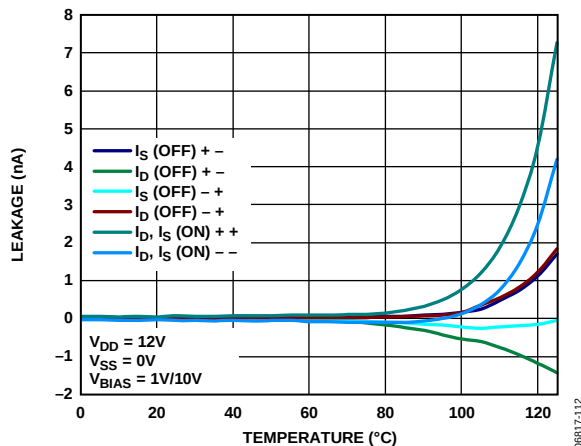
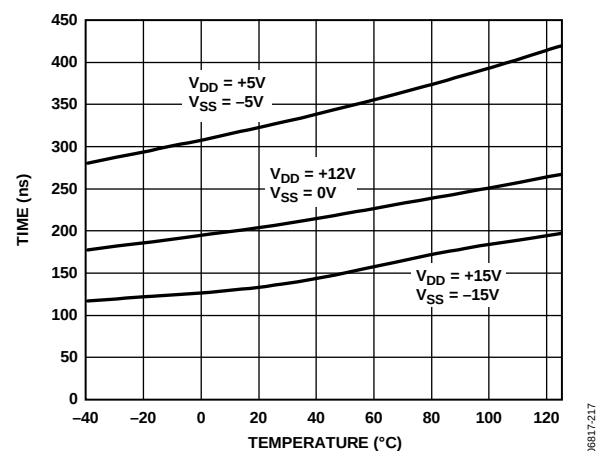


Figure 13. Leakage Currents vs. Temperature, 12 V Single Supply

Figure 16. $t_{TRANSITION}$ Time vs. Temperature

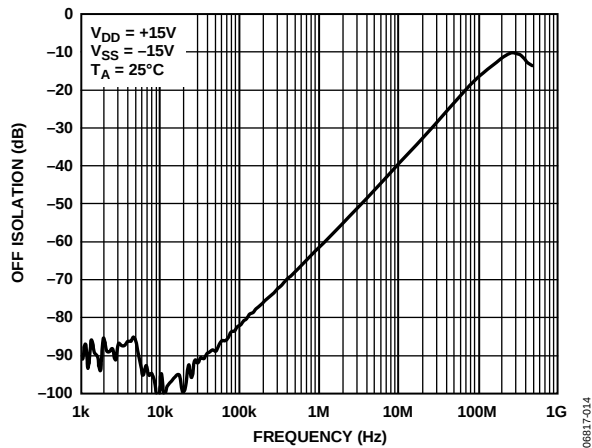


Figure 17. Off Isolation vs. Frequency

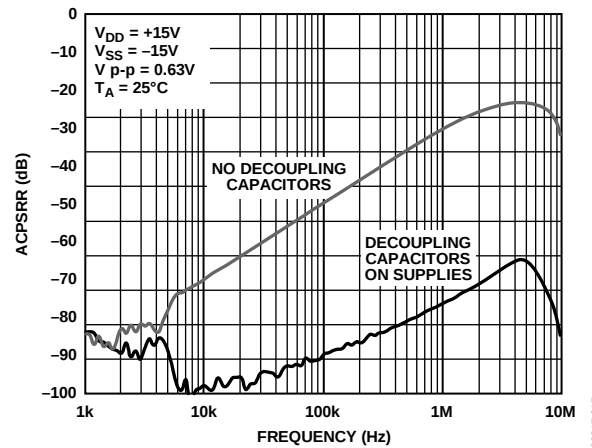


Figure 20. ACPSRR vs. Frequency

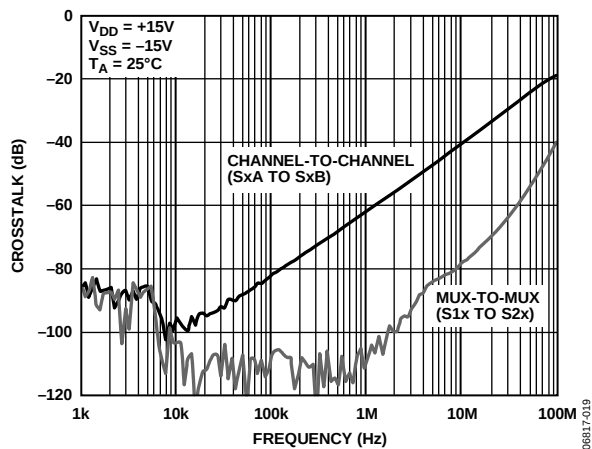


Figure 18. Crosstalk vs. Frequency

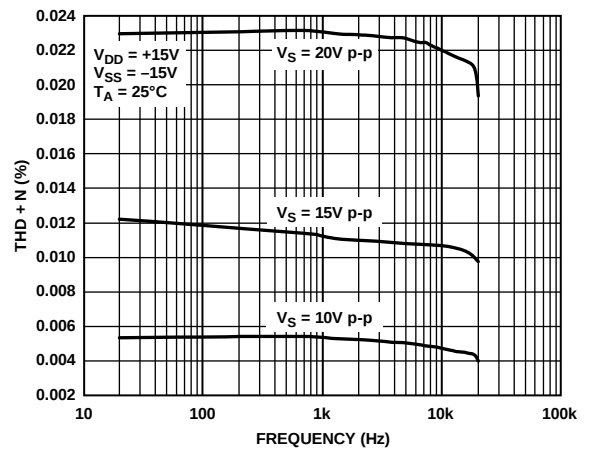


Figure 21. THD + N vs. Frequency, 15 V Dual Supply

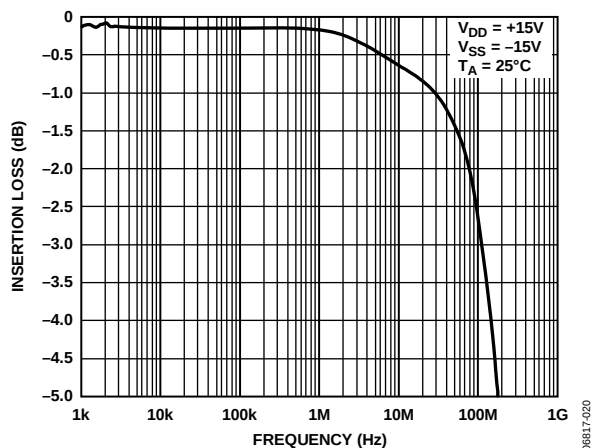


Figure 19. On Response vs. Frequency

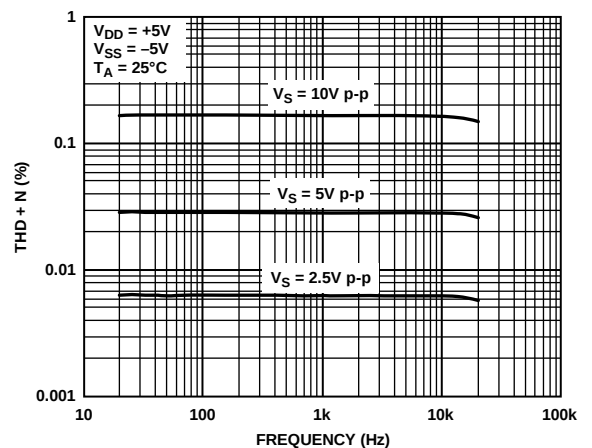


Figure 22. THD + N vs. Frequency, 5 V Dual Supply

TERMINOLOGY

I_{DD}

The positive supply current.

I_{SS}

The negative supply current.

V_D, V_S

The analog voltage on Terminal D and Terminal S.

R_{ON}

The ohmic resistance between Terminal D and Terminal S.

R_{FLAT(ON)}

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)

The source leakage current with the switch off.

I_D (Off)

The drain leakage current with the switch off.

I_D, I_S (On)

The channel leakage current with the switch on.

V_{INL}

The maximum input voltage for Logic 0.

V_{INH}

The minimum input voltage for Logic 1.

I_{INL}, I_{INH}

The input current of the digital input.

C_S (Off)

The off-switch source capacitance, which is measured with reference to ground.

C_D (Off)

The off-switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)

The on-switch capacitance, which is measured with reference to ground.

C_{IN}

The digital input capacitance.

t_{TRANSITION}

The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TEST CIRCUITS

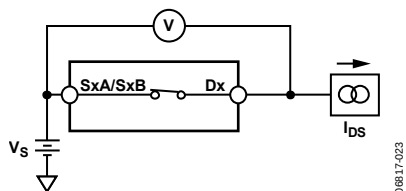


Figure 23. On Resistance

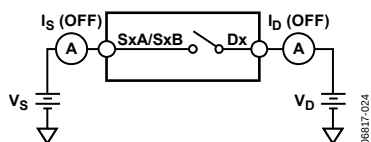


Figure 24. Off Leakage

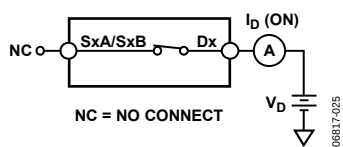


Figure 25. On Leakage

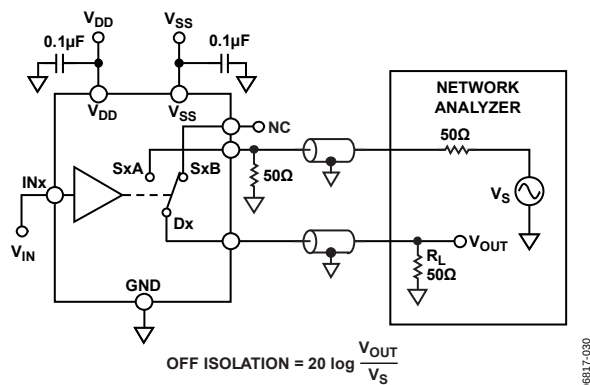


Figure 26. Off Isolation

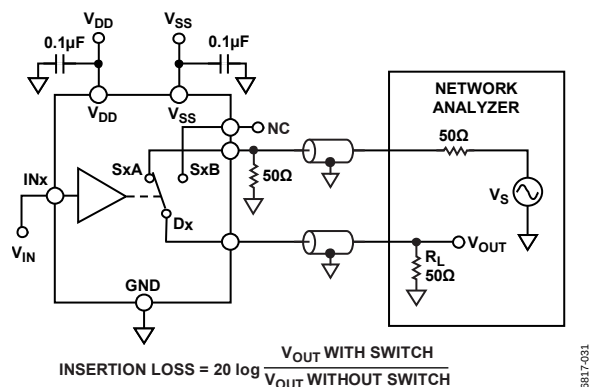


Figure 27. Channel-to-Channel Crosstalk

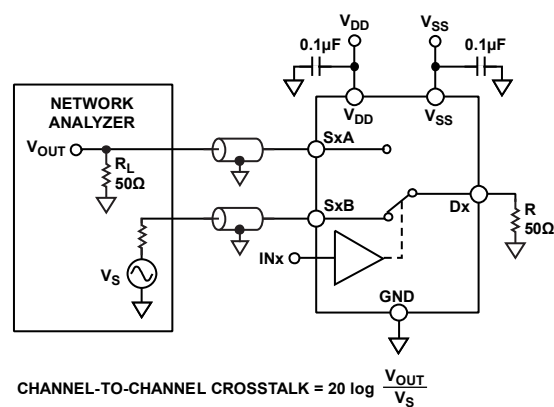


Figure 28. Bandwidth

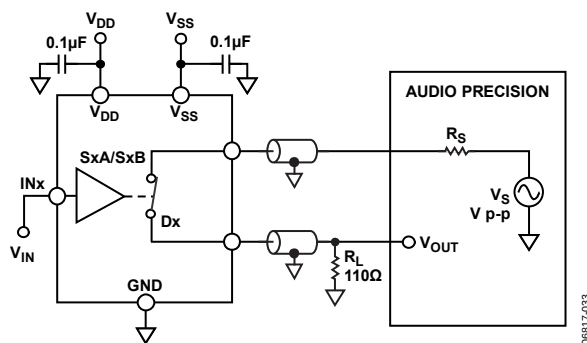


Figure 29. THD + Noise

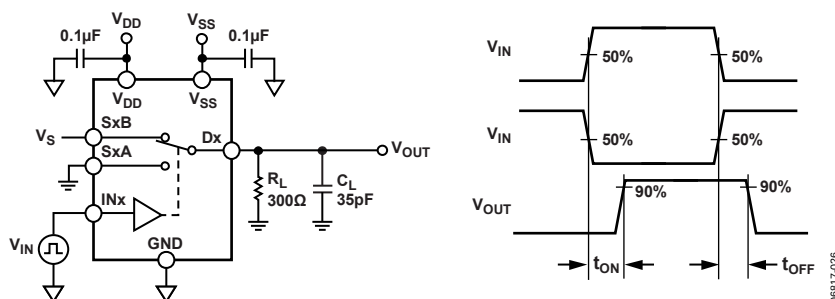


Figure 30. Switching Times

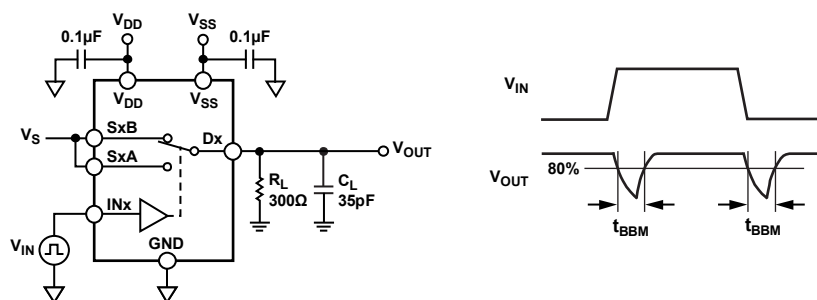


Figure 31. Break-Before-Make Time Delay

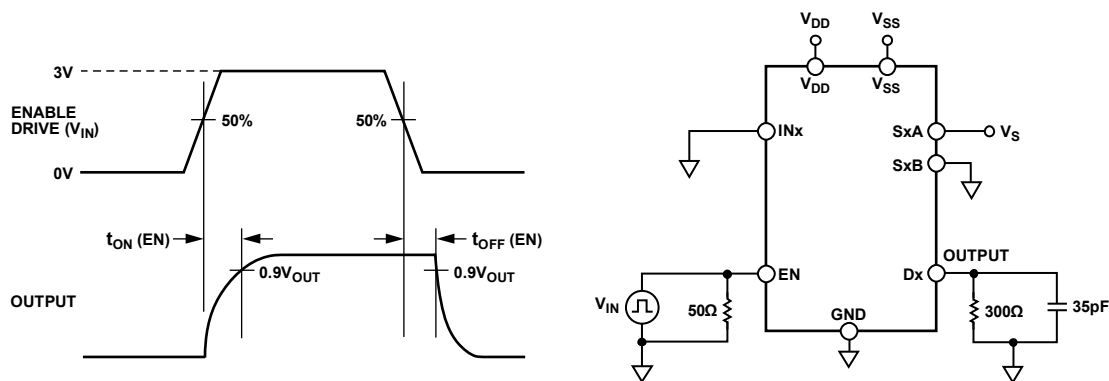
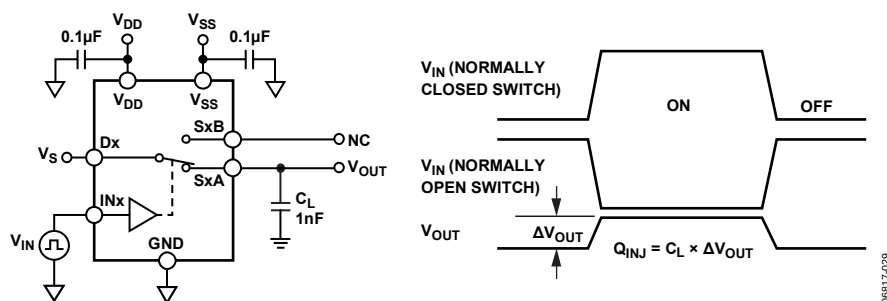
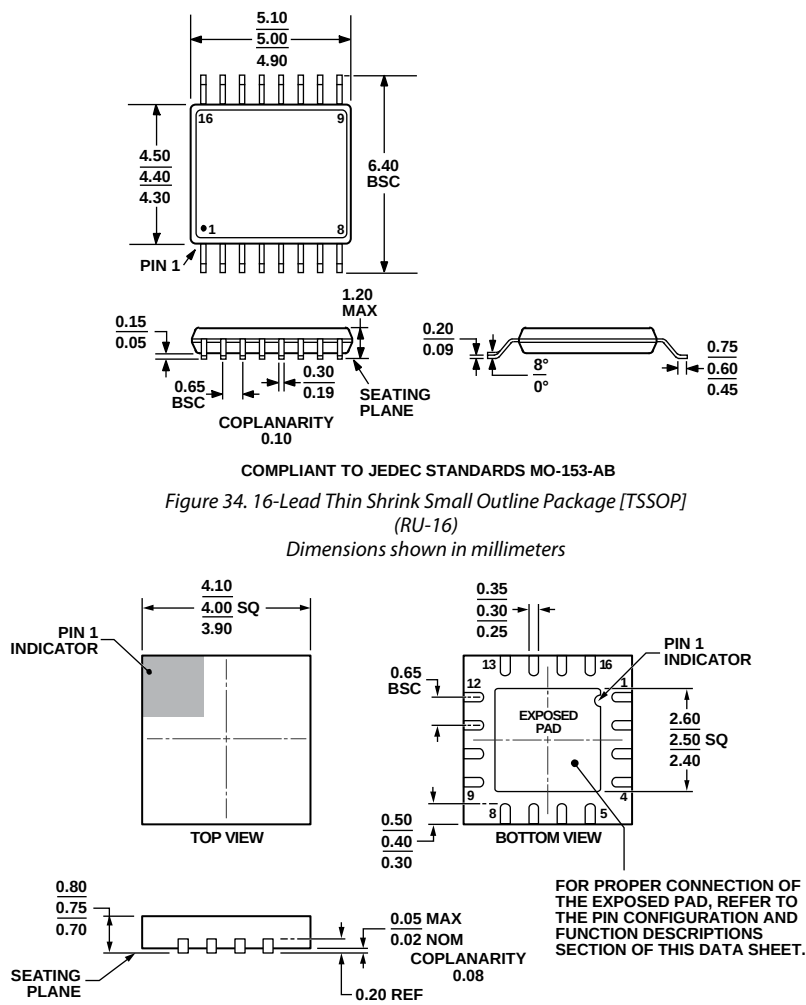
Figure 32. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$ 

Figure 33. Charge Injection

OUTLINE DIMENSIONS



ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG1436YRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1436YRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1436YCPZ-REEL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1436YCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26

¹ Z = RoHS Compliant Part.