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REVISION HISTORY

4/07—Rev. C to Rev. D

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11/05—Rev. B to Rev. C

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9/04—Rev. A to Rev. B

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3/01—Rev. 0 to Rev. A

4/00—Rev. 0: Initial Version

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SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, 5 V ± 10%; AV_{DD} ≤ V_P ≤ 6.0 V; AGND = DGND = CPGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Table 1.

Parameter	B Version[1]	Y Version[2]	Unit	Test Conditions/Comments
RF CHARACTERISTICS				
RF Input Sensitivity	−15 to 0	−10 to 0	dBm min to max	AV_{DD} = 3 V
	−10 to 0	−10 to 0	dBm min to max	AV_{DD} = 5 V
RF Input Frequency				See Figure 26 for input circuit
ADF4116	80 to 550		MHz min to max	
	45 to 550		MHz min to max	Input level = −8 dBm; for lower frequencies, ensure slew rate (SR) > 36 V/µs
ADF4117	0.1 to 1.2		GHz min to max	
ADF4118	0.1 to 3.0	0.1 to 3.0	GHz min to max	Input level = −10 dBm
	0.2 to 3.0		GHz min to max	Input level = −15 dBm
Maximum Allowable Prescaler	165	165	MHz max	AV_{DD}, DV_{DD} = 3 V
Output Frequency[3]	200	200	MHz max	AV_{DD}, DV_{DD} = 5 V
REF_{IN} CHARACTERISTICS				
Reference Input Frequency	5 to 100	5 to 100	MHz min to max	For f < 5 MHz, ensure SR > 100 V/µs
Reference Input Sensitivity[4,5]	0.4 to AV_{DD}	0.4 to AV_{DD}	V p-p min to max	AV_{DD} = 3.3 V, biased at AV_{DD}/2
	0.7 to AV_{DD}	0.7 to AV_{DD}	V p-p min to max	For f ≥ 10 MHz, AV_{DD} = 5 V, biased at AV_{DD}/2
REF_{IN} Input Capacitance	10	10	pF max	
REF_{IN} Input Current	±100	±100	µA max	
PHASE DETECTOR FREQUENCY[5]	55	55	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				
High Value	1	1	mA typ	
Low Value	250	250	µA typ	
Absolute Accuracy	2.5	2.5	% typ	
I_{CP} Three-State Leakage Current	3	25	nA max	
	1	16	nA typ	
Sink and Source Current Matching	3	3	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5
I_{CP} vs. V_{CP}	2	2	% typ	0.5 V ≤ V_{CP} ≤ V_P − 0.5
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8 × DV_{DD}	0.8 × DV_{DD}	V min	
V_{INL}, Input Low Voltage	0.2 × DV_{DD}	0.2 × DV_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	± 1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
Reference Input Current	±100	± 100	µA max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	DV_{DD} − 0.4	DV_{DD} − 0.4	V min	I_{OH} = 500 µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA

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Parameter	B Version[1]	Y Version[2]	Unit	Test Conditions/Comments
POWER SUPPLIES				
AV_{DD}	2.7 to 5.5	2.7 to 5.5	V min to V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD} to 6.0	AV_{DD} to 6.0	V min to V max	$AV_{DD} \le V_P \le 6.0$ V
I_{DD} (AI_{DD} + DI_{DD})[6]				
ADF4116	5.5		mA max	4.5 mA typical
ADF4117	5.5		mA max	4.5 mA typical
ADF4118	7.5	7.5	mA max	6.5 mA typical
I_P	0.4	0.4	mA max	T_A = 25°C
Low-Power Sleep Mode	1	1	µA typ	
NOISE CHARACTERISTICS				
ADF4118 Normalized Phase Noise Floor[7]	−213	−213	dBc/Hz typ	
Phase Noise Performance[8]				@ VCO output
ADF4116 540 MHz Output[9]	−89	−89	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4117 900 MHz Output[10]	−87	−87	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4118 900 MHz Output[10]	−90	−90	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4117 836 MHz Output[11]	−78	−78	dBc/Hz typ	@ 300 Hz offset and 30 kHz PFD frequency
ADF4118 1750 MHz Output[12]	−85	−85	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
ADF4118 1750 MHz Output[13]	−65	−65	dBc/Hz typ	@ 200 Hz offset and 10 kHz PFD frequency
ADF4118 1960 MHz Output[14]	−84	−84	dBc/Hz typ	@ 1 kHz offset and 200 kHz PFD frequency
Spurious Signals				
ADF4116 540 MHz Output[10]	−88/−99	−88/−99	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4117 900 MHz Output[10]	−90/−104	−90/−104	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4118 900 MHz Output[10]	−91/−100	−91/−100	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4117 836 MHz Output[11]	−80/−84	−80/−84	dBc typ	@ 30 kHz/60 kHz and 30 kHz PFD frequency
ADF4118 1750 MHz Output[12]	−88/−90	−88/−90	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency
ADF4118 1750 MHz Output[13]	−65/−73	−65/−73	dBc typ	@ 10 kHz/20 kHz and 10 kHz PFD frequency
ADF4118 1960 MHz Output[14]	−80/−86	−80/−86	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD frequency

[1] Operating temperature range for the B version is −40°C to +85°C.
[2] Operating temperature range for the Y version is −40°C to +125°C.
[3] This is the maximum operating frequency of the CMOS counters.
[4] AC coupling ensures $AV_{DD}/2$ bias. See Figure 35 for typical circuit.
[5] Guaranteed by design.
[6] T_A = 25°C; AV_{DD} = DV_{DD} = 3 V; RF_{IN} for ADF4116 = 540 MHz; RF_{IN} for ADF4117, ADF4118 = 900 MHz.
[7] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO, PN_{TOT}, and subtracting 20logN (where N is the N divider value) and $10\log F_{PFD}$: $PN_{SYNTH} = PN_{TOT} - 10\log F_{PFD} - 20\log N$.
[8] The phase noise is measured with the EVAL-ADF411xEB and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REF_{IN} for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).
[9] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 540 MHz; N = 2700; loop bandwidth = 20 kHz.
[10] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 900 MHz; N = 4500; loop bandwidth = 20 kHz.
[11] f_{REFIN} = 10 MHz; f_{PFD} = 30 kHz; offset frequency = 300 Hz; f_{RF} = 836 MHz; N = 27867; loop bandwidth = 3 kHz.
[12] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 1750 MHz; N = 8750; loop bandwidth = 20 kHz.
[13] f_{REFIN} = 10 MHz; f_{PFD} = 10 kHz; offset frequency = 200 Hz; f_{RF} = 1750 MHz; N = 175000; loop bandwidth = 1 kHz.
[14] f_{REFIN} = 10 MHz; f_{PFD} = 200 kHz; offset frequency = 1 kHz; f_{RF} = 1960 MHz; N = 9800; loop bandwidth = 20 kHz.

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TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = 3 V ± 10%, 5 V ± 10%; $AV_{DD} \leq V_P < 6.0$ V; AGND = DGND = CPGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Guaranteed by design, but not production tested.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B, Y Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLK setup time
t_2	10	ns min	DATA to CLK hold time
t_3	25	ns min	CLK high duration
t_4	25	ns min	CLK low duration
t_5	10	ns min	CLK to LE setup time
t_6	20	ns min	LE pulse width

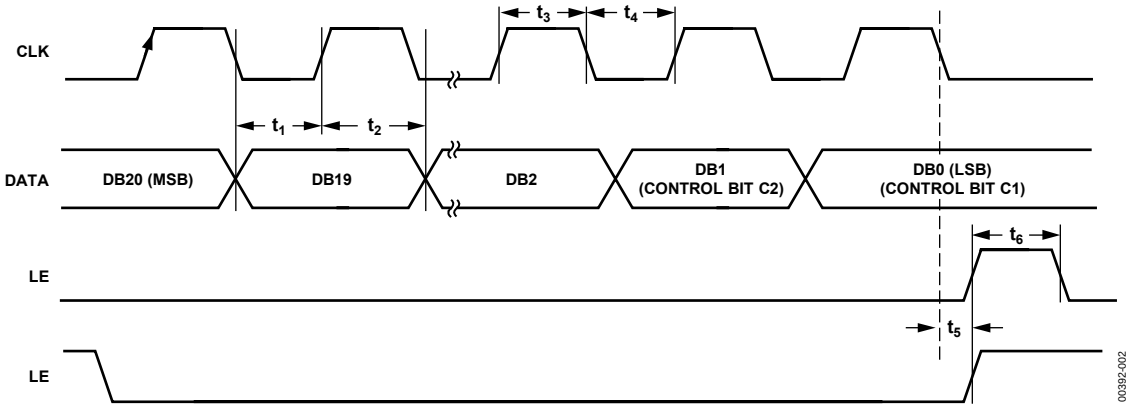

Figure 2. Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +7 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND[1]	−0.3 V to +7 V
V_P to AV_{DD}	−0.3 V to +5.5 V
Digital I/O Voltage to GND[1]	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND[1]	−0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND[1]	−0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±320 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Extended (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	112°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Transistor Count	
CMOS	6425
Bipolar	303

[1] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

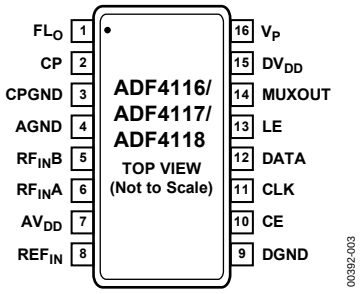

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FL_O	Fast Lock Switch Output. This can be used to switch an external resistor to change the loop filter bandwidth and speed up locking the PLL.
2	CP	Charge Pump Output. When enabled, this provides the ± I_{CP} to the external loop filter, which in turn drives the external VCO.
3	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	AGND	Analog Ground. This is the ground return path for the prescaler.
5	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 26.
6	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is ac-coupled from the VCO.
7	AV_{DD}	Analog Power Supply. This can range from 2.7 V to 5.5 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must have the same value as DV_{DD}.
8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. See Figure 25. The oscillator input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
9	DGND	Digital Ground.
10	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device depending on the status of the power-down bit F2.
11	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 21-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This input is a high impedance CMOS input.
13	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
14	MUXOUT	This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	DV_{DD}	Digital Power Supply. This can range from 2.7 V to 5.5 V. Decoupling capacitors to the digital ground plane (1 µF, 1 nF) should be placed as close as possible to this pin. For best performance, the 1 µF capacitor should be placed within 2 mm of the pin. The placing of the 1 nF capacitor is less critical, but should still be within 5 mm of the pin. DV_{DD} must have the same value as AV_{DD}.
16	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, this supply can be set to 6 V and used to drive a VCO with a tuning range of up to 6 V.

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TYPICAL PERFORMANCE CHARACTERISTICS

FREQ-UNIT	PARAM-TYPE	DATA-FORMAT	KEYWORD	IMPEDANCE-OHMS		
GHz	S	MA	R	50		
FREQ	MagS11	AngS11	FREQ	MagS11	AngS11	
0.05	0.89207	–2.0571	0.95	0.92087	–36.961	
0.10	0.8886	–4.4427	1.00	0.93788	–39.343	
0.15	0.89022	–6.3212	1.05	0.9512	–40.134	
0.20	0.96323	–2.1393	1.10	0.93458	–43.747	
0.25	0.90566	–12.13	1.15	0.94782	–44.393	
0.30	0.90307	–13.52	1.20	0.96875	–46.937	
0.35	0.89318	–15.746	1.25	0.92216	–49.6	
0.40	0.89806	–18.056	1.30	0.93755	–51.884	
0.45	0.89565	–19.693	1.35	0.96178	–51.21	
0.50	0.88538	–22.246	1.40	0.94354	–53.55	
0.55	0.89699	–24.336	1.45	0.95189	–56.786	
0.60	0.89927	–25.948	1.50	0.97647	–58.781	
0.65	0.87797	–28.457	1.55	0.98619	–60.545	
0.70	0.90765	–29.735	1.60	0.95459	–61.43	
0.75	0.88526	–31.879	1.65	0.97945	–61.241	
0.80	0.81267	–32.681	1.70	0.98864	–64.051	
0.85	0.90357	–31.522	1.75	0.97399	–66.19	
0.90	0.92954	–34.222	1.80	0.97216	–63.775	

00392-004

Figure 4. S-Parameter Data for the ADF4118 RF Input (Up to 1.8 GHz)

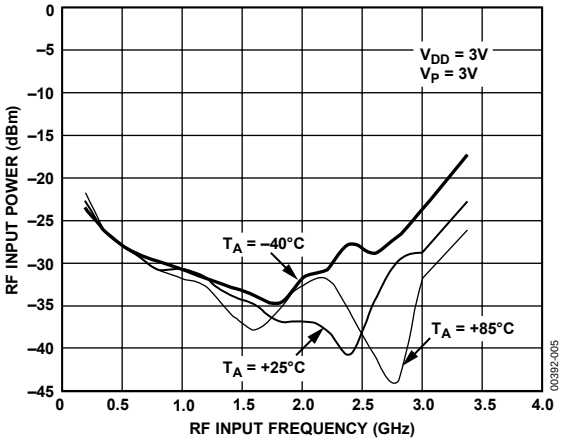

Figure 5. Input Sensitivity (ADF4118)

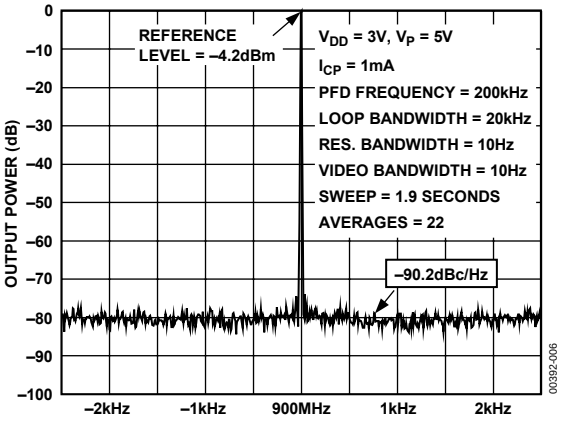

Figure 6. ADF4118 Phase Noise (900 MHz, 200 kHz, 20 kHz)

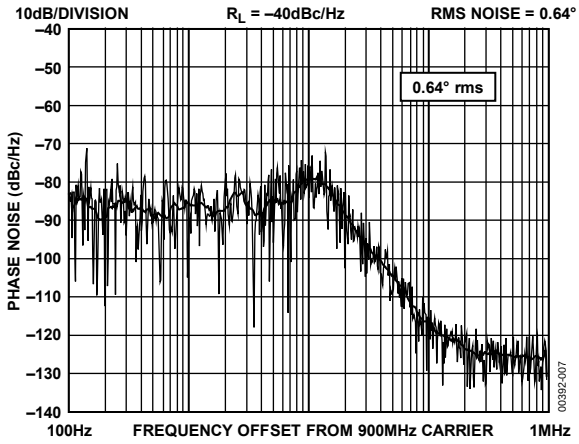

Figure 7. ADF4118 Integrated Phase Noise (900 MHz, 200 kHz, 35 kHz, Typical Lock Time: 200 µs)

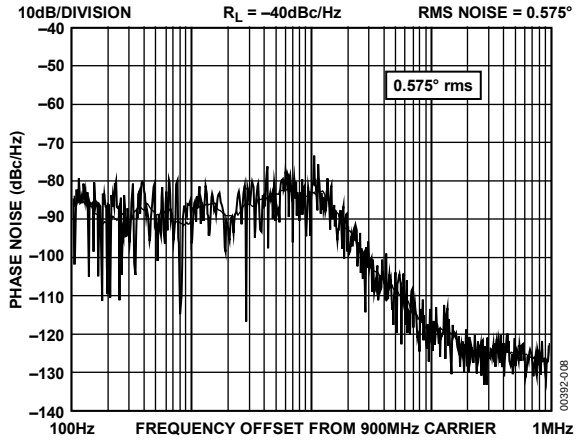

Figure 8. ADF4118 Integrated Phase Noise (900 MHz, 200 kHz, 20 kHz, Typical Lock Time: 400 µs)

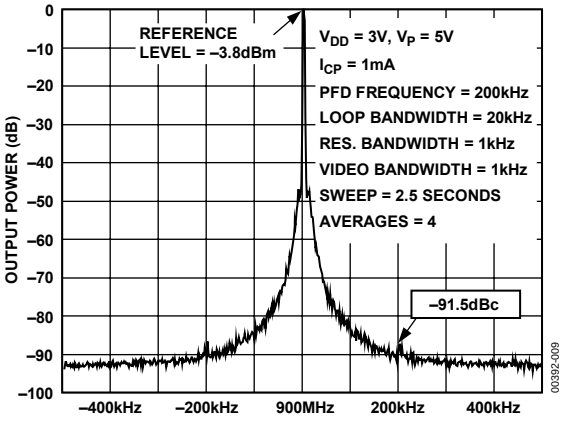

Figure 9. ADF4118 Reference Spurs (900 MHz, 200 kHz, 20 kHz)

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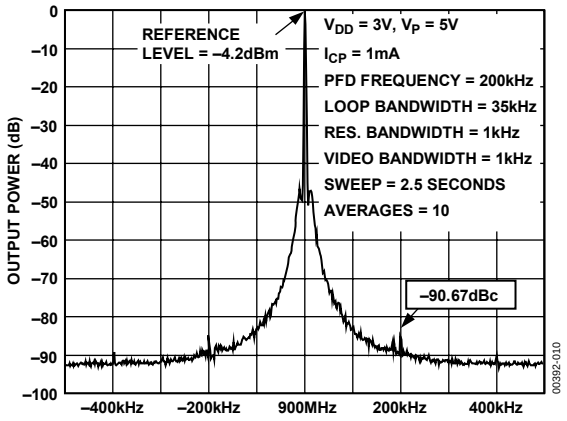

Figure 10. ADF4118 Reference Spurs (900 MHz, 200 kHz, 35 kHz)

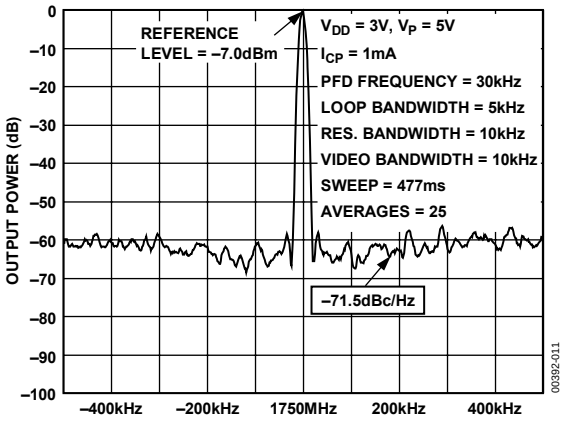

Figure 11. ADF4118 Phase Noise (1750 MHz, 30 kHz, 3 kHz)

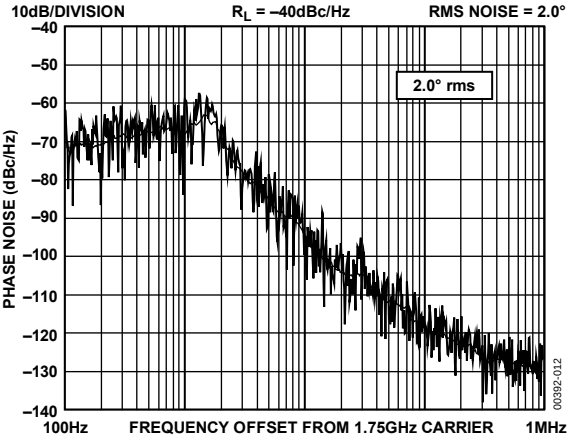

Figure 12. ADF4118 Integrated Phase Noise (1750 MHz, 30 kHz, 3 kHz)

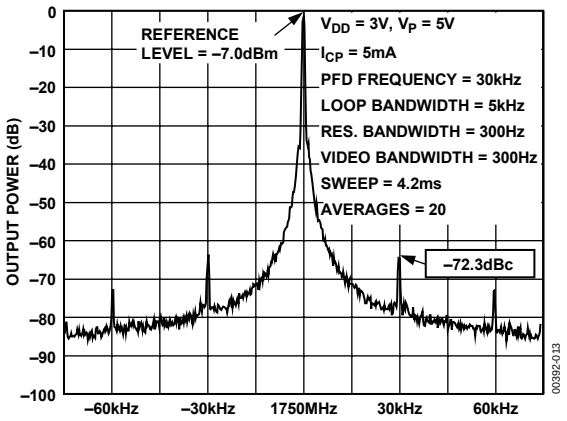

Figure 13. ADF4118 Reference Spurs (1750 MHz, 30 kHz, 3 kHz)

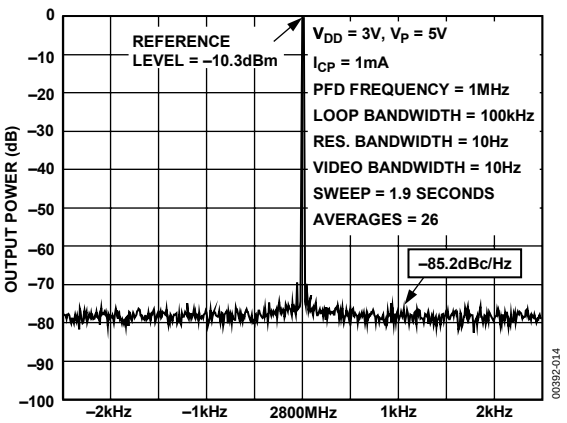

Figure 14. ADF4118 Phase Noise (2800 MHz, 1 MHz, 100 kHz)

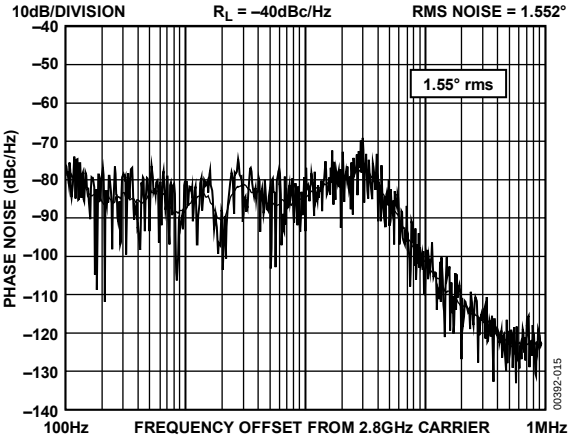

Figure 15. ADF4118 Integrated Phase Noise (2800 MHz, 1 MHz, 100 kHz)

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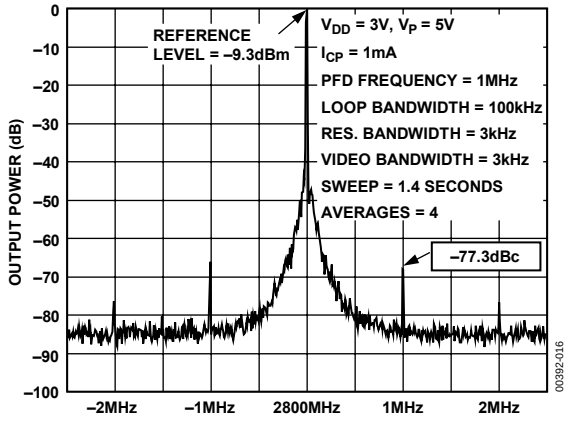

Figure 16. ADF4118 Reference Spurs (2800 MHz, 1 MHz, 100 kHz)

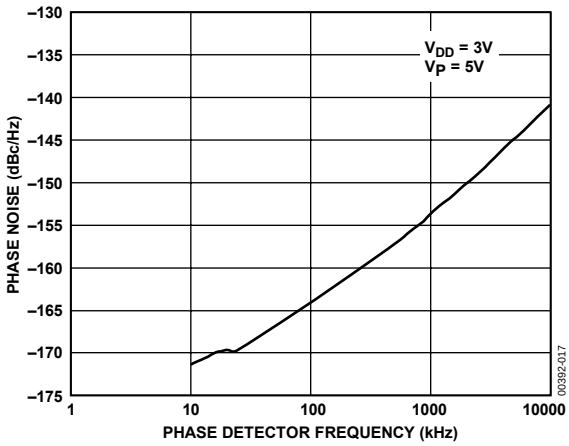

Figure 17. ADF4118 Phase Noise (Referred to CP Output) vs. PFD Frequency

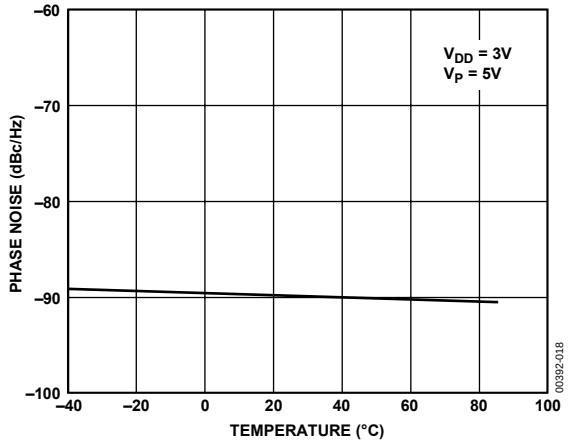

Figure 18. ADF4118 Phase Noise vs. Temperature (900 MHz, 200 kHz, 20 kHz)

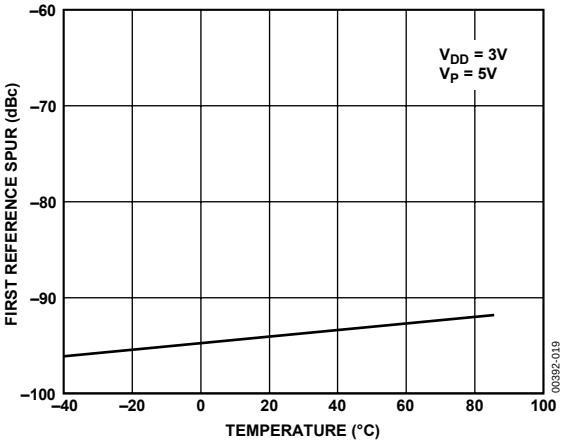

Figure 19. ADF4118 Reference Spurs vs. Temperature (900 MHz, 200 kHz, 20 kHz)

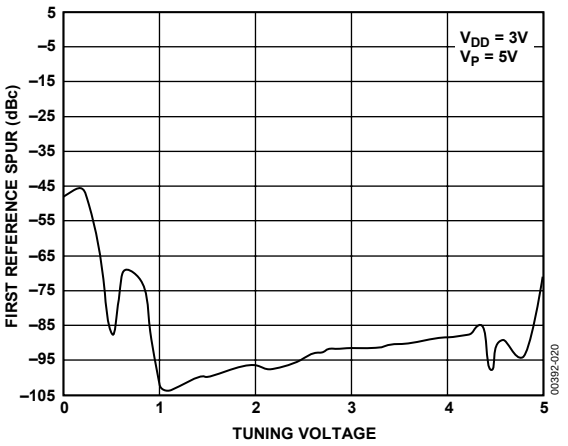

Figure 20. ADF4118 Reference Spurs (200 kHz) vs. V_{TUNE} (900 MHz, 200 kHz, 20 kHz)

Figure 21. ADF4118 Phase Noise vs. Temperature (836 MHz, 30 kHz, 3 kHz)

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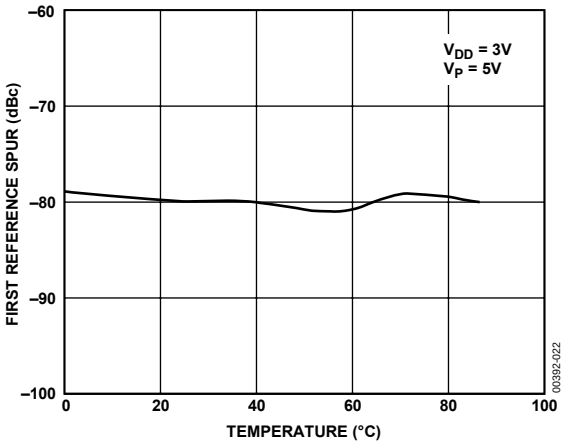

Figure 22. ADF4118 Reference Spurs vs. Temperature (836 MHz, 30 kHz, 3 kHz)

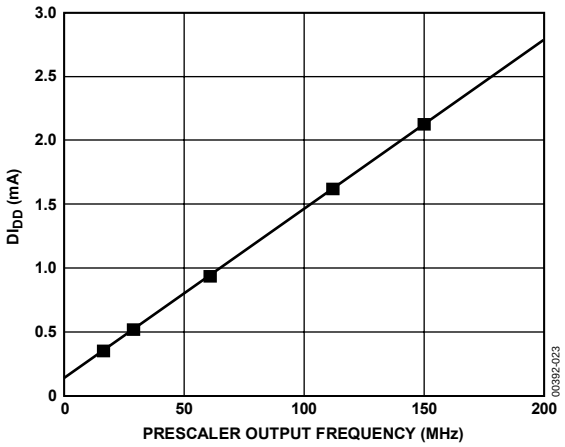

Figure 23. DI_{DD} vs. Prescaler Output Frequency

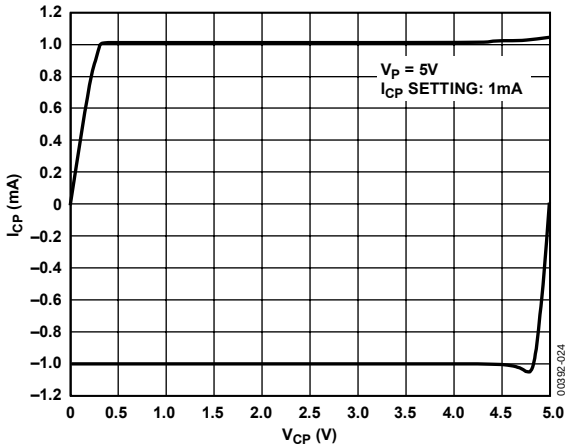

Figure 24. Charge Pump Output Characteristics

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CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 25. SW1 and SW2 are normally closed switches; SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

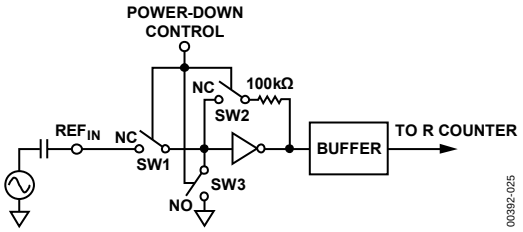

Figure 25. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 26. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

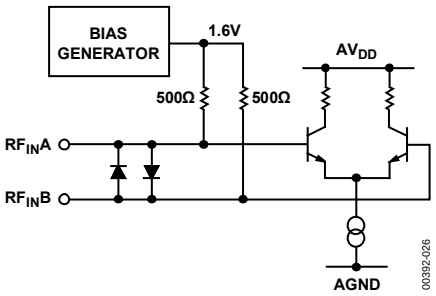

Figure 26. RF Input Stage

PRESCALER (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the A counter and B counter, enables the large division ratio, N, to be realized (N = PB + A). The dual-modulus prescaler takes the CML clock from the RF input stage and divides it down to a manageable frequency for the CMOS A counter and CMOS B counter. The prescaler is programmable. It can be set in software to 8/9 for the ADF4116 and to 32/33 for the ADF4117 and ADF4118. It is based on a synchronous 4/5 core.

A COUNTER AND B COUNTER

The A CMOS counter and B CMOS counter combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 200 MHz or less.

Pulse Swallow Function

The A counter and B counter, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times f_{REFIN} / R$$

where:

f_{VCO} is the output frequency of external voltage controlled oscillator (VCO).
P is the preset modulus of dual-modulus prescaler.
B is the preset divide ratio of binary 13-bit counter (3 to 8191).
A is the preset divide ratio of binary 5-bit swallow counter (0 to 31).
f_{REFIN} is the output frequency of the external reference frequency oscillator.
R is the preset divide ratio of binary 14-bit programmable reference counter (1 to 16,383).

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the input clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

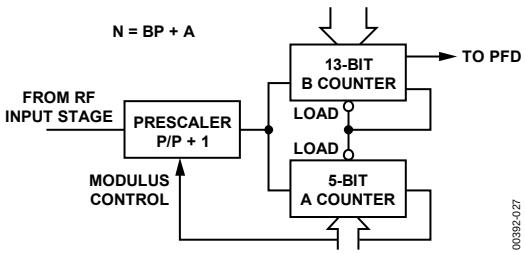

Figure 27. A Counter and B Counter

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PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 28 is a simplified schematic of the PFD. The PFD includes a fixed delay element that sets the width of the antibacklash pulse. This is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

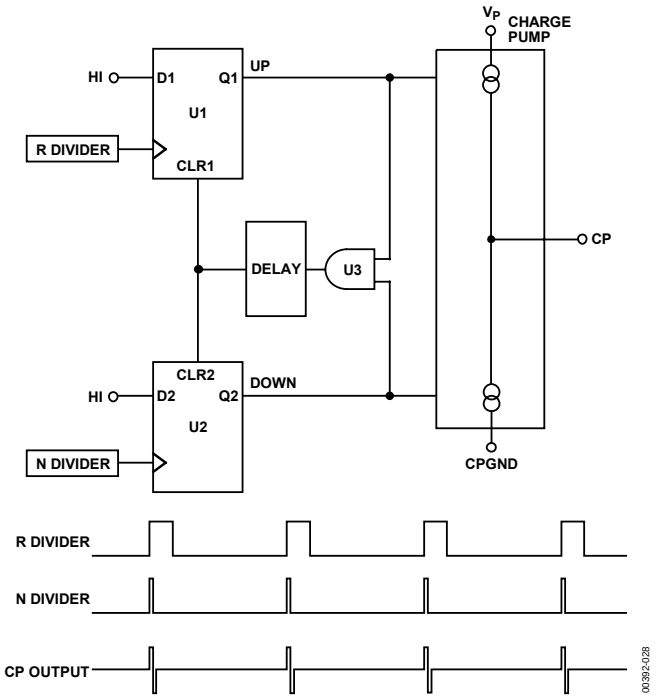

Figure 28. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF411x family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 33 shows the full truth table. Figure 29 shows the MUXOUT section in block diagram form.

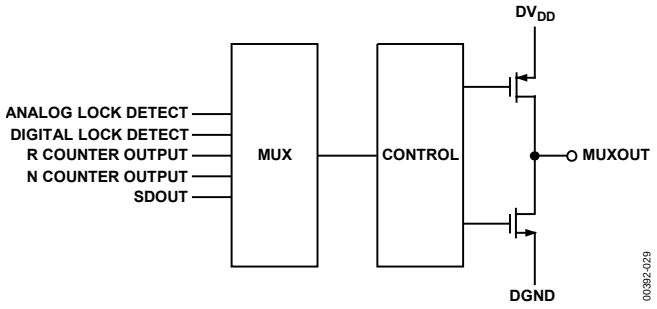

Figure 29. MUXOUT Circuit

Lock Detect

MUXOUT can be programmed for both digital lock detect and analog lock detect.

Digital lock detect is active high. It is set high when the phase error on three consecutive phase detector cycles is less than 15 ns. It stays set high until a phase error greater than 25 ns is detected on any subsequent PD cycle.

The N channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock is detected, it is high with narrow low going pulses.

INPUT SHIFT REGISTER

The ADF411x family digital section includes a 21-bit input shift register, a 14-bit R counter, and an 18-bit N counter, comprising a 5-bit A counter and a 13-bit B counter. Data is clocked into the 21-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram in Figure 2. The truth table for these bits is shown in Figure 34. Table 5 summarizes how the latches are programmed.

Table 5. Programming Data Latches

Control Bits		
C2	**C1**	**Data Latch**
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch
1	1	Initialization Latch

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LATCH SUMMARIES

REFERENCE COUNTER LATCH

LOCK DETECT PRECISION	TEST MODE BITS				14-BIT REFERENCE COUNTER, R														CONTROL BITS	
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LDP	T4	T3	T2	T1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

AB COUNTER LATCH

CP GAIN	13-BIT B COUNTER													5-BIT A COUNTER					CONTROL BITS	
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

RESERVED	POWER-DOWN 2	RESERVED			TIMER COUNTER CONTROL				FASTLOCK MODE	RESERVED	FASTLOCK ENABLE	CP THREE-STATE	PHASE DETECTOR POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	PD2	X	X	X	TC4	TC3	TC2	TC1	F6	X	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

RESERVED	POWER-DOWN 2	RESERVED			TIMER COUNTER CONTROL				FASTLOCK MODE	RESERVED	FASTLOCK ENABLE	CP THREE-STATE	PHASE DETECTOR POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	PD2	X	X	X	TC4	TC3	TC2	TC1	F6	X	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

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Figure 30. ADF411x family Latch Summary

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LATCH MAPS

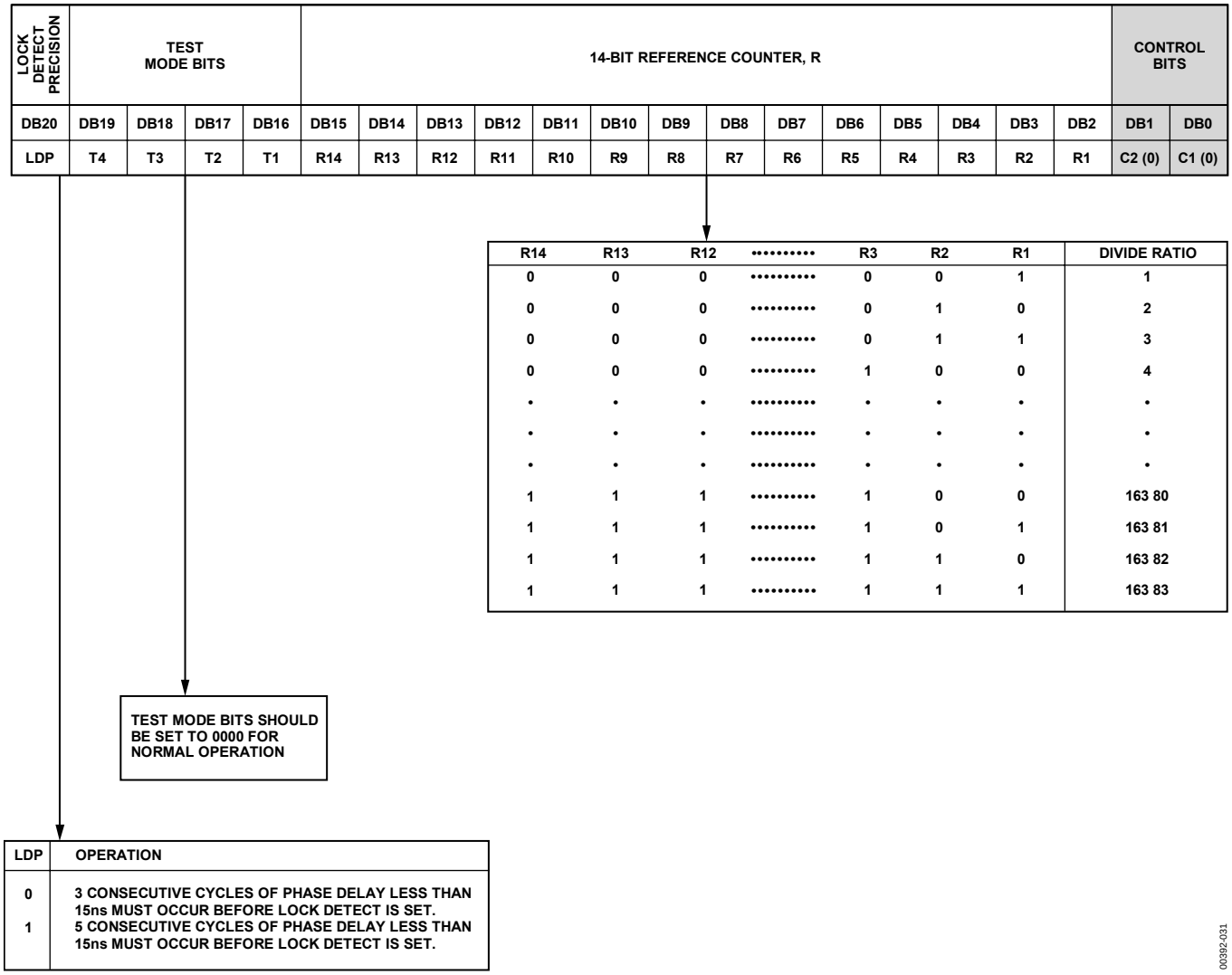

Figure 31. Reference Counter Latch Map

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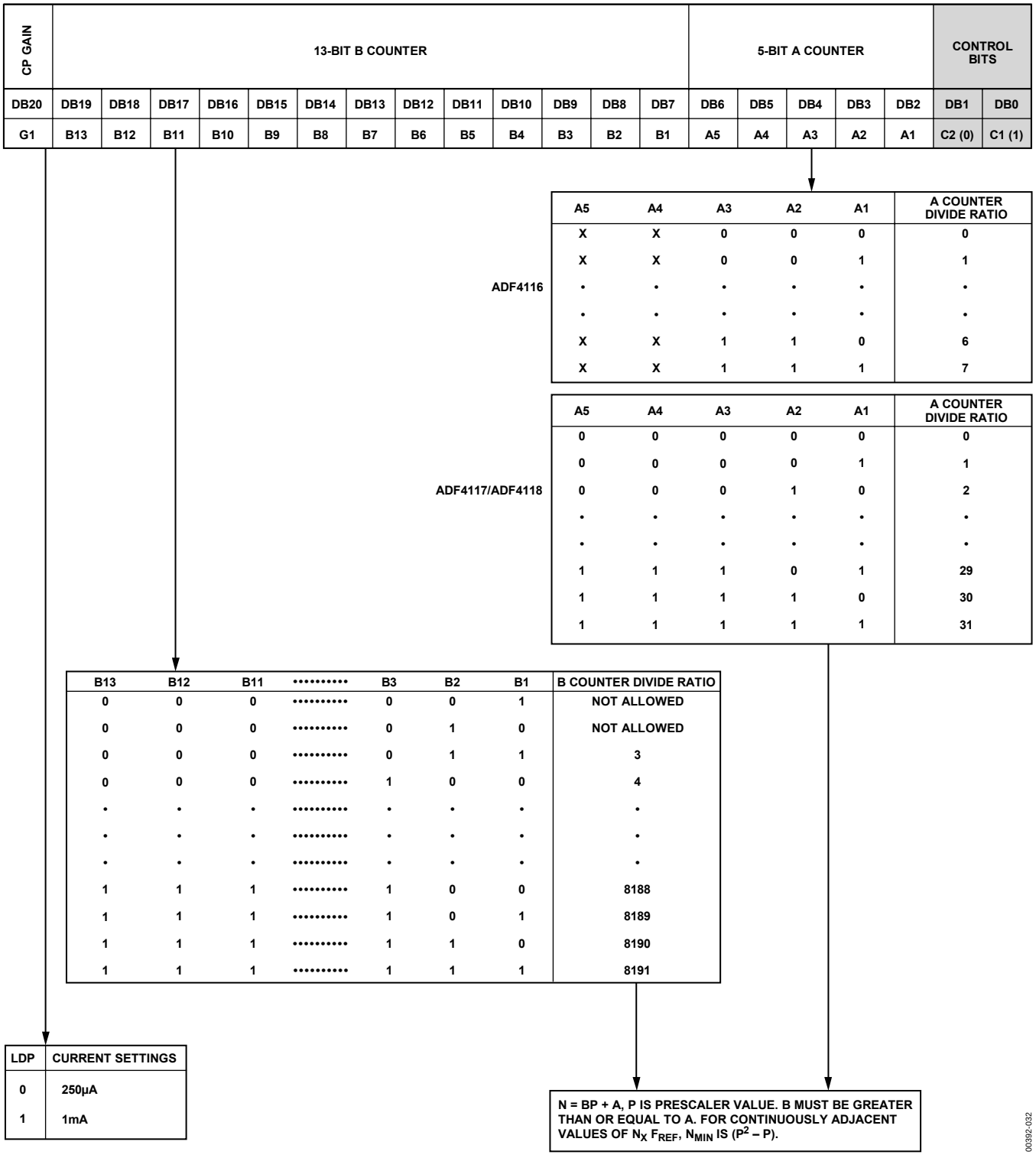

Figure 32. A Counter/B Counter Latch Map

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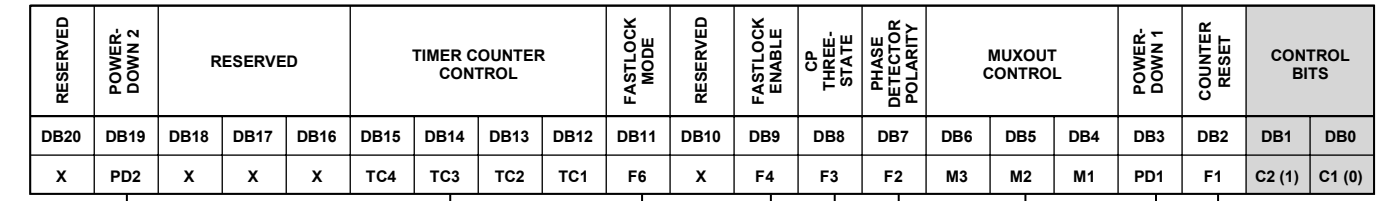

RESERVED	POWER-DOWN 2	RESERVED			TIMER COUNTER CONTROL				FASTLOCK MODE	RESERVED	FASTLOCK ENABLE	CP THREE-STATE	PHASE DETECTOR POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	PD2	X	X	X	TC4	TC3	TC2	TC1	F6	X	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	AV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	ANALOG LOCK DETECT (N CHANNEL OPEN DRAIN)
1	1	0	SERIAL DATA OUTPUT (INVERSE POLARITY OF SERIAL DATA INPUT)
1	1	1	DGND

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F6	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

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Figure 33. Function Latch Map

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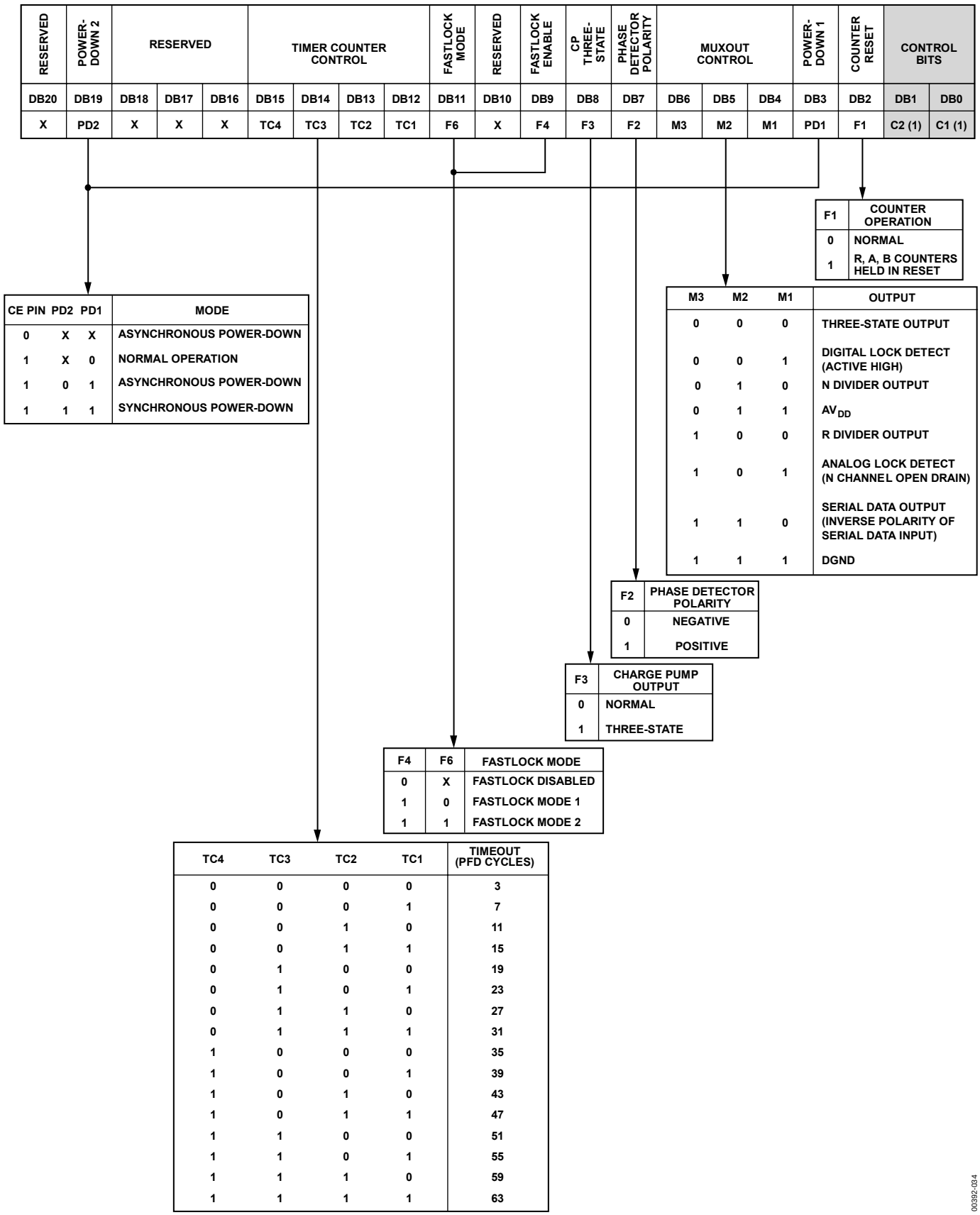

Figure 34. Initialization Latch Map

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FUNCTION LATCH

With C2 and C1 set to 1 and 0, respectively, the on-chip function latch is programmed. Figure 33 shows the input data format for programming the function latch.

COUNTER RESET

DB2 (F1) is the counter reset bit. When this bit is set to 1, the R counter, A counter, and B counter are reset. For normal operation, this bit should be set to 0. On power-up, the F1 bit needs to be disabled, for the N counter to resume counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle.)

POWER-DOWN

DB3 (PD1) and DB19 (PD2) on the ADF411x family provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2 and PD1.

In programmed asynchronous power-down, the device powers down immediately after latching a 1 into the PD1 bit, with the condition that PD2 is loaded with a 0.

In programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once power-down is enabled by writing a 1 into the PD1 bit (on condition that a 1 is also loaded to PD2), the device goes into power-down after the first successive charge pump event.

When a power-down is activated (either synchronous or asynchronous mode including CE pin-activated power-down), the following events occur:

- All active dc current paths are removed.
- The R counter, N counter, and timeout counter are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The oscillator input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT CONTROL

The on-chip multiplexer is controlled by DB6 (M3), DB5 (M2), and DB4 (M1) on the ADF411x family. Figure 33 shows the truth table.

PHASE DETECTOR POLARITY

DB7 (F2) of the function latch sets the phase detector polarity. When the VCO characteristics are positive, DB7 should be set to 1. When they are negative, it should be set to 0.

CHARGE PUMP THREE-STATE

The DB8 (F3) bit puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

FASTLOCK ENABLE BIT

DB9 (F4) of the function latch is the fastlock enable bit. Fastlock is enabled only when DB9 is set to 1.

FASTLOCK MODE BIT

DB11 (F6) of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, Fastlock Mode 1 is selected; if the fastlock mode bit is 1, Fastlock Mode 2 is selected.

If fastlock is not enabled (DB9 = 0), DB11 (ADF4116) determines the state of the FL_O output. FL_O state is the same as that programmed to DB11.

Fastlock Mode 1

In the ADF411x family, the output level of FL_O is programmed to a low state, and the charge pump current is switched to the high value (1 mA). FL_O is used to switch a resistor in the loop filter and to ensure stability while in fastlock by altering the loop bandwidth.

The device enters fastlock by having a 1 written to the CP Gain bit in the N register. The device exits fastlock by having a 0 written to the CP Gain bit in the N register.

Fastlock Mode 2

In the ADF411x family, the output level of FL_O is programmed to a low state, and the charge pump current is switched to the high value (1 mA). FL_O is used to switch a resistor in the loop filter and to ensure stability while in fastlock by altering the loop bandwidth.

The device enters fastlock by having a 1 written to the CP gain bit in the N register. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4 to TC1, the CP Gain bit in the N register is automatically reset to 0, and the device reverts to normal mode instead of fastlock.

TIMER COUNTER CONTROL

In the ADF411x family, the user has the option of switching between two charge pump current values to speed up locking to a new frequency.

When using the fastlock feature with the ADF411x family, the following should be noted:

- The user must make sure that fastlock is enabled. Set DB9 to 1. The user must also choose which fastlock mode to use.

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- Fastlock Mode 2 uses the values in the timer counter to determine the timeout period before reverting to normal mode operation after fastlock. Fastlock Mode 2 is chosen by setting DB11 to 1.
- The user must also decide how long to keep the high current (1 mA) active before reverting to low current (250 µA). This is controlled by the timer counter control bits, DB14 to DB11 (TC4 to TC1), in the function latch. The truth table is given in Figure 33.
- To program a new output frequency, program the A counter and B counter latch with new values for A and B. At the same time, set the CP Gain bit to a 1, which sets the charge pump to 1 mA for a period of time determined by TC4 to TC1. When this time is up, the charge pump current reverts to 250 µA. At the same time, the CP Gain bit in the A counter and B counter latch is reset to 0 and is ready for the next time that the user wants to change the frequency.

INITIALIZATION LATCH

When C2 and C1 are both set to 1, the initialization latch is programmed. This is essentially the same as the function latch that is programmed when C2, C1 = 1, 0.

However, when the initialization latch is programmed, an additional internal reset pulse is applied to the R counter and N counter. This pulse ensures that the N counter is at a load point when the N counter data is latched and that the device begins counting in close phase alignment.

If the latch is programmed for synchronous power-down (CE pin is high; PD1 bit is high; PD2 bit is low), the internal pulse also triggers this power-down. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse, so close phase alignment is maintained when counting resumes.

When the first N counter data is latched after initialization, the internal reset pulse is again activated. However, successive N counter loads do not trigger the internal reset pulse.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initial power-up, the device can be programmed by the initialization latch method, the CE pin method, or the counter reset method.

Initialization Latch Method

1. Apply V_{DD}.
2. Program the initialization latch (11 in 2 LSBs of input word). Make sure that F1 bit is programmed to 0.
3. Do an R load (00 in 2 LSBs).
4. Do an N load (01 in 2 LSBs).

When the initialization latch is loaded, the following occurs:

- The function latch contents are loaded.
- An internal pulse resets the R, N, and timeout counters to load state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
- Latching the first N counter data after the initialization word activates the same internal reset pulse. Successive N loads do not trigger the internal reset pulse unless there is another initialization.

CE Pin Method

1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
3. Program the function latch (10).
4. Program the R counter latch (00).
5. Program the N counter latch (01).
6. Bring CE high to take the device out of power-down.

The R counter and N counter resume counting in close alignment.

Note that after CE goes high, a duration of 1 µs may be required for the prescaler band gap voltage and oscillator input buffer bias to reach a steady state.

CE can be used to power up and power down the device to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled, as long as it is programmed at least once after V_{CC} is initially applied.

Counter Reset Method

1. Apply V_{DD}.
2. Do a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Do an R counter load (00 in 2 LSBs).
4. Do an N counter load (01 in 2 LSBs).
5. Do a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but it does not trigger synchronous power-down. The counter reset method requires an extra function latch load compared to the initialization latch method.

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APPLICATIONS INFORMATION

LOCAL OSCILLATOR FOR THE GSM BASE STATION TRANSMITTER

Figure 35 shows the ADF4117/ADF4118 being used with a VCO to produce the LO for a GSM base station transmitter.

The reference input signal is applied to the circuit at F_{REFIN} and, in this case, is terminated in 50 Ω. A typical GSM system has a 13 MHz TCXO driving the reference input without a 50 Ω termination. To have a channel spacing of 200 kHz (the GSM standard), the reference input must be divided by 65, using the on-chip reference divider of the ADF4117/ADF1118.

The charge pump output of the ADF4117/ADF1118 (Pin 2) drives the loop filter. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system is 45°. Other PLL system specifications include:

K_D = 1 mA
K_V = 12 MHz/V
Loop bandwidth = 20 kHz
F_{REF} = 200 kHz
N = 4500
Extra reference spur attenuation = 10 dB

All of these specifications are needed and are used to produce the loop filter component values shown in Figure 36.

The loop filter output drives the VCO, which, in turn, is fed back to the RF input of the PLL synthesizer; it also drives the RF output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output, and the RF_{IN} terminal of the synthesizer.

In a PLL system, it is important to know when the system is in locked mode. In Figure 35, this is accomplished by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or lock-detect signal.

SHUTDOWN CIRCUIT

The attached circuit in Figure 36 shows how to shut down both the ADF411x family and the accompanying VCO. The ADG702 switch goes open-circuit when a Logic 1 is applied to the IN input. The low cost switch is available in both SOT-23 and MSOP packages.

DIRECT CONVERSION MODULATOR

In some applications, a direct conversion architecture can be used in base station transmitters. Figure 37 shows the combination available from Analog Devices, Inc. to implement this solution.

The circuit diagram shows the AD9761 being used with the AD8346. The use of dual integrated DACs, such as the AD9761 with specified ±0.02 dB and ±0.004 dB gain and offset matching characteristics, ensures minimum error contribution (over temperature) from this portion of the signal chain.

The local oscillator is implemented by using the ADF4117/ADF4118. In this case, the FOX801BH-130 provides the stable 13 MHz reference frequency. The system is designed for 200 kHz channel spacing and an output center frequency of 1960 MHz. The target application is a WCDMA base station transmitter. Typical phase noise performance from this LO is −85 dBc/Hz at a 1 kHz offset. The LO port of the AD8346 is driven in single-ended fashion. LOIN is ac-coupled to ground with the 100 pF capacitor, and LOIP is driven through the ac-coupling capacitor from a 50 Ω source. An LO drive level between −6 dBm and −12 dBm is required. The circuit in Figure 37 gives a typical level of −8 dBm.

The RF output is designed to drive a 50 Ω load, but it must be ac-coupled as shown in Figure 37. If the I and Q inputs are driven in quadrature by 2 V p-p signals, the resulting output power is approximately −10 dBm.

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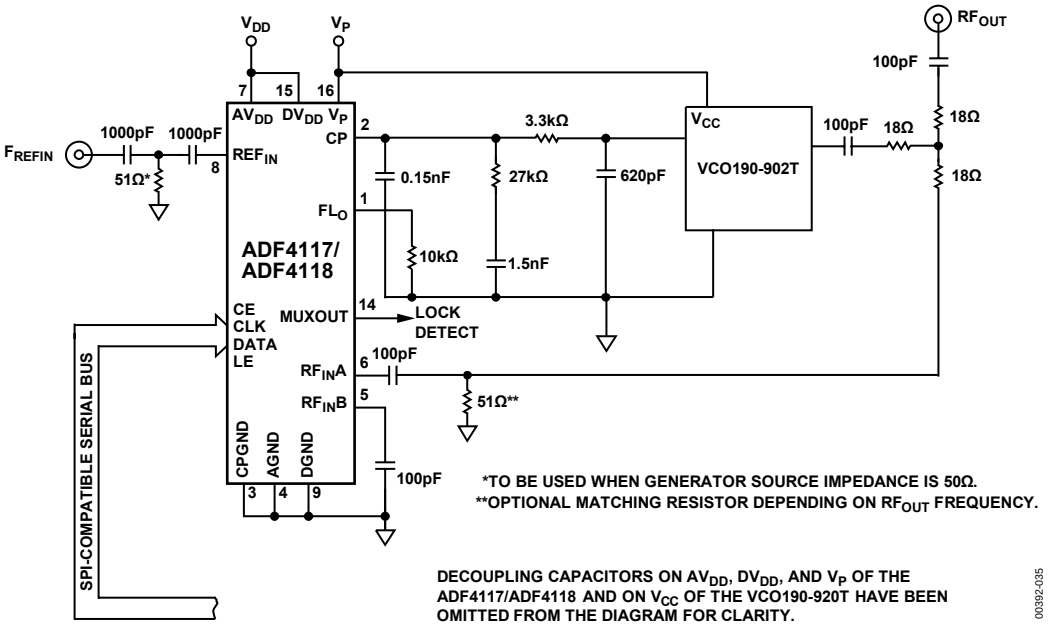

Figure 35. Local Oscillator for GSM Base Station

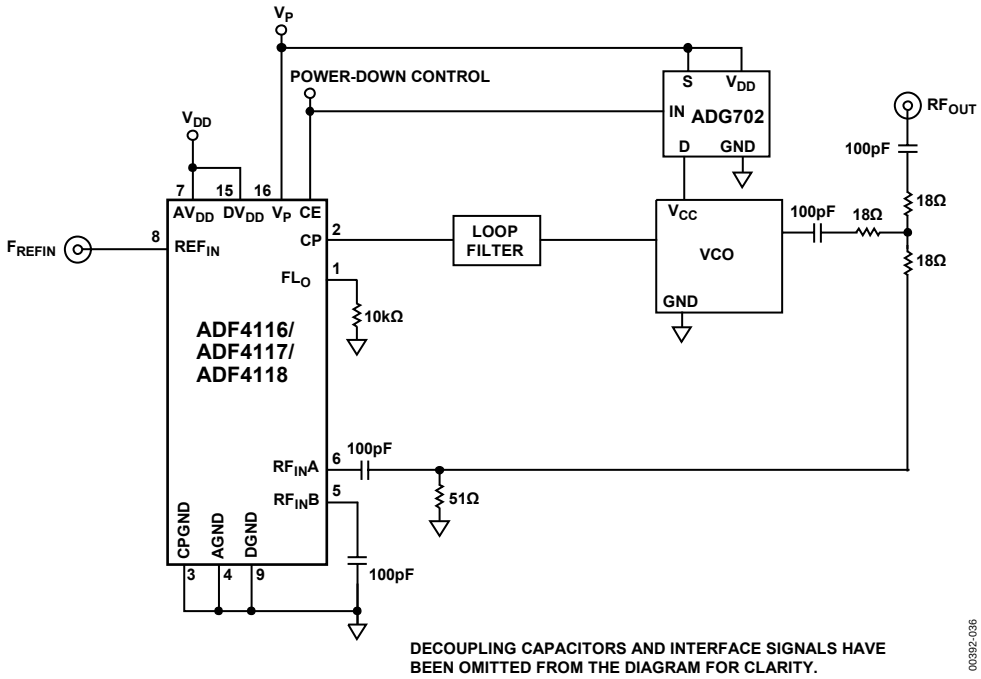

Figure 36. Local Oscillator Shutdown Circuit

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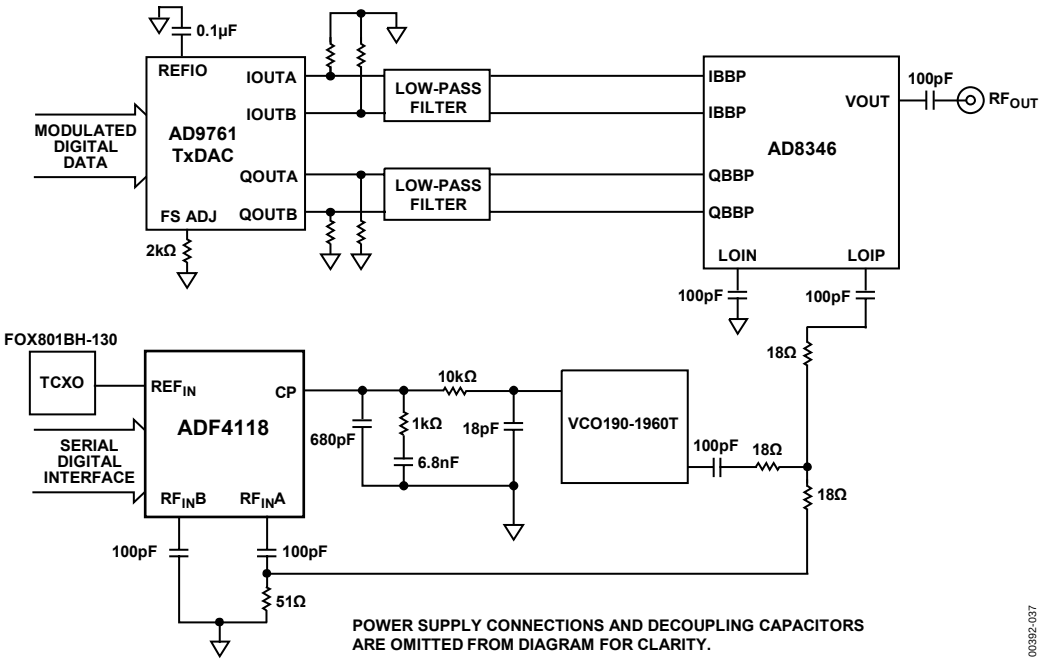

Figure 37. Direct Conversion Transmitter Solution

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INTERFACING

The ADF411x family has a simple SPI®-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that are clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 µs. This is more than adequate for systems that have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 38 shows the interface between the ADF411x family and the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF411x family needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

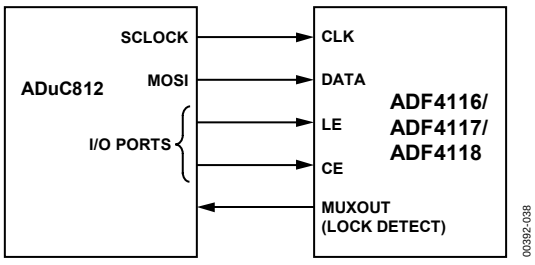

Figure 38. ADuC812 to ADF411x family Interface

On first applying power to the ADF411x family, it requires three writes (one each to the R counter latch, the N counter latch, and the initialization latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

ADSP-21xx Interface

Figure 39 shows the interface between the ADF411x family and the ADSP-21xx digital signal processor. The ADF411x family needs a 21-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

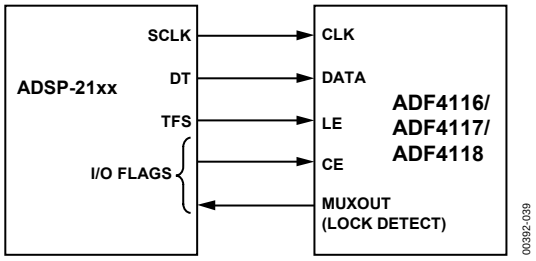

Figure 39. ADSP-21xx to ADF411x family Interface

Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 21-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

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OUTLINE DIMENSIONS

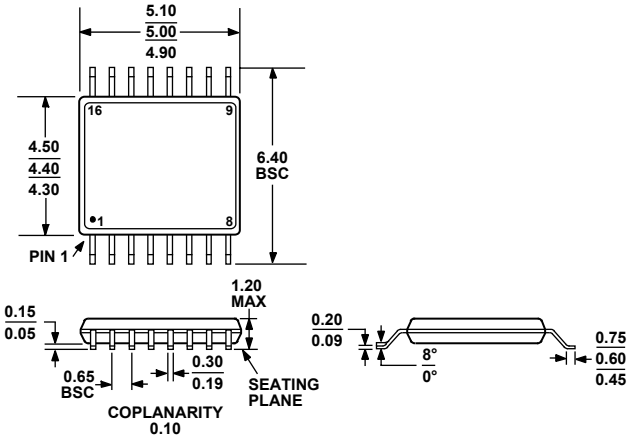

Figure 40. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4116BRU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4116BRU-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4116BRU-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4116BRUZ[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4116BRUZ-REEL[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4116BRUZ-REEL7[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4117BRU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4117BRU-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4117BRU-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4117BRUZ[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4117BRUZ-RL[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4117BRUZ-RL7[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118BRU	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118BRU-REEL	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118BRU-REEL7	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118BRUZ[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118BRUZ-RL[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118BRUZ-RL7[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118YRUZ-RL[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADF4118YRUZ-RL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
EVAL-ADF4118EBZ1[1]		Evaluation Board	
EVAL-ADF411XEBZ1[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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