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- 2 AD9625 ADC's running at 2.5GSPS with an effective sampling rate of 5GSPS
- AD9625 Evaluation and Synchronization
- AD9625 Evaluation Board
- ADA4961 & AD9625 Analog Signal Chain Evaluation and Converter Synchronization
- ADL5567 & AD9625 Analog Signal Chain Evaluation and ADF4355-2 Wideband Synthesizer with VCO

DOCUMENTATION

Data Sheet

- AD9625: 12-Bit, 2.6 GSPS/2.5 GSPS/2.0 GSPS, 1.3 V/2.5 V Analog-to-Digital Converter Data Sheet

User Guides

- AD-FMCADC2-EBZ FMC Board User Guide

TOOLS AND SIMULATIONS

- Visual Analog
- AD9625 AMI Model

REFERENCE MATERIALS

Informational

- JESD204 Serial Interface

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- Analog Devices Unveils 2.5-GSPS A/D Converter, Driver Amplifier and Rapid Prototyping FMC Module
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- New PLLs Deliver Widest Frequency Range Coverage and Lowest VCO Phase Noise in a Single Device

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- MS-2660: Understanding Spurious-Free Dynamic Range in Wideband GSPS ADCs
- MS-2670-1: The Demand for Digital: Challenges and Solutions for High Speed Analog-to-Digital Converters and Radar Systems
- MS-2672: JESD204B Subclasses - Part 1: An Introduction to JESD204B Subclasses and Deterministic Latency
- MS-2677: JESD204B Subclasses - Part 2: Subclass 1 vs. Subclass 2 System Considerations
- MS-2702: Gigasample ADCs Run Fast to Solve New Challenges
- MS-2708: GSPS Data Converters to the Rescue for Electronics Surveillance and Warfare Systems
- MS-2714: Understanding Layers in the JESD204B Specificaton: A High Speed ADC Perspective, Part 1
- MS-2728: Demystifying the Conversion Error Rate of High Speed ADCs
- MS-2735: Maximizing the Dynamic Range of Software-Defined Radio
- Taming the Wideband Conundrum with RF Sampling ADCs

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- AD9625 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

9/2016—Rev. B to Rev. C

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Changes to Table 110 and Table 111 69
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5/2015—Rev. A to Rev. B

Added AD9625-2.6 .... Throughout
Change to Figure 1 1
Changes to Table 1 4
Changes to Table 2 5
Change to Figure 5 10
Added Endnote 1, Table 8 11
Added Endnote 2, Table 9 13
Added AD9625-2.6 Section 24
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9/2014—Rev. 0 to Rev. A

Added AD9625-2.5 .... Throughout
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5/2014—Revision 0: Initial Version

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SPECIFICATIONS

DC SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling rate, 1.2 V internal reference, AIN = −1.0 dBFS, default SPI settings, dc-coupled output data, unless otherwise noted.

Table 1.

Parameter	Test Conditions/ Comments	Temperature[1]	AD9625-2.0			AD9625-2.5			AD9625-2.6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			12			12			12			Bits
ACCURACY												
No Missing Codes		Full	Guaranteed			Guaranteed			Guaranteed			
Offset Error		Full	−7	±0.5	+6.4	−7	±0.5	+6.4	−8.5	±0.5	+7.0	LSB
Gain Error		Full	−8		+8	−10.8		+14.2	−13.8		+20.9	%FSR
Differential Nonlinearity (DNL)		Full	−0.7	±0.3	+0.7	−0.5	±0.3	+0.7	−0.6	±0.3	+0.7	LSB
Integral Nonlinearity (INL)		Full	−3.6	±0.9	+3.6	−2.1	±1.0	+2.1	−2.7	±1.0	+2.3	LSB
ANALOG INPUTS												
Differential Input												
Voltage Range	Internal V_{REF} = 1.2 V	Full		1.1			1			1		V p-p
Resistance		25°C		100			100			100		Ω
Capacitance		25°C		1.5			1.5			1.5		pF
Internal Common-Mode Voltage (V_{CM})		Full	492	525	563	492	525	563	492	525	563	mV
Analog Full-Power Bandwidth[2]	Internal termination	25°C		3.2			3.2			3.2		GHz
Input Referred Noise		25°C		2			2			2		LSB_{RMS}
POWER SUPPLIES												
AVDD1		Full	1.26	1.3	1.32	1.26	1.3	1.32	1.26	1.3	1.32	V
AVDD2		Full	2.4	2.5	2.6	2.4	2.5	2.6	2.4	2.5	2.6	V
DRVDD1		Full	1.26	1.3	1.32	1.26	1.3	1.32	1.26	1.3	1.32	V
DRVDD2		Full	2.4	2.5	2.6	2.4	2.5	2.6	2.4	2.5	2.6	V
DVDD1		Full	1.26	1.3	1.32	1.26	1.3	1.32	1.26	1.3	1.32	V
DVDD2		Full	2.4	2.5	2.6	2.4	2.5	2.6	2.4	2.5	2.6	V
DVDDIO		Full	2.4	2.5	3.3	2.4	2.5	3.3	2.4	2.5	3.3	V
SPI_VDDIO		Full	2.4	2.5	3.3	2.4	2.5	3.3	2.4	2.5	3.3	V
I_{AVDD1}		Full		1120	1222		1250	1351		1267	1390	mA
I_{AVDD2}		Full		383	460		427	491		432	492	mA
I_{DRVDD1}		Full		456	470		476	518		497	544	mA
I_{DRVDD2}		Full		9	10		9	10		9	10	mA
I_{DVDD1}		Full		410	430		425	473		441	503	mA
I_{DVDD2}		Full		<1			<1			<1		mA
I_{DVDDIO}		Full		<1			<1			<1		mA
I_{SPI_VDDIO}		Full		<1			<1			<1		mA
Power Dissipation	Eight lane mode	Full		3.48	3.8		3.90	4.2		4.0	4.3	W
Power-Down Dissipation				125	3.8		125			125		mW

[1] Full temperature range is −40°C to +85°C measured at the case (T_C).
[2] See Figure 75 and Figure 76 for networks.

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AC SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling, 1.2 V internal reference, AIN = −1.0 dBFS, sample clock input = 1.65 V p-p differential, default SPI settings, unless otherwise noted.

Table 2.

Parameter	Test Conditions/ Comments	Temperature[1]	AD9625-2.0			AD9625-2.5			AD9625-2.6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SPEED GRADE					2.0			2.5			2.6	GSPS
ANALOG INPUT	Full scale	Full		1.1			1.2			1.1		V p-p
NOISE DENSITY		25°C		−149.0			−149.5			−150.0		dBFS/Hz
SIGNAL-TO-NOISE RATIO (SNR)												
f_{IN} = 100 MHz		25°C		59.5			58.3			58.1		dBFS
f_{IN} = 500 MHz		25°C		59.4			58.0			58.0		dBFS
f_{IN} = 1000 MHz		25°C		59.0			57.6			57.5		dBFS
f_{IN} = 1800 MHz		Full	55.4	58.2		54.1	57.0		55.0	56.6		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)												
f_{IN} = 100 MHz		25°C		58.4			57.2			57.0		dBc
f_{IN} = 500 MHz		25°C		58.4			57.0			56.9		dBc
f_{IN} = 1000 MHz		25°C		58.0			56.5			56.4		dBc
f_{IN} = 1800 MHz		Full	54.1	57.2		53.1	55.9		53.9	55.6		dBc
EFFECTIVE NUMBER OF BITS (ENOB)												
f_{IN} = 100 MHz		25°C		9.4			9.2			9.2		Bits
f_{IN} = 500 MHz		25°C		9.4			9.2			9.2		Bits
f_{IN} = 1000 MHz		25°C		9.3			9.1			9.1		Bits
f_{IN} = 1800 MHz		25°C		9.2			9.0			8.9		Bits
SPURIOUS FREE DYNAMIC RANGE (SFDR)	Including second or thrid harmonic											
f_{IN} = 100 MHz		25°C		80			77			80.5		dBc
f_{IN} = 500 MHz		25°C		81			76			79.6		dBc
f_{IN} = 1000 MHz		25°C		80			79			77.3		dBc
f_{IN} = 1800 MHz		Full	67	76		70	77		65	75.4		dBc
WORST OTHER SPUR	Excluding second or third harmonic											
f_{IN} = 100 MHz		25°C		−80			−77			−81		dBc
f_{IN} = 500 MHz		25°C		−86			−76			−83		dBc
f_{IN} = 1000 MHz		25°C		−83			−82			−80		dBc
f_{IN} = 1800 MHz		Full		−85	−73		−78	−70		−78.0	−66.0	dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)	At −7 dBFS per tone											
f_{IN1} = 728.5 MHz, f_{IN2} = 731.5 MHz		25°C		−82.8			−81.2			−78.3		dBc
f_{IN1} = 1805.5 MHz, f_{IN2} = 1808.5 MHz		25°C		−77.6			−76.3			−77.7		dBc

[1] Full temperature range is −40°C to +85°C measured at the case (T_C).

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DIGITAL SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling rate, 1.2 V internal reference, AIN = −1.0 dBFS, default SPI settings, unless otherwise noted.

Table 3.

Parameter	Temperature[1]	Min	Typ	Max	Unit
CLOCK INPUTS (CLK+, CLK−)					
Differential Input Voltage	Full	500		1800	mV p-p
Common-Mode Input Voltage	Full		0.88		V
Input Resistance (Differential)	Full		40		kΩ
Input Capacitance	Full		1.5		pF
SYSREF INPUTS (SYSREF+, SYSREF−)					
Differential Input Voltage	Full	500		1800	mV p-p
Common-Mode Input Voltage	Full		0.88		V
Input Resistance (Differential)	Full		40		kΩ
Input Capacitance	Full		1.5		pF
LOGIC INPUTS (SDIO, SCLK, CSB)					
Logic Compliance			CMOS		
Voltage					
Logic 1	Full	0.8 × SPI_DVDDIO			V
Logic 0	Full			0.5	V
Input Resistance	Full		30		kΩ
Input Capacitance	Full		0.5		pF
SYNCB+/SYNCB− INPUT					
Logic Compliance	Full		LVDS		
Input Voltage					
Differential	Full	250		1200	mV p-p
Common Mode	Full		1.2		V
Input Resistance (Differential)	Full		100		Ω
Input Capacitance	Full		2.5		pF
LOGIC OUTPUT (SDIO)					
Logic Compliance			CMOS		
Voltage					
Logic 1 (I_{OH} = 800 µA)	Full		0.8 × SPI_VDDIO		V
Logic 0 (I_{OL} = 50 µA)	Full		0.3		V
DIGITAL OUTPUTS (SERDOUT[x]±)					
Compliance	Full		CML		
Output Voltage					
Differential	Full	360	700	800	mV p-p
Offset	Full		DRVDD/2		mV p-p
Differential Return Loss (RL_{DIFF})[2]	25°C	8			dB
Common-Mode Return Loss (RL_{CM})	25°C	6			dB
Differential Termination Impedance	25°C			100	Ω
RESET (RSTB)					
Voltage					
Logic 1	Full	0.8 × DVDDIO			V
Logic 0	Full			0.5	V
Input Resistance (Differential)	Full		20		kΩ
Input Capacitance	Full		2.5		pF
FAST DETECT (FD), PWDN, AND INTERRUPT (IRQ)					
Logic Compliance			CMOS		
Voltage					
Logic 1	Full	0.8 × DVDDIO			V
Logic 0	Full			0.5	V
Input Resistance (Differential)	Full		20		kΩ
Input Capacitance	Full		2.5		pF

[1] Full temperature range is −40°C to +85°C measured at the case (T_C).
[2] Differential and common-mode return loss measured from 100 MHz to 0.75 × baud rate.

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SWITCHING SPECIFICATIONS

AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V, specified maximum sampling rate, 1.2 V internal reference, AIN = −1.0 dBFS, default SPI settings, unless otherwise noted.

Table 4.

Parameter	Test Conditions/Comments	Temperature[1]	Min	Typ	Max	Unit
CLOCK (CLK)						
Maximum Clock Rate		Full			2600	MSPS
Minimum Clock Rate		Full	330[2]			MSPS
Clock Pulse Width High		Full	50 ± 5			% duty cycle
Clock Pulse Width Low		Full	50 ± 5			% duty cycle
SYSREF (SYSREF±)[3]						
Setup Time (t_{SU_SR})		25°C		+200		ps
Hold Time (t_{H_SR})		25°C		−100		ps
FAST DETECT OUTPUT (FD)						
Latency		Full		82		Clock cycles
OUTPUT PARAMETERS (SERDOUT[x]±)						
Rise Time		25°C		70		ps
Fall Time		25°C		70		ps
Pipeline Latency	Eight lane mode	25°C		226		Clock cycles
SYNCB± Falling Edge to First K.28 Characters		25°C	4			Multiframes
CGS Phase K.28 Characters Duration		25°C	1			Multiframes
Differential Termination Resistance		25°C		100		Ω
APERTURE						
Delay		Full		200		ps
Uncertainty (Jitter)		Full		80		f_S rms
Out-of-Range Recovery Time		Full		2		Clock cycles

[1] Full temperature range is −40°C to +85°C measured at the case (T_C).
[2] Must use a two-lane, generic output lane configuration for minimum sample rate. For more information, see the lane table in the JESD204B specification document.
[3] SYSREF± setup and hold times are defined with respect to the rising SYSREF± edge and rising clock edge. Positive setup time leads the clock edge. Negative hold time also leads the clock edge.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns

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Timing Diagrams

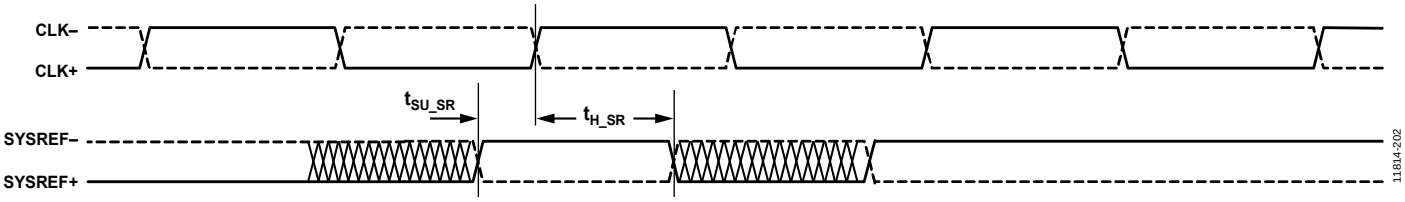

Figure 2. SYSREF± Setup and Hold Timing

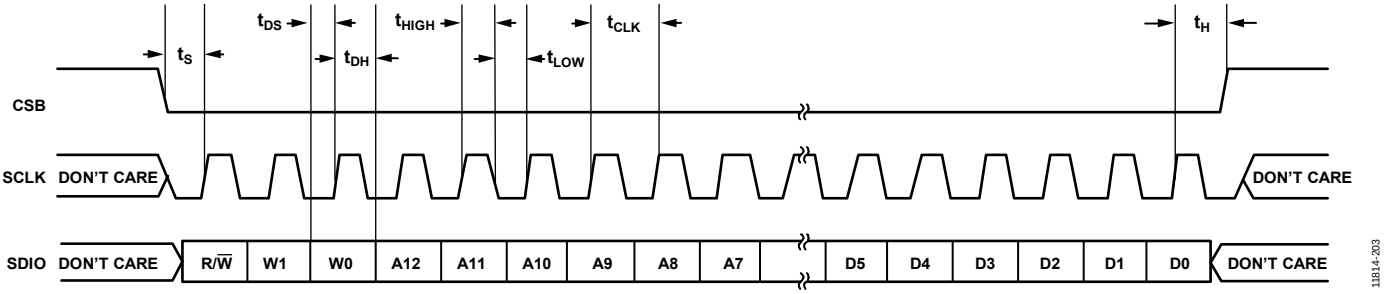

Figure 3. Serial Port Interface Timing Diagram (MSB First)

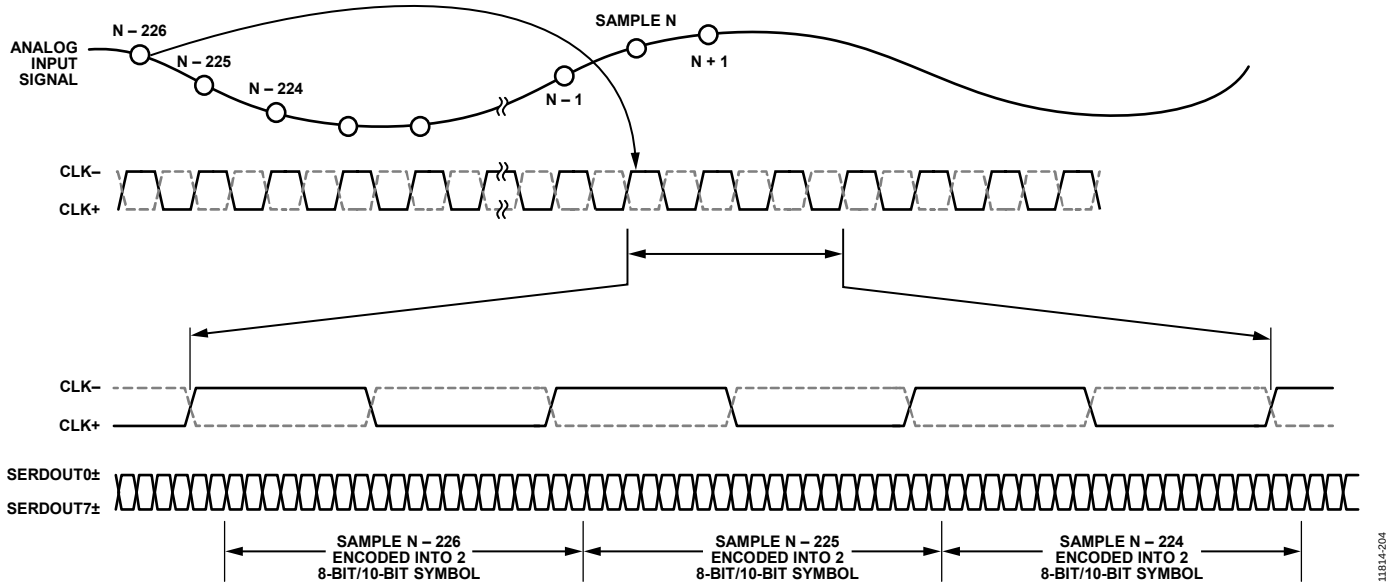

Figure 4. Data Output Timing for Eight Lane Mode

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ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD1 to AGND	−0.3 V to +1.32 V
AVDD2 to AGND	−0.3 V to +2.75 V
DRVDD1 to DRGND	−0.3 V to +1.32 V
DRVDD2 to DRGND	−0.3 V to +2.75 V
DVDD1 to DGND	−0.3 V to +1.32 V
DVDD2 to DGND	−0.3 V to +2.75 V
DVDDIO to DGND	−0.3 V to +3.63 V
SPI_VDDIO to DGND	−0.3 V to +3.63 V
AGND to DRGND	−0.3 V to +0.3 V
VIN± to AGND	−0.3 V to AVDD1 + 0.2 V
VCM to AGND	−0.3 V to AVDD1 + 0.2 V
VMON to AGND	−0.3 V to AVDD1 + 0.2 V
CLK± to AGND	−0.3 V to AVDD1 + 0.2 V
SYSREF± to AGND	−0.3 V to AVDD1 + 0.2 V
SYNCINB± to DRGND	−0.3 V to DRVDD2 + 0.2 V
SCLK to DRGND	−0.3 V to SPI_VDDIO + 0.2 V
SDIO to DRGND	−0.3 V to SPI_VDDIO + 0.2 V
IRQ to DRGND	−0.3 V to DVDDIO + 0.2 V
RSTB to DRGND	−0.3 V to DVDDIO + 0.2 V
CSB to DRGND	−0.3 V to SPI_VDDIO + 0.2 V
FD to DRGND	−0.3 V to DVDDIO + 0.2 V
DIVCLK± to DRGND	−0.3 V to DRVDD2 + 0.2 V
SERDOUT[x]± to DRGND	−0.3 V to DRVDD1 + 0.2 V
Environmental	
Storage Temperature Range	−60°C to +150°C
Operating Case Temperature Range	−40°C to +85°C (measured at case)
Maximum Junction Temperature	110°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

The following characteristics are for a 4-layer and 10-layer printed circuit board (PCB).

Table 7. Thermal Resistance

PCB	T_A (°C)	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)	θ_{JC} (°C/W)
4-Layer	85.0	18.7	0.61	6.1	1.4
10-Layer	85.0	11.5	0.61	4.1	N/A[1]

[1] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AD9625
TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AGND	AGND	AGND	AVDD1	AGND	AVDD2	VCM	AGND	VIN+	VIN–	AGND	VM_BYP	AVDD2	AVDD2
B	AGND	AGND	AGND	AGND	AVDD1	AGND	AVDD2	AGND	AGND	AGND	AGND	AVDD2	AGND	AGND
C	AGND	AGND	AGND	AGND	AGND	AVDD1	AGND	AVDD2	AGND	AGND	AVDD2	AGND	AGND	AVDD1
D	DVDD1	DVDD1	DVDD1	DNC	AGND	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AVDD1	AVDD1
E	DGND	DGND	DGND	DVDD2	VMON	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	AGND
F	DVDD1	DVDD1	DVDD1	SPI_VDDIO	DVDDIO	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	CLK+
G	DGND	DGND	DGND	CSB	DVDDIO	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	CLK–
H	DVDD1	DVDD1	DVDD1	SCLK	IRQ	AGND	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	AGND
J	DGND	DGND	DGND	SDIO	FD	RBIAS_EXT	AVDD1	AVDD2	AGND	AGND	AVDD2	AVDD1	AGND	SYSREF+
K	DVDD1	DVDD1	RSTB	PWDN	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	AGND	SYSREF–
L	DGND	DNC	SYNCINB–	SYNCINB+	DGND	DGND	DGND	DGND	DGND	DNC	DNC	DNC	AGND	AGND
M	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRGND	DRVDD1	REXT	DRGND	DRGND
N	DRVDD1	SERDOUT [7]+	SERDOUT [6]+	SERDOUT [5]+	SERDOUT [4]+	DRVDD1	SERDOUT [3]+	SERDOUT [2]+	SERDOUT [1]+	SERDOUT [0]+	DRVDD1	VP_BYP	DRVDD2	DRVDD2
P	DRVDD1	SERDOUT [7]–	SERDOUT [6]–	SERDOUT [5]–	SERDOUT [4]–	DRVDD1	SERDOUT [3]–	SERDOUT [2]–	SERDOUT [1]–	SERDOUT [0]–	DRVDD1	DRGND	DIVCLK–	DIVCLK+

NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN. LEAVE THIS PIN FLOATING.

11814-009

Figure 5. Pin Configuration

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Table 8. Pin Function Descriptions (By Pin Number)

Pin No.	Mnemonic	Type	Description
A1 to A3	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
A4	AVDD1	Power	ADC Analog Power Supply (1.30 V).
A5	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
A6	AVDD2	Power	ADC Analog Power Supply (2.50 V).
A7	VCM	Output	Analog Input, Common Mode (0.525 V).
A8	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
A9	VIN+	Input	Differential Analog Input, True.
A10	VIN−	Input	Differential Analog Input, Complement.
A11	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
A12	VM_BYP	Input	Voltage Bypass.
A13	AVDD2	Power	ADC Analog Power Supply (2.50 V).
A14	AVDD2	Power	ADC Analog Power Supply (2.50 V).
B1 to B4	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
B5	AVDD1	Power	ADC Analog Power Supply (1.30 V).
B6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
B7	AVDD2	Power	ADC Analog Power Supply (2.50 V).
B8 to B11	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
B12	AVDD2	Power	ADC Analog Power Supply (2.50 V).
B13, B14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
C1 to C5	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
C6	AVDD1	Power	ADC Analog Power Supply (1.30 V).
C7	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
C8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
C9, C10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
C11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
C12, C13	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
C14	AVDD1	Power	ADC Analog Power Supply (1.30 V).
D1 to D3	DVDD1	Power	ADC Digital Power Supply (1.30 V).
D4	DNC	N/A[1]	Do Not Connect. Do not connect to this pin. Leave this pin floating.
D5, D6	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
D7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
D8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
D9, D10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
D11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
D12 to D14	AVDD1	Power	ADC Analog Power Supply (1.30 V).
E1 to E3	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
E4	DVDD2	Power	ADC Digital Power Supply (2.5 V).
E5	VMON	Output	CTAT Voltage Monitor Output.
E6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
E7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
E8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
E9, E10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
E11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
E12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
E13, E14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
F1 to F3	DVDD1	Power	ADC Digital Power Supply (1.30 V).
F4	SPI_VDDIO	Power	SPI Digital Power Supply (2.50 V).
F5	DVDDIO	Power	Digital I/O Power Supply (2.50 V).
F6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
F7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
F8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
F9, F10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.

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Pin No.	Mnemonic	Type	Description
F11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
F12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
F13	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
F14	CLK+	Input	ADC Clock Input, True.
G1 to G3	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
G4	CSB	Input	SPI Chip Select CMOS Input. Active low.
G5	DVDDIO	Power	Digital I/O Power Supply (2.50 V).
G6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
G7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
G8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
G9, G10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
G11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
G12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
G13	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
G14	CLK–	Input	ADC Clock Input, Complement.
H1 to H3	DVDD1	Power	ADC Digital Power Supply (1.30 V).
H4	SCLK	Input	SPI Serial Clock CMOS Input.
H5	IRQ	Output	Interrupt Request Output Signal.
H6	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
H7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
H8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
H9, H10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
H11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
H12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
H13, H14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
J1 to J3	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
J4	SDIO	I/O	SPI Serial Data CMOS Input/Output; Scan Output 1.
J5	FD	Output	Fast Detect Output. This pin requires an external 10 kΩ resistor connected to ground.
J6	RBIAS_EXT	Input	Reference Bias. This pin requires an external 10 kΩ resistor connected to ground.
J7	AVDD1	Power	ADC Analog Power Supply (1.30 V).
J8	AVDD2	Power	ADC Analog Power Supply (2.50 V).
J9, J10	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
J11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
J12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
J13	AGND	Ground	ADC Analog Ground. This pin connects to the analog ground plane.
J14	SYSREF+	Input	System Reference Chip Synchronization, True.
K1 to K2	DVDD1	Power	ADC Digital Power Supply (1.30 V).
K3	RSTB	Input	Chip Digital Reset, Active Low.
K4	PWDN	Input	Power-down.
K5 to K13	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
K14	SYSREF–	Input	System Reference Chip Synchronization, Complement.
L1	DGND	Ground	Digital Control Ground Supply. This pin connects to the digital ground plane.
L2	DNC	N/A[1]	Do Not Connect. Do not connect to this pin. Leave this pin floating.
L3	SYNCINB–	Input	Synchronization, Complement.
L4	SYNCINB+	Input	Synchronization, True. SYNCINB LVDS input (active low, true).
L5 to L9	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
L10 to L12	DNC	N/A[1]	Do Not Connect. Do not connect to these pins. Leave these pins floating.
L13, L14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
M1 to M10	DRGND	Ground	Digital Driver Ground Supply. These pins connect to the digital driver ground plane.
M11	DRVDD1	Power	Power Supply (1.3 V) Reference Clock Divider, VCO, and Synthesizer.
M12	REXT	Input	External Resistor, 10 kΩ to Ground.
M13, M14	DRGND	Ground	Digital Driver Ground Supply. This pin connects to the digital driver ground plane.

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Pin No.	Mnemonic	Type	Description
N1	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
N2	SERDOUT[7]+	Output	Lane 7 CML Output Data, True.
N3	SERDOUT[6]+	Output	Lane 6 CML Output Data, True.
N4	SERDOUT[5]+	Output	Lane 5 CML Output Data, True.
N5	SERDOUT[4]+	Output	Lane 4 CML Output Data, True.
N6	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
N7	SERDOUT[3]+	Output	Lane 3 CML Output Data, True.
N8	SERDOUT[2]+	Output	Lane 2 CML Output Data, True.
N9	SERDOUT[1]+	Output	Lane 1 CML Output Data, True.
N10	SERDOUT[0]+	Output	Lane 0 CML Output Data, True.
N11	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
N12	VP_BYP	Input	Voltage Bypass.
N13, N14	DRVDD2	Power	Power Supply (2.5 V) Reference Clock Divider for SYNCINB±, DIVCLK±.
P1	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
P2	SERDOUT[7]–	Output	Lane 7 CML Output Data, Complement.
P3	SERDOUT[6]–	Output	Lane 6 CML Output Data, Complement.
P4	SERDOUT[5]–	Output	Lane 5 CML Output Data, Complement.
P5	SERDOUT[4]–	Output	Lane 4 CML Output Data, Complement.
P6	DRVDD1	Power	Serializer Digital Power Supply (1.30 V).
P7	SERDOUT[3]–	Output	Lane 3 CML Output Data, Complement.
P8	SERDOUT[2]–	Output	Lane 2 CML Output Data, Complement.
P9	SERDOUT[1]–	Output	Lane 1 CML Output Data, Complement.
P10	SERDOUT[0]–	Output	Lane 0 CML Output Data, Complement.
P11	DRVDD1	Power	Serializer Digital Power Supply (1.30 V).
P12	DRGND	Ground	Digital Driver Ground Supply. This pin connects to the digital driver ground plane.
P13	DIVCLK–	Output	Divide-by-4 Reference Clock LVDS, Complement.
P14	DIVCLK+	Output	Divide-by-4 Reference Clock LVDS, True.

[1] N/A means not applicable.

Table 9. Pin Function Descriptions (By Function)[1]

Pin No.	Mnemonic	Type	Description
General Power and Ground Supply Pins			
A1 to A3, A5, A8, A11, B1 to B4, B6, B8 to B11, B13, B14, C1 to C5, C7, C9, C10, C12, C13, D5, D6, D9, D10, E6, E9, E10, E13, E14, F6, F9, F10, F13, G6, G9, G10, G13, H6, H9, H10, H13, H14, J9, J10, J13, K5 to K13, L13, L14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.
J6	RBIAS_EXT	Input	Reference Bias. This pin requires an external 10 kΩ resistor connected to ground.
Clock Pins			
F14	CLK+	Input	ADC Clock Input, True.
G14	CLK–	Input	ADC Clock Input, Complement.
ADC Analog Power and Ground Supplies Pins			
A6, A13, A14, B7, B12, C8, C11, D8, D11, E8, E11, F8, F11, G8, G11, H8, H11, J8, J11	AVDD2	Power	ADC Analog Power Supply (2.50 V).
A4, B5, C6, C14, D7, D12 to D14, E7, E12, F7, F12, G7, G12, H7, H12, J7, J12	AVDD1	Power	ADC Analog Power Supply (1.30 V).
A12	VM_BYP	Input	Voltage Bypass.
A1 to A3, A5, A8, A11, B1 to B4, B6, B8 to B11, B13, B14, C1 to C5, C7, C9, C10, C12, C13,D5, D6, D9, D10, E6, E9, E10, E13, E14, F6, F9, F10, F13, G6, G9, G10, G13, H6, H9, H10, H13, H14, J9, J10, J13, K5 to K13, L13, L14	AGND	Ground	ADC Analog Ground. These pins connect to the analog ground plane.

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Pin No.	Mnemonic	Type	Description
ADC Analog Input and Outputs Pins			
A9	VIN+	Input	Differential Analog Input, True.
A10	VIN−	Input	Differential Analog Input, Complement.
A7	VCM	Output	Analog Input, Common Mode (0.525 V).
E5	VMON	Output	CTAT Voltage Monitor Output (Diode Temperature Sensor).
JESD204B High Speed Power and Ground Pins			
N1, N6, N11, P1, P6, P11	DRVDD1	Power	Serial Digital Power Supply (1.3 V).
M1 to M10, M13, M14, P12	DRGND	Ground	Digital Driver Ground Supply. These pins connect to the digital driver ground plane.
N13, N14	DRVDD2	Power	Power Supply (2.5 V) Reference Clock Divider, SYNCINB±, DIVCLK±.
M11	DRVDD1	Power	Power Supply (1.3 V) Reference Clock Divider, VCO, and Synthesizer.
N12	VP_BYP	Input	Voltage Bypass.
L2	DNC	N/A[2]	Do Not Connect. Do not connect to this pin.
JESD204B High Speed Serial I/O Pins			
J14	SYSREF+	Input	System Reference Chip Synchronization, True.
K14	SYSREF−	Input	System Reference Chip Synchronization, Complement.
L4	SYNCINB+	Input	Synchronization, True. SYNCINB LVDS input (active low, true).
L3	SYNCINB−	Input	Synchronization, Complement. SYNCINB LVDS input (active low, complement).
N10	SERDOUT[0]+	Output	Lane 0 CML Output Data, True.
P10	SERDOUT[0]−	Output	Lane 0 CML Output Data, Complement.
N9	SERDOUT[1]+	Output	Lane 1 CML Output Data, True.
P9	SERDOUT[1]−	Output	Lane 1 CML Output Data, Complement.
N8	SERDOUT[2]+	Output	Lane 2 CML Output Data, True.
P8	SERDOUT[2]−	Output	Lane 2 CML Output Data, Complement.
N7	SERDOUT[3]+	Output	Lane 3 CML Output Data, True.
P7	SERDOUT[3]−	Output	Lane 3 CML Output Data, Complement.
N5	SERDOUT[4]+	Output	Lane 4 CML Output Data, True.
P5	SERDOUT[4]−	Output	Lane 4 CML Output Data, Complement.
N4	SERDOUT[5]+	Output	Lane 5 CML Output Data, True.
P4	SERDOUT[5]−	Output	Lane 5 CML Output Data, Complement.
N3	SERDOUT[6]+	Output	Lane 6 CML Output Data, True.
P3	SERDOUT[6]−	Output	Lane 6 CML Output Data, Complement.
N2	SERDOUT[7]+	Output	Lane 7 CML Output Data, True.
P2	SERDOUT[7]−	Output	Lane 7 CML Output Data, Complement.
P14	DIVCLK+	Output	Divide-by-4 Reference Clock LVDS, True.
P13	DIVCLK−	Output	Divide-by-4 Reference Clock LVDS, Complement.
Digital Supply and Ground Pins			
D1 to D3, F1 to F3, H1 to H3, K1 to K2	DVDD1	Power	ADC Digital Power Supply (1.3 V).
F5, G5	DVDDIO	Power	Digital I/O Power Supply (2.5 V).
F4	SPI_VDDIO	Power	SPI Digital Power Supply (2.5 V).
E4	DVDD2	Power	ADC Digital Power Supply (2.5 V).
E1 to E3, G1 to G3, J1 to J3, L1, L5 to L9	DGND	Ground	Digital Control Ground Supply. These pins connect to the digital ground plane.
D4	DNC	N/A[2]	Do Not Connect. Do not connect to this pin. Leave this pin floating.
Digital Control Pins			
K3	RSTB	Input	Chip Digital Reset, Active Low.
K4	PWDN	Input	Power-down for the AD9625.
M12	REXT	Input	External Resistor, 10 kΩ to Ground.
G4	CSB	Input	SPI Chip Select CMOS Input. Active low.
H4	SCLK	Input	SPI Serial Clock CMOS Input.

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Pin No.	Mnemonic	Type	Description
J4	SDIO	I/O	SPI Serial Data CMOS Input/Output.
J5	FD	Output	Fast Detect Output. This pin requires an external 10 kΩ resistor connected to ground.
H5	IRQ	Output	Interrupt Request Output Signal.
L10 to L12	DNC	N/A[2]	Do Not Connect. Do not connect to these pins. Leave these pins floating.

[1] Note that when pins are relevant to multiple categories, they are repeated in Table 9. Pins may not appear in alphanumeric order within Table 9.
[2] N/A means not applicable.

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TYPICAL PERFORMANCE CHARACTERISTICS

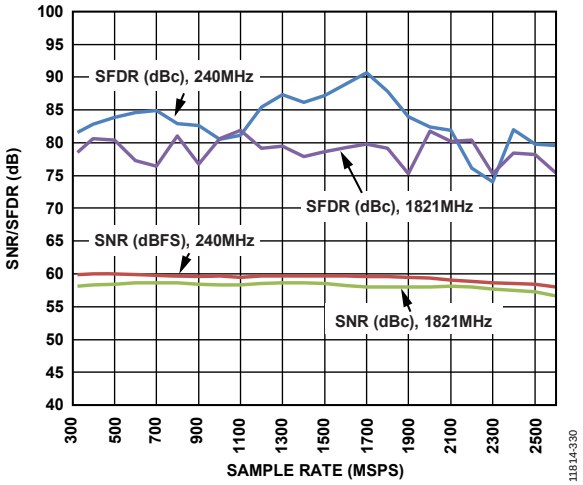

Figure 6. SNR/SFDR vs. Sample Rate

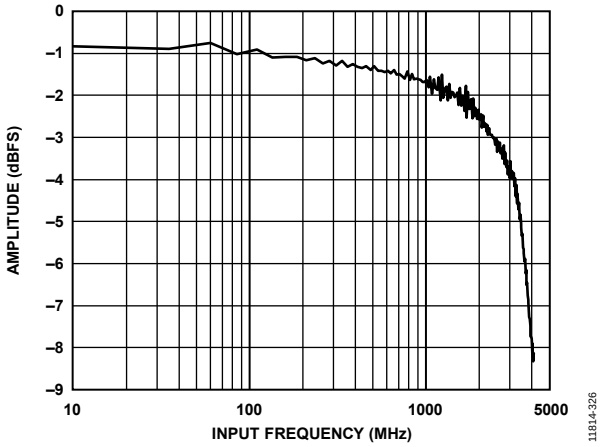

Figure 8. Full Power Input Bandwidth (Input Network in Figure 76 Used >2 GHz, Input Network in Figure 75 Used <2 GHz)

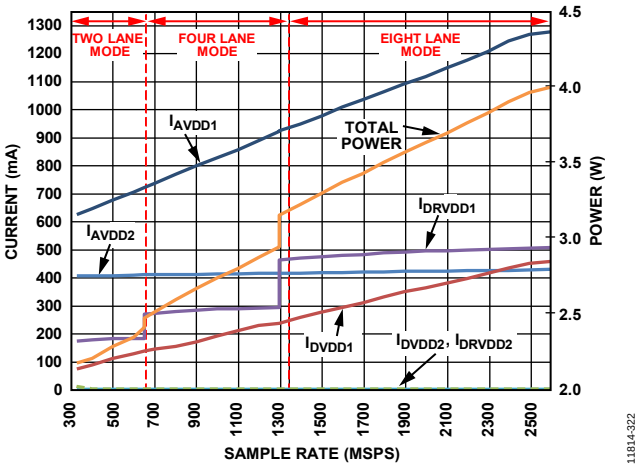

Figure 7. Current and Power vs. Sample Rate: Two Lane, Four Lane, and Eight Lane Output Modes

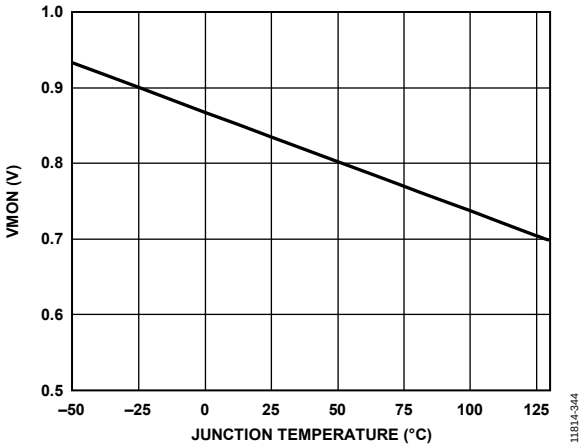

Figure 9. VMON Output Voltage vs. Junction Temperature VMON (V) = −0.0013 × TEMP(C) + 0.8675

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AD9625-2.0

For the AD9625-2.0 model, the full-scale range used is 1.1 V.

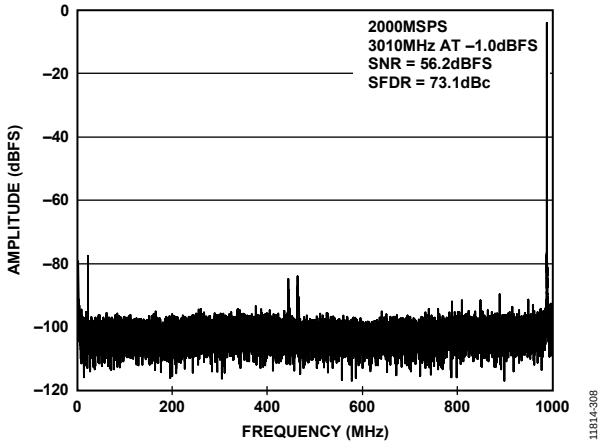

Figure 10. FFT Plot at 2.0 GSPS, f_{IN} = 3010 MHz at AIN (SFDR = 73.1 dBc, SNR = 56.2 dBFS) (Input Network in Figure 76 Used)

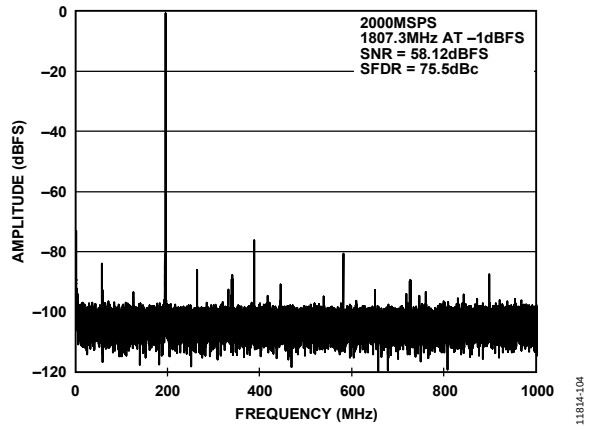

Figure 11. FFT Plot at 2.0 GSPS, f_{IN} = 1807.3 MHz at AIN (SFDR = 75.5 dBc, SNR = 58.12 dBFS)

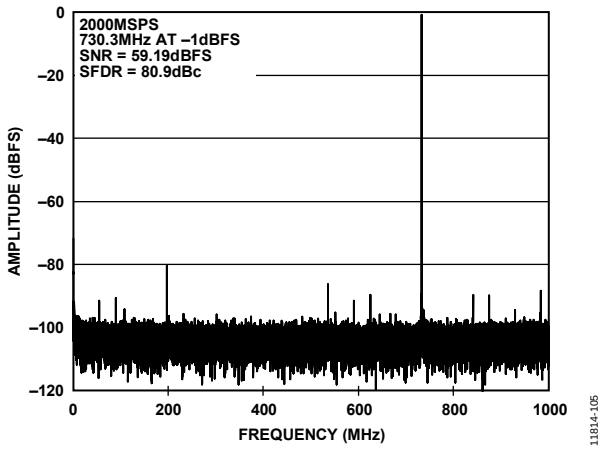

Figure 12. FFT Plot at 2.0 GSPS, f_{IN} = 730.3 MHz at AIN (SFDR = 80.9 dBc, SNR = 59.19 dBFS)

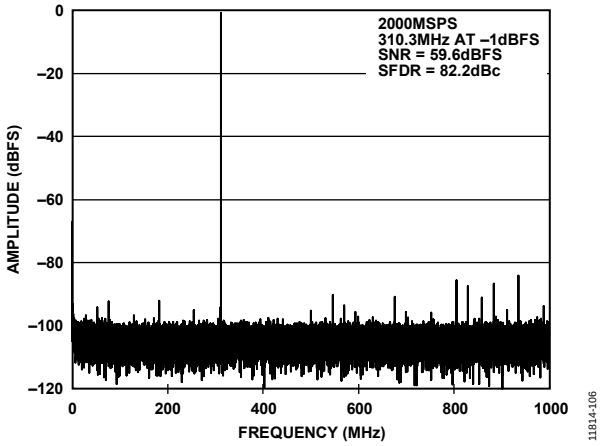

Figure 13. FFT Plot at 2.0 GSPS, f_{IN} = 310.3 MHz at AIN (SFDR = 82.2 dBc, SNR = 59.6 dBFS)

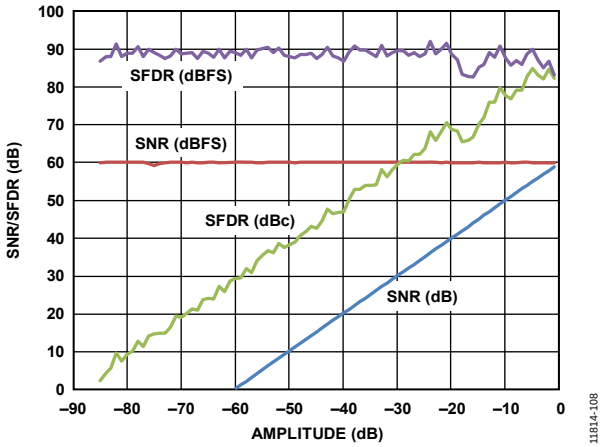

Figure 14. SNR/SFDR vs. Analog Input Amplitude at 2.0 GSPS, f_{IN} = 241.1 MHz at AIN

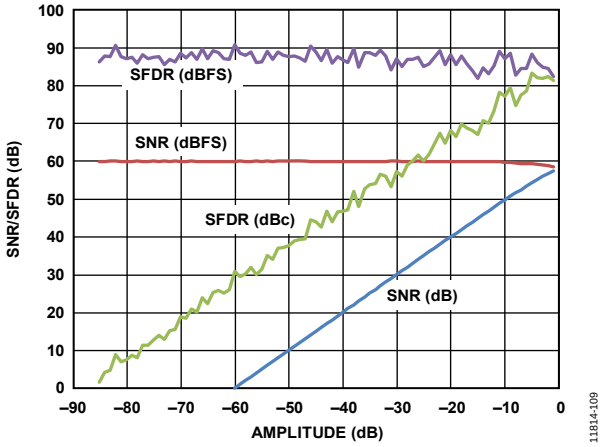

Figure 15. SNR/SFDR vs. Analog Input Amplitude at 2.0 GSPS, f_{IN} = 1811.3 MHz at AIN

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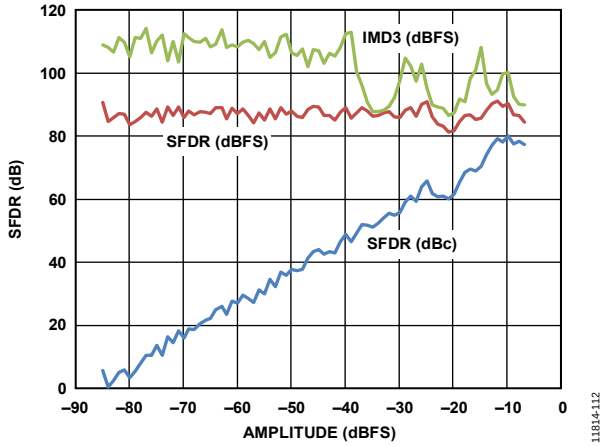

Figure 16. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.0 GSPS at 1800 MHz AIN

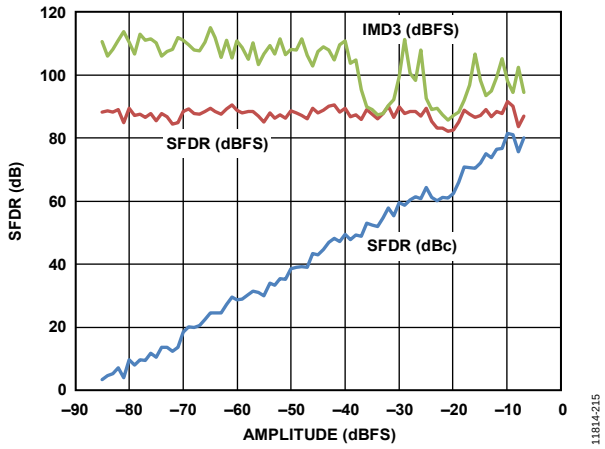

Figure 17. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.0 GSPS at 230 MHz AIN

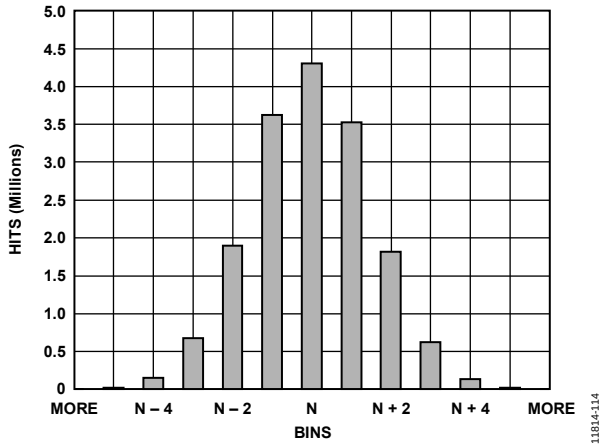

Figure 18. Input Referred Noise Histogram with 2.0 GSPS

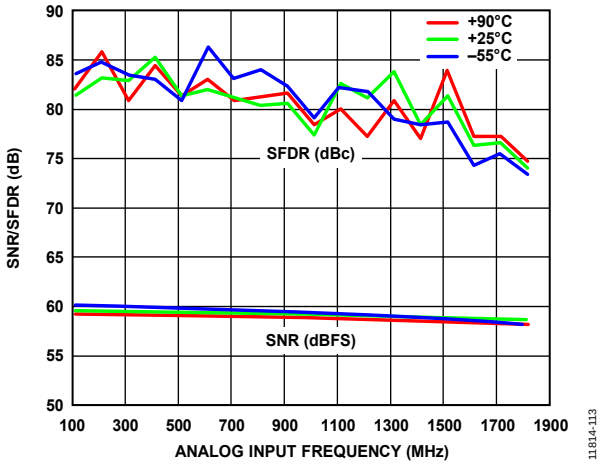

Figure 19. SNR/SFDR vs. Analog Input Frequency at Different Temperatures at 2.0 GSPS

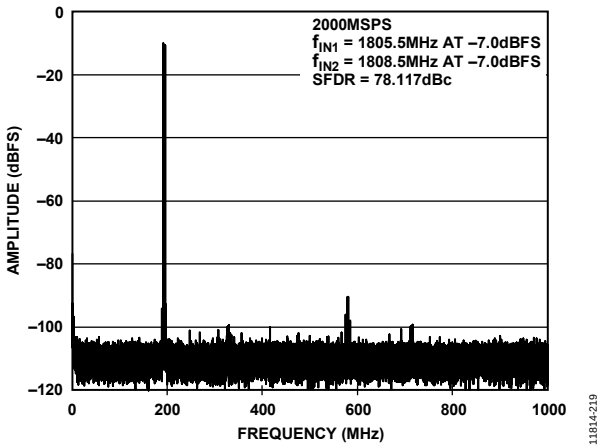

Figure 20. Two Tone FFT Plot at 2.0 GSPS, f_{IN1} = 1805.5 MHz and f_{IN2} = 1808.5 MHz at AIN, –7.0 dBFS (SFDR = 78.117 dBc)

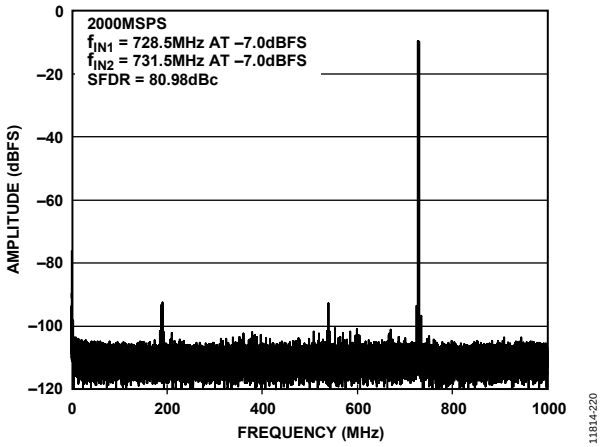

Figure 21. Two Tone FFT Plot at 2.0 GSPS, f_{IN1} = 728.5 MHz and f_{IN2} = 731.5 MHz at AIN, –7.0 dBFS (SFDR = 80.98 dBc)

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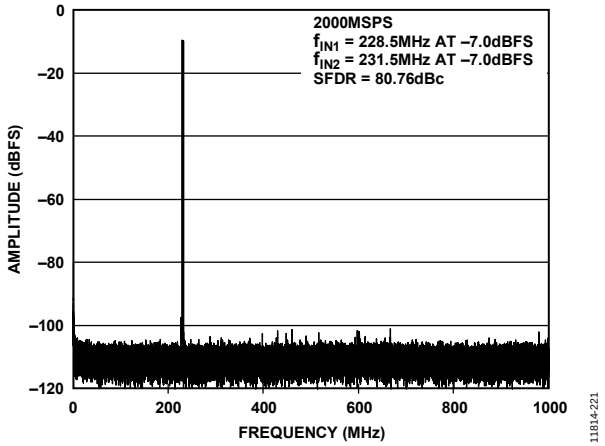

Figure 22. Two Tone FFT Plot at 2.0 GSPS, f_{IN1} = 228.5 MHz and f_{IN2} = 231.5 MHz at AIN, −7.0 dBFS (SFDR = 80.76 dBc)

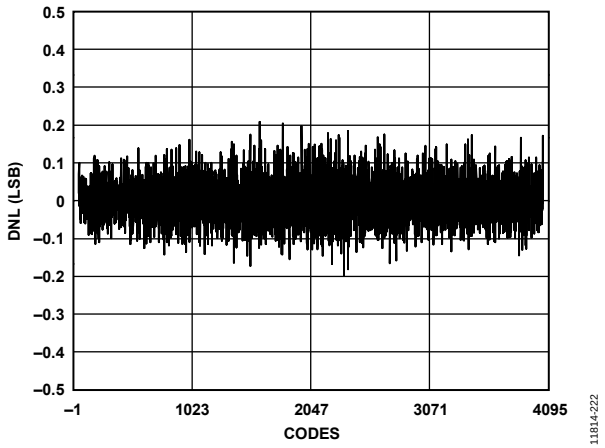

Figure 23. Differential Nonlinearity (DNL), ±0.2 LSB at 2.0 GSPS

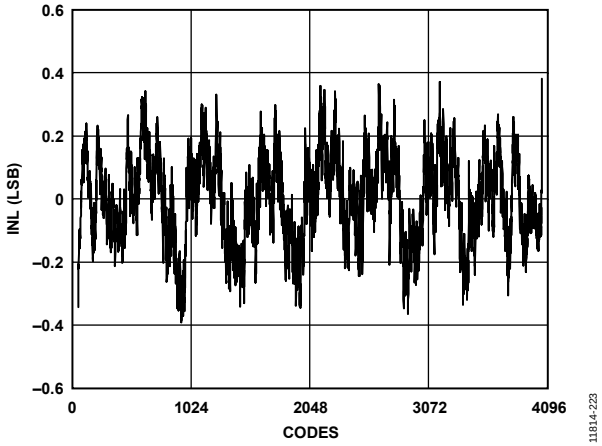

Figure 24. Integral Nonlinearity (INL), ±0.4 LSB at 2.0 GSPS

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AD9625-2.5

For the AD9625-2.5 model, full-scale range used is 1.2 V.

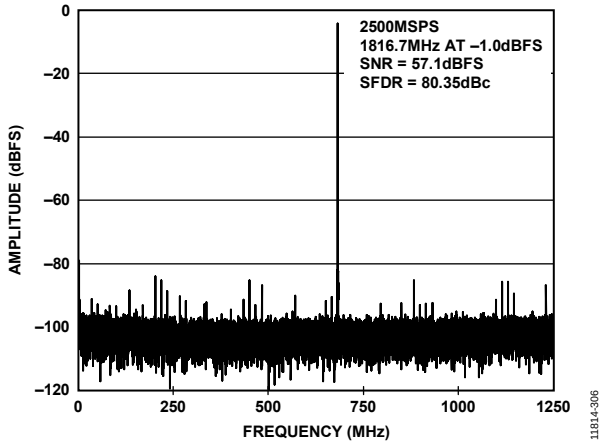

Figure 25. FFT Plot at 2.5 GSPS, f_{IN} = 1816.7 MHz at AIN (SFDR = 80.35 dBc, SNR = 57.1 dBFS)

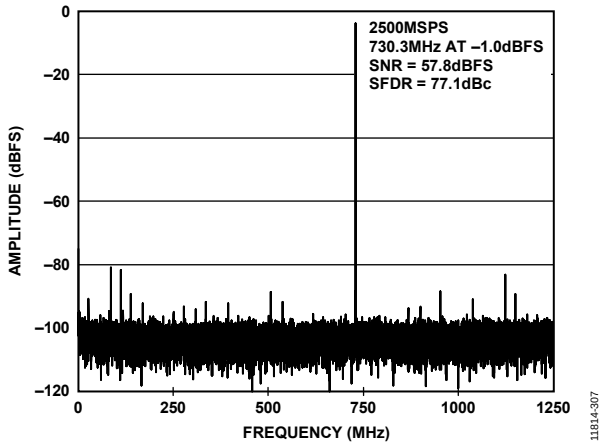

Figure 26. FFT Plot at 2.5 GSPS, f_{IN} = 730.3 MHz at AIN (SFDR = 77.1 dBc, SNR = 57.8 dBFS)

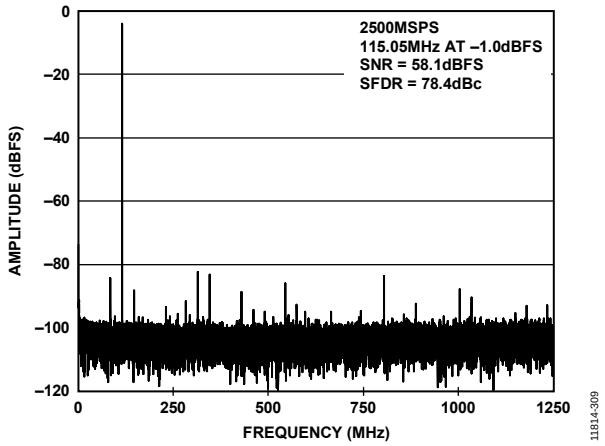

Figure 27. FFT Plot at 2.5 GSPS, f_{IN} = 115.05 MHz at AIN (SFDR = 78.4 dBc, SNR = 58.1 dBFS)

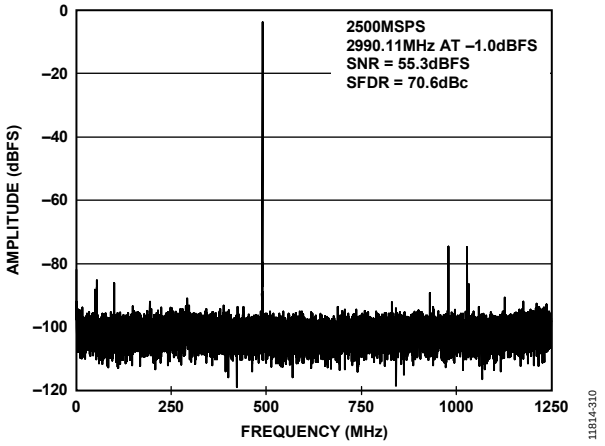

Figure 28. FFT Plot at 2.5 GSPS, f_{IN} = 2990.11 MHz at AIN (SFDR = 70.6 dBc, SNR = 55.3 dBFS) (Input Network in Figure 75 Used)

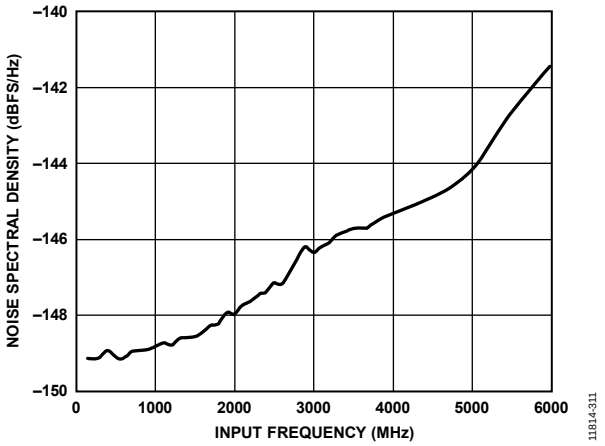

Figure 29. Noise Specrtal Density (NSD) vs. AIN at 2.5 GSPS (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 Used >2 GHz)

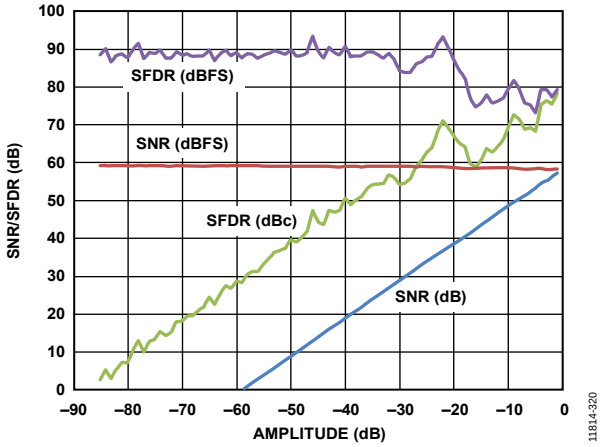

Figure 30. SNR/SFDR vs. Analog Input Amplitude at 2.5 GSPS, f_{IN} = 241 MHz at AIN

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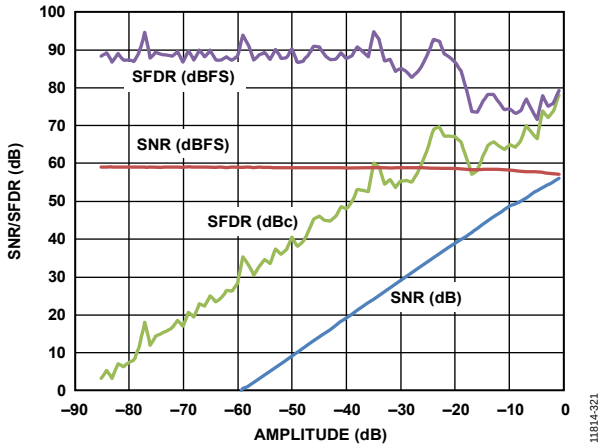

Figure 31. SNR/SFDR vs. Analog Input Amplitude at 2.5 GSPS, f_{IN} = 1811 MHz at AIN

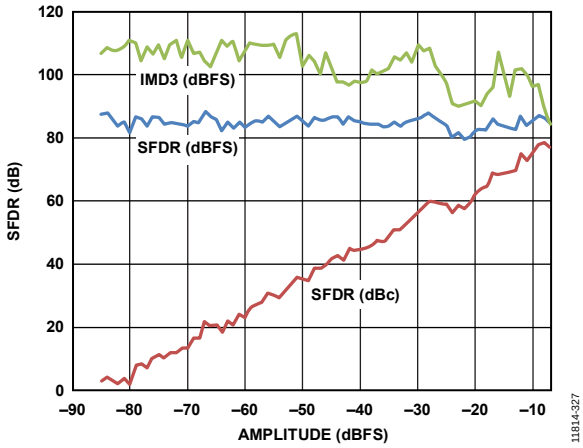

Figure 34. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.5 GSPS at 1800 MHz AIN

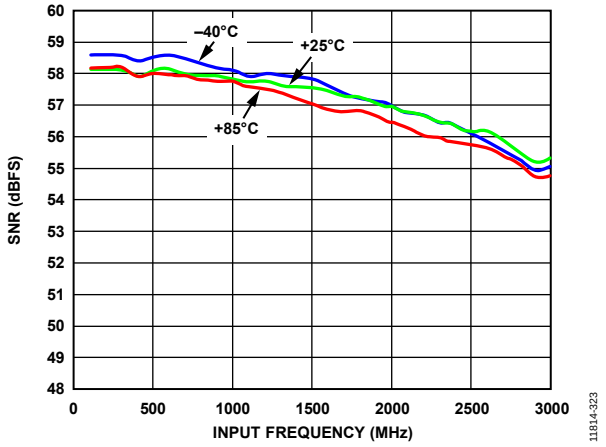

Figure 32. SNR at 2.5 GSPS vs. Temperature (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 Used >2 GHz)

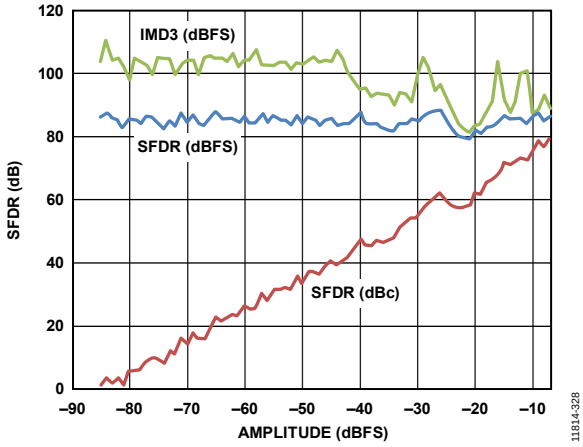

Figure 35. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.5 GSPS at 230 MHz AIN

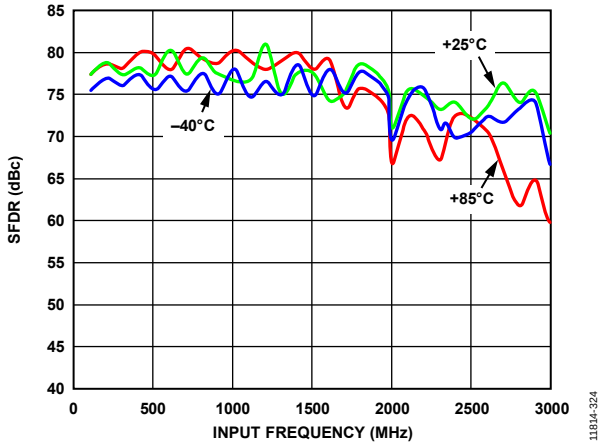

Figure 33. SFDR at 2.5 GSPS vs. Temperature (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 Used >2 GHz)

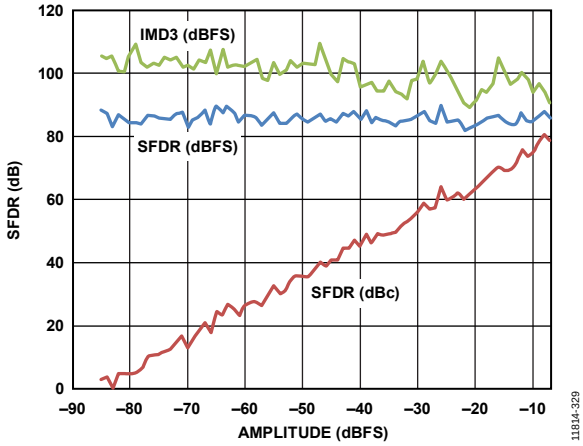

Figure 36. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.5 GSPS at 730 MHz AIN

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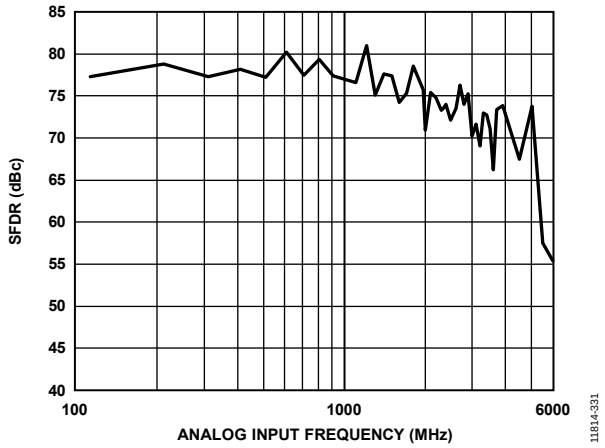

Figure 37. SFDR vs. AIN Frequency at 2.5 GSPS (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 used >2 GHz)

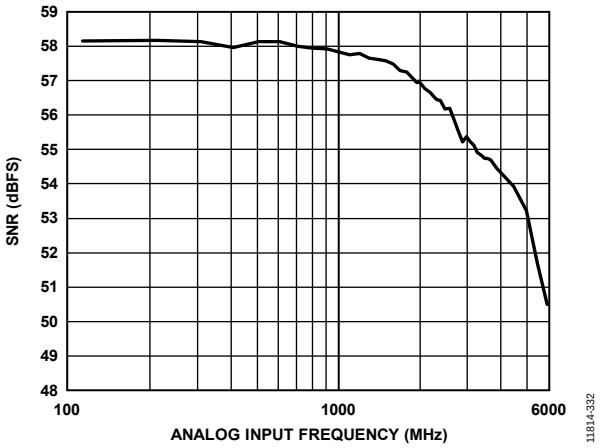

Figure 40. SNRFS vs. AIN Frequency at 2.5 GSPS (Input Network in Figure 76 Used <2 GHz, Input Network in Figure 75 Used >2 GHz)

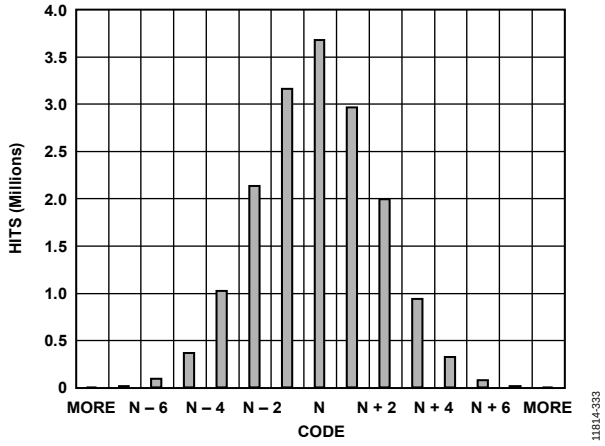

Figure 38. Input Referred Noise Histogram with 2.5 GSPS

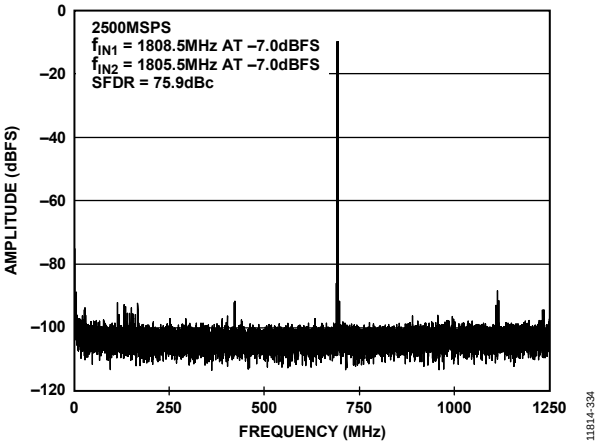

Figure 41. Two Tone FFT Plot at 2.5 GSPS, f_{IN1} = 1808.5 MHz and f_{IN2} = 1805.5 MHz at AIN, −7.0 dBFS (SFDR = 75.9 dBc)

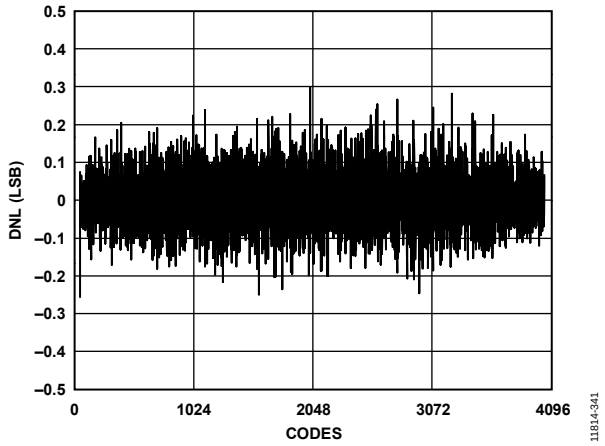

Figure 39. Differential Nonlinearity (DNL), ±0.3 LSB at 2.5 GSPS

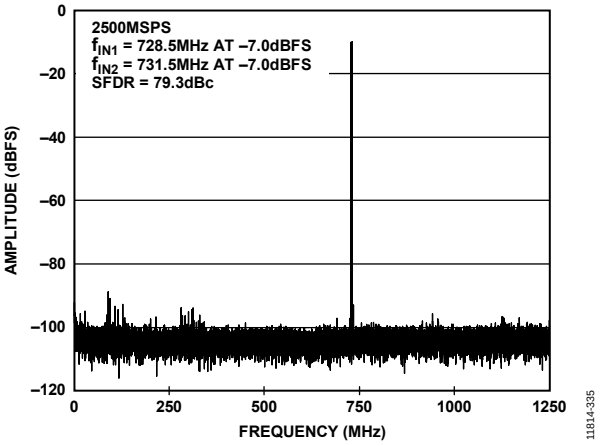

Figure 42. Two Tone FFT Plot at 2.5 GSPS, f_{IN1} = 728.5 MHz and f_{IN2} = 731.5 MHz at AIN, −7.0 dBFS (SFDR = 79.3 dBc)

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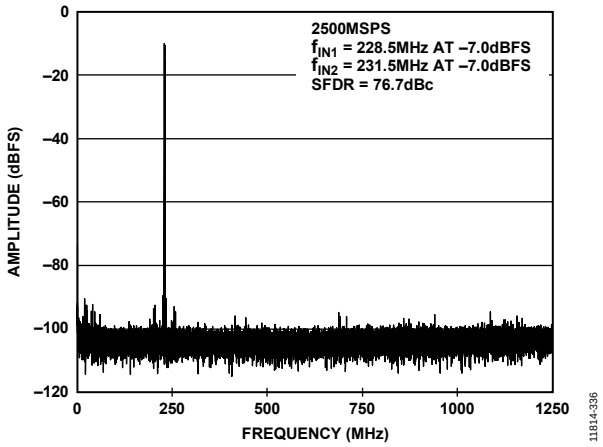

Figure 43. Two Tone FFT Plot at 2.5 GSPS, f_{IN1} = 228.5 MHz and f_{IN2} = 231.5 MHz at AIN, −7.0 dBFS (SFDR = 76.7 dBc)

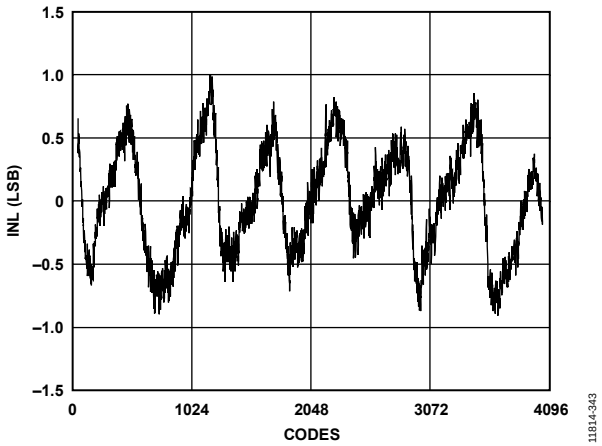

Figure 44. Integral Nonlinearity (INL), ±1.0 LSB at 2.5 GSPS

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AD9625-2.6

For the AD9625-2.6 model, full-scale range used is 1.1 V.

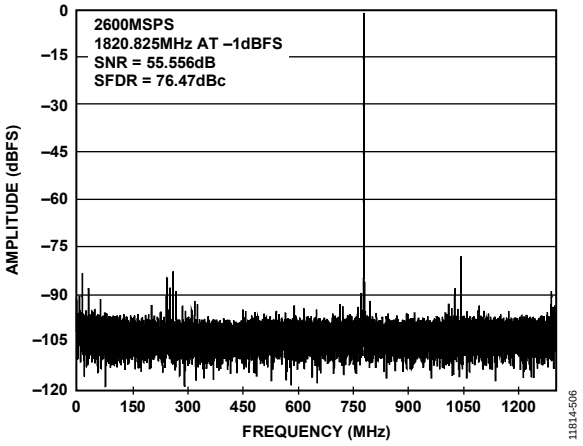

Figure 45. FFT Plot at 2.6 GSPS, f_{IN} = 1820.825 MHz at AIN (SFDR = 76.47 dBc, SNR = 55.556 dB)

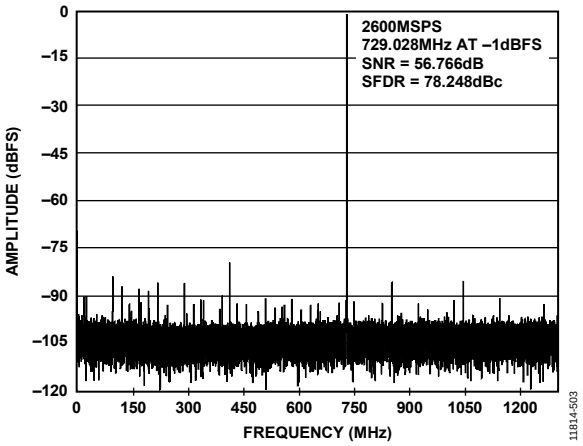

Figure 46. FFT Plot at 2.6 GSPS, f_{IN} = 729.028 MHz at AIN (SFDR = 78.248 dB, SNR = 56.766)

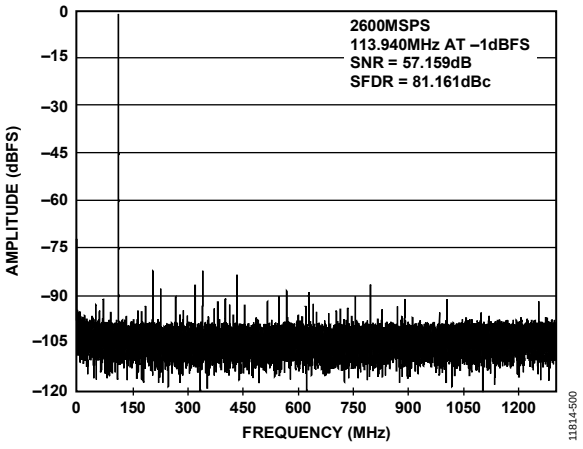

Figure 47. FFT Plot at 2.6 GSPS, f_{IN} = 113.940 MHz at AIN (SFDR = 81.161, SNR = 57.159)

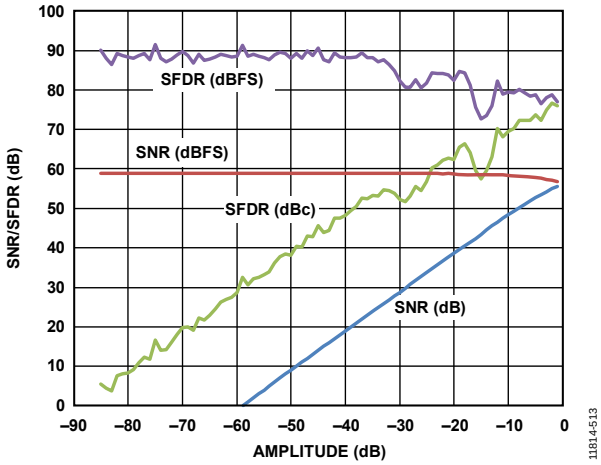

Figure 48. SNR/SFDR vs. Analog Input Amplitude at 2.6 GSPS, f_{IN} = 1811 MHz at AIN

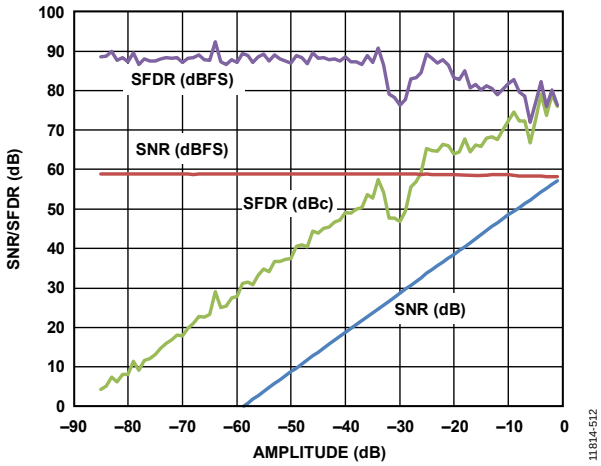

Figure 49. SNR/SFDR vs. Analog Input Amplitude at 2.6 GSPS, f_{IN} = 241 MHz at AIN

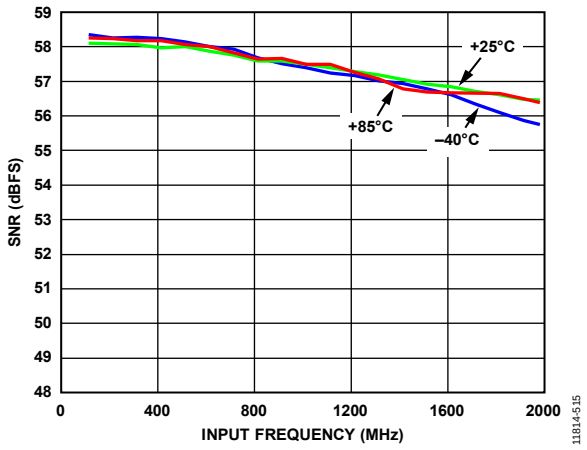

Figure 50. SNR vs. Temperature at 2.6 GSPS

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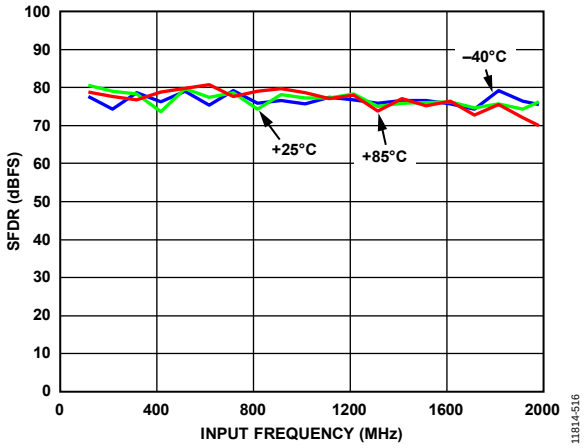

Figure 51. SFDR vs. Temperature at 2.6 GSPS

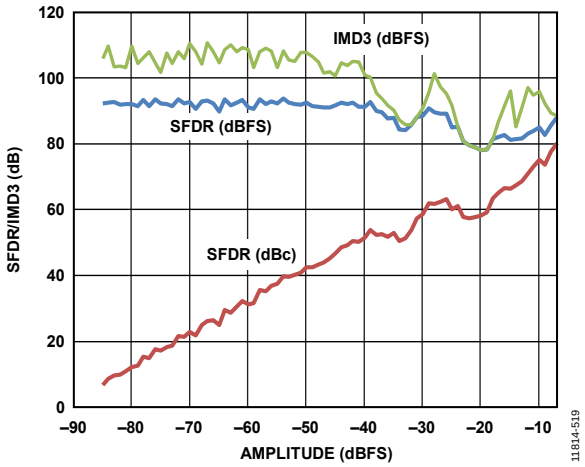

Figure 54. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.6 GSPS at 1807 MHz AIN

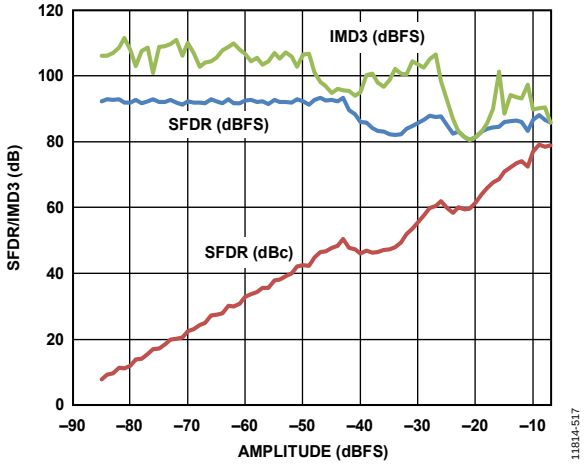

Figure 52. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.6 GSPS at 230 MHz AIN

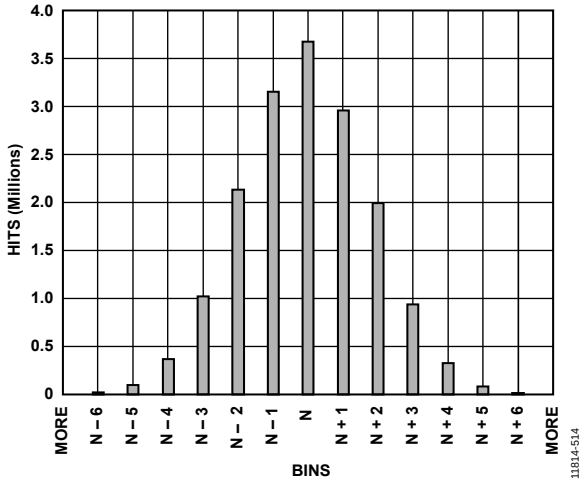

Figure 55. Input Referred Noise Histogram with 2.6 GSPS

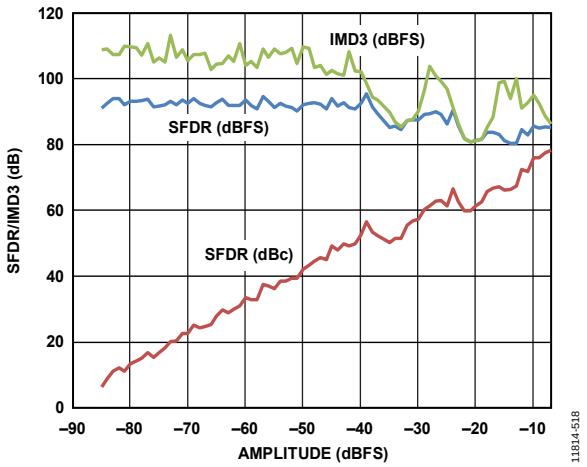

Figure 53. Two Tone SFDR and IMD3 vs. Analog Input Amplitude at 2.6 GSPS at 730 MHz AIN

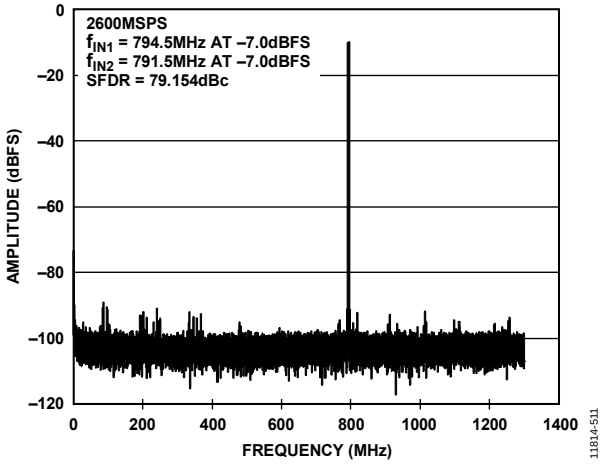

Figure 56. Two Tone FFT Plot at 2.6 GSPS AIN = 1807 MHz

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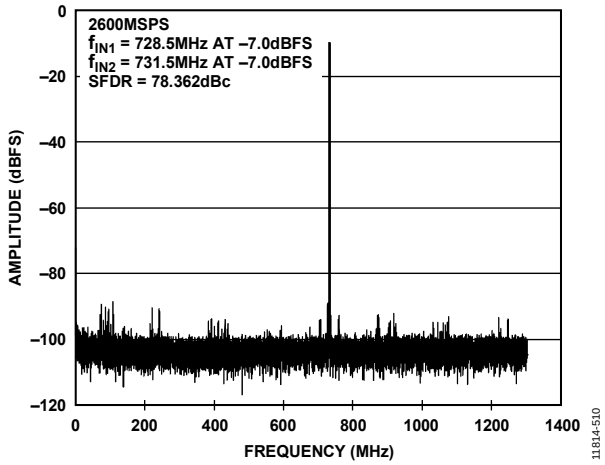

Figure 57. Two Tone FFT Plot at 2.6 GSPS AIN = 730 MHz

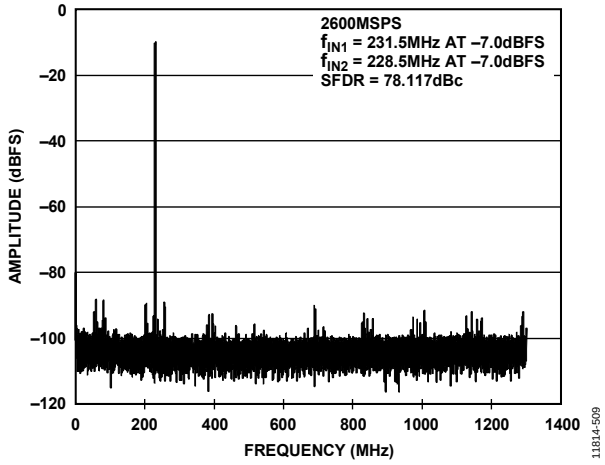

Figure 58. Two Tone FFT Plot at 2.6 GSPS AIN = 230 MHz

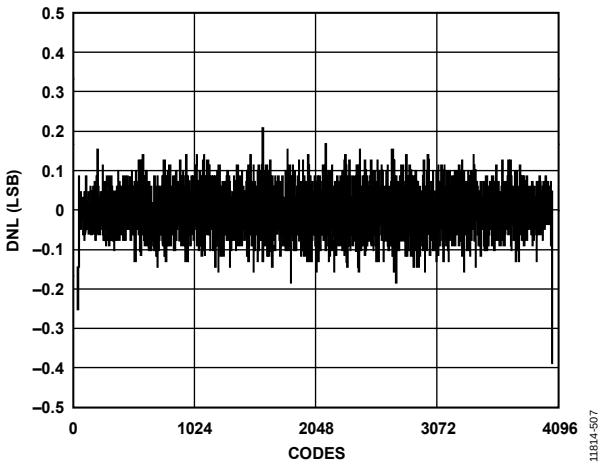

Figure 59. Differential Nonlinearity (DNL) at 2.6 GSPS

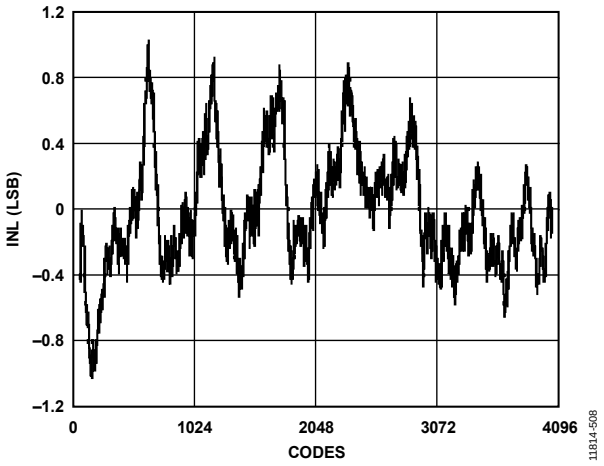

Figure 60. Integral Nonlinearity (INL) at 2.6 GSPS

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EQUIVALENT TEST CIRCUITS

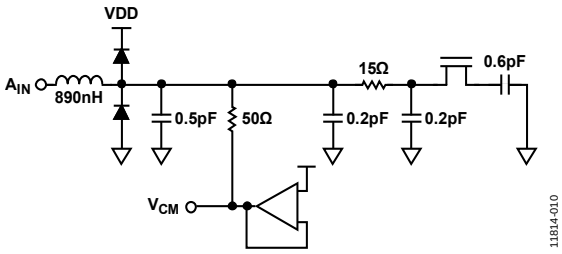

Figure 61. Equivalent Analog Input Circuit

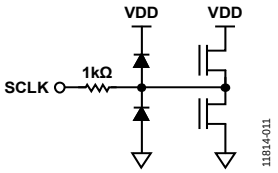

Figure 62. Equivalent SCLK Circuit

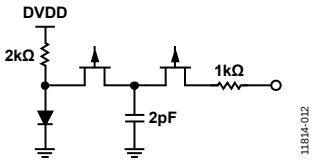

Figure 63. Equivalent VMON Temperature Sensor Circuit (DVDD)

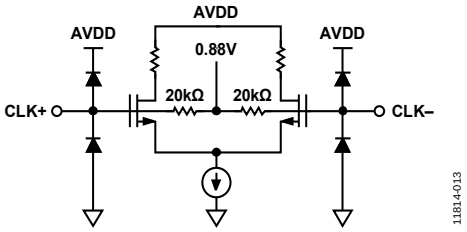

Figure 64. Equivalent Clock Input Circuit

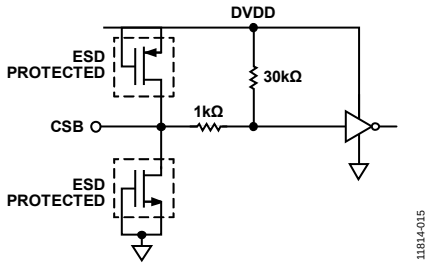

Figure 65. Equivalent CSB/PWDN Input Circuit

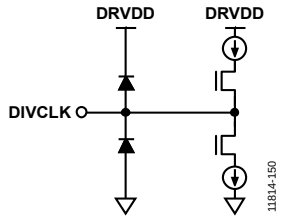

Figure 66. Equivalent DIVCLK Output Circuit (DRVDD)

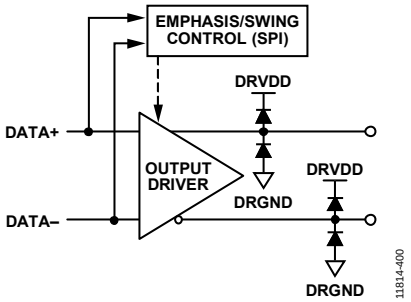

Figure 67. Digital Outputs

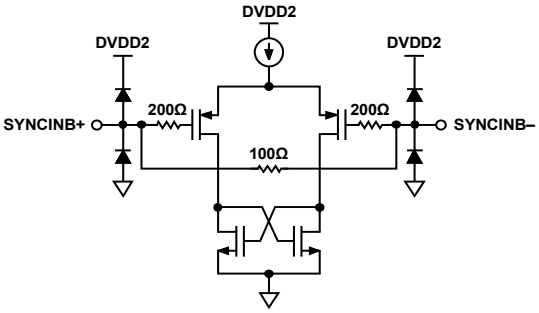

Figure 68. Equivalent SYNCINB± Input

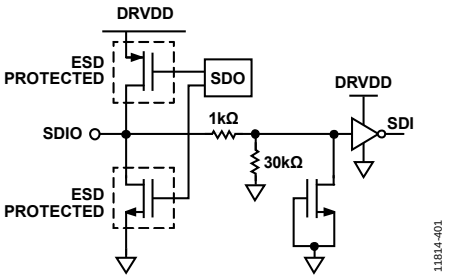

Figure 69. Equivalent SDIO Circuit

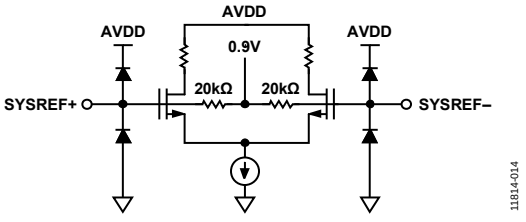

Figure 70. Equivalent SYSREF± Input Circuit

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THEORY OF OPERATION

ADC ARCHITECTURE

The AD9625 is a pipelined ADC. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output drive current.

Synchronization capability is provided to allow synchronized timing between multiple devices.

FAST DETECT

The fast detect block within the AD9625 generates a fast detection bit (FD), which, when used with variable gain amplifier front-end blocks, reduces the gain and prevents the ADC input signal levels from exceeding the converter range.

Figure 71 shows the rapidity by which the detection bit is programmable using an upper threshold, lower threshold, and dwell time.

The FD bit is set when the absolute value of the input signal exceeds the programmable upper threshold level. The FD bit clears only when the absolute value of the input signal drops below the lower threshold level for greater than the programmable dwell time, thereby providing hysteresis and preventing the FD bit from excessive toggling.

GAIN THRESHOLD OPERATION

For best performance, the AD9625 needs an input signal to perform internal calibration. This signal needs to exceed a set threshold that is established through register settings. The threshold prohibits background calibration updates for small signal amplitudes. The threshold for gain calibration is enabled by default.

Threshold Operation

The absolute value of every sample is accumulated to produce an average voltage estimate.

When the calibration has run for its predetermined number of samples, the voltage estimate is compared to the data set threshold. If the voltage estimate is greater than the threshold, the calibration coefficients update; otherwise, no update occurs.

Threshold Format

The threshold registers are all 16-bit registers loaded via the SPI one byte at a time. The threshold values range from 0 to 16,384, corresponding to a voltage range of 0.0 V to 1.2 V (full scale).

The calibration threshold range is 0 to 16,384 (0x00 to 0x4000, hexadecimal) and represents the average magnitude of the input. For example, to set the threshold so that a −6 dBFS input sine wave sits precisely at the threshold requires a threshold setting of

$$16{,}384 \times 10^{\frac{-6}{20}} \times \frac{2}{\pi} \geq 5228$$

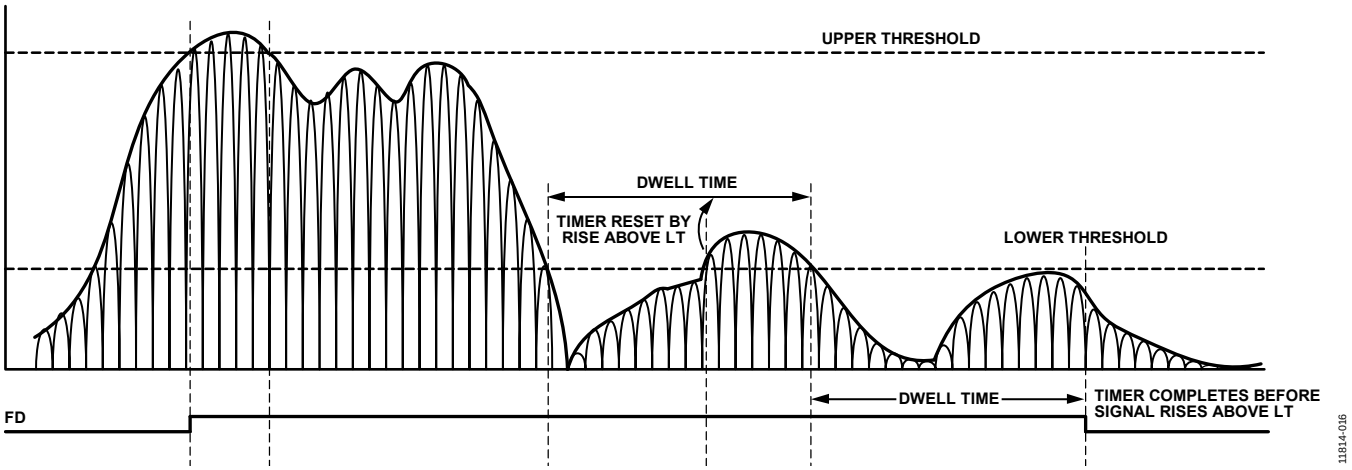

Figure 71. Fast Detection Bit

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TEST MODES

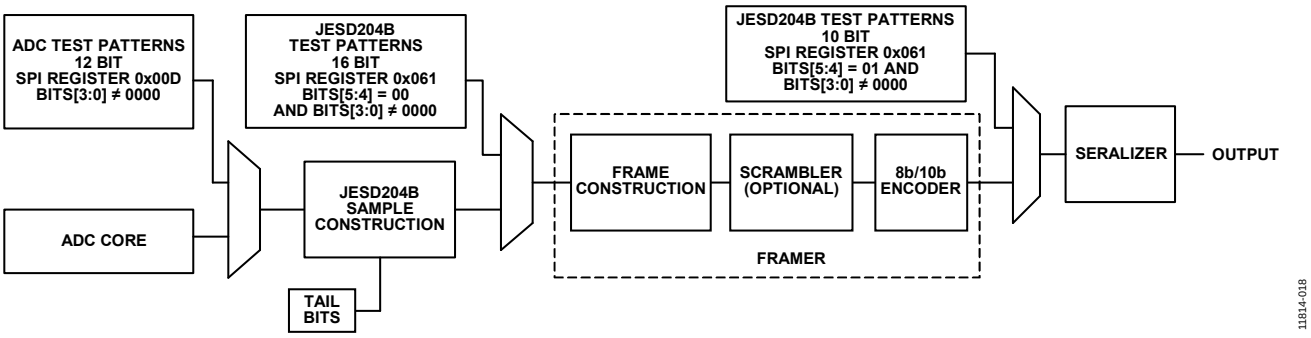

Figure 72. Test Modes

Table 10. Flexible Output Test Modes from SPI Register 0x00D

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1 (Default Twos Complement Format)	Digital Output Word 2 (Default Twos Complement Format)	Subject to Data Format Select
0000	Off (default)	Not applicable	Not applicable	Yes
0001	Midscale short	0000 0000 0000	= Word 1	Yes
0010	Positive full scale	0111 1111 1111	= Word 1	Yes
0011	Negative full scale	1000 0000 0000	= Word 1	Yes
0100	Alternating checkerboard	1010 1010 1010	0101 0101 0101	No
0101	PN sequence long	Not applicable	Not applicable	Yes
0111	One-/zero-word toggle	1111 1111 1111	0000 0000 0000	No
1000	User test mode	User data from Register 0x019 to Register 0x020	User data from Register 0x019 to Register 0x020	Yes
1111	Ramp output	N	N + 1	No

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ANALOG INPUT CONSIDERATIONS

The AD9625 has a differential analog input, which is optimized to provide superior wideband performance and must be driven differentially. For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. Mismatch between VIN+ and VIN− introduces undesired distortion. A wideband transformer, balun, or amplifier can provide the differential analog inputs for applications that require a single-ended to differential conversion.

DIFFERENTIAL INPUT CONFIGURATIONS

Optimum performance is achieved while driving the AD9625 in a differential input configuration. A passive input configuration can be used with a single to differential balun at the analog input to the AD9625. Because the AD9625 does not make use of an internal input buffer, an external network needs to be designed to reduce bandwidth peaking and minimize kickback from the ADC sampling capacitor.

Small series resistors (R3 and R4) limit input bandwidth, but can be installed to further improve performance. Choose the input network components such that its equivalent impedance, in parallel with the 100 Ω input impedance of the AD9625, is matched to the output impedance of the balun or amplifier.

Using a larger value for R3 and R4 suppresses the input kickback from the sampling capacitor seen at the input to the AD9625. However, the tradeoff is a lower usable input bandwidth and an increase in the amount of signal power needed to drive into the network for the AD9625 to sample a full-scale signal.

Series isolation resistors (R5 and R6) are recommended to reduce bandwidth peaking and minimize kickback from the ADC sampling capacitor. Table 11 lists the front-end requirements.

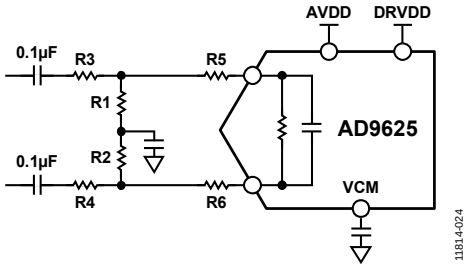

Figure 73. Recommended Front-End Network

Table 11. Recommended Front-End Components

Component	Component Value
R1	33 Ω to 50 Ω (termination)
R2	33 Ω to 50 Ω (termination)
R3	0 Ω to 33 Ω (lower for higher bandwidth)
R4	0 Ω to 33 Ω (lower for higher bandwidth)
R5	33 Ω
R6	33 Ω

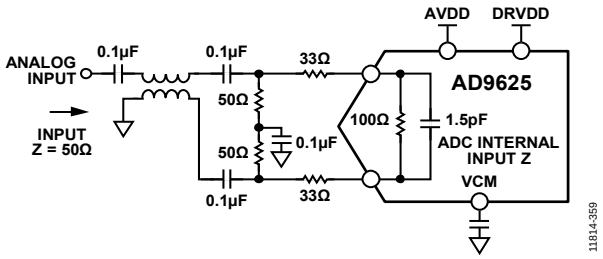

Figure 74. Input Network Example for Passive Balun with High Bandwidth

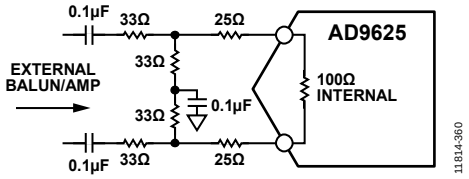

Figure 75. Input Network Example for Passive Balun and >2 GHz ADC Bandwidth

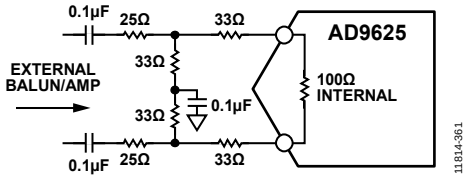

Figure 76. Input Network Example for Passive Balun and <2 GHz ADC Bandwidth

USING THE ADA4961

As an alternative to using only a passive differential balun input for wideband applications, the ADA4961 differential amplifier driver can be used (see Figure 80).

The ADA4961 is a high performance BiCMOS RF differential gain amplifier (DGA) optimized for driving heavy loads out to 2.0 GHz and beyond. It typically achieves −90 dBc IMD3 performance at 500 MHz and −85 dBc at 1.5 GHz. The device also exhibits very low output noise (6.8 nV/√Hz). Together, these performance numbers result in an SFDR of 133 dB/Hz at 1.5 GHz.

The ADA4961 has an internal differential input impedance of 100 Ω and a differential dynamic output impedance of 50 Ω, eliminating the need for external termination resistors. The digital adjustability provides for 1 dB resolution, thus optimizing SNR for input levels spanning 21 dB.

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Figure 80 uses a 1:2 impedance transformer to provide the 100 Ω input impedance of the ADA4961 with a matched input. The open collector outputs of the ADA4961 are biased through the two 560 nH inductors. The two 0.1 µF capacitors on the outputs decouple the 5 V inductor voltage from the input common-mode voltage of the ADA4961. The two 50 Ω resistors in parallel with the 100 Ω input impedance of the AD9625 provide the 50 Ω load to the ADA4961, whose gain is load dependent. The 2 nH inductors and the 1.5 pF internal capacitance of the AD9625 constitute a 1 GHz low-pass filter to −1 dB. The two 10 Ω isolation resistors suppress any switching currents from the AD9625 sample-and-hold circuitry. The circuit depicted in Figure 80 provides variable gain, isolation, filtering and source matching for the AD9625. By using this circuit with the ADA4961 in a gain of 15 dB (maximum gain) an SNRFS of 55 dB and an SFDR performance of 77 dBc are achieved with a 1 GHz input as shown in Figure 80.

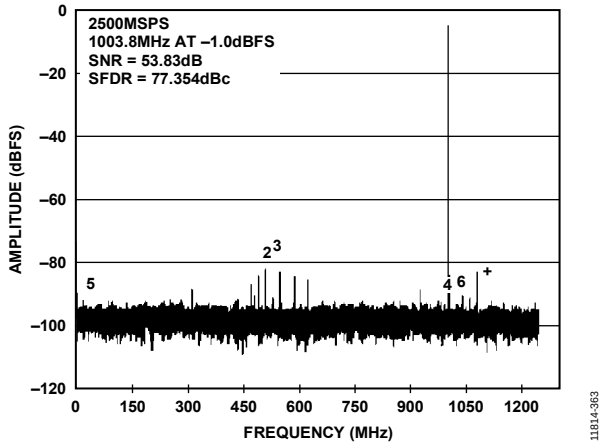

Figure 77. Measured Single-Tone Performance of the Circuit Shown in Figure 80 for a 1 GHz Input Signal Using Maximum Gain (15 dB)

The two-tone 1 GHz IMD of two 0.55 V p-p signals have an SFDR of greater than 75 dBc, as shown in Figure 78.

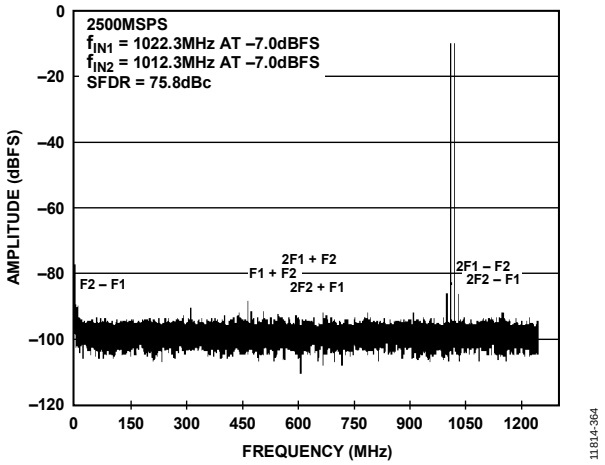

Figure 78. Measured Two-Tone Performance of the Circuit Shown in Figure 80 for a 1 GHz input Signal Using Maximum Gain (15 dB)

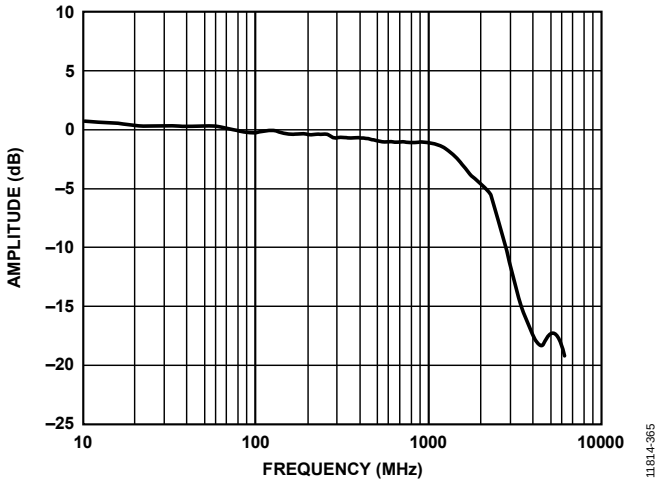

Figure 79. Measured Frequency Response of the AD9625 Interface with ADA4961 Depicted in Figure 80

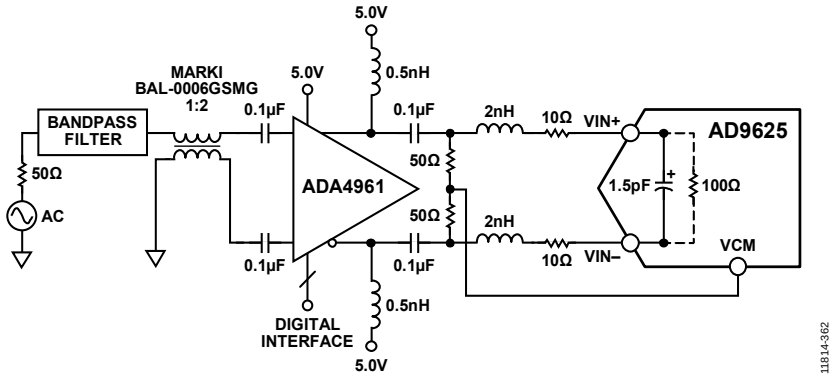

Figure 80. Configuration for Driving the AD9625 with ADA4961

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DC COUPLING

The AD9625 can operate using a dc-coupled input configuration. The differential analog common-mode input signal would need to be referenced to the V_{CM} output of the AD9625.

CLOCK INPUT CONSIDERATIONS

For optimum performance, drive the AD9625 sample clock inputs (CLK+ and CLK−) with a differential signal. This signal is typically ac-coupled to the CLK+ and CLK− pins via a transformer or capacitors. These pins are biased internally and require no additional biasing.

Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_A) due only to aperture jitter (t_J) can be calculated by

$$SNR = 20 \times \log 10(1/(2 \times \pi \times f_A \times t_J))$$

In this equation, the rms aperture jitter represents the root-mean-square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 81).

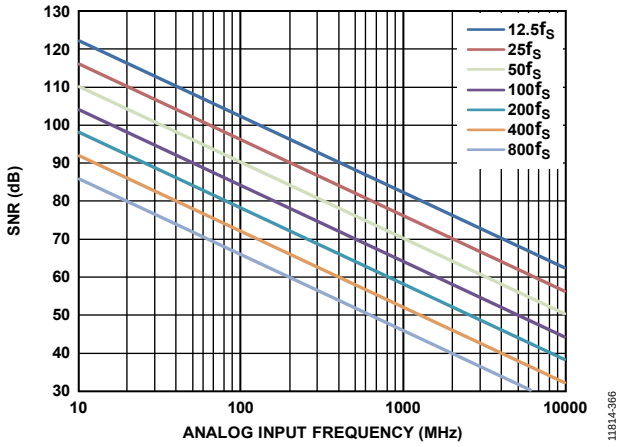

Figure 81. Ideal SNR vs. Analog Input Frequency and Jitter

In cases where aperture jitter may affect the dynamic range of the AD9625, treat the clock input as an analog signal. To avoid modulating the clock signal with digital noise, separate power supplies for clock drivers from the ADC output driver supplies. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step. Refer to the AN-501 Application Note and the AN-756 Application Note for more information about jitter performance as it relates to ADCs.

Clock Duty Cycle Considerations

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

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DIGITAL DOWNCONVERTERS (DDC)

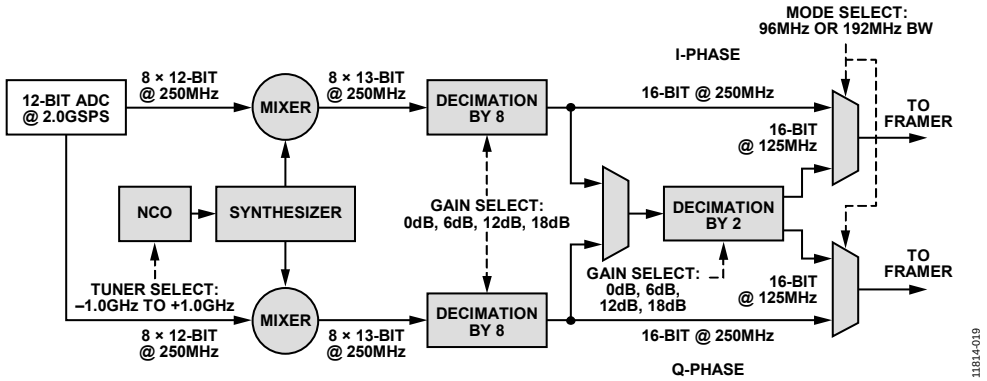

Figure 82. Digital Downconverter Block Diagram Operating at 2.0 GSPS

The AD9625 architecture includes two DDCs, each designed to extract a portion of the full digital spectrum captured by the ADC. Each tuner consists of an independent frequency synthesizer and quadrature mixer; a chain of low-pass filters for rate conversion follows these components. Assuming a sampling frequency of 2.500 GSPS, the frequency synthesizer (10-bit NCO) allows for 1024 discrete tuning frequencies, ranging from −1.2499 GHz to +1.2500 GHz, in steps of 2500/1024 = 2.44 MHz. The low-pass filters allow for two modes of decimation.

- A high bandwidth mode, 240 MHz wide (from −120 MHz to +120 MHz), sampled at 2.5 GHz/8 = 312.5 MHz for the I and Q branches separately. The 16-bit samples from the I and Q branches are transmitted through a dedicated JESD204B interface.
- A low bandwidth mode, 120 MHz wide (from −60 MHz to +60 MHz), sampled at 2.5 GHz/16 = 156.25 MHz for the I and Q branches separately. The 16-bit samples from the I and Q branches are transmitted through a dedicated JESD204B interface.

By design, all of the blocks operate at a single clock frequency of 2.5 GHz/8 = 312.5 MHz.

Each filter stage includes a gain control block that is programmable by the user. The gain varies from 0 dB to 18 dB, in steps of 6 dB, and the gain is applied before final scaling and rounding. The gain control feature may be useful in cases where the tuner filters out a strong out-of-band interferer, leaving a weak in-band signal.

FREQUENCY SYNTHESIZER AND MIXER

For a sampling rate of 2.500 GHz, the synthesizer (10-bit NCO) outputs one of 1024 possible complex frequencies from −1.249 GHz to +1.250 GHz. The synthesizer employs the direct digital synthesis technique, using look-up sine tables and a phase accumulator. The user specifies the tuner frequency by writing to a 10-bit phase increment register.

NUMERICALLY CONTROLLED OSCILLATOR

Each DDC has a 10-bit oscillator that is synthesized and mixed with the ADC output data. The 10-bit phase can be tuned for each DDC based on the value used in its NCO registers. The phase for DDC0 is located with Register 0x132 and Register 0x131. The phase for DDC1 is located with Register 0x13A and Register 0x139. The NCO output frequency for DDC0 = (decimal(Register 0x132[1:0]; Register 0x131[7:0]) × f_S)/1024. The NCO output frequency for DDC1 = (decimal(Register 0x13A[1:0]; Register 0x139[7:0]) × f_S)/1024.

HIGH BANDWIDTH DECIMATOR

The first filter stage is designed for a rate reduction factor of 8, yielding a sample rate of 2.500 GHz/8 = 312.5 MHz. To achieve a combination of low complexity and low clock rate, the DDC employs a decimate-by-8 polyphase fuse filter that receives eight 13-bit samples from the mixer block at every clock cycle.

The block design provides user specified gain control, from 0 dB to 18 dB in steps of 6 dB. The gain is applied before final scaling and rounding to 16 bits.

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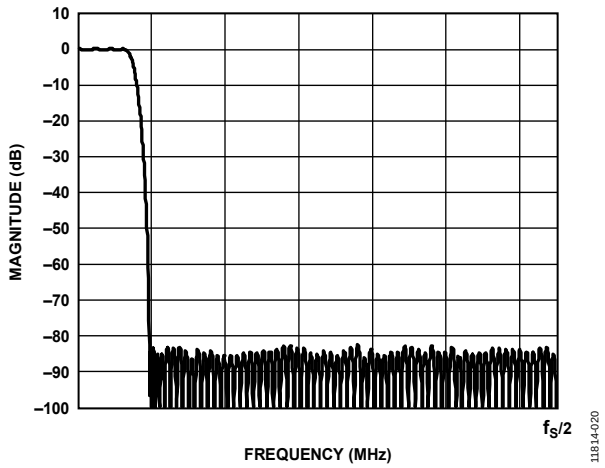

Figure 83. Magnitude Response of the Decimate-by-8 Polyphase Fuse Filter

Filter performance is shown in Figure 83 and Figure 84. The filter yields an effective bandwidth of 120 MHz, with a transition band of 156.5 MHz − 120 MHz = 36.5 MHz. Therefore, the two-sided complex bandwidth of the filter is 240 MHz.

A rejection ratio of 85 dB ensures that the seven aliases that fold back into the pass band yield an SNR of 85 dB − $10\log^{10}(7)$ = 76.5 dB, which ensures that the aliases remain sufficiently below the noise floor of the input signal. The pass-band ripple is ±0.05 dB, as shown in Figure 84.

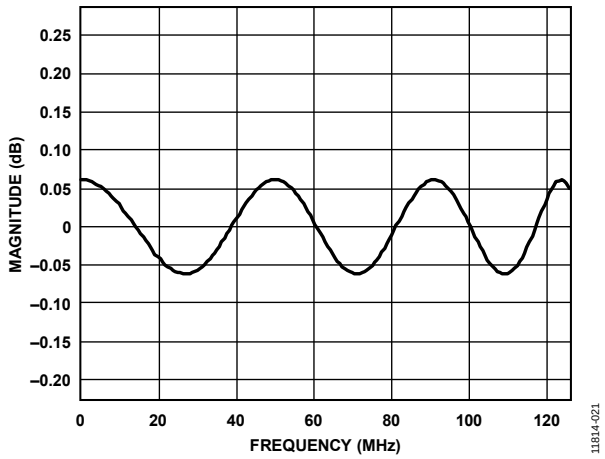

Figure 84. Magnitude Ripple in the High Bandwidth Pass Band

The high bandwidth decimator has a filter architecture that consists of a 142 tap delay line. The coefficients are 17 bits each and are listed in Table 12.

Table 12. Filter Tap Coefficients for High Bandwidth Decimator

Tap Number	Coefficient
1	−38
2	−57
3	−92
4	−132
5	−172
6	−204
7	−219
8	−207
9	−162
10	−79
11	+43
12	+196
13	+369
14	+540
15	+685
16	+780
17	+800
18	+727
19	+554
20	+289
21	−48
22	−420
23	−778
24	−1069
25	−1238
26	−1242
27	−1055
28	−677
29	−135
30	+513
31	+1186
32	+1785
33	+2210
34	+2372
35	+2209
36	+1698
37	+869
38	−200
39	−1382
40	−2516
41	−3425
42	−3945
43	−3944
44	−3353
45	−2179
46	−519
47	+1446
48	+3467
49	+5250
50	+6496
51	+6945

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Tap Number	Coefficient
52	+6412
53	+4831
54	+2276
55	−1031
56	−4725
57	−8330
58	−11304
59	−13098
60	−13222
61	−11306
62	−7160
63	−808
64	+7498
65	+17281
66	+27882
67	+38515
68	+48340
69	+56550
70	+62451
71	+65536
72	+65536
73	+62451
74	+56550
75	+48340
76	+38515
77	+27882
78	+17281
79	+7498
80	−808
81	−7160
82	−11306
83	−13222
84	−13098
85	−11304
86	−8330
87	−4725
88	−1031
89	+2276
90	+4831
91	+6412
92	+6945
93	+6496
94	+5250
95	+3467
96	+1446
97	−519
98	−2179
99	−3353
100	−3944
101	−3945
102	−3425
103	−2516
104	−1382
105	−200
106	+869
107	+1698
108	+2209
109	+2372
110	+2210
111	+1785
112	+1186
113	+513
114	−135
115	−677
116	−1055
117	−1242
118	−1238
119	−1069
120	−778
121	−420
122	−48
123	+289
124	+554
125	+727
126	+800
127	+780
128	+685
129	+540
130	+369
131	+196
132	+43
133	−79
134	−162
135	−207
136	−219
137	−204
138	−172
139	−132
140	−92
141	−57
142	−38

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LOW BANDWIDTH DECIMATOR

Use the second filter stage in the optional low bandwidth mode only. It achieves an additional rate reduction factor of 2, yielding a final sample rate of 2.500 GHz/16 = 156.25 MHz. The internal architecture of the low bandwidth decimation filter is similar to that of a high bandwidth decimator. Moreover, for ease of physical design, the block operates at 312.5 MHz, a result of which both the I- and Q-phases can share the filter engine.

The performance of the low bandwidth decimation filter is shown in Figure 85 and Figure 86. The filter yields an effective bandwidth of 60 MHz, with a transition band of 81.25 MHz − 60 MHz = 21.25 MHz. Thus, the two sided, complex bandwidth of the filter is 120 MHz. A rejection ratio of 85 dB ensures that the alias region folds back well below the noise floor of the input signal.

As with the high bandwidth filter, this block provides user specified gain control, from 0 dB to 18 dB, in steps of 6 dB. The gain is applied before final quantization at the output of the low bandwidth decimation filter to 16 bits.

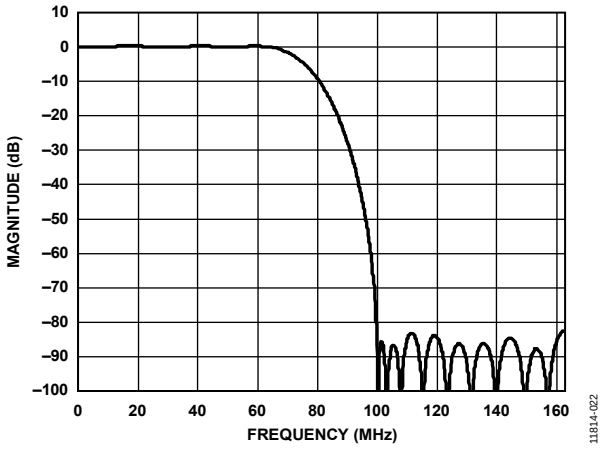

Figure 85. Magnitude Response of Decimate-by-2 Filter

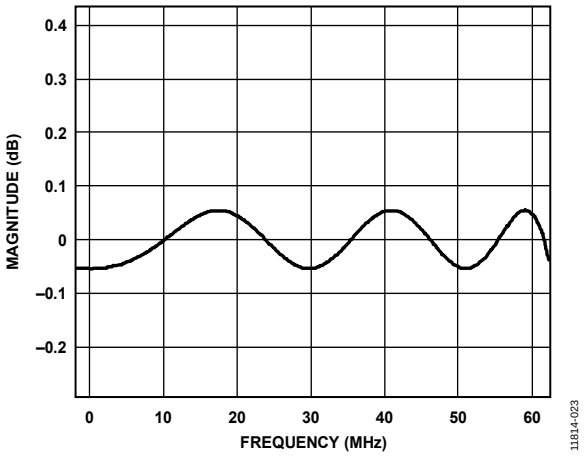

Figure 86. Magnitude Ripple in the Low Bandwidth Pass Band

The low bandwidth decimator has a filter architecture that consists of a 31 tap delay line. The coefficients are 17 bits each and are listed in Table 13.

Table 13. Filter Tap Coefficients for Low Bandwidth Decimator

Tap Number	Coefficient
1	+126
2	+312
3	−16
4	−859
5	−628
6	+1217
7	+1428
8	−1944
9	−3227
10	+2511
11	+6302
12	−3099
13	−13075
14	+3441
15	+43442
16	+65536
17	+43442
18	+3441
19	−13075
20	−3099
21	+6302
22	+2511
23	−3227
24	−1944
25	+1428
26	+1217
27	−628
28	−859
29	−16
30	+312
31	+126

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DIGITAL OUTPUTS

INTRODUCTION TO THE JESD204B INTERFACE

The AD9625 digital output complies with the JEDEC Standard No. JESD204B, *Serial Interface for Data Converters*. JESD204B is a protocol to link the AD9625 to a digital processing device over a serial interface up to and above 6.5 Gbps link speeds. The benefits of the JESD204B interface over LVDS include a reduction in required board area for data interface routing, and enabling smaller packages for converter and logic devices. The AD9625 supports one, two, four, six, or eight output lanes.

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8-bit/10-bit encoding as well as optional scrambling to form serial output data. Lane synchronization is supported using special characters during the initial establishment of the link. Additional data that is used to maintain synchronization is embedded in the data stream thereafter. A JESD204B receiver is required to complete the serial link. For additional details on the JESD204B interface, users are encouraged to refer to the JESD204B standard.

The AD9625 JESD204B transmit block maps to two digital down converters for the outputs of the ADC over a link. A link can be configured to use up to eight JESD204B lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (AD9625 output) and receiver (FPGA, ASIC, or logic device).

Table 14 describes the JESD204B interface nomenclature (the terms, converter device and link, are used interchangeably in the specification).

Table 14. JESD204B Interface Nomenclature

Symbol	Description
S	Samples transmitted per single converter per frame cycle
M	Number of converters per converter device (link)
L	Number of lanes per converter device (link)
N	Converter resolution
N'	Total number of bits per sample
CF	Number of control words per frame clock cycle per converter device (link)
CS	Number of control bits per conversion sample
K	Number of frames per multiframe
HD	High density mode
F	Octets per frame
C	Control bit (overrange, timestamp)
T	Tail bit

The AD9625 adheres to the JESD204B draft specification, which provides a high speed, serial, embedded clock interface standard for data converters and logic devices. It is designed as an MCDA-ML, Subclass 1 device that uses the SYSREF± input signal for multichip synchronization and deterministic latency. This design adheres to the following basic JESD204B link configuration parameters:

- M = 1 (single converter, always for AD9625)
- L = 1 to 8 (up to eight lanes)
- S = 4 (four samples per JESD204B frame)
- F = 1, 2, 4, 8 (up to 8 octets per frame)
- N' = 12, 16 (12- or 16-bit JESD204B word size)
- HD = 0, 1 (high density mode, sample span multiple lanes)

FUNCTIONAL OVERVIEW

The block diagram in Figure 87 shows the flow of data through the JESD204B hardware from the sample input to the physical output. The processing can be divided into layers that are derived from the OSI model widely used to describe the abstraction layers of communications systems. These are the transport layer, data link layer, and physical layer (serializer). Each of these layers are described in detail in the following sections.

Transport Layer

The transport layer handles packing the data (consisting of samples and optional control bits) into 8-bit words that are sent to the data link layer. The transport layer is controlled by rules derived from the link configuration data. It packs data according to the rules, adding tail bits to fill gaps when required.

Data Link Layer

The data link layer is responsible for the low level functions of passing data across the link. These include optionally scrambling the data, handling the synchronization process for characters, frames, and lanes across the links, encoding 8-bit data-words into 10-bit characters, and inserting appropriate control characters into the data output. The data link layer is also responsible for sending the initial lane alignment sequence (ILAS), which contains the link configuration data, used by the receiver (Rx) to verify the settings in the transport layer.

Physical Layer

The physical layer consists of the high speed circuitry clocked at the serial clock rate. The physical layer includes the serialization circuits and the high speed drivers.

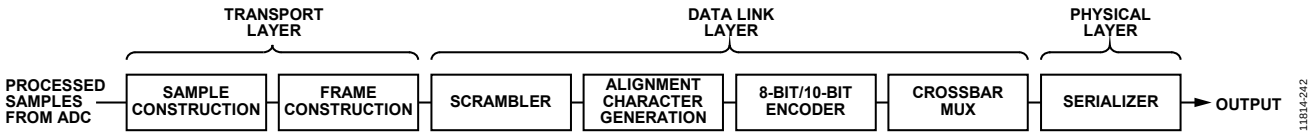

Figure 87. Data Flow

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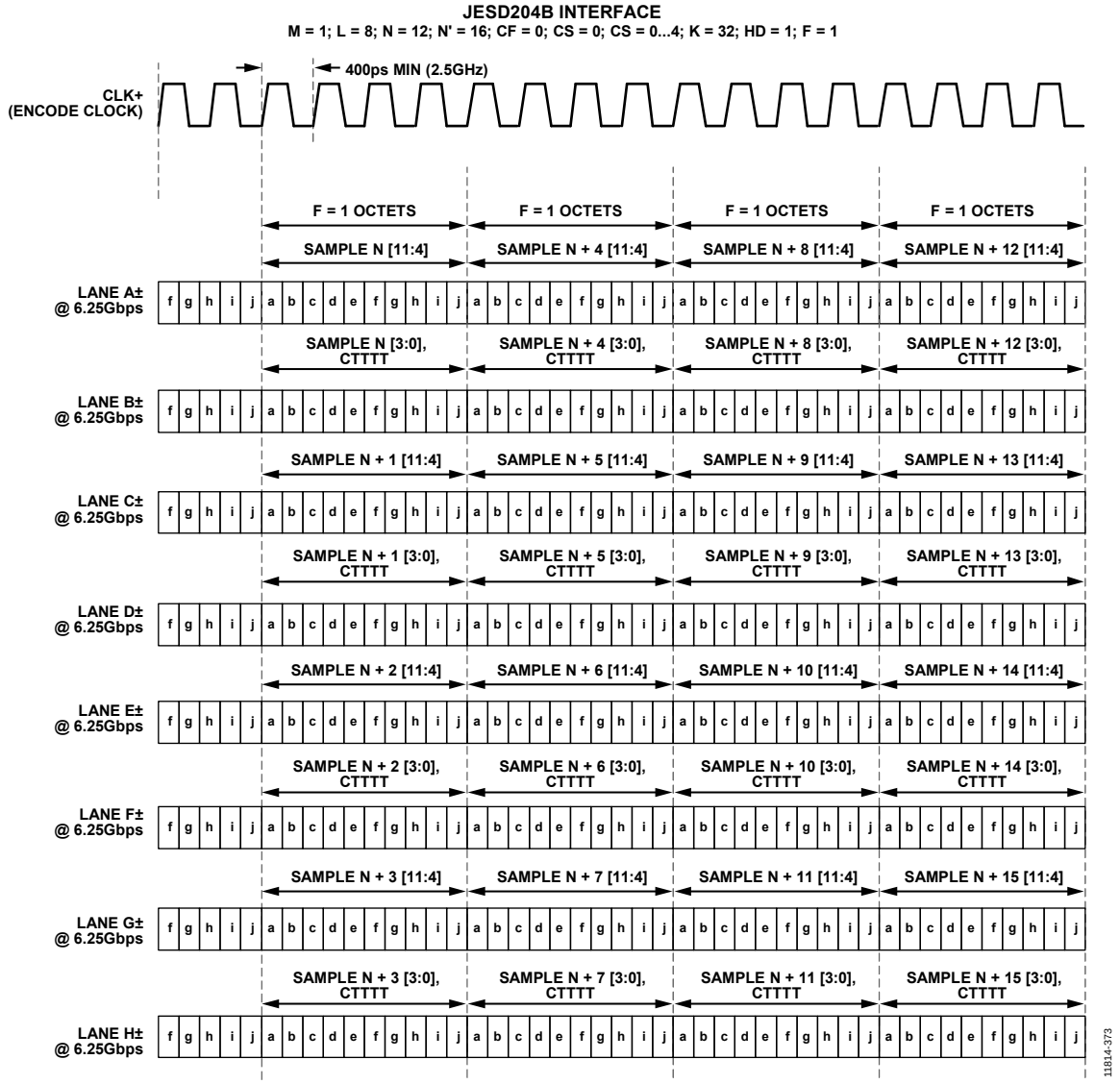

Figure 88. JESD204B Lane Data Mapping

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JESD204B LINK ESTABLISHMENT

The AD9625 JESD204B Tx interface operates in Subclass 1 as defined in the JEDEC Standard No. 204B-July 2011 specification. It is divided into the following steps: code group synchronization, initial lane alignment sequence, and data streaming.

Code Group Synchronization (CGS) and SYNCINB±

CGS is the process where the JESD204B receiver finds the boundaries between the 10-bit characters in the stream of data. During the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver (external logic device) must locate the /K28.5/ characters in its input data stream using clock and data recovery (CDR) techniques.

The receiver issues a synchronization request by activating the SYNCINB± pins of the AD9625. The JESD204B Tx begins sending /K28.5/ characters until the next LMFC boundary. When the receiver has synchronized, it waits for the correct reception of at least four consecutive /K28.5/ symbols. It then deactivates SYNCINB±. The AD9625 then transmits an initial lane alignment sequence (ILAS) on the following LMFC boundary.

For more information on the code group synchronization phase, refer to the JEDEC Standard No. 204B-July 2011, Section 5.3.3.1.

The SYNCINB± pin operation can be controlled by SPI. The SYNCINB± signal is a differential LVDS mode signal by default, but it can also be driven single ended. For more information on configuring the SYNCINB± pin operation, refer to the Memory Map section.

Initial Lane Alignment Sequence (ILAS)

The ILAS phase follows the CGS phase and begins on the next LMFC boundary. The ILAS consists of four mulitframes, with an /R/ character marking the beginning and an /A/ character marking the end. The ILAS begins by sending an /R/ character followed by 0 to 255 ramp data for one multiframe. On the second multiframe, the link configuration data is sent starting with the third character. The second character is a /Q/ character to confirm that the link configuration data follows. All undefined data slots are filled with ramp data. The ILAS sequence is never scrambled.

The ILAS sequence construction is shown in Figure 90. The four multiframes include the following:

- Multiframe 1: begins with an /R/ character (K28.0) and ends with an /A/ character (K28.3).
- Multiframe 2: begins with an /R/ character followed by a /Q/ [K28.4] character, followed by link configuration parameters over 14 configuration octets and ends with an /A/ character. Many of the parameter values are of the notation of the value, −1.
- Multiframe 3: this is the same as Multiframe 1.
- Multiframe 4: this is the same as Multiframe 1.

Data Streaming

After the initial lane alignment sequence is complete, the user data is sent. In a usual frame, all characters are user data. However, to monitor the frame clock and multiframe clock synchronization, there is a mechanism for replacing characters with /F/ or /A/ alignment characters when the data meets certain conditions. These conditions are different for unscrambled and scrambled data. The scrambling operation is enabled by default but may be disabled using SPI.

For scrambled data, any 0xFC character at the end of a frame is replaced by an /F/, and any 0x7C character at the end of a multiframe is replaced with an /A/. The JESD204B Rx checks for /F/ and /A/ characters in the received data stream and verifies that they only occur in the expected locations. If an unexpected /F/ or /A/ character is found, the receiver handles the situation by using dynamic realignment or activating the SYNCINB± signal for more than four frames to initiate a resynchronization. For unscrambled data, if the final character of two subsequent frames is equal, the second character is replaced with an /F/ if it is at the end of a frame, and an /A/ if it is at the end of a multiframe.

Insertion of alignment characters may be modified using SPI. The frame alignment character insertion is enabled by default. More information on the link controls is available in the Memory Map section, Register 0x062.

Link Setup Parameters

The following steps demonstrate how to configure the AD9625 JESD204B interface and the output:

1. Disable the lanes before changing configuration.
2. Select one quick configuration option.
3. Configure the detailed options.
4. Check FCHK, checksum of JESD204B interface parameters.
5. Set additional digital output configuration options.
6. Reenable the required lane(s).
7. Before modifying the JESD204B link parameters, disable the link and hold it in reset.

8-Bit/10-Bit Encoder

The 8-bit/10-bit encoder converts 8-bit octets into 10-bit characters and inserts control characters into the stream when needed. The control characters used in JESD204B are shown in Table 15. The 8-bit/10-bit encoding allows the signal to be dc balanced by using the same number of ones and zeros.

The 8-bit/10-bit interface has options that may be controlled via SPI. These operations include bypass, invert or mirror. These options are intended to be a troubleshooting tool for the verification of the digital front end (DFE).

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Digital Outputs, Timing, and Controls

The AD9625 physical layer consists of drivers that are defined in the JEDEC Standard No. 204B-July 2011. The differential digital outputs are powered up by default. The drivers utilize a dynamic 100 Ω internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 300 mV p-p swing at the receiver (see Figure 89). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage should be DRVDD/2; otherwise, 0.1 µF ac coupling capacitors can be used to terminate to any single-ended voltage.

The AD9625 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver inputs as possible.

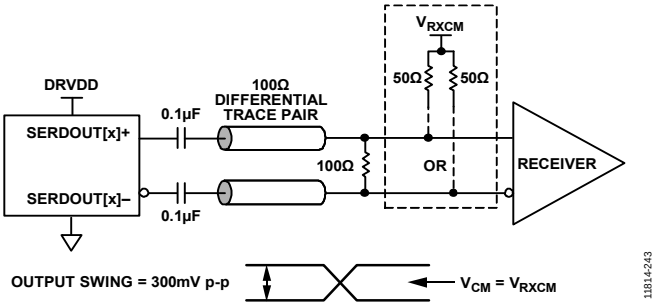

Figure 89. AC-Coupled Digital Output Termination Example

If there is no far end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

De-Emphasis

De-emphasis enables the receiver eye diagram mask to be met in conditions where the interconnect insertion loss does not meet the JESD204B specification. The de-emphasis feature should only be used when the receiver is unable to recover the clock due to excessive insertion loss. Under normal conditions, it is disabled to conserve power. Additionally, enabling and setting too high a de-emphasis value on a short link may cause the receiver eye diagram to fail. Using the de-emphasis setting may increase EMI. See the Memory Map section for details.

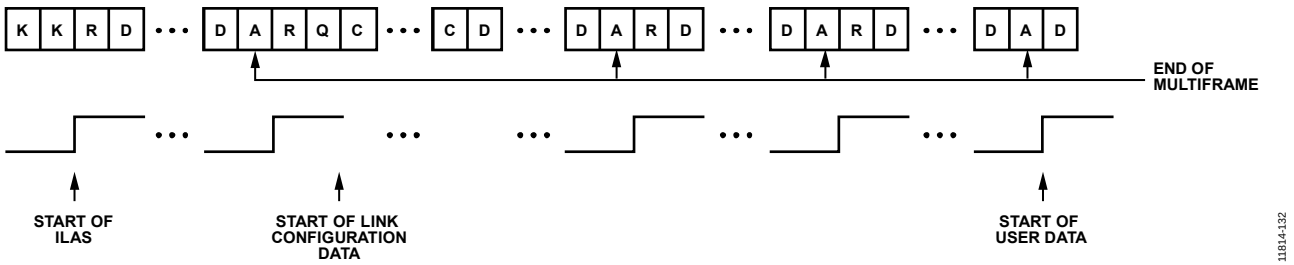

Figure 90. Initial Lane Alignment Sequence

Table 15. AD9625 Control Characters Used in JESD204B

Abbreviation	Control Symbol	8-Bit Value	10-Bit Value RD (Running Disparity) = −1	10-Bit Value RD (Running Disparity) = +1	Description
/R/	/K28.0/	000 11100	001111 0100	110000 1011	Start of multiframe
/A/	/K28.3/	011 11100	001111 0011	110000 1100	Lane alignment
/Q/	/K28.4/	100 11100	001111 0010	110000 1101	Start of link configuration data
/K/	/K28.5/	101 11100	001111 1010	110000 0101	Group synchronization
/F/	/K28.7/	111 11100	001111 1000	110000 0111	Frame alignment

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Table 16. JESD204B Mode of Operation (M = 1, S = 4, N' = 16, Unless Otherwise Noted)

Quick Configuration Value	Description[1]	Lanes (L)	Octets/ Frame (F)	Sample Clock Rate		Sample Clock Multiplier	JESD204B Lane Rate	
				Minimum MSPS	Maximum MSPS		Minimum Mbps	Maximum Mbps
0x02	Generic	2	4	330	650	10	3300	6500
0x04	Generic	4	2	650	1300	5	3250	6500
0x06	Generic (N' = 12)	6	1	1300	2500	2.5	3250	6250
0x08	Generic	8	1	1300	2500	2.5	3250	6250
0x42	$f_S \times 8$	2	4	406	813	8	3250	6500
0x44	$f_S \times 4$	4	2	813	1625	4	3250	6500
0x48	$f_S \times 2$	8	1	1625	2500	2	3250	5000
0x81	Single DDC, high BW	1	8	650	1300	5	3250	6500
0x82	Single DDC, high BW	2	4	1300	2500	2.5	3250	6250
0x91	Single DDC, low BW	1	8	1300	2500	2.5	3250	6250
0xC1	Dual DDC, high BW	1	8	330	650	10	3300	6500
0xC2	Dual DDC, high BW	2	4	650	1300	5	3250	6500
0xC4	Dual DDC, high BW	4	2	1300	2500	2.5	3250	6250
0xE1	Dual DDC, mixed BW	1	8	330	650	10	3300	6500
0xE2	Dual DDC, mixed BW	2	4	650	1300	5	3250	6500
0xE4	Dual DDC, mixed BW	4	2	1300	2500	2.5	3250	6250
0xD1	Dual DDC, low BW	1	8	650	1300	5	3250	6500
0xD2	Dual DDC, low BW	2	4	1300	2500	2.5	3250	6250

[1] DDC means digital downconverter, BW means bandwidth, $f_S \times$ x means sample rate multiplied by an integer (where x is an integer: 2, 4, 8).

Table 17. JESD204B Logical Lane Mapping

Quick Configuration Value	Description	Lanes (L)	Logical Lane 0	Logical Lane 1	Logical Lane 2	Logical Lane 3	Logical Lane 4	Logical Lane 5	Logical Lane 6	Logical Lane 7
0x02	Generic	2	S[N], S[N + 1]	S[N + 2], S[N + 3]	Off	Off	Off	Off	Off	Off
0x04	Generic	4	S[N]	S[N + 1]	S[N + 2]	S[N + 3]	Off	Off	Off	Off
0x06	Generic (N' = 12)	6	S_{MSB}[N], S_{LSB}[N], S_{MSB}[N + 1], S_{LSB}[N + 1], S_{MSB}[N + 2], S_{LSB}[N + 2], S_{MSB}[N + 3], S_{LSB}[N + 3]						Off	Off
0x08	Generic	8	S_{MSB}[N]	S_{LSB}[N]	S_{MSB}[N + 1]	S_{LSB}[N + 1]	S_{MSB}[N + 2]	S_{LSB}[N + 2]	S_{MSB}[N + 3]	S_{LSB}[N + 3]
0x42	$f_S \times 8$	2	See Figure 104, $f_S \times 2$ mode application layer (transmit)							
0x44	$f_S \times 4$	4	See Figure 104, $f_S \times 2$ mode application layer (transmit)							
0x48	$f_S \times 2$	8	S_{MSB}[N], S_{LSB}[N], S_{MSB}[N + 1], S_{LSB}[N + 1], S_{MSB}[N + 2], S_{LSB}[N + 2], S_{MSB}[N + 3], S_{LSB}[N + 3], S_{MSB}[N + 4], S_{LSB}[N + 4]; see Figure 104, $f_S \times 2$ mode application layer (transmit)							
0x81	Single DDC, high BW	1	I_0[N], Q_0[N], I_0[N + 1], Q_0[N + 1]	Off	Off	Off	Off	Off	Off	Off
0x82	Single DDC, high BW	2	I_0[N], Q_0[N]	I_0[N+1], Q_0[N+1]	Off	Off	Off	Off	Off	Off
0x91	Single DDC, low BW	1	I_0[N], Q_0[N], I_0[N + 1], Q_0[N + 1]	Off	Off	Off	Off	Off	Off	Off
0xC1	Dual DDC, high BW	1	I_0[N], Q_0[N], I_1[N], Q_1[N]	Off	Off	Off	Off	Off	Off	Off
0xC2	Dual DDC, high BW	2	I_0[N], Q_0[N]	I_1[N], Q_1[N]	Off	Off	Off	Off	Off	Off
0xC4	Dual DDC, high BW	4	I_0[N]	Q_0[N]	I_1[N]	Q_1[N]	Off	Off	Off	Off
0xE1	Dual DDC, mixed BW	1	I_0[N], Q_0[N], I_1[N], Q_1[N]	Off	Off	Off	Off	Off	Off	Off
0xE2	Dual DDC, mixed BW	2	I_0[N], Q_0[N]	I_1[N], Q_1[N]	Off	Off	Off	Off	Off	Off

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Quick Configuration Value	Description	Lanes (L)	Logical Lane 0	Logical Lane 1	Logical Lane 2	Logical Lane 3	Logical Lane 4	Logical Lane 5	Logical Lane 6	Logical Lane 7
0xE4	Dual DDC, mixed BW	4	I_0[N]	Q_0[N]	I_1[N]	Q_1[N]	Off	Off	Off	Off
0xD1	Dual DDC, low BW	1	I_0[N], Q_0[N], I_1[N], Q_1[N]	Off	Off	Off	Off	Off	Off	Off
0xD2	Dual DDC, low BW	2	I_0[N], Q_0[N]	I_1[N], Q_1[N]	Off	Off	Off	Off	Off	Off

Table 18. Typical Current Consumption per ADC Mode (Unused Output Lanes are Powered Down)

Quick Configuration Value	Mode	Lanes (L)	Sample Rate (MSPS)	Typical Current Consumption (A)						
				I_{AVDD1}	I_{AVDD2}	I_{DRVDD1}	I_{DRVDD2}	I_{DVDD1}	I_{DVDD2}	Total Power (W)
0x02	Generic, two lane	2	650	0.7	0.3	0.2	0.0	0.1	0.0	2.1
0x04	Generic, four lane	4	1300	0.9	0.3	0.3	0.0	0.2	0.0	2.6
0x06	Generic, six lane	6	2600	1.2	0.4	0.4	0.0	0.4	0.0	3.4
0x08	Generic, eight lane	8	2600	1.2	0.4	0.5	0.0	0.4	0.0	3.9
0x42	$f_S \times 8$	2	813	0.7	0.4	0.2	0.0	0.2	0.0	2.3
0x44	$f_S \times 4$	4	1625	1.0	0.4	0.3	0.0	0.3	0.0	3.0
0x48	$f_S \times 2$	8	2600	1.2	0.4	0.5	0.0	0.4	0.0	3.8
0x81	Single DDC high BW, one lane	1	1300	0.9	0.4	0.1	0.0	0.3	0.0	2.7
0x82	Single DDC high BW, two lane	2	2600	1.2	0.4	0.2	0.0	0.6	0.0	3.6
0x91	Single DDC low BW, one lane	1	2600	1.2	0.4	0.1	0.0	0.6	0.0	3.5
0xC1	Dual DDC high BW, one lane	1	650	0.7	0.4	0.1	0.0	0.2	0.0	2.3
0xC2	Dual DDC high BW, two lane	2	1300	0.9	0.4	0.2	0.0	0.5	0.0	2.9
0xC4	Dual DDC high BW, four lane	4	2600	1.2	0.4	0.3	0.0	0.8	0.0	4.0
0xE1	Dual DDC mixed BW, one lane	1	650	0.7	0.4	0.1	0.0	0.2	0.0	2.3
0xE2	Dual DDC mixed BW, two lane	2	1300	0.9	0.4	0.2	0.0	0.5	0.0	2.9
0xE4	Dual DDC mixed BW, four lane	4	2600	1.2	0.4	0.3	0.0	0.8	0.0	4.0
0xD1	Dual DDC low BW, one lane	1	1300	0.9	0.4	0.1	0.0	0.4	0.0	2.8
0xD2	Dual DDC low BW, two lane	2	2600	1.2	0.4	0.2	0.1	0.8	0.0	4.0

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PHYSICAL LAYER OUTPUT

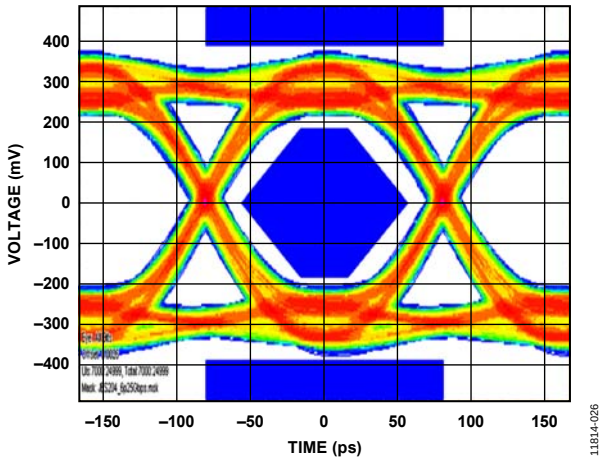

Figure 91. Recovered Data Eye of JESD204B Lane at 6.25 Gbps

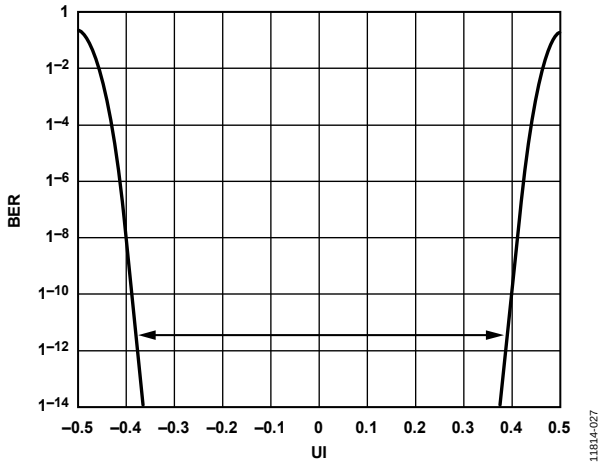

Figure 92. Bathtub Plot of JESD204B Output at 6.25 Gbps

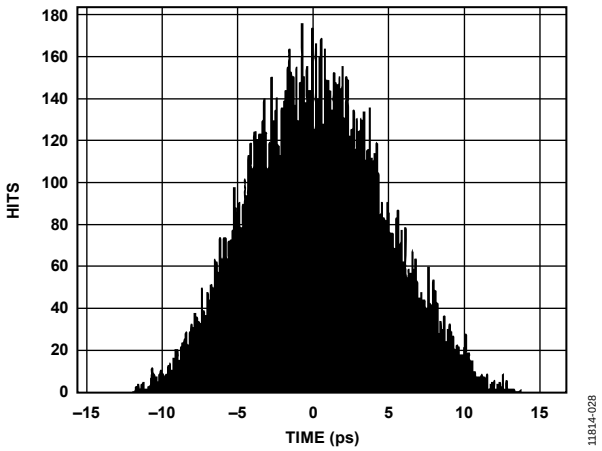

Figure 93. Time Interval Histogram Error of JESD204B Output at 6.25 Gbps

SCRAMBLER

The scrambler polynomial is $1 + x^{14} + x^{15}$. The scrambler enable bit is located in Register 0x06E[7].

- Setting Bit 7 to 0 disables the scrambler.
- Setting Bit 7 to 1 enables the scrambler.

TAIL BITS

The tail bit, PN generator, is located in Register 0x05F[6].

- Setting Bit 6 to 0 disables the tail bit generator.
- Setting Bit 6 to 1 enables the tail bit generator.

DDC MODES (SINGLE AND DUAL)

The AD9625 contains two separate DDCs that can digitally downconvert real ADC output data into I/Q decimated data at a reduced bandwidth. This feature is useful when the full bandwidth supplied by the 2.6 GSPS converter is not needed.

Figure 94 shows a simplified block diagram of the DDC blocks as they traverse through the AD9625. Because all JESD204B frames contain four samples (S = 4), the output from the DDCs must also output four samples. Table 19 shows the remapping of I/Q samples to converter samples for the JESD204B interface, specific to the AD9625.

When in mixed bandwidth mode, DDC 0 is always in high bandwidth mode and DDC 1 is always in low bandwidth mode. To match the data throughput of the high bandwidth mode, the low bandwidth samples are repeated twice in mixed bandwidth mode. Table 20 lists the four frames of data for both DDC 0 (high bandwidth mode) and DDC 1 (low bandwidth mode).

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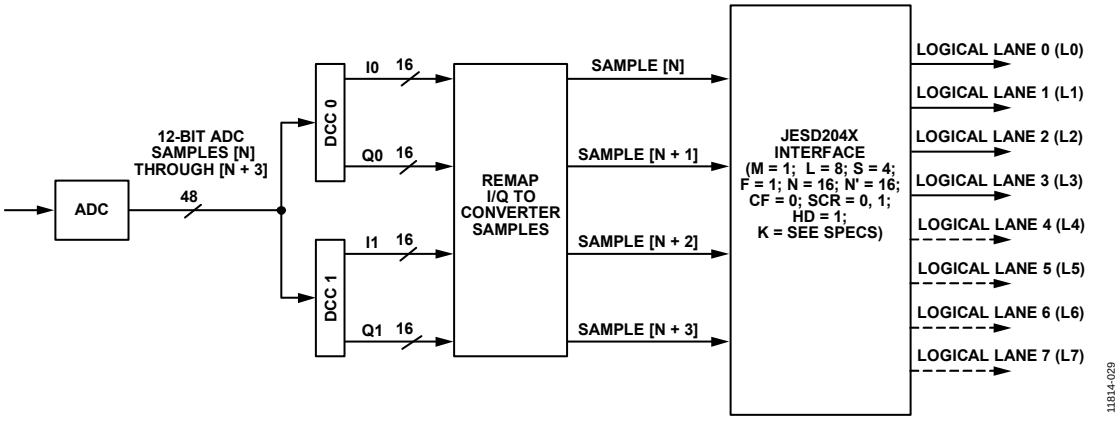

Figure 94. DDC Mapping

Table 19. DDC Remap I/Q to Converter Samples

Application Mode	Sample[N]	Sample[N + 1]	Sample[N + 2]	Sample[N + 3]
Single DDC	I_0[N]	Q_0[N]	I_0[N + 1]	Q_0[N + 1]
Dual DDCs	I_0[N]	Q_0[N]	I_1[N]	Q_1[N]

Table 20. DDC Mixed Bandwidth Mode

JESD204B Frame Number	Sample[N]	Sample[N + 1]	Sample[N + 2]	Sample[N + 3]
Frame 0	I_0[N]	Q_0[N]	I_1[N]	Q_1[N]
Frame 1	I_0[N + 1]	Q_0[N + 1]	I_1[N]	Q_1[N]
Frame 2	I_0[N + 2]	Q_0[N + 2]	I_1[N + 1]	Q_1[N + 1]
Frame 3	I_0[N + 3]	Q_0[N + 3]	I_1[N + 1]	Q_1[N + 1]

CHECKSUM

The JESD204B checksum value is sent with the configuration parameters during the initial lane alignment sequence. Disabling the checksum is primarily for debug purposes only.

8-BIT/10-BIT ENCODER CONTROL

The 8-bit/10-bit encoder must be controlled in the following manner:

- The bypass 8-bit/10-bit encoder is controlled by Register 0x60, Bit 2 (0 = 8-bit/10-bit enabled; 1 = 8-bit/10-bit bypassed).
- The invert 10-bit encoder is controlled by Register 0x060, Bit 1 (0 = normal; 1 = invert).
- The mirror 10-bit encoder is controlled by Register 0x060, Bit 0 (0 = normal; 1 = mirrored).

The inversion of the 10-bit values allows the user to swap the true/complement differential pins swapped on the boards. For details about Register 0x060, see the Memory Map Register section.

INITIAL LANE ALIGNMENT SEQUENCE (ILAS)

The AD9625 must support three different ILAS modes that are controlled using Bits[3:2] in Register 0x05F as follows:

- 00: disabled
- 01: enabled
- 10: reserved
- 11: always on test mode

When enabled, the device must also support the capability to repeat the ILAS using Bits[7:0] in Register 0x062 to determine the number of times ILAS is repeated (0 = repeat 0 times, ILAS runs one time only, 1 = repeat one time, ILAS runs twice, and so forth). Because the number of frames per multiframe is determined by the value of K, the total number of frames transmitted during the initial lane alignment sequence is

$$4 \times (K + 1) \times (ILAS_COUNT + 1)$$

where the value of K is defined in Register 0x070, Bits[4:0]. Note that only values divisible by four can be used.

For details about Register 0x05F and Register 0x062, see the Memory Map Register section.

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LANE SYNCHRONIZATION

Lane synchronization is defined by Register 0x05F, Bit 4 (0 = disabled, 1 = enabled). For more information, see the Memory Map Register section.

Multichip Synchronization Using SYSREF± Timestamp

The SYSREF± pin in the AD9625 can also be used as a timestamp of data as it passes through the ADC and out the JESD204B interface. This can be accomplished in two ways:

- Replace the least significant converter bit with the synchronous low to high captured SYSREF± signal. If the AD9625 were configured as a 12-bit converter, this would effectively reduce it to a 11-bit converter. This is accomplished by setting Register 0x03A[7] = 1 in the register map.
- Use the extra output JESD204B control bits to insert the synchronous low to high captured SYSREF± signal. These extra control bits are only available while in the JESD204B generic two, four, and eight lane modes. The generic six lane mode does not support control bits as both N and N' = 12.

Six Lane Output Mode

The full data output bandwidth of the eight lane mode can alternately by output using a six lane mode. This is achieved by using an N' = 12 in the six lane mode vs. N' = 16 in the eight lane mode for N = 12 ADC data.

The benefit of using the six lane mode is that only six lanes of output data are needed instead of eight lanes and two output data lanes can be powered down. A drawback of the six lane mode is that because there is full efficiency of the link for N = N' = 12, there is no spare bandwidth available for control bits. Therefore, control bit timestamping using SYSREF± cannot be used in the six lane mode. The LSB of the 12-bit ADC data can be substituted to output the SYSREF± timestamp.

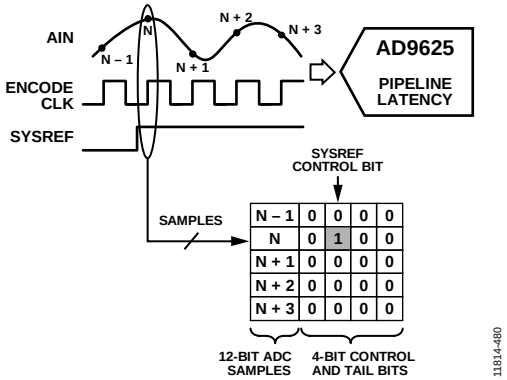

Figure 95. A SYSREF± Control Bit Can Be Used to Mark the Same Analog Sample that is Coincident with a Sampled SYSREF± Edge by CLK±

ADC Output Control Bits on JESD204B Samples

When N' = 16 and the ADC resolution is 12, there are four spare bits available per sample. Two of these spare bits can be used as control bits, depending on the configuration options. The control bits are set in Register 0x072, Bits[7:6]. (CS means control bits per sample.)

- 00: no control bits sent per sample (CS = 0).
- 01: one control bit sent per sample, overrange bit enabled, (CS = 1).
- 10: two control bits sent per sample, overrange and time stamped SYSREF± control bit (marks the sample of a rising edge seen on the SYSREF± pin), (CS = 2). Use of the SYSREF± control bit (CS = 2) time stamps a particular analog sample that is seen coincident with a rising signal on the SYSREF± pins. See the Register 0x08A description to disable the LMFC JESD204B alignment for timestamping.

SYSREF± Setup and Hold IRQ

The differential SYSREF± inputs to AD9625 are critical for JESD204B deterministic latency and sample timestamping. At a 2.5 GSPS sample rate, the clock period is only 400 ps in duration from which to accurately latch a SYSREF± edge to meet setup and hold time to the sample clock. Therefore, it is important to know the location of the SYSREF± edge relative to the sampling edge of the encode clock. To help identify the SYSREF± edge location within the clock period, the AD9625 provides a setup and hold time edge detector circuit to provide feedback to the system for SYSREF± timing skew and other alignment procedures. This is a fine timing detector (<1 clock cycle) and does not provide useful information if coarse timing (>1 clock cycle) skew adjustment is needed on SYSREF±.

The AD9625 provides an interrupt request (IRQ) bit that identifies either a setup or a hold time error for the SYSREF± edge relative to the sampling clock. The error indicates that the SYSREF± edge is present within the designated time window. There is a default detector window for both the actual setup and hold time, with each being nominally 35 ps in time. This error flag can be identified internal to the AD9625 IRQ register or the status can be sent externally via the IRQ pin, provided that the appropriate interrupts are masked or enabled as desired.

A SYSREF± edge located in either the setup or hold violation window causes ambiguity as to whether the event latchs on CLK±[N] or CLK±[N + 1]. As a best practice, the SYSREF± edge must be earlier than both the setup and hold violation windows so that a deterministic clock can be used to latch SYSREF±.

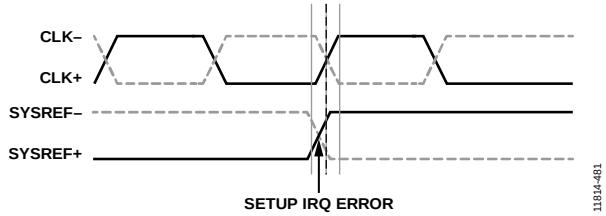

Figure 96. SYSREF± Edge Falls Within the Actual Setup Time Window and Triggers an IRQ Error

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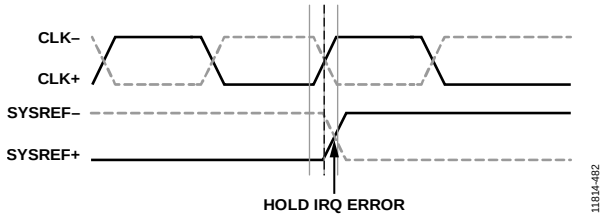

Figure 97. SYSREF± Edge Falls Within the Actual Hold Time Window and Triggers an IRQ Error

IRQ Guardband Delays (SYSREF± Setup and Hold)

Additional guardband delays can be added to each of the default setup and hold time windows. This yields more information to the system about the placement of the SYSREF± edge within the clock period and help identify the proximity of the SYSREF± edge to the actual setup and hold time windows. With a default setting of 00b for both setup and hold, each has seven additional settings to increase the guardband timing feedback information.

There are 3 bits that define the SYSREF± setup time guardband located in Register 0x13C[7:5]. There are 3 bits that define the SYSREF± hold time guardband located in Register 0x13B[7:5]. A setting of 000b for either is the default of no additional timing guardband, with just the actual setup and hold time window used as the IRQ.

The IRQ flag for the SYSREF± setup window is in Register 0x100[2], while the IRQ flag for the SYSREF± hold window is in Register 0x100[3]. The IRQ flag mask for the SYSREF± setup window is in Register 0x101[2], while the IRQ flag mask for the SYSREF± hold window is in Register 0x101[3].

After each IRQ alert, the status needs to be cleared, as it does not automatically clear itself, even if the alert conditions are no longer valid. For either the SYSREF± setup or hold IRQ alert, the status is cleared using Register 0x03A[6]. Setting Register 0x03A[6] = 1 clears and hold the IRQ in a reset value of 0. To allow IRQ flags pertaining to SYSREF± again, set Register 0x03A[6] = 0.

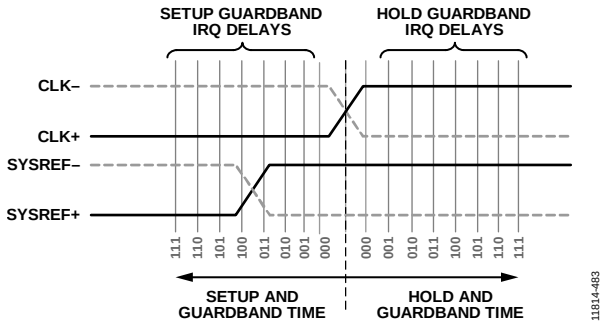

Figure 98. SYSREF± Edge Falls Within the Guardbanded Setup Time Window and Triggers an IRQ Error

In Figure 98, the SYSREF± edge meets the default setup and hold time of the clock, but would trigger an IRQ event only if certain setup time guardband delays were used. For this figure, all of the setup guardband delays that would place the SYSREF± crossing edge between it and the dotted black line would incur an IRQ event equal to 1. All other settings would be 0. Because there is no edge in the hold guardband delays, those would all be 0 if they were set.

Table 21. IRQ Outcomes for All Setup or Hold Guardband Settings for the Case in Figure 98

Setting/IRQ	Setup	Hold
000	0	0
001	0	0
010	0	0
011	0	0
100	1	0
101	1	0
110	1	0
111	1	0

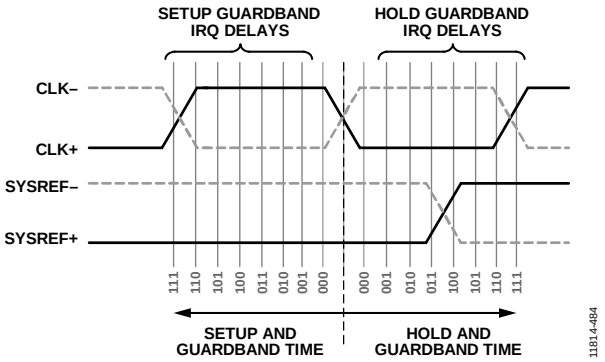

Figure 99. SYSREF± Edge Falls Within the Guardbanded Hold Time Window and Triggers an IRQ Error

In Figure 99, the SYSREF± edge misses the default setup and hold time of the clock, but would trigger an IRQ event only if certain hold time guardband delays were used. For this figure, all of the hold guardband delays that would place the SYSREF± crossing edge between it and the dotted black line would incur an IRQ event equal to 1. All other settings would be 0. Because there is no edge in the setup guardband delays, those would all be 0 if they were set.

Table 22. IRQ Outcomes for All Setup or Hold Guardband Settings Using the Case in Figure 99

Setting/IRQ	Setup	Hold
000	0	0
001	0	0
010	0	0
011	0	0
100	0	1
101	0	1
110	0	1
111	0	1

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In the case where the encode clock used for the AD9625 is sufficiently fast (>1.75 GSPS), the guardband delays for the earliest setup and latest hold condition starts to overlap in time due to the fast clock period. This case occurs when the encode clock period is smaller than 16× the nominal delay guardband window of 35 ps or ($1/f_S < 16 \times 35$ ps). The earliest setup guardband delays from clock N can overlap with the latest guardband delays from CLK±[N + 1]. When this is the case, a SYSREF± edge located in one of these overlapped guardband delays triggers an IRQ event for both the setup and hold detection. While it is possible to make use of this information, it is suggested to limit the number of valid settings to no more than 5 (100b) and below when sampling above 1.75 GSPS to avoid this situation.

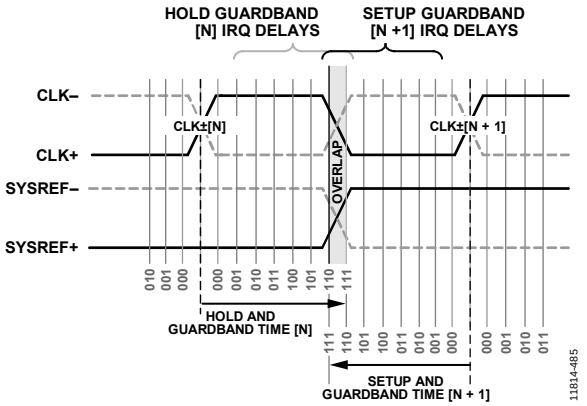

Figure 100. SYSREF± Edge Falls Within Both the Latest Hold Time Guardbanded of CLK±[N] and the Earliest Setup Time Guardband of CLK±[N + 1] and Triggers an IRQ Error

Table 23. IRQ Outcomes for All Setup or Hold Guardband Settings Using the Case in Figure 100

Setting/IRQ	Setup	Hold
000	0	0
001	0	0
010	0	0
011	0	0
100	0	0
101	0	0
110	0	0
111	1	1

As a secondary use, the SYSREF± edge detector can also alert the system about phase shift drift between SYSREF± and CLK due to temperature or supply changes. For example, a conservative guardband setting could be used, such that an IRQ status of 0 would be seen in ideal conditions. If timing drifts were significant enough to trigger the IRQ, the system would take action to adjust the skew of the SYSREF± to CLK accordingly to reestablish an IRQ of 0.

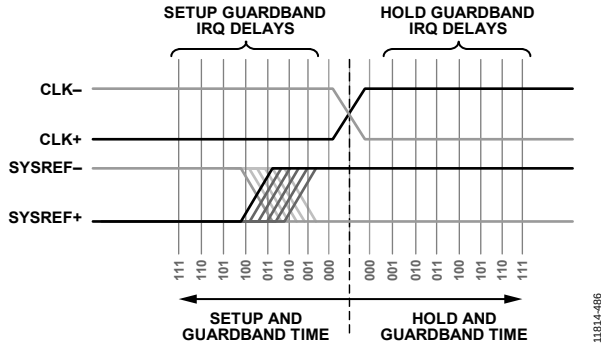

Figure 101. SYSREF± Edge Changes Phase Relative to the Encode Clock, Which can be Detected When the Edge Crosses Through the Guardband Setup Time

Table 24. IRQ Outcomes for all Setup or Hold Guardband Settings Using the Case in Figure 101

Setting/IRQ	Setup	Hold	Setting/IRQ	Setup	Hold
000	0	0	000	0	0
001	0	0	001	0	0
010	0	0	010	1	0
011	0	0	011	1	0
100	1	0	100	1	0
101	1	0	101	1	0
110	1	0	110	1	0
111	1	0	111	1	0

Using Rising/Falling Edges of the CLK to Latch SYSREF±

The SYSREF± signal can be latched on either the rising or falling edge of the encode clock, based on the value of register 0x03A[3] = 0 (latch on rising edge) or 0x03A[3] = 1 (latch on falling edge). This does not impact the analog input, which is always sampled on the rising edge of the encode clock. For sampling SYSREF±, the falling edge encode capture of CLK±[N] precedes the rising edge encode capture of CLK±[N], both corresponding to the same analog sample.

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For synchronous sampling of multiple converters using SYSREF±, it may be possible to have a scenario shown in Figure 102. This case uses a SYSREF± capture with the falling edge of the encode clock first to test the SYSREF± position using the edge detection window. The three ADC's each receive a SYSREF± input that may be skewed in time due to board trace length or source variance. For ADC[0] SYSREF± meets setup/hold to CLK±[N], ADC[1] misses setup/hold to CLK±[N], and ADC[2] is indeterminate as it falls within the setup/hold window and may be latched by either CLK±[N] or CLK±[N + 1].

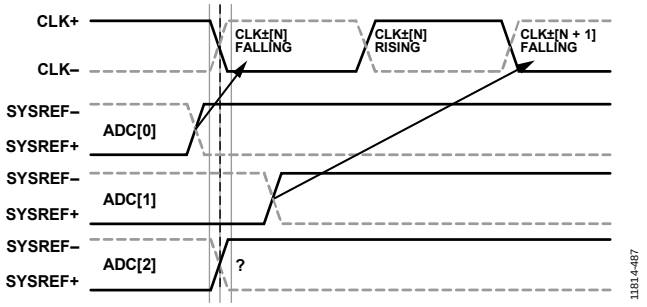

Figure 102. SYSREF± Case From Three ADCs Having Various Phase Delays Relative to the Falling Edge of the Encode Clock and is Latched on Different Sample Clock Edges CLK±[N] or CLK±[N + 1]

As a solution to this case, the SYSREF± capture edge can be changed from falling to rising, which is still captured to the analog sample from CLK±[N]. When this is done, all three ADC's now meet the setup/hold time for the rising edge capture of CLK±[N].

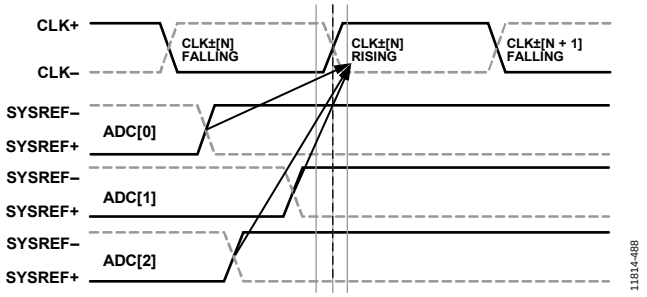

Figure 103. Changing the Latching Edge to Rising for All Three ADCs, SYSREF± Can Now be Aligned to CLK±[N]

Test Modes

Bits[5:4] in Register 0x061 control the JESD204B interface test injection points.

- 00: 16-bit test generation data injected at the sample input to the link.
- 01: 10-bit test generation data injected at the output of the 8-bit/10-bit encoder (at the input to PHY).
- 10: 8-bit test generation data injected at the input of the scrambler.
- 11: reserved.

Bits[3:0] in Register 0x061 determine the type of test patterns that are injected, as follows:

- 0000: normal operation (test mode disabled).
- 0001: alternating checkerboard.
- 0010: 1/0 word toggle.
- 0011: PN sequence: long ($x^{23} + x^{18} + 1$).
- 0101: continuous/repeat user test mode; most significant bits from 16-bit user pattern (1, 2, 3, 4) are placed on the output for one clock cycle and then repeated. (Output user pattern: 1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4, ….)
- 0110: single user test mode; most significant bits from the 16-bit user pattern (1, 2, 3, 4) placed on the output for one clock cycle and then outputs all zeros. (Output user pattern: 1, 2, 3, 4, then output all zeros.)
- 0111: Ramp output (dependent on test injection point and number of bits, N).
- 1000: modified RPAT test sequence.
- 1001: unused.
- 1010: JSPAT test sequence.
- 1011: JTSPAT test sequence.
- 1100 to 1111: unused.

JESD204B APPLICATION LAYERS

The AD9625 supports the following application layer modes via Register 0x063[3:0]:

- 0100: $f_S \times x$ mode which supports line rates at integer multiples of the sample rates
- 1000: single DDC mode, high bandwidth mode (only DDC 0 used)
- 1001: single DDC mode, low bandwidth mode (only DDC 0 used)
- 1010 to 1011: unused
- 1100: dual DDC mode, high bandwidth mode (both DDC 0 and DDC 1 used)
- 1101: dual DDC mode, low bandwidth mode (both DDC 0 and DDC 1 used)
- 1110: dual DDC mode, mixed bandwidth mode (DDC 0 high bandwidth mode, DDC 1 low bandwidth mode, samples repeated)

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$f_S \times 2$, $f_S \times 4$, $f_S \times 8$ Modes

The JESD204B low multiplier mode application layer adds a rate conversion on top of a JESD204B transmitter/receiver with the following configuration parameters: M = 1; L = 8; S = 4; F = 1; N = 16; N' = 16; CS = 0; CF = 0; SCR = 0, 1; HD = 1; K = reference JESD204B specification.

In this mode, there are five actual samples per frame and scrambling can be optionally enabled in the JESD204B interface. The transmit portion of the low multiplier mode JESD204B application layer is shown in Figure 104.

The first step in this application layer is where 12-bit ADC samples are divided into six bytes.

To allow the line rate of the JESD204B interface to map directly into an integer of the converter sample rate, a four to five rate conversion takes place to group the 12-bit ADC samples into blocks of five samples. During this rate conversion, for every five 12-bit ADC sample, an extra user defined, 4-bit nibble is appended to create a 64-bit frame. Next, the 64-bit low multiplier frame maps into the four 16-bit JESD204B samples. The most significant 16-bits of the 64-bit low multiplier frame map to the oldest 16-bit JESD204B sample and the least significant 16-bits of the 64-bit low multiplier frame map to the most recent 16-bit JESD204B sample.

The receive portion of the $f_S \times 2$ JESD204B application layer is shown in Figure 105.

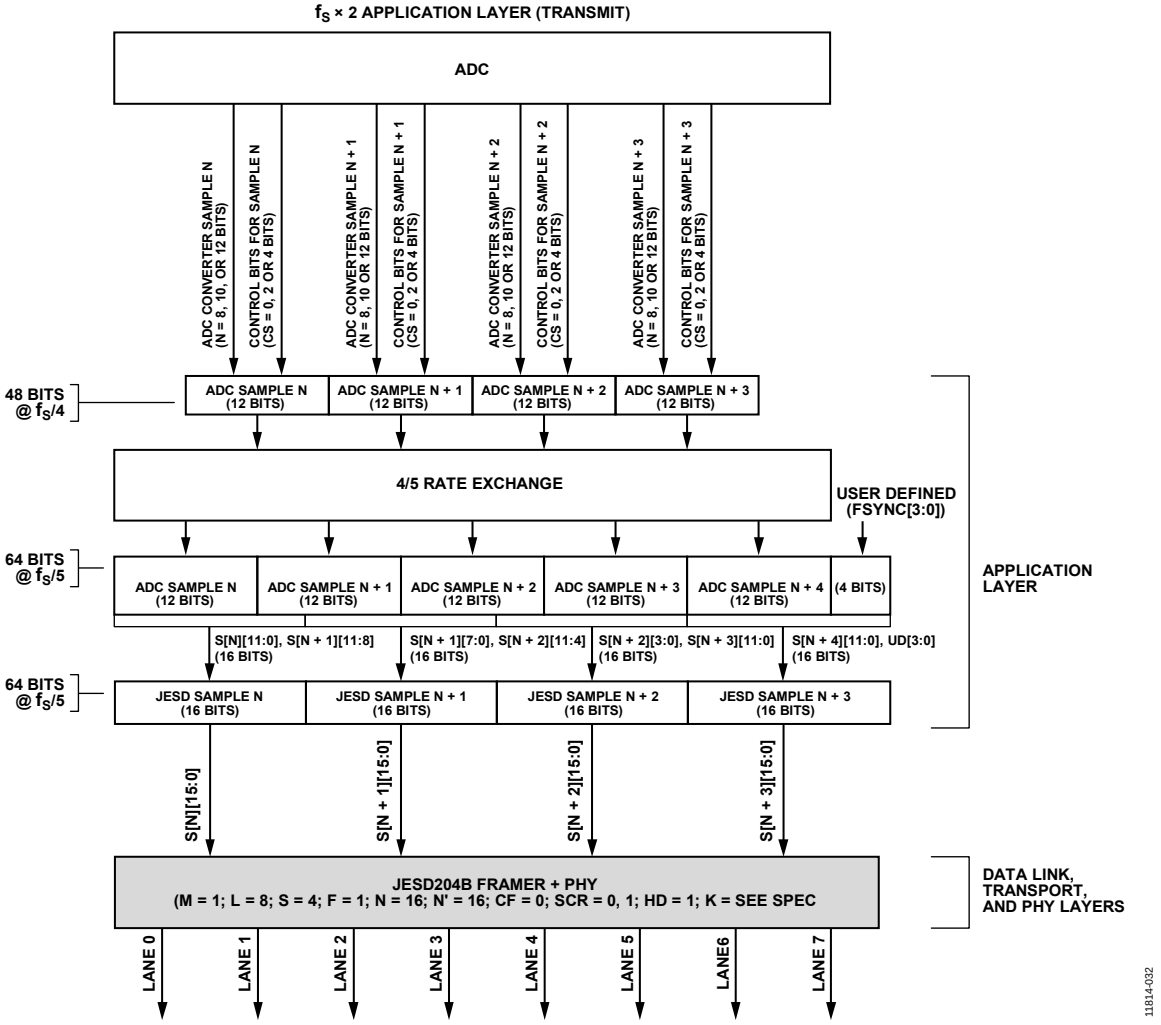

Figure 104. $f_S \times 2$ Mode Application Layer (Transmit)

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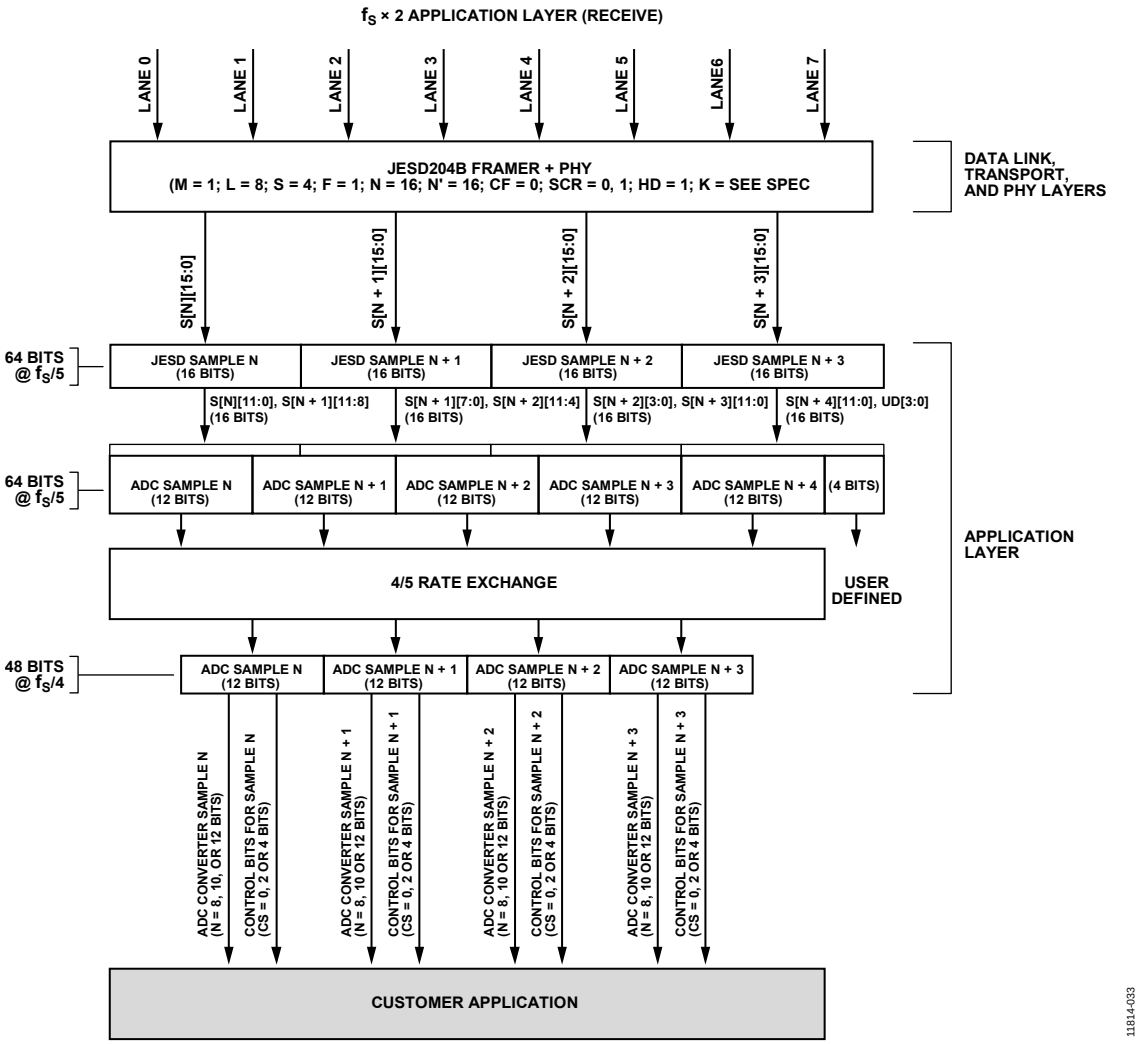

Figure 105. $f_S \times 2$ Application Layer (Receive)

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FRAME ALIGNMENT CHARACTER INSERTION

Frame alignment character insertion (FACI) is defined in the register map (see the Memory Map Register section). Disable FACI only when it is used as a test feature.

The FACI disable bit is located in Register 0x05F, Bit 1. Use the following settings:

- Setting Bit 1 to 0 = FACI enabled
- Setting Bit 1 to 1 = FACI disabled

THERMAL CONSIDERATIONS

Because of the high power nature of the device, it is critical to provide airflow and/or install a heat sink when operating at a high temperature. This ensures that the maximum case temperature does not exceed 85°C.

POWER SUPPLY CONSIDERATIONS

The AD9625 must be powered by the following two supplies: AVDD1 = DVDD1 = DRVDD1 = 1.3 V, AVDD2 = DVDD2 = DRVDD2 = 2.5 V. An optional DVDDIO and SPI_DVDDIO may be required at 2.5 V.

For applications requiring an optimal high power efficiency and low noise performance, it is recommended that ADP2386 switching regulator is used to convert the 12 V input rail into two intermediate rails (2.1 V and 3.6 V). These intermediate rails are then postregulated by very low noise, low dropout (LDO) regulators (ADP1740, ADP7104, and ADP125). Figure 106 shows the recommended method.

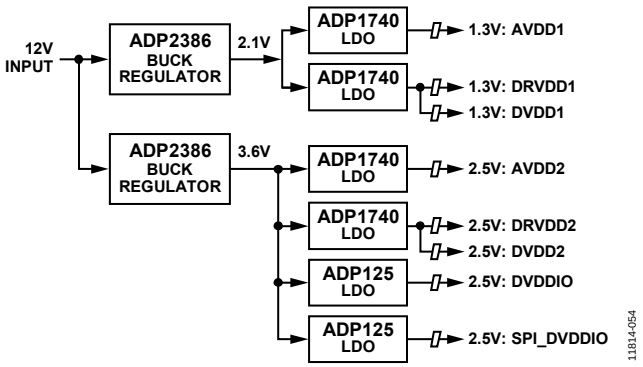

Figure 106. Power Supply Recommendation

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SERIAL PORT INTERFACE (SPI)

The AD9625 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 25). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 25. Serial Port Interface Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input, which is used to synchronize serial interface, reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip Select Bar. An active low control that gates the read and write cycles.

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing.

Other modes involving the CSB pin are available. The CSB pin can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB pin can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a read operation, performing a read causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register.

HARDWARE INTERFACE

The pins described in Table 25 comprise the physical interface between the user programming device and the serial port of the AD9625. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during read.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9625 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

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MEMORY MAP

READING THE MEMORY MAP REGISTER

Each row in the memory map register contains eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x000 to Address 0x002); the transfer register (Address 0x0FF); and the ADC functions registers, including setup, control, and test (Address 0x008 to Address 0x13A).

The memory map register tables provide the default hexadecimal value for each hexadecimal address that is listed.

The column with the heading, Bit 7 (MSB), is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Open and Reserved Locations

All address and bit locations are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when a portion of an address location is open. If the entire address location is open, this address location should not be written.

Default Values

After the AD9625 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register tables.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Register addresses for the AD9625 are shadowed. Register writes do not affect device operation until a transfer command is issued by writing 0x01 to Address 0x0FF, thereby setting the transfer bit. This allows the registers to update internally and simultaneously when the transfer bit is set. The internal update occurs when the transfer bit is set, and then the bit automatically clears.

MEMORY MAP REGISTERS

Address and bit locations that are not included in Table 26 through Table 116 are not currently supported for this device.

Table 26. SPI Configuration Register, Address 0x000 (Default = 0x18)

Bit No.	Access	Bit Description
7		Unused.
6	RW	SPI least significant bit (LSB) first. 1: LSB shifted first for all SPI operations. For multibyte SPI operations, the addressing increments automatically. 0: most significant bit (MSB) shifted first for all SPI operations. For multibyte SPI operations, the addressing decrements automatically.
5	RW	Self clearing soft reset. 1: reset the SPI registers (self clearing). 0: do nothing.
4	R	13-bit addressing enabled.
3	R	13-bit addressing enabled.
2	RW	Self clearing soft reset. 1: reset the SPI registers(self clearing). 0: do nothing.
1	RW	SPI LSB first. 1: LSB shifted first for all SPI operations. For multibyte SPI operations, the addressing increments automatically. 0: MSB shifted first for all SPI operations. For multibyte SPI operations, the addressing decrements automatically.
0	Unused	Unused.

Table 27. Chip ID Register, Address 0x001 (Default = 0x41)

Bit No.	Access	Bit Description
[7:0]	R	Chip ID.

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Table 28. Chip Grade Register, Address 0x002 (Default = 0x14)

Bit No.	Access	Bit Description
[7:6]		Unused.
[5:4]	R	Chip ID/speed grade. 11: 2.6 GSPS. 10: 2.5 GSPS. 01: 2.0 GSPS.
[3:0]		Unused.

Table 29. Power Control Mode Register, Address 0x008 (Default = 0x80)

Bit No.	Access	Bit Description
7		Reserved.
6		Reserved.
5		Reserved.
[4:2]		Reserved.
[1:0]	RW	Chip power modes. 00: normal mode (power-up). 01: Power-down. 10: standby mode; digital datapath clocks disabled, JESD204B interface enabled, outputs enabled. 11: digital datapath reset mode; digital data path clocks enabled, digital data path held in reset, JESD204B interface held in reset, outputs enabled.

Table 30. PLL Status Register, Address 0x00A (Default = 0x00)

Bit No.	Access	Bit Description
7	RO	PLL locked status bit. 0: PLL is unlocked. 1: PLL is locked.
[6:0]		Reserved.

Table 31. ADC Test Control Register, Address 0x00D (Default = 0x00)

Bit No.	Access	Bit Description
7	RW	ADC datapath user test mode control. Note that these bits are only used when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000); otherwise, they are ignored. 0: continuous/repeat pattern mode. Place each user pattern (1, 2, 3, 4) on the output for one clock cycle and then repeat. (Output user pattern: 1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4, …) 1: single pattern mode. Place each user pattern (1, 2, 3, 4) on the output for one clock cycle and then output all zeros. (Output user pattern: 1, 2, 3, 4, then output all zeros.)
6		Unused.
5	RW	ADC long psuedo random number test generator reset. 0: long PN enabled. 1: long PN held in reset.
4	RW	Unused.
[3:0]	RW	ADC data output test generation mode. 0000: off, normal operation. 0001: midscale short. 0010: positive full scale. 0011: negative full scale. 0100: alternating checkerboard. 0101: PN sequence, long. 0110: unused. 0111: one-/zero-word toggle. 1000: user test mode. Used with Register 0x00D[7] and user pattern (1, 2, 3, 4) registers. 1001 to 1110: unused. 1111: ramp output.

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Table 32. Data Path Customer Offset Register, Address 0x010 (Default = 0x00)

Bit No.	Access	Bit Description
[7:6]		Unused.
[5:0]	RW	Digital datapath offset. Twos complement offset adjustment aligned with least converter resolution. 011111: +31. 011110: +30. … 000001: +1. 000000: 0. 111111: −1. … 100001: −31. 100000: −32.

Table 33. Output Mode Register, Address 0x014 (Default = 0x01)

Bit No.	Access	Bit Description
[7:5]		Unused.
4	RW	Chip output disable. Bit 4 enables and disables the digital outputs from the ADC. 0: enable. 1: disable.
3		Unused.
2	RW	Digital ADC sample invert. 0: ADC sample data is not inverted. 1: ADC sample data is inverted.
[1:0]	RW	Digital ADC data format select (DFS). Note that the use of the muxed SDIO pin to control Register 0x014[1:0] is not supported on the AD9625. 00: offset binary. 01: twos complement (default). 10: reserved. 11: reserved.

Table 34. Serializer Output Adjust, Register, Address 0x015 (Default = 0x54)

Bit No.	Access	Bit Description
7	RW	Serializer output polarity selection. 0: normal, not inverted. 1: output driver polarity inverted.
[6:5]	RW	Serializer output emphasis amplitude control. 00: 0 mV de-emphasis differential peak to peak. 01: 160 mV de-emphasis differential peak to peak. 10: 80 mV de-emphasis differential peak to peak. 11: 40 mV de-emphasis differential peak to peak.
[4:0]	RW	Reserved.

Table 35. User Test Pattern 1 LSB Register, Address 0x019 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	User Test Pattern 1 least significant byte. Note that these bits are used only when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000), or when Register 0x061, Bits[3:0] is in the scrambler or 10-bit test modes (Register 0x061[3:0] = 0100 to 0111). Otherwise, these bits are ignored.

Table 36. User Test Pattern 1 MSB Register, Address 0x01A (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	User Test Pattern 1 most significant byte. Note that these bits are used only when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000). Otherwise, these bits are ignored.

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Table 37. User Test Pattern 2 LSB Register, Address 0x01B (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	User Test Pattern 2 least significant byte. Note that these bits are used only when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000). Otherwise, these bits are ignored.

Table 38. User Test Pattern 2 MSB Register, Address 0x01C (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	User Test Pattern 2 most significant byte. Note that these bits are used only when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000). Otherwise, these bits are ignored.

Table 39. User Test Pattern 3 LSB Register, Address 0x01D (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	User Test Pattern 3 least significant byte. Note that these bits are used only when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000). Otherwise, these bits are ignored.

Table 40. User Test Pattern 3 MSB Register, Address 0x01E (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	User Test Pattern 3 most significant byte. Note that these bits are used only when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000). Otherwise, these bits are ignored.

Table 41. User Test Pattern 4 LSB Register, Address 0x01F (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	User Test Pattern 4 least significant byte. Note that these bits are used only when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000). Otherwise, these bits are ignored.

Table 42. User Test Pattern 4 MSB Register, Address 0x020 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	User Test Pattern 4 most significant byte. Note that these bits are used only when Register 0x00D, Bits[3:0] is in user input mode (Register 0x00D[3:0] = 1000). Otherwise, these bits are ignored.

Table 43. Synthesizer PLL Control Register, Address 0x021 (Default = 0x00)

Bit No.	Access	Bit Description
[7:5]		Unused.
4	RW	1: force power-down of VCO LDO.
3	RW	Reserved for future use.
[2:0]		Unused.

Table 44. ADC Analog Input Control Register, Address 0x02C (Default = 0x00)

Bit No.	Access	Bit Description
[7:3]		Unused.
2	RW	Set function on VMON pin. 0: unused. 1: allows external reference on VMON pin.
[1:0]		Unused.

Table 45. SYSREF± Control Register, Address 0x03A (Default = 0x00)

Bit No.	Access	Bit Description
7	RW	SYSREF± status bit replaces the LSB from the converter. 0: normal mode. 1: SYSREF± status bit replaces the LSB.
6	RW	SYSREF± status bit flag reset. To use the flags, Register 0x03A, Bit 1 must be set to high. 0: normal flag operation. 1: SYSREF± status bit flags held in reset.
5		Unused.

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Bit No.	Access	Bit Description
4	RW	SYSREF± transition selection. 0: SYSREF± is valid on low to high transitions using selected CLK edge. 1: SYSREF± is valid on high to low transitions using selected CLK edge.
3	RW	SYSREF± capture edge selection. 0: captured on rising edge of CLK input. 1: captured on falling edge of CLK input.
2	RW	SYSREF± next mode. 0: continuous mode. 1: next SYSREF± mode: uses the next valid edge only of the SYSREF± pin. Subsequent edges of the SYSREF± pin are ignored. When the next system reference is found, Bit 1 of Register 0x03A clears.
1	RW	SYSREF± pins enable. 0: SYSREF± disabled. 1: SYSREF± enabled. When Register 0x03A, Bit 2 = 1, only the next valid edge of the SYSREF± pins is used. Subsequent edges of the SYSREF± pin are ignored.
0		Unused.

Table 46. Fast Detect Control Register, Address 0x045 (Default = 0x00)

Bit No.	Access	Bit Description
[7:4]		Unused.
3	RW	Force the fast detect output pin. 0: normal operation of fast detect pin. 1: force a value on the fast detect pin (see Bit 2 in this table, Table 46).
2	RW	The fast detect output pin is set to the value in this bit (Register 0x045[2]) when the output is forced.
1		Unused.
0	RW	Enable fast detect on the corrected ADC data. 0: fine fast detect disabled. 1: fine fast detect enabled.

Table 47. Fast Detect Upper Threshold Register, Address 0x047 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	These bits are the LSBs of the fast detect upper threshold. These eight LSBs of the programmable 12-bit upper threshold are compared to the fine ADC magnitude.

Table 48. Fast Detect Upper Threshold Register, Address 0x048 (Default = 0x00)

Bit No.	Access	Bit Description
[7:4]		Unused.
[3:0]	RW	These bits are the MSBs of the fast detect upper threshold. These four MSBs of the programmable 12-bit upper threshold are compared to the fine ADC magnitude.

Table 49. Fast Detect Lower Threshold Register, Address 0x049 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	These bits are the LSBs of the fast detect lower threshold. These eight LSBs of the programmable 12-bit lower threshold are compared to the fine ADC magnitude.

Table 50. Fast Detect Lower Threshold Register, Address 0x04A (Default = 0x00)

Bit No.	Access	Bit Description
[7:4]		Unused.
[3:0]	RW	MSBs of the fast detect lower threshold. These four MSBs of the programmable 12-bit lower threshold are compared to the fine ADC magnitude.

Table 51. Fast Detect Dwell Time Counter Threshold Register, Address 0x04B (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	These bits are the LSBs of the fast detect dwell time counter target. This is the value for a 16-bit counter that determines the length of time that the ADC data must remain below the lower threshold before the FD pin reset to 0.

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Table 52. Fast Detect Dwell Time Counter Threshold Register, Address 0x04C (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	These bits are the MSBs of the fast detect dwell time counter target. This is the value for a 16-bit counter that determines the length of time that the ADC data must remain below the lower threshold before the FD pin resets to 0. Note that the fast detect (FD) pin deasserts after the ADC codes stay below the lower target for the number of samples indicated by the value in Register 0x04C[7:0].

Table 53. JESD204B Quick Configuration Register, Address 0x05E (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	JESD204B serial quick configuration (self clearing). This register is self clearing and does not control anything in the AD9625 directly; it only changes the value of the other JESD240B registers that control the chip. Because this register is self clearing, it always returns to 000 after each write. To use the quick configuration feature, write to this register first, then, if there are any changes that need to be made to any of the following settings, write to the other JESD204B registers. 0x00: configuration determined by other registers. Because the register is self clearing, it always returns to this value after each write. 0x01: reserved. 0x02: Generic Two Lane Configuration Register 0x063[3:0] = 0x0; Register 0x06E[4:0] = 0x1; Register 0x072[4:0] = 0xB; Register 0x073[4:0] = 0xF. 0x04: Generic Four Lane Configuration Register 0x063[3:0] = 0x0; Register 0x06E[4:0] = 0x3; Register 0x072[4:0] = 0xB; Register 0x073[4:0] = 0xF. 0x06: Generic Six Lane Configuration Register 0x063[3:0] = 0x0; Register 0x06E[4:0] = 0x5; Register 0x072[4:0] = 0xB; Register 0x073[4:0] = 0xB. 0x08: Generic Eight Lane Configuration Register 0x063[3:0] = 0x0; Register 0x06E[4:0] = 0x7; Register 0x072[4:0] = 0xB; Register 0x073[4:0] = 0xF. 0x42: reserved. 0x44: reserved. 0x48: $f_S \times 2$ mode, eight lanes. Register 0x063[3:0] = 0x4; Register 0x06E[4:0] = 0x7; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0x81: 1 DDC (high BW), one lane. Register 0x063[3:0] = 0x8; Register 0x06E[4:0] = 0x0; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0x82: 1 DDC (high BW), two lanes. Register 0x063[3:0] = 0x8; Register 0x06E[4:0] = 0x1; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0x91: 1 DDC (low BW), one lane. Register 0x063[3:0] = 0x9; Register 0x06E[4:0] = 0x0; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0xC1: 2 DDCs (high BW), one lane. Register 0x063[3:0] = 0xC; Register 0x06E[4:0] = 0x0; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0xC2: 2 DDCs (high BW), two lanes. Register 0x063[3:0] = 0xC; Register 0x06E[4:0] = 0x1; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0xC4: 2 DDCs (high BW), four lanes. Register 0x063[3:0] = 0xC; Register 0x06E[4:0] = 0x3; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0xD1: 2 DDCs (low BW), one lane. Register 0x063[3:0] = 0xD; Register 0x06E[4:0] = 0x0; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0xD2: 2 DDCs (low BW), two lanes. Register 0x063[3:0] = 0xD; Register 0x06E[4:0] = 0x1; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0xE1: 2 DDCs (mixed BW), one lane. Register 0x063[3:0] = 0xE; Register 0x06E[4:0] = 0x0; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0xE2: 2 DDCs (mixed BW), two lanes. Register 0x063[3:0] = 0xE; Register 0x06E[4:0] = 0x1; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. 0xE4: 2 DDCs (mixed BW), four lanes. Register 0x063[3:0] = 0xE; Register 0x06E[4:0] = 0x3; Register 0x072[4:0] = 0xF; Register 0x073[4:0] = 0xF. All other values have no effect.

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Table 54. JESD204B Link Control Register 1, Address 0x05F (Default = 0x14)

Bit No.	Access	Bit Description
7		Unused.
6	RW	JESD204B serial tail bit, PN, enable. Note that the following equation can be used to determine the number of PN bits sent per sample = N' − N − CS (the number of control bits per sample). 0: serial tail bit, PN, disabled. Unused extra tail bits are padded with zeros. 1: serial tail bit, PN, enabled. Unused extra tail bits are padded with a pseudo random number sequence from a 31-bit LFSR (see JESD204B 5.1.4).
5	RW	JESD204B serial test sample enable. 0: JESD204B test samples disabled. 1: JESD204B test samples enabled. The transport layer test sample sequence (as specified in JESD204B Section 5.1.6.2) is sent on all link lanes.
4	RW	JESD204B serial lane synchronization enable. Note that the frame character insertion must be enabled (Register 0x05F[1] = 0) to enable lane synchronization. 0: lane synchronization disabled. Both sides do not perform lane synchronization; frame alignment character insertion always uses /K28.7/ control characters (see JESD204B 5.3.3.4). 1: lane synchronization enabled. Both sides perform lane sync; frame alignment character insertion uses either /K28.3/ or /K28.7/ control characters (see JESD204B 5.3.3.4).
[3:2]	RW	JESD204B serial initial lane alignment sequence mode. 00: initial lane alignment sequence disabled (JESD204B 5.3.3.5). 01: initial lane alignment sequence enabled (JESD204B 5.3.3.5). 10: reserved. 11: initial lane alignment sequence always on test mode; the JESD204B data link layer test mode (where repeated lane alignment sequence, as specified in JESD204B section 5.3.3.9.2) is sent on all lanes.
1	RW	JESD204B serial frame alignment character insertion (FACI) disable. 0: frame alignment character insertion enabled (JESD204B 5.3.3.4). 1: frame alignment character insertion disabled. Note that this is for debug only (JESD204B 5.3.3.4).
0	RW	JESD204B serial transmit link power-down (active high). Note that the JESD204B transmitter link must be powered down while changing any of the link configuration bits. 0: JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNCINB± pins. 1: JESD204B serial transmit link powered down (held in reset and clock gated).

Table 55. JESD204B Link Control Register 2, Address 0x060 (Default = 0x00)

Bit No.	Access	Bit Description
[7:6]	RW	JESD204B serial synchronization mode. 00: normal mode. 01: reserved. 10: SYNCINB± active mode. SYNCINB± pins are active: force code group synchronization. 11: SYNCINB± pins disabled.
5	RW	JESD204B serial synchronization pin invert. 0: SYNCINB± pins not inverted. 1: SYNCINB± pins inverted.
[4:3]		Unused.
2	RW	JESD204B Serial 8-bit/10-bit bypass (test mode only). 0: 8-bit/10-bit enabled. 1: 8-bit/10-bit bypassed (most significant two bits are 0).
1	RW	JESD204B 10-bit serial transmit bit invert. Note that in the event that the CML signals are reversed in a system board layout, this bit effectively inverts the differential outputs from the PHY. 0: normal. 1: invert the a, b, c, d, e, f, g, h, i, j bits.
0	RW	JESD204B 10-bit serial transmit bit mirror. 0: 10-bit serial bits are not mirrored. Transmit bit order is alphabetical: a, b, c, d, e, f, g, h, i, j. 1: 10-bit serial bits are mirrored. Transmit bit order is alphabetically reversed: j, i, h, g, f, e, d, c, b, a.

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Table 56. JESD204B Link Control Register 3, Address 0x061 (Default = 0x00)

Bit No.	Access	Bit Description
7	RW	JESD204B checksum disable. 0: checksum enabled in the link configuration parameter. Normal operation. 1: checksum disabled in the link configuration parameter (set to zero). For testing purposes only.
6	RW	JESD204B checksum mode. 0: checksum is the sum of all 8-bit registers in the link configuration fields. 1: checksum is the sum of all individual link configuration fields (LSB aligned).
[5:4]	RW	JESD204B serial test generation input selection. 00: 16-bit test generation data injected at the sample input to the link. 01: 10-bit test generation data injected at the output of the 8-bit/10-bit encoder (at the input to PHY). 10: 8-bit test generation data injected at the input of the scrambler. 11: reserved.
[3:0]	RW	JESD204B serial test generation mode. 0000: normal operation (test mode disabled). 0001: alternating checkerboard. 0010: 1/0 word toggle. 0011: PN sequence (long). 0100: unused. 0101: continuous/repeat user test mode. The most significant bits from the user pattern (1, 2, 3, 4) are placed on the output for one clock cycle and then repeated (the output user pattern is 1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4, …). 0110: single user test mode. The most significant bits from the user pattern (1, 2, 3, 4) are placed on the output for one clock cycle and then output all zeros (the output user pattern is 1, 2, 3, 4, and then outputs all zeros). 0111: ramp output. 1000: modified RPAT test sequence (10-bit value). 1001: unused. 1010: JSPAT test sequence (10-bit value). 1011: JTSPAT test sequence (10-bit value). 1100 to 1111: unused.

Table 57. JESD204B Link Control Register 4, Address 0x062 (Default 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	Initial lane alignment sequence repeat count. Bits[7:0] specify the number of times the initial lane alignment sequence repeats. For ADCs, the JESD204B specification states that the initial lane alignment sequence always spans four multiframes (JESD204B 5.3.3.5). Because Register 0x070, Bits[4:0] determine the number of frames per multiframe, the total number of frames transmitted during the initial lane alignment sequence = 4 × (Register 0x070[4:0] + 1) × (Register 0x062[7:0] + 1).

Table 58. JESD204B Link Control Register 5, Address 0x063 (Default = 0x80)

Bit No.	Access	Bit Description
7		Reserved
[6:4]		Reserved
[3:0]	RW	JESD204B application layer mode. DDC bandwidth modes are as follows: high bandwidth, decimate by 8 (effective output bandwidth = $f_S/10$) and low bandwidth, decimate by 16 (effective output bandwidth = $f_S/20$). 0000: generic (no application layer used). 0001: unused. 0010: unused. 0011: unused. 0100: $f_S \times x$ mode (where x is an integer: 2, 4, 8). 0101 to 0111: unused. 1000: single DDC mode (high bandwidth mode (only DDC0 used). 1001: single DDC mode (low bandwidth mode (only DDC0 used). 1010 to 1011: unused. 1100: dual DDC mode, high bandwidth mode (both DDC 0 and DDC 1 used). 1101: dual DDC mode, low bandwidth mode (both DDC 0 and DDC 1 used). 1110: dual DDC mode, mixed bandwidth mode (DDC 0 high bandwidth mode, DDC 1 low bandwidth mode, samples repeated). 1111: unused.

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Table 59. JESD204B Configuration Register, Address 0x064 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	JESD204B serial device identification (DID) number.

Table 60. JESD204B Configuration Register, Address 0x065 (Default = 0x00)

Bit No.	Access	Bit Description
[7:4]		Unused.
[3:0]	RW	JESD204B serial bank identification (BID) number (extension to DID).

Table 61. JESD204B Configuration Register, Address 0x066 (Default = 0x00)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B serial lane identification (LID) number for Lane 0.

Table 62. JESD204B Configuration Register, Address 0x067 (Default = 0x01)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B serial lane identification (LID) number for Lane 1.

Table 63. JESD204B Configuration Register, Address 0x068 (Default = 0x02)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B serial lane identification (LID) number for Lane 2.

Table 64. JESD204B Configuration Register, Address 0x069 (Default = 0x03)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B serial lane identification (LID) number for Lane 3.

Table 65. JESD204B Configuration Register, Address 0x06A (Default = 0x04)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B serial lane identification (LID) number for Lane 4.

Table 66. JESD204B Configuration Register, Address 0x06B (Default = 0x05)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B serial lane identification (LID) number for Lane 5.

Table 67. JESD204B Configuration Register, Address 0x06C (Default = 0x06)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B serial lane identification (LID) number for Lane 6.

Table 68. JESD204B Configuration Register, Address 0x06D (Default = 0x07)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B serial lane identification (LID) number for Lane 7.

Table 69. JESD204B Configuration Register, Address 0x06E (Default = 0x87)

Bit No.	Access	Bit Description
7	RW	JESD204B serial scrambler mode. 0: JESD204B scrambler disabled (SCR = 0). 1: JESD204B scrambler enabled (SCR = 1).
[6:5]		Unused.

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Bit No.	Access	Bit Description
[4:0]	RW	JESD204B serial lane control (L = Register 0x06E[4:0] + 1). 0: one lane per link (L = 1). 1: two lanes per link (L = 2). 2: unused. 3: four lanes per link (L = 4). 4: unused. 5: six lanes per link (L = 6). 6: unused. 7: eight lanes per link (L = 8). 8 to 31: unused.

Table 70. JESD204B Configuration Register, Address 0x06F (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B number of octets per frame (F = Register 0x06F[7:0] + 1). These bits are calculated using the following equation: $F = (N')/(2 \times L)$ The following are valid values of F: M = 1, S = 4, N' = 16, L = 1, F = 8. M = 1, S = 4, N' = 16, L = 2, F = 4. M = 1, S = 4, N' = 16, L = 4, F = 2. M = 1, S = 4, N' = 12, L = 6, F = 1. M = 1, S = 4, N' = 16, L = 8, F = 1 (default).

Table 71. JESD204B Configuration Register, Address 0x070 (Default = 0x1F)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	JESD204B number of frames per multiframe (K = Register 0x070[4:0] + 1). Only those values that are divisible by four can be used.

Table 72. JESD204B Configuration Register, Address 0x071 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B number of converters per link/device. 0: link connected to one ADC (M = 1). 1 to 255: unused.

Table 73. JESD204B Configuration Register, Address 0x072 (Default = 0x0B)

Bit No.	Access	Bit Description
[7:6]	RW	JESD204B number of control bits per sample (CS, based on the JESD204B specification). 00: no control bits sent per sample (CS = 0). 01: one control bit sent per sample, overrange bit enabled (CS = 1). 10: two control bits sent per sample, overrange + timestamp SYSREF bit (CS = 2). 11: reserved.
5		Unused.
[4:0]	RW	JESD204B converter resolution (N = Register 0x072[4:0] + 1). 0x00 to 0x06: reserved. 0x07 to 0x09: reserved. 0x0A: reserved. 0x0B: N = 12-bit ADC converter resolution. 0x0C to 0x0E: reserved. 0x0F: N = 16-bit ADC converter resolution. 0x10 to 0x1F: reserved.

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Table 74. JESD204B Configuration Register, Address 0x073 (Default = 0x2F)

Bit No.	Access	Bit Description
[7:5]	RW	JESD204B device subclass version. 0x0: Subclass 0. 0x1: Subclass 1 (default). 0x2: Subclass 2 (not supported). 0x3: undefined.
[4:0]	RW	JESD204B total number of bits per sample (N' = Register 0x073[4:0] + 1). 0x0 to 0xA: unused. 0xB: N' = 12 (L must be equal to 6). 0xC to 0xE: unused. 0xF: N' = 16 (L must be equal to 1, 2, 4, or 8).

Table 75. JESD204B Configuration Register, Address 0x074 (Default = 0x23)

Bit No.	Access	Bit Description
[7:5]	RW	JESD204B version. 0x0: JESD204A. SYNCINB± pins input are internally gated by the frame clock. SYNCINB± must be low for at least two frame clock cycles to be interpreted as a synchronization request. 0x1: JESD204B. SYNCINB± pins input are internally gated by the local multiframe clock. SYNCINB± must be low for at least four frame clock cycles to be interpreted as a synchronization request. 0x2 to 0x7: undefined.
[4:0]	RO	JESD204B samples per converter frame cycle (S = Register 0x074[4:0] + 1). These are read-only bits. For the AD9625, S must be equal to 4 (Register 0x074[4:0] = 3).

Table 76. JESD204B Configuration Register, Address 0x075 (Default = 0x80)

Bit No.	Access	Bit Description
7	RO	JESD204B high density (HD) format. This is a read-only bit. 0: HD format disabled. 1: HD format enabled. High density mode is automatically enabled based on the values of N' and L. The values of HD for the AD9625 are as follows: N' = 16, L = 1, HD = 0. N' = 16, L = 2, HD = 0. N' = 16, L = 4, HD = 0. N' = 12, L = 6, HD = 1. N' = 16, L = 8, HD = 1 (default).
[6:5]		Unused.
[4:0]	RO	JESD204B Number of control words per frame clock cycle per link (CF). These are read-only bits. For the AD9625, CF must equal 0 (Register 0x075[4:0] = 0).

Table 77. JESD204B Configuration Register, Address 0x076 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	JESD204B Serial Reserved Field 1.

Table 78. JESD204B Configuration Register, Address 0x077 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	JESD204B Serial Reserved Field 2.

Table 79. JESD204B Configuration Register, Address 0x078 (Default = 0xC3)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B serial checksum value for Lane 0. This value is automatically calculated The value = (the sum of all link configuration parameters for Lane 0) Modulus 256. Checksum is enabled/disabled using Register 0x061, Bit 7.

Table 80. JESD204B Configuration Register, Address 0x079 (Default = 0xC4)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B serial checksum value for Lane 1. This value is automatically calculated. The value = (the sum of all link configuration parameters for Lane 1) Modulus 256. Checksum is enabled/disabled using Register 0x061, Bit 7.

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Table 81. JESD204B Configuration Register, Address 0x07A (Default = 0xC5)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B serial checksum value for Lane 2. This value is automatically calculated. The value = (the sum of all link configuration parameters for Lane 2) Modulus 256. Checksum is enabled/disabled using Register 0x061, Bit 7.

Table 82. JESD204B Configuration Register, Address 0x07B (Default = 0xC6)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B serial checksum value for Lane 3. This value is automatically calculated. The value = (the sum of all link configuration parameters for Lane 3) Modulus 256. Checksum is enabled/disabled using Register 0x061, Bit 7.

Table 83. JESD204B Configuration Register, Address 0x07C (Default = 0xC7)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B serial checksum value for Lane 4. This value is automatically calculated. The value = (the sum of all link configuration parameters for Lane 4) Modulus 256. Checksum is enabled/disabled using Register 0x061, Bit 7.

Table 84. JESD204B Configuration Register, Address 0x07D (Default = 0xC8)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B serial checksum value for Lane 5. This value is automatically calculated. The value = (the sum of all link configuration parameters for Lane 5) Modulus 256. Checksum is enabled/disabled using Register 0x061, Bit 7.

Table 85. JESD204B Configuration Register, Address 0x07E (Default = 0xC9)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B serial checksum value for Lane 6. This value is automatically calculated. The value = (the sum of all link configuration parameters for Lane 6) Modulus 256. Checksum is enabled/disabled using Register 0x061, Bit 7.

Table 86. JESD204B Configuration Register, Address 0x07F (Default = 0xCA)

Bit No.	Access	Bit Description
[7:0]	RO	JESD204B serial checksum value for Lane 6. This value is automatically calculated. The value = (the sum of all link configuration parameters for Lane 6) Modulus 256. Checksum is enabled/disabled using Register 0x061, Bit 7.

Table 87. JESD204B Lane Power-Down Register, Address 0x080 (Default = 0x00)

Bit No.	Access	Bit Description
7	RW	Physical Lane H power-down. 0: Lane H enabled. 1: Lane H powered down.
6	RW	Physical Lane G power-down. 0: Lane G enabled. 1: Lane G powered down.
5	RW	Physical Lane F power-down. 0: Lane F enabled. 1: Lane F powered down.
4	RW	Physical Lane E power-down. 0: Lane E enabled. 1: Lane E powered down.
3	RW	Physical Lane D power-down. 0: Lane D enabled. 1: Lane D powered down.
2	RW	Physical Lane C power-down. 0: Lane C enabled. 1: Lane C powered down.
1	RW	Physical Lane B power-down. 0: Lane B enabled. 1: Lane B powered down.
0	RW	Physical Lane A power-down. 0: Lane A enabled. 1: Lane A powered down.

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Table 88. JESD204B Lane Control Register 1, Address 0x082 (Default = 0x10)

Bit No.	Access	Bit Description
7		Unused.
[6:4]	RW	Physical Lane B assignment. 000: Logical Lane 0. 001: Logical Lane 1 (default). 010: Logical Lane 2. 011: Logical Lane 3. 100: Logical Lane 4. 101: Logical Lane 5. 110: Logical Lane 6. 111: Logical Lane 7.
3		Unused.
[2:0]	RW	Physical Lane A assignment. 000: Logical Lane 0 (default). 001: Logical Lane 1. 010: Logical Lane 2. 011: Logical Lane 3. 100: Logical Lane 4. 101: Logical Lane 5. 110: Logical Lane 6. 111: Logical Lane 7.

Table 89. JESD204B Lane Control Register 2, Address 0x083 (Default = 0x32)

Bit No.	Access	Bit Description
7		Unused.
[6:4]	RW	Physical Lane D assignment. 000: Logical Lane 0. 001: Logical Lane 1. 010: Logical Lane 2. 011: Logical Lane 3 (default). 100: Logical Lane 4. 101: Logical Lane 5. 110: Logical Lane 6. 111: Logical Lane 7.
3		Unused.
[2:0]	RW	Physical Lane C assignment. 000: Logical Lane 0. 001: Logical Lane 1. 010: Logical Lane 2 (default). 011: Logical Lane 3. 100: Logical Lane 4. 101: Logical Lane 5. 110: Logical Lane 6. 111: Logical Lane 7.

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Table 90. JESD204B Lane Control Register 3, Address 0x084 (Default = 0x54)

Bit No.	Access	Bit Description
7		Unused.
[6:4]	RW	Physical Lane F assignment. 000: Logical Lane 0. 001: Logical Lane 1. 010: Logical Lane 2. 011: Logical Lane 3. 100: Logical Lane 4. 101: Logical Lane 5 (default). 110: Logical Lane 6. 111: Logical Lane 7.
3		Unused.
[2:0]	RW	Physical Lane E assignment. 000: Logical Lane 0. 001: Logical Lane 1. 010: Logical Lane 2. 011: Logical Lane 3. 100: Logical Lane 4 (default). 101: Logical Lane 5. 110: Logical Lane 6. 111: Logical Lane 7.

Table 91. JESD204B Lane Control Register 4, Address 0x085 (Default = 0x76)

Bit No.	Access	Bit Description
7		Unused.
[6:4]	RW	Physical Lane H assignment. 000: Logical Lane 0. 001: Logical Lane 1. 010: Logical Lane 2. 011: Logical Lane 3. 100: Logical Lane 4. 101: Logical Lane 5. 110: Logical Lane 6. 111: Logical Lane 7 (default).
3		Unused.
[2:0]	RW	Physical Lane G assignment. 000: Logical Lane 0. 001: Logical Lane 1. 010: Logical Lane 2. 011: Logical Lane 3. 100: Logical Lane 4. 101: Logical Lane 5. 110: Logical Lane 6 (default). 111: Logical Lane 7.

Table 92. Unused, Address 0x088 (Default = 0x67)

Bit No.	Access	Bit Description
[7:0]	RW	Unused.

Table 93. Unused, Address 0x089 (Default = 0xF0)

Bit No.	Access	Bit Description
[7:0]	RW	Unused.

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Table 94. Control Register, Address 0x08A (Default = 0x20)

Bit No.	Access	Bit Description
[7:6]		Unused.
[5:4]	RW	Reserved; Bits[5:4] must be set to 10.
[3:2]		Unused.
[1:0]	RW	Bits[1:0] must be set to 00 for LMFC JESD204B alignment with SYSREF±. Bits[1:0] must be set to 10 for control bit timestamping with SYSREF±.

Table 95. JESD204B Local Multiframe Clock Offset Control Register, Address 0x08B (Default = 0x00)

Bit No.	Access	Bit Description
[7:5]		Unused.
[4:0]	RW	Local multiframe clock (LMFC) phase offset value. These bits provide the reset value for LMFC phase counter when SYSREF± pins are asserted; this is used for deterministic delay applications.

Table 96. JESD204B Local Frame Clock Offset Control Register, Address 0x08C (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	Local frame clock phase offset value. Reset value for frame clock phase counter when SYSREF± pins are asserted. For the AD9625, only values from 0 to 7 are valid. This is used for deterministic delay applications.

Table 97. DIVCLK± Register, Address 0x0F8 (Default = 0x00)

Bit No.	Access	Bit Description
[7:1]	RW	Spare customer register.
0	RW	Register control to set the ratio between ADC sampling clock and DIVCLK±. 0: divide by 4. 1: not used.

Table 98. Reserved Register, Address 0x0F9

Bit No.	Access	Bit Description
[7:0]	RW	Reserved.

Table 99. Customer Spare Register, Address 0x0FF (Default = 0x00)

Bit No.	Access	Bit Description
[7:1]		Unused.
0	RW	Register map master/slave transfer bit. Self-clearing bit used to synchronize the transfer of data from the master to the slave registers. 0: no effect. 1: transfers data from the master registers, written by the register maps, to the slave registers.

Table 100. Interrupt Request (IRQ) Status Register, Address 0x100 (Default = 0x00)

Bit No.	Access	Bit Description
7	RO	Interrupt request PLL lock error. 1: the PLL is unlocked.
6		Unused.
5	RO	Unused.
4	RO	Unused.
3	RO	Interrupt request SYSREF± hold error. 1: a hold error has occurred with the last SYSREF± signal received. To clear this error, set and clear Bit 6 in Register 0x03A.
2	RO	Interrupt request SYSREF± setup error. 1: a setup error has occurred with the last SYSREF± signal received. To clear this error, set and clear Bit 6 in Register 0x03A.
1		Unused.
0	RO	Interrupt request clock error.

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Table 101. Interrupt Request (IRQ) Mask Control Register, Address 0x101 (Default = 0xBC)

Bit No.	Access	Bit Description
7	RW	Interrupt request PLL lock error masked. 1: PLL unlocked events are masked.
6		Unused.
5	RW	Must be set to 1.
4	RW	Must be set to 1.
3	RW	Interrupt request SYSREF± hold error. 1: a hold error has occurred with the last SYSREF± signal received. To clear this error, set and clear Bit 6 in Register 0x03A.
2	RW	Interrupt request SYSREF± setup error. 1: a setup error has occurred with the last SYSREF± signal received. To clear this error, set and clear Bit 6 in Register 0x03A.
1		Unused.
0	RW	Interrupt request clock error mask. 1: clock error has occurred and the validity of the output data cannot be guaranteed. The only way to recover from this error is to reset the device.

Table 102. Digital Control Register, Address 0x105 (Default = 0x00)

Bit No.	Access	Bit Description
[7:5]		Unused.
4	RW	Must be set to 0.
3	RW	Must be set to 0.
2	RW	Must be set to 0.
1	RW	Must be set to 0.
0	RW	Must be set to 0.

Table 103. Digital Calibration Threshold Control Register, Address 0x10A (Default = 0x10)

Bit No.	Access	Bit Description
[7:5]		Unused.
4	RW	Enable data set threshold logic for background gain.
[0:3]		Unused.

Table 104. Digital Calibration Data Set Threshold Register, Address 0x10D (Default = 0x3D)

Bit No.	Access	Bit Description
[7:0]	RW	Data set threshold for background gain calibration.

Table 105. Digital Calibration Data Set Threshold Register, Address 0x10E (Default = 0x14)

Bit No.	Access	Bit Description
[7:0]	RW	Data set threshold for background gain calibration.

Table 106. DIVCLK± Output Control Register, Address 0x120 (Default = 0x11)

Bit No.	Access	Bit Description
[7:5]		Unused.
4	RW	DIVCLK± output disable. DIVCLK± is 1/4th of the sample clock frequency. 0: DIVCLK± output is disabled. 1: DIVCLK± output is enabled.
3	RW	DIVCLK± output termination selection. 0: DIVCLK± output uses an external 100 Ω resistive termination. 1: DIVCLK± output uses no external resistive termination.
2		Unused.
[1:0]	RW	Control the differential swing for the DIVCLK± output. 00: 100 mV p-p differential. 01: 200 mV p-p differential. 10: 300 mV p-p differential. 11: 400 mV p-p differential.

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Table 107. Trim Setting Control Register, Address 0x121 (Default = 0x00 for AD9625-2.5 and AD9625-2.6; Default = 0x03 for AD9625-2.0)

Bit No.	Access	Bit Description
[7:2]		Reserved.
[1:0]	RW	Select trim setting, based on sample rate (AD9625-2.0 and AD9625-2.5): 00: Trim 0: for 2.5 GSPS encode rate (default for AD9625-2.5) (not available for AD9625-2.0). 01: Trim 1: for 2.4 GSPS to 2.5 GSPS encode rate (not available for AD9625-2.0). 10: Trim 2: for 2.2 GSPS to 2.4 GSPS encode rate (not available for AD9625-2.0). 11: Trim 3: for 330 MSPS to 2.2 GSPS encode rate (default for AD9625-2.0).
		Select trim setting, based on sample rate (AD9625-2.6): 00: Trim 0: for 2.55 GSPS to 2.6 GSPS encode rate (default for AD9625-2.6). 01: Trim 1: for 2.4 GSPS to 2.55 GSPS encode rate. 10: Trim 2: for 2.2 GSPS to 2.4 GSPS encode rate. 11: Trim 3: for 330 MSPS to 2.2 GSPS encode rate.

Table 108. Unused Register, Address 0x12A (Default = 0x05)

Bit No.	Access	Bit Description
[7:0]	RW	Reserved; maintain default setting of 0x05.

Table 109. DDC 0 Gain Control Register, Address 0x130 (Default = 0x00)

Bit No.	Access	Bit Description
[7:6]		Unused.
[5:4]	RW	DDC 0 polyphase (decimate by 2) gain in units of 6 dB. 00: 0 dB gain. 01: 6 dB gain. 10: 12 dB gain. 11: 18 dB gain.
[3:2]		Unused.
[1:0]	RW	DDC 0 polyphase (decimate by 8) gain in units of 6 dB. 00: 0 dB gain. 01: 6 dB gain. 10: 12 dB gain. 11: 18 dB gain.

Table 110. DDC 0 Phase Increment Least Significant Bits Register, Address 0x131 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	DDC 0 NCO phase increment value. Phase increment for the NCO within DDC 0 (Bits[7:0]). The output frequency = (decimal(Register 0x132[1:0]; Register 0x131[7:0]) × f_S)/1024.

Table 111. DDC 0 Phase Increment Most Significant Bits Register, Address 0x132 (Default = 0x00)

Bit No.	Access	Bit Description
[7:2]		Unused.
[1:0]	RW	DDC 0 NCO phase increment value. Phase increment for the NCO within DDC 0 (Bits[9:8]).

Table 112. DDC 1 Gain Control Register, Address 0x138 (Default = 0x00)

Bit No.	Access	Bit Description
[7:6]		Unused.
[5:4]	RW	DDC 1 polyphase (decimate by 2) gain in units of 6 dB. 00: 0 dB gain. 01: 6 dB gain. 10: 12 dB gain. 11: 18 dB gain.
[3:2]		Unused.

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Bit No.	Access	Bit Description
[1:0]	RW	DDC 1 polyphase (decimate by 8) gain in units of 6 dB. 00: 0 dB gain. 01: 6 dB gain 10: 12 dB gain. 11: 18 dB gain.

Table 113. DDC 1 Phase Increment Least Significant Bits Register, Address 0x139 (Default = 0x00)

Bit No.	Access	Bit Description
[7:0]	RW	DDC 1 NCO phase increment value. Phase increment for the NCO within DDC 1 (Bits[7:0]). The output frequency = (decimal(Register 0x13A[1:0]; Register 0x139[7:0]) × f_S)/1024.

Table 114. DDC 1 Phase Increment Most Significant Bits Register, Address 0x13A (Default = 0x00)

Bit No.	Access	Bit Description
[7:2]		Unused.
[1:0]	RW	DDC1 NCO phase increment value (Bits[9:8]).

Table 115. SYSREF±Hold Time Guardband Register, Address 0x13B (Default = 0x00)

Bit No.	Access	Bit Description
[7:5]	RW	These bits increase the SYSREF± hold time guardband that is used to assert the SYSREF± hold IRQ flag in register 0x100[3]. This time is informational only and does not change the actual hold time for SYSREF±. 000: No additional guardband hold time. 001: 35 ps of additional hold time guardband for 0x100[3]. 010: 70 ps of additional hold time guardband for 0x100[3]. 011: 105 ps of additional hold time guardband for 0x100[3]. 100: 140 ps of additional hold time guardband for 0x100[3]. 101: 175 ps of additional hold time guardband for 0x100[3]. 110: 210 ps of additional hold time guardband for 0x100[3]. 111: 245 ps of additional hold time guardband for 0x100[3].
[4:0]	RW	Reserved.

Table 116. SYSREF± Setup Time Guardband Register, Address 0x13C (Default = 0x00)

Bit No.	Access	Bit Description
[7:5]	RW	These bits increase the SYSREF± setup time guardband that is used to assert the SYSREF± setup IRQ flag in register 0x100[2]. This time is informational only and does not change the actual setup time for SYSREF±. 000: No additional guardband setup time. 001: 35 ps of additional setup time guardband for 0x100[2]. 010: 70 ps of additional setup time guardband for 0x100[2]. 011: 105 ps of additional setup time guardband for 0x100[2]. 100: 140 ps of additional setup time guardband for 0x100[2]. 101: 175 ps of additional setup time guardband for 0x100[2]. 110: 210 ps of additional setup time guardband for 0x100[2]. 111: 245 ps of additional setup time guardband for 0x100[2].
[4:0]	RW	Reserved.

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APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting system level design and layout of the AD9625, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

POWER AND GROUND RECOMMENDATIONS

When connecting power to the AD9625, it is recommended that separate supplies are used: one supply for the analog output (AVDD), and a separate supply for the digital outputs (DRVDD and DVDD). The designer can use several different decoupling capacitors to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PCB level and close to the pins of the part with minimal trace length.

When using the AD9625, a single PCB ground plane is sufficient. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

CLOCK STABILITY CONSIDERATIONS

When powered on, the AD9625 enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the AD9625 needs a stable clock. If the ADC clock source is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in a less than optimum state. To correct this, an initialization sequence must be invoked after the ADC clock is stable or any change in the sampling clock frequency is made. By issuing a digital reset via Register 0x00. The pseudo code sequence for a digital reset is as follows:

#Stable Clock at the input to the AD9625

SPI_Write (0x00, 0x3C); # Reset

SPI_Write (0x080 0xFF) #SPI register transfer

SPI_Write (0x00, 0x00); # Clear Reset

SPI_Write (0x080 0xFF) #SPI register transfer

#Write further configurations

SPI PORT

When the full dynamic performance of the converter is required, do not activate the SPI port. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9625 to keep these signals from transitioning at the converter input pins during critical sampling periods.

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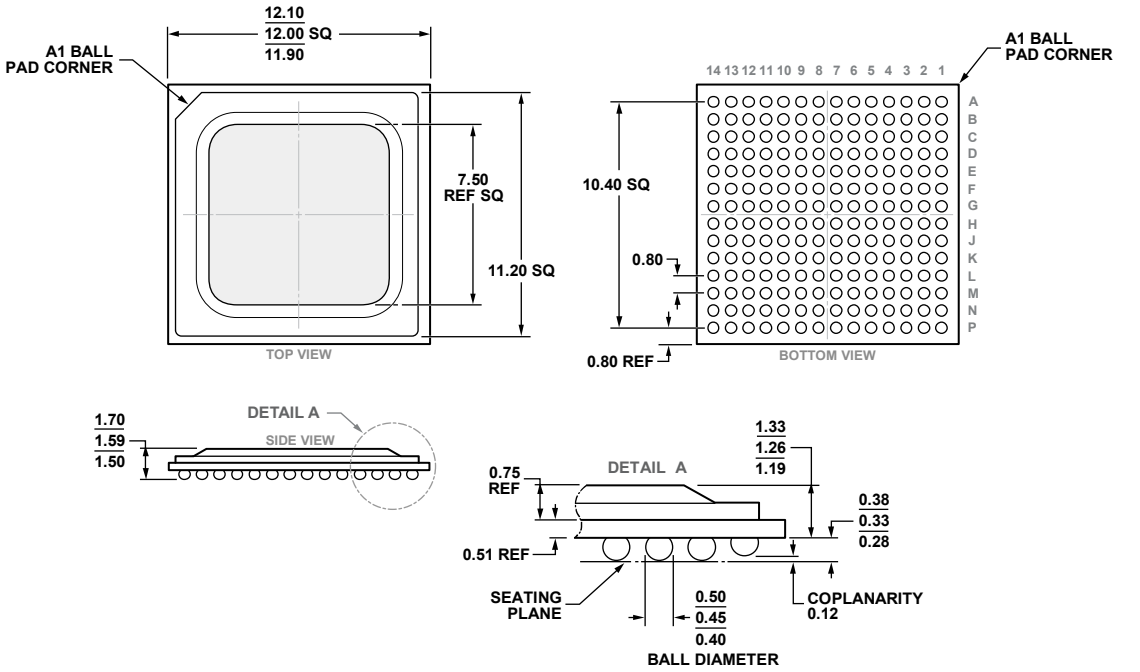
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-GGAB-1.

Figure 107. 196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]
(BP-196-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9625BBPZ-2.5	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-196-2
AD9625BBPZ-2.0	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-196-2
AD9625BBPZ-2.6	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED]	BP-196-2
AD9625BBP-2.6	−40°C to +85°C	196-Ball Ball Grid Array, PbSn, Thermally Enhanced [BGA_ED]	BP-196-2
AD9625BBP-2.5	−40°C to +85°C	196-Ball Ball Grid Array, PbSn, Thermally Enhanced [BGA_ED]	BP-196-2
AD9625BBPZRL-2.5	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED], 13″Tape and Reel	BP-196-2
AD9625BBPZRL-2.0	−40°C to +85°C	196-Ball Ball Grid Array, Thermally Enhanced [BGA_ED], 13″Tape and Reel	BP-196-2
AD9625BBPRL-2.5	−40°C to +85°C	196-Ball BGA, PbSn, Thermally Enhanced [BGA_ED], 13″Tape and Reel	BP-196-2
AD9625BBPRL-2.6	−40°C to +85°C	196-Ball BGA, PbSn, Thermally Enhanced [BGA_ED], 13″Tape and Reel	BP-196-2
AD9625-2.6EB		Evaluation Board with AD9625	
AD9625-2.5EBZ		Evaluation Board with AD9625	
AD9625-2.0EBZ		Evaluation Board with AD9625	

[1] Z = RoHS Compliant Part.

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