AD8000* PRODUCT PAGE QUICK LINKS

Last Content Update: 12/18/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- Universal Evaluation Board for Single High Speed Operational Amplifiers

DOCUMENTATION

Application Notes

- AN-0993: Active Filter Evaluation Board for Analog Devices, Inc., - Low Distortion Pinout Op Amps

Data Sheet

- AD8000: 1.5 GHz Ultrahigh Speed Op Amp Data Sheet

User Guides

- UG-755: 8-Lead SOIC Amplifier Evaluation Board User Guide
- UG-919: Universal Evaluation Board for Single, 8-Lead LFCSP Operational Amplifiers

TOOLS AND SIMULATIONS

- AD8000 SPICE Macro Model

REFERENCE MATERIALS

Informational

- Advantiv™ Advanced TV Solutions

Product Selection Guide

- Amplifiers for Video Distribution
- High Speed Amplifiers Selection Table

Tutorials

- MT-034: Current Feedback (CFB) Op Amps
- MT-051: Current Feedback Op Amp Noise Considerations
- MT-057: High Speed Current Feedback Op Amps
- MT-059: Compensating for the Effects of Input Capacitance on VFB and CFB Op Amps Used in Current-to-Voltage Converters

DESIGN RESOURCES

- AD8000 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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AD8000* PRODUCT PAGE QUICK LINKS

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1/05—Rev. 0: Initial Version

SPECIFICATIONS WITH ±5 V SUPPLY

At T_A = 25°C, V_S = ±5 V, R_L = 150 Ω, Gain = +2, R_F = R_G = 432 Ω, unless otherwise noted. Connect the exposed paddle to ground.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p, SOIC/LFCSP		1580/1350		MHz
	G = +2, V_O = 2 V p-p, SOIC/LFCSP		650/610		MHz
Bandwidth for 0.1 dB Flatness	V_O = 2 V p-p, SOIC/LFCSP		190/170		MHz
Slew Rate	G = +2, V_O = 4 V step		4100		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		12		ns
NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic	V_O = 2 V p-p, f = 5 MHz, LFCSP only		86/89		dBc
Second/Third Harmonic	V_O = 2 V p-p, f = 20 MHz, LFCSP only		75/79		dBc
Input Voltage Noise	f = 100 kHz		1.6		nV/√Hz
Input Current Noise	f = 100 kHz, −IN		26		pA/√Hz
	f = 100 kHz, +IN		3.4		pA/√Hz
Differential Gain Error	NTSC, G = +2		0.02		%
Differential Phase Error	NTSC, G = +2		0.01		Degree
DC PERFORMANCE					
Input Offset Voltage			1	10	mV
Input Offset Voltage Drift			11		µV/°C
Input Bias Current (Enabled)	$+I_B$		−5	+4	µA
	$-I_B$		−3	+45	µA
Transimpedance		570	890	1600	kΩ
INPUT CHARACTERISTICS					
Noninverting Input Impedance			2/3.6		MΩ/pF
Input Common-Mode Voltage Range			−3.5 to +3.5		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	−52	−54	−56	dB
Overdrive Recovery	G = +1, f = 1 MHz, triangle wave		30		ns
$\overline{\text{POWER DOWN}}$ PIN					
Power-Down Input Voltage	Power-down		< $+V_S$ − 3.1		V
	Enabled		> $+V_S$ − 1.9		V
Turn-Off Time	50% of power-down voltage to 10% of V_{OUT} final, V_{IN} = 0.3 V p-p		150		ns
Turn-On Time	50% of power-down voltage to 90% of V_{OUT} final, V_{IN} = 0.3 V p-p		300		ns
Input Bias Current					
Enabled		−1.1	+0.17	+1.4	µA
Power-Down		−300	−235	−160	µA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 100 Ω	±3.7	±3.9		V
Output Voltage Swing	R_L = 1 kΩ	±3.9	±4.1		V
Linear Output Current	V_O = 2 V p-p, second HD < −50 dBc		100		mA
Overdrive Recovery	G = + 2, f = 1 MHz, triangle wave		45		ns
	G = +2, V_{IN} = 2.5 V to 0 V step		22		ns
POWER SUPPLY					
Operating Range		4.5		12	V
Quiescent Current		12.7	13.5	14.3	mA
Quiescent Current (Power-Down)		1.1	1.3	1.65	mA
Power Supply Rejection Ratio	−PSRR/+PSRR	−56/−61	−59/−63		dB

SPECIFICATIONS WITH +5 V SUPPLY

At T_A = 25°C, V_S = 5 V, R_L = 150 Ω, Gain = +2, R_F = R_G = 432 Ω, unless otherwise noted. Connect the exposed paddle to ground.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p		980		MHz
	G = +2, V_O = 2 V p-p		477		MHz
	G = +10, V_O = 0.2 V p-p		328		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p		136		MHz
	V_O = 2 V p-p		136		MHz
Slew Rate	G = +2, V_O = 2 V step		2700		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		16		ns
NOISE/HARMONIC PERFORMANCE					
Second/Third Harmonic	V_O = 2 V p-p, 5 MHz, LFCSP only		71/71		dBc
Second/Third Harmonic	V_O = 2 V p-p, 20 MHz, LFCSP only		60/62		dBc
Input Voltage Noise	f = 100 kHz		1.6		nV/√Hz
Input Current Noise	f = 100 kHz, −IN		26		pA/√Hz
	f = 100 kHz, +IN		3.4		pA/√Hz
Differential Gain Error	NTSC, G = +2		0.01		%
Differential Phase Error	NTSC, G = +2		0.06		Degree
DC PERFORMANCE					
Input Offset Voltage			1.3	10	mV
Input Offset Voltage Drift			18		µV/°C
Input Bias Current (Enabled)	$+I_B$		−5	+3	µA
	$-I_B$		−1	+45	µA
Transimpedance		440	800	1500	kΩ
INPUT CHARACTERISTICS					
Noninverting Input Impedance			2/3.6		MΩ/pF
Input Common-Mode Voltage Range			1.5 to 3.6		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	−51	−52	−54	dB
Overdrive Recovery	G = +1, f = 1 MHz, triangle wave		60		ns
$\overline{\text{POWER DOWN}}$ PIN					
Power-Down Input Voltage	Power-down		< $+V_S$ − 3.1		V
	Enable		> $+V_S$ − 1.9		V
Turn-Off Time	50% of power-down voltage to 10% of V_{OUT} final, V_{IN} = 0.3 V p-p		200		ns
Turn-On Time	50% of power-down voltage to 90% of V_{OUT} final, V_{IN} = 0.3 V p-p		300		ns
Input Current					
Enabled		−1.1	+0.17	+1.4	µA
Power-Down		−50	−40	−30	µA
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 100 Ω	1.1 to 3.9	1.05 to 4.1		V
	R_L = 1 kΩ	1 to 4.0	0.85 to 4.15		V
Linear Output Current	V_O = 2 V p-p, second HD < −50 dBc		70		mA
Overdrive Recovery	G = +2, f = 100 kHz, triangle wave		65		ns
POWER SUPPLY					
Operating Range		4.5		12	V
Quiescent Current		11	12	13	mA
Quiescent Current (Power-Down)		0.7	0.95	1.25	mA
Power Supply Rejection Ratio	−PSRR/+PSRR	−55/−60	−57/−62		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage Range	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in the circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	80	30	°C/W
3 mm × 3 mm LFCSP	93	35	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the AD8000 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8000. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the AD8000 drive at the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

Consider the RMS output voltages. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package vs. the ambient temperature for the exposed paddle SOIC (80°C/W) and the LFCSP (93°C/W) package on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

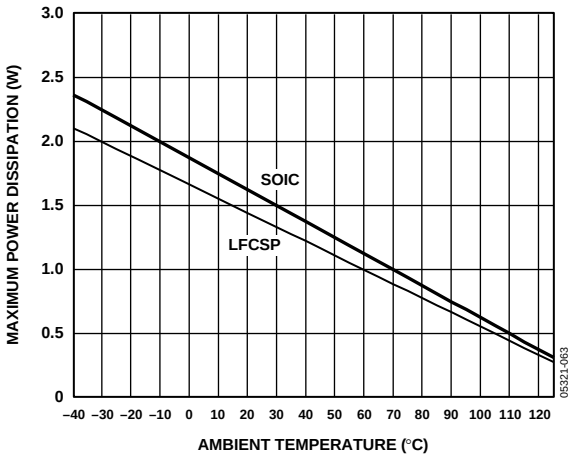

Figure 4. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

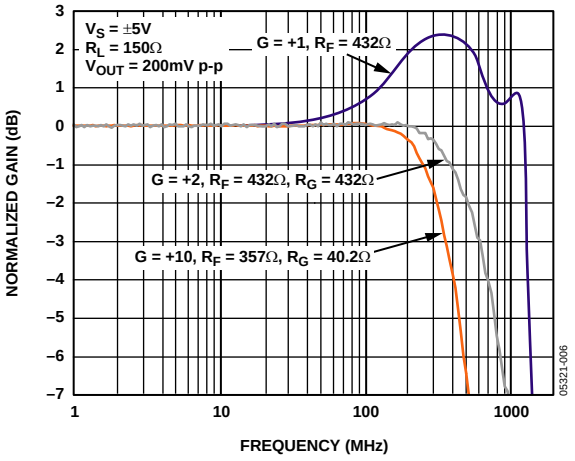

Figure 5. Small Signal Frequency Response vs. Various Gains

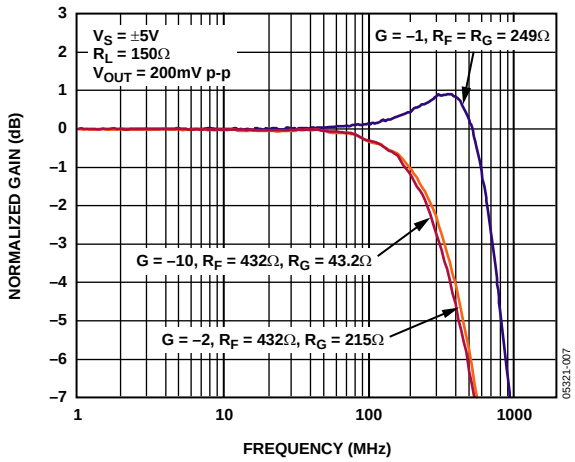

Figure 6. Small Signal Frequency Response vs. Various Gains

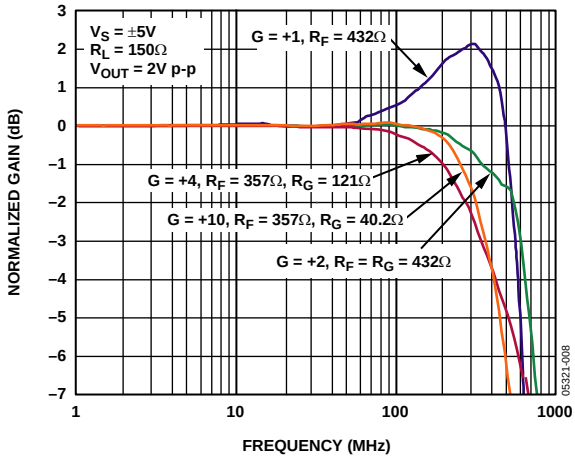

Figure 7. Large Signal Frequency Response vs. Various Gains

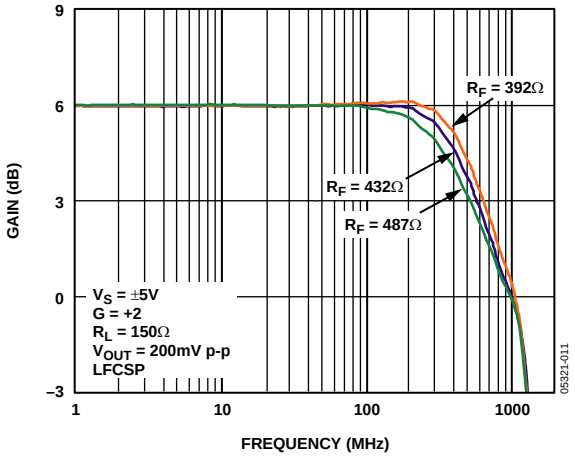

Figure 8. Small Signal Frequency Response vs. R_F

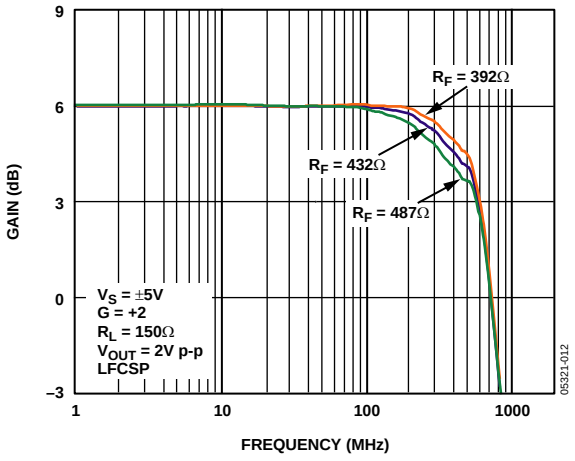

Figure 9. Large Signal Frequency Response vs. R_F

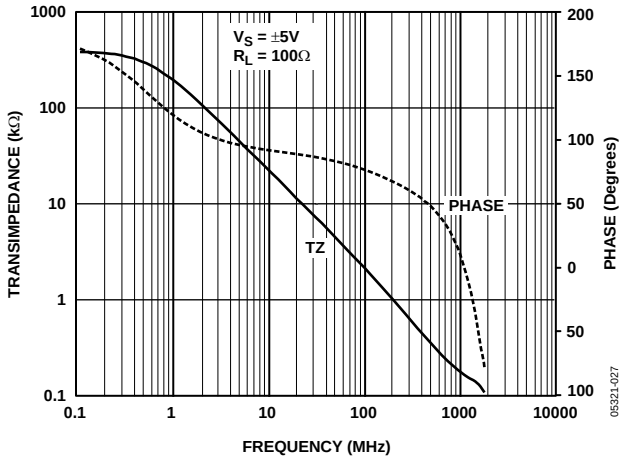

Figure 10. Transimpedance and Phase vs. Frequency

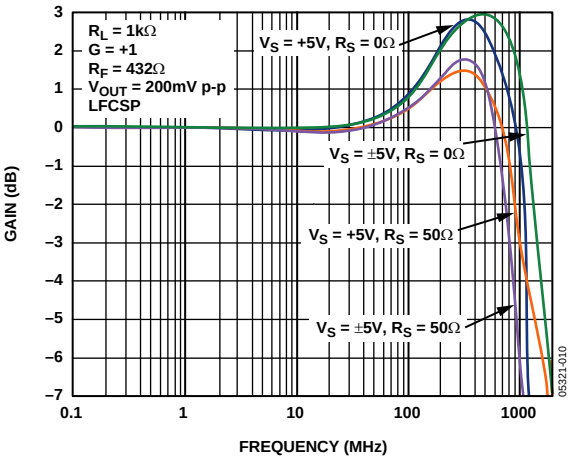

Figure 11. Small Signal Frequency Response vs. Supply Voltage

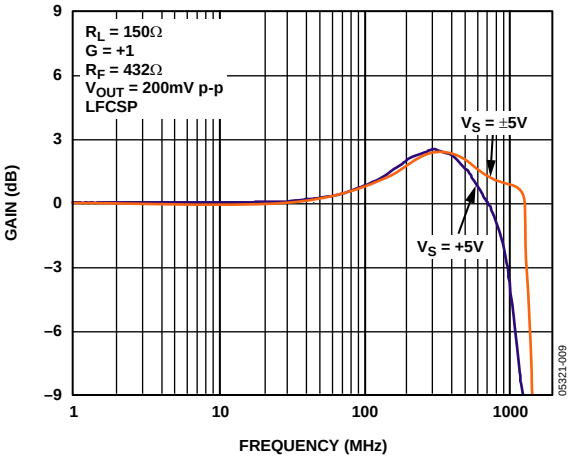

Figure 12. Small Signal Frequency Response vs. Supply Voltage

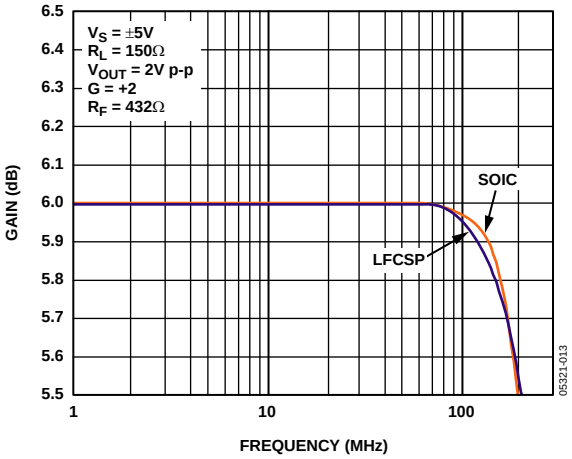

Figure 13. 0.1 dB Flatness

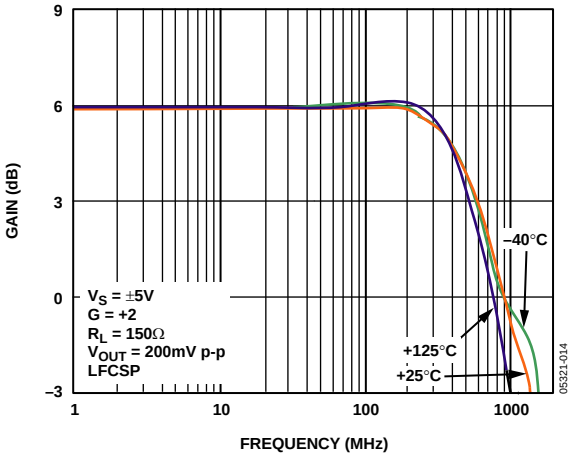

Figure 14. Small Signal Frequency Response vs. Temperature

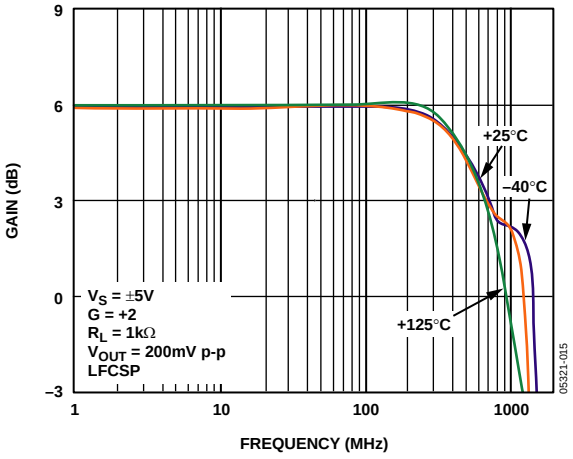

Figure 15. Small Signal Frequency Response vs. Temperature

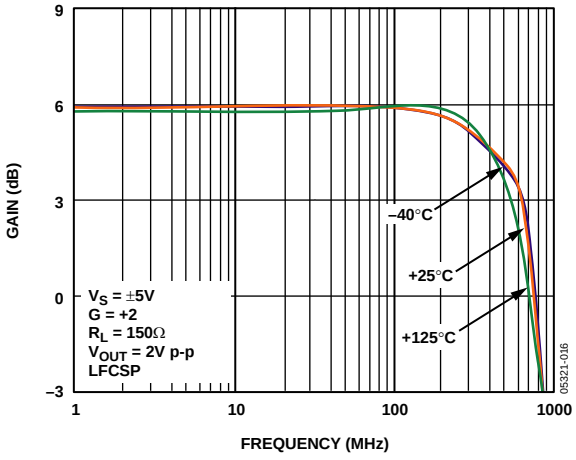

Figure 16. Large Signal Frequency Response vs. Temperature

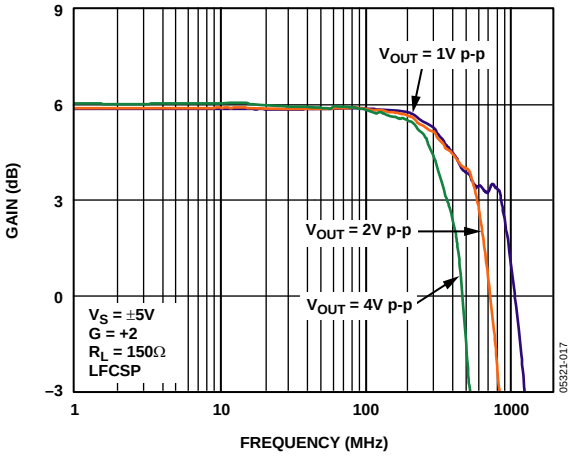

Figure 17. Large Signal Frequency Response vs. Various Outputs

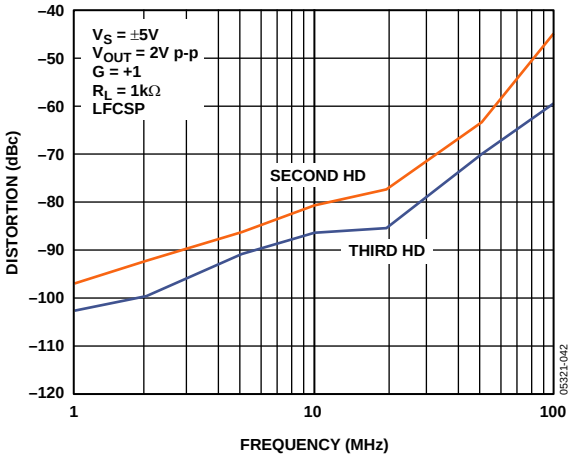

Figure 20. Harmonic Distortion vs. Frequency

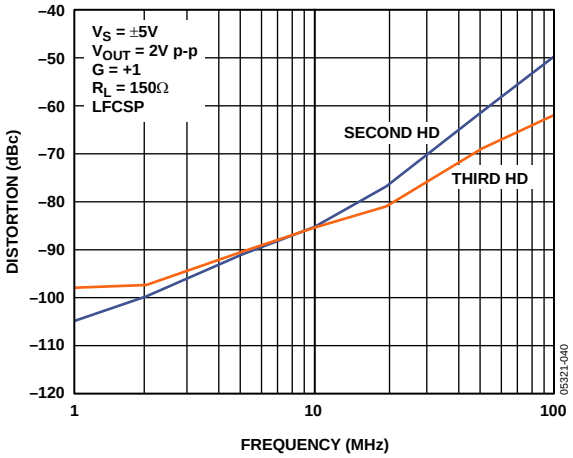

Figure 18. Harmonic Distortion vs. Frequency

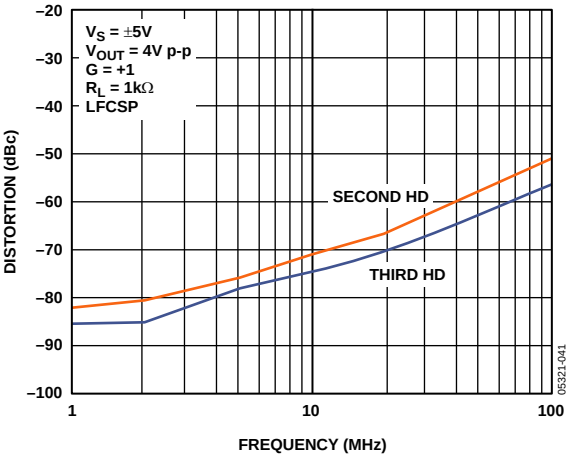

Figure 21. Harmonic Distortion vs. Frequency

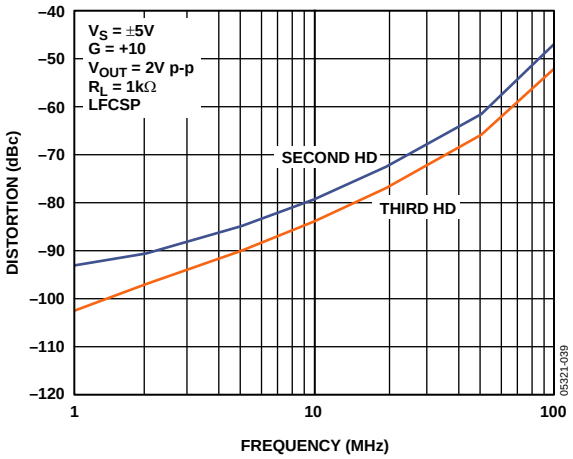

Figure 19. Harmonic Distortion vs. Frequency

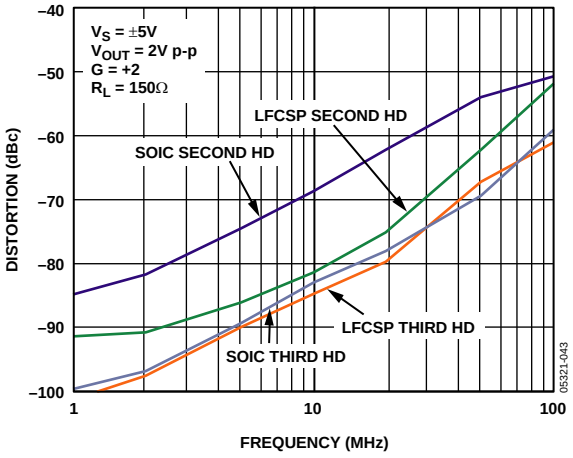

Figure 22. Harmonic Distortion vs. Frequency

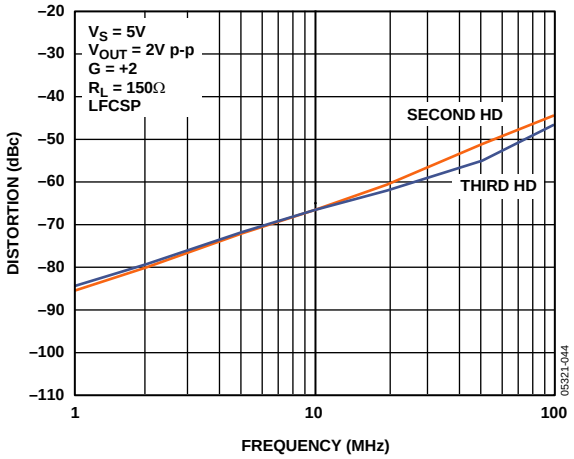

Figure 23. Harmonic Distortion vs. Frequency

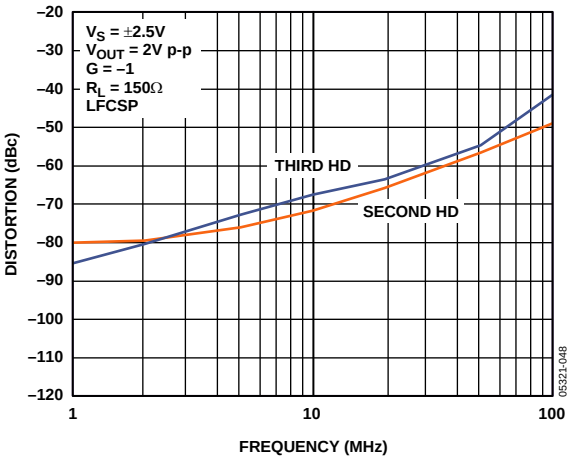

Figure 26. Harmonic Distortion vs. Frequency

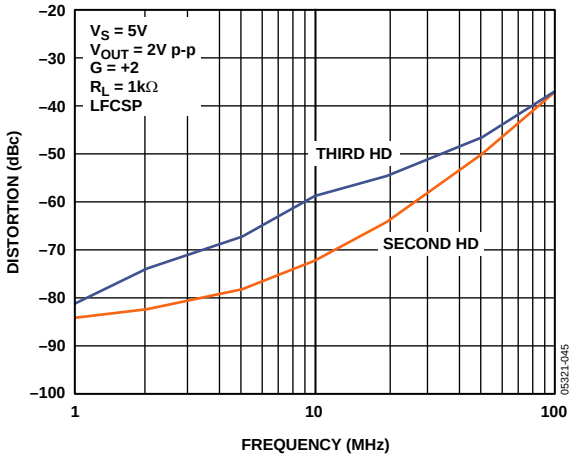

Figure 24. Harmonic Distortion vs. Frequency

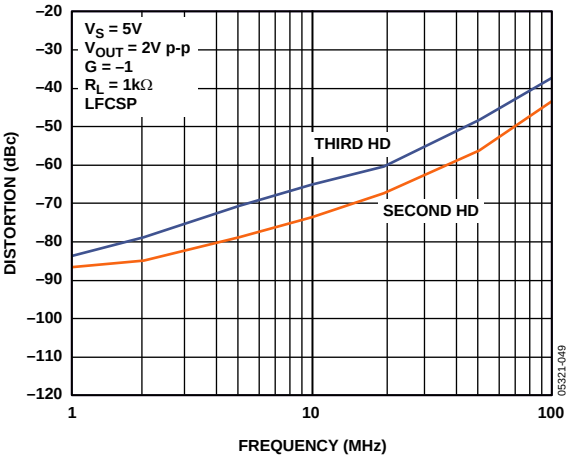

Figure 27. Harmonic Distortion vs. Frequency

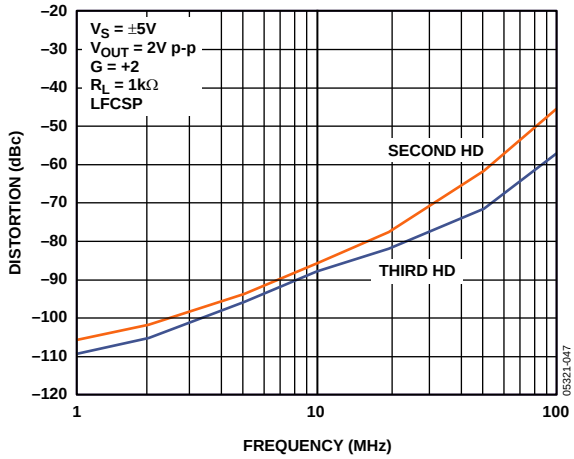

Figure 25. Harmonic Distortion vs. Frequency

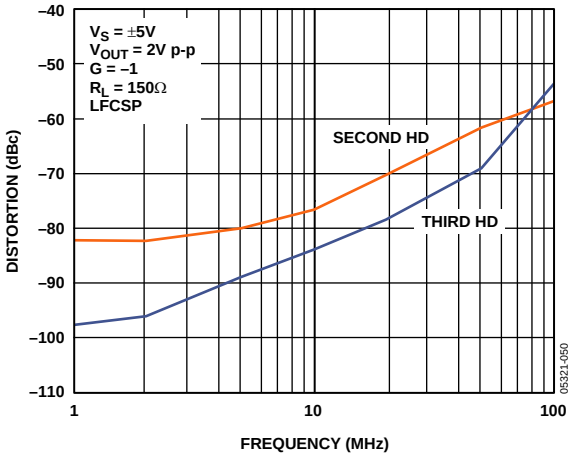

Figure 28. Harmonic Distortion vs. Frequency

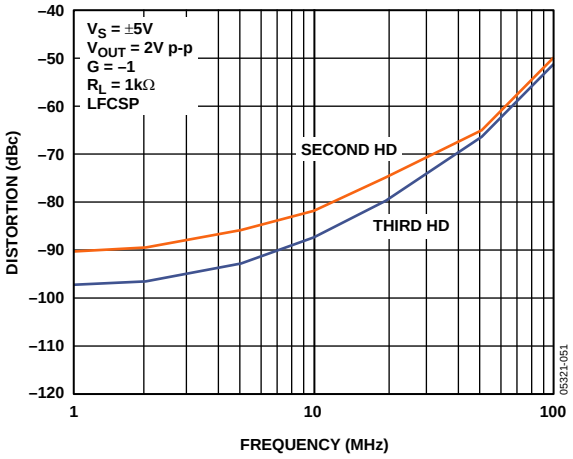

Figure 29. Harmonic Distortion vs. Frequency

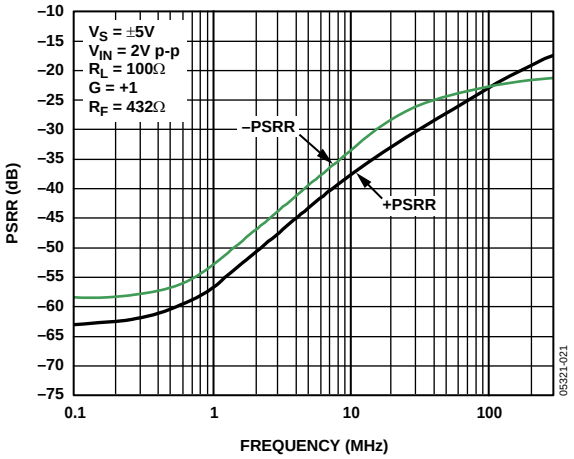

Figure 32. Power Supply Rejection Ratio (PSRR) vs. Frequency

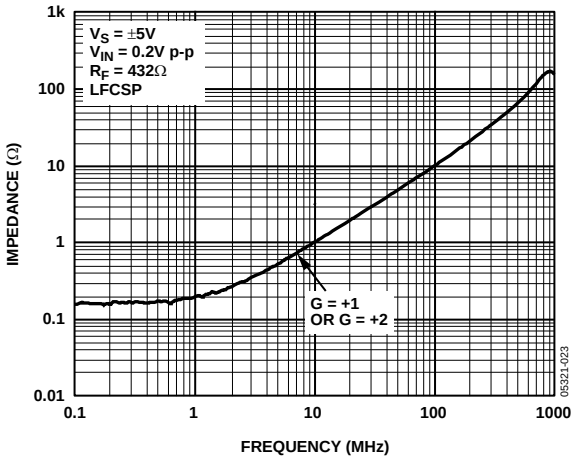

Figure 30. Output Impedance vs. Frequency

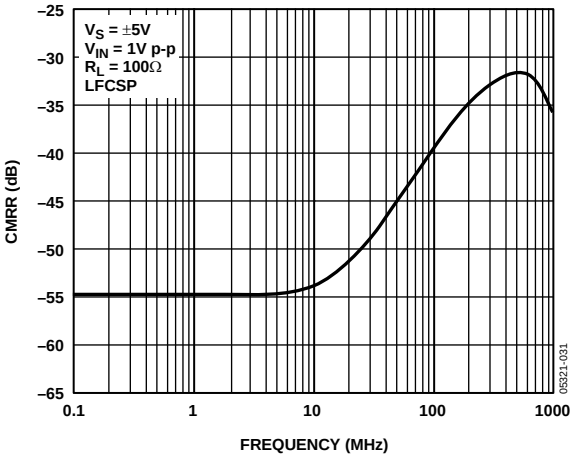

Figure 33. Common-Mode Rejection Ratio vs. Frequency

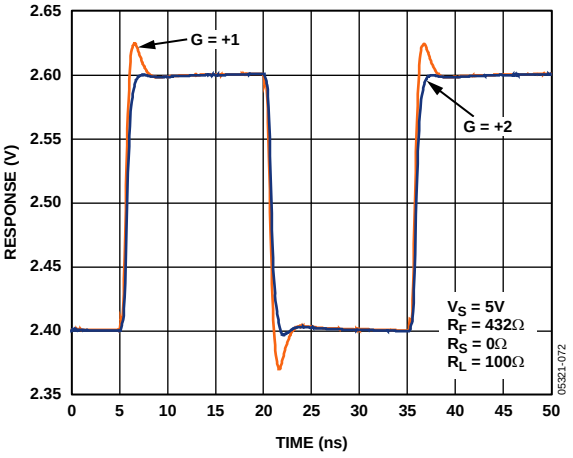

Figure 31. Small Signal Transient Response

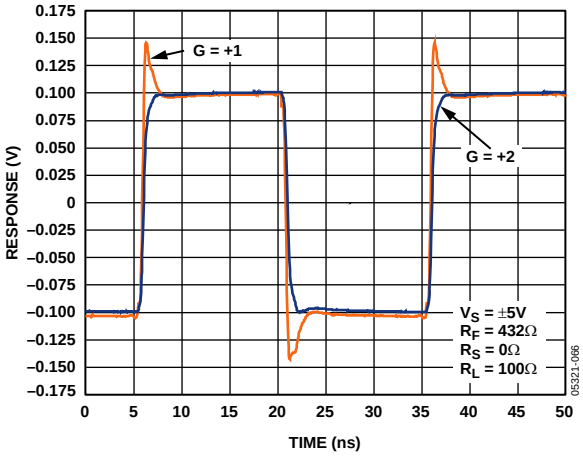

Figure 34. Small Signal Transient Response

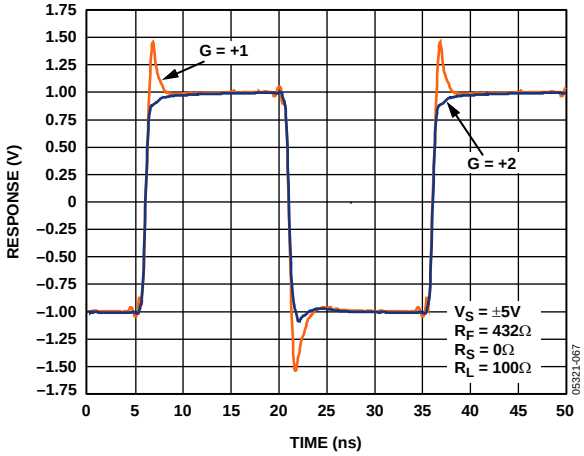

Figure 35. Large Signal Transient Response

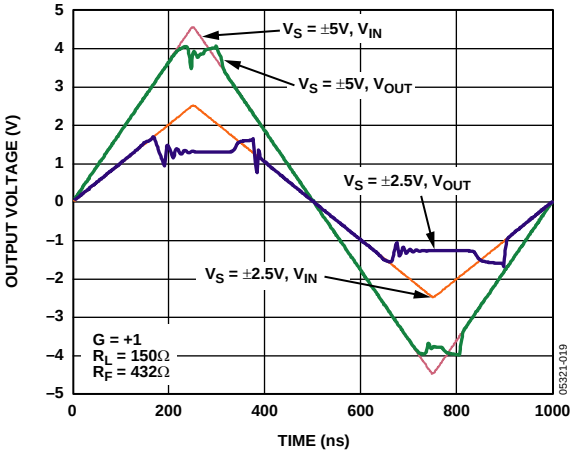

Figure 38. Input Overdrive

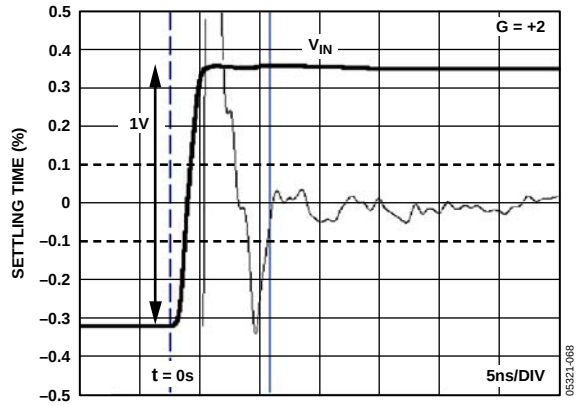

Figure 36. Settling Time

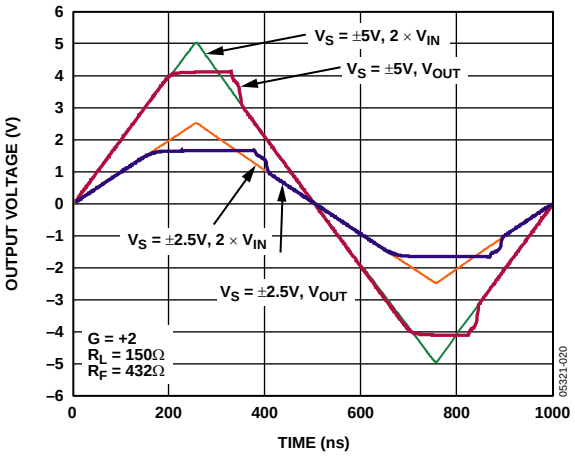

Figure 39. Output Overdrive

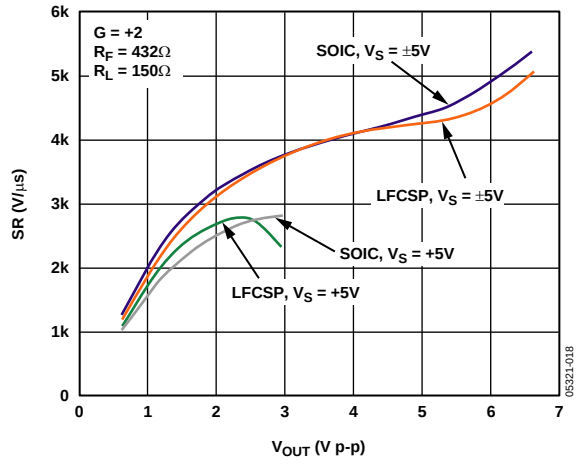

Figure 37. Slew Rate vs. Output Level

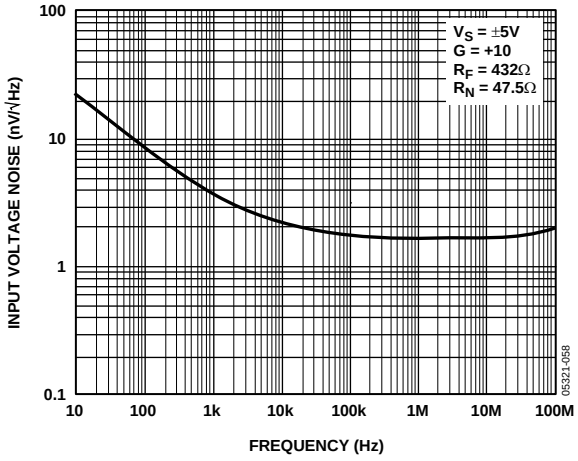

Figure 40. Input Voltage Noise

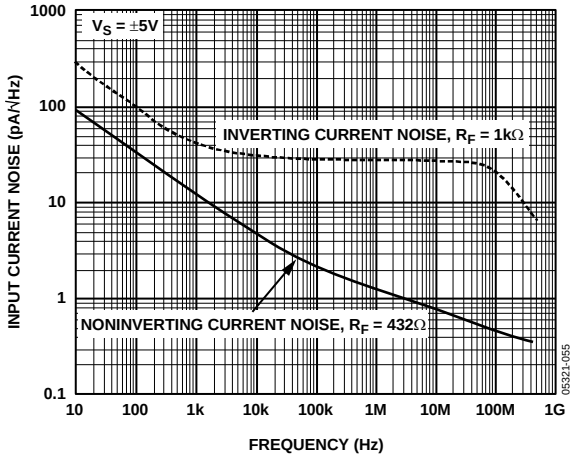

Figure 41. Input Current Noise

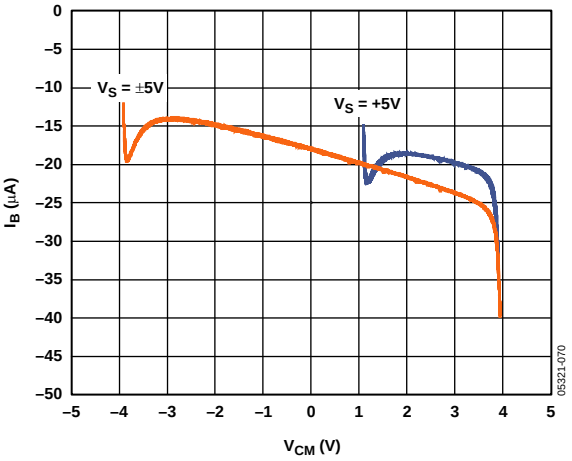

Figure 44. Input Bias Current vs. Common-Mode Voltage

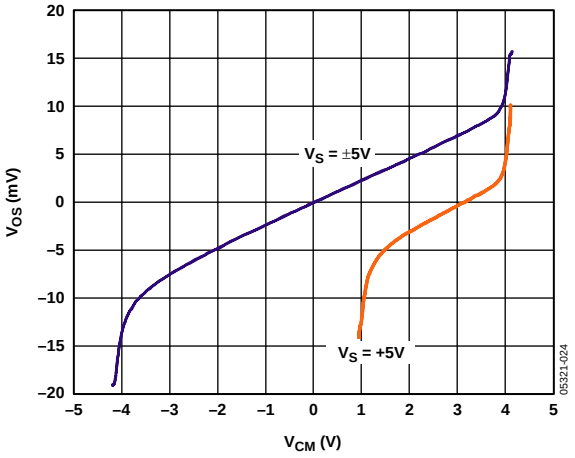

Figure 42. Input V_{OS} vs. Common-Mode Voltage

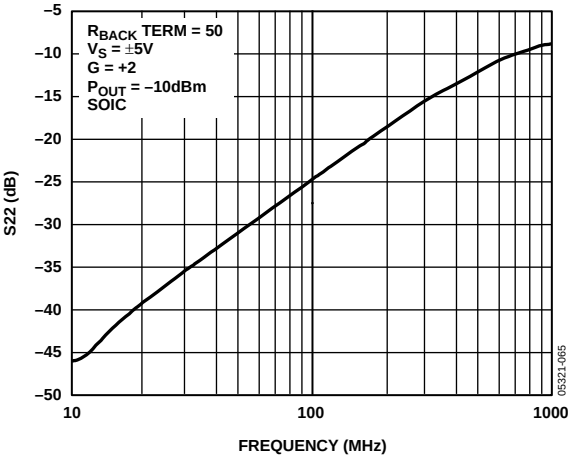

Figure 45. Output Voltage Standing Wave Ratio (S22)

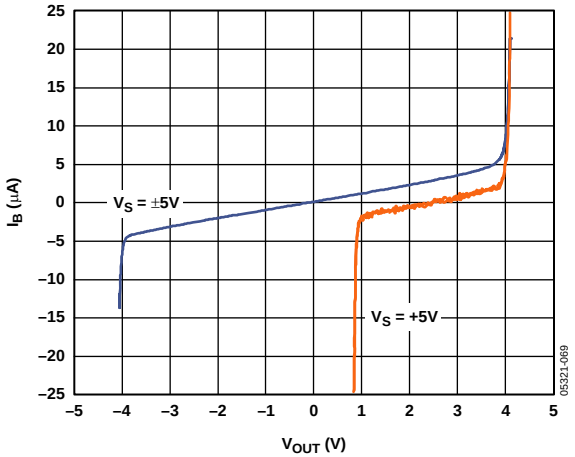

Figure 43. Input Bias Current vs. Output Voltage

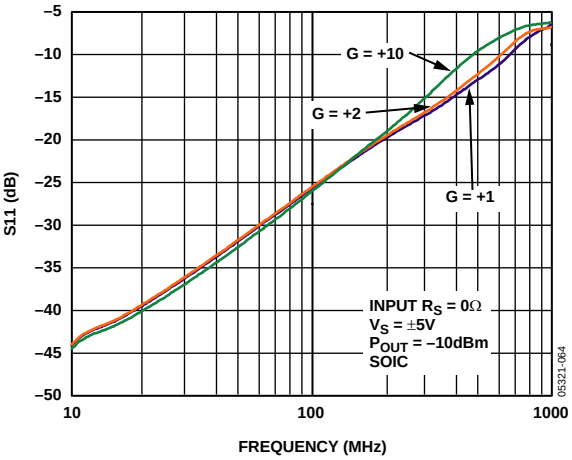

Figure 46. Input Voltage Standing Wave Ratio (S11)

TEST CIRCUITS

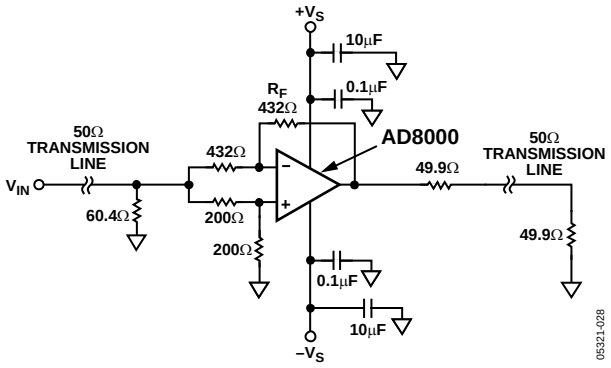

Figure 47. CMRR

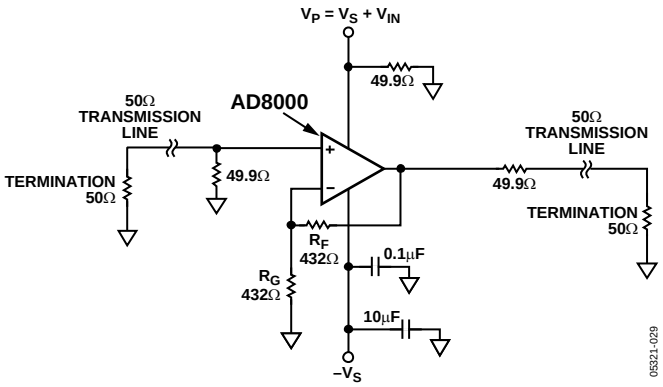

Figure 48. Positive PSRR

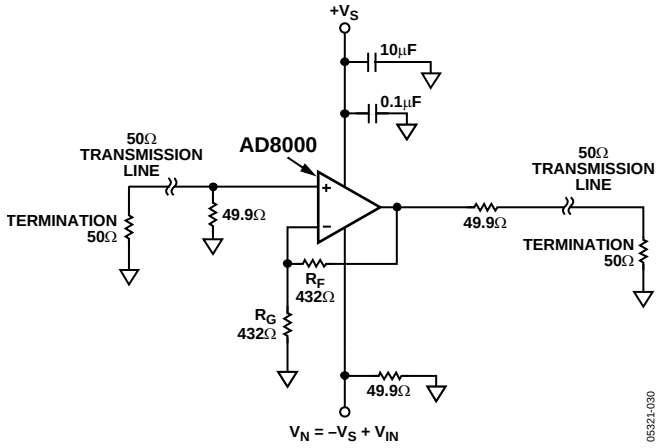

Figure 49. Negative PSRR

APPLICATIONS INFORMATION

All current feedback amplifier operational amplifiers are affected by stray capacitance at the inverting input pin. As a practical consideration, the higher the stray capacitance on the inverting input to ground, the higher R_F needs to be to minimize peaking and ringing.

CIRCUIT CONFIGURATIONS

Figure 50 and Figure 51 show typical schematics for noninverting and inverting configurations. For current feedback amplifiers, the value of feedback resistance determines the stability and bandwidth of the amplifier. The optimum performance values are shown in Table 5 and should not be deviated from by more than ±10% to ensure stable operation. Figure 8 shows the influence varying RF has on bandwidth. In noninverting unity-gain configurations, it is recommended that an R_S of 50 Ω be used, as shown in Figure 50.

Table 5 provides a quick reference for the circuit values, gain, and output voltage noise.

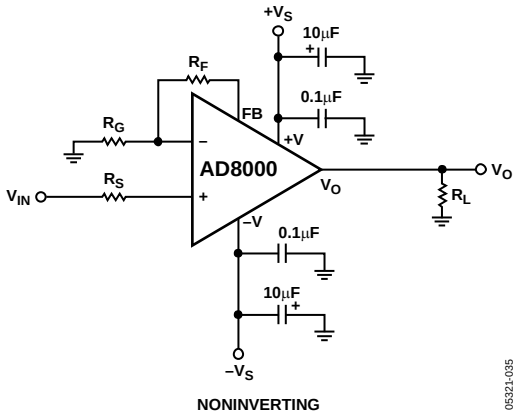

Figure 50. Noninverting Configuration

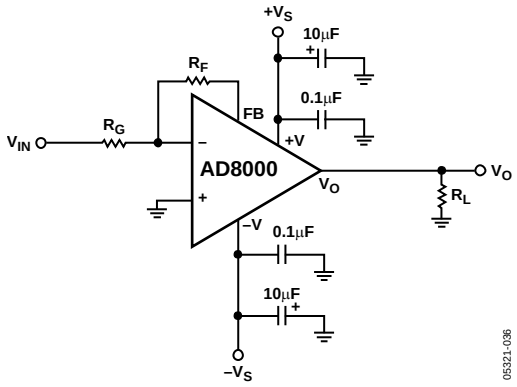

Figure 51. Inverting Configuration

VIDEO LINE DRIVER

The AD8000 is designed to offer outstanding performance as a video line driver. The important specifications of differential gain (0.02%), differential phase (0.01°), and 650 MHz bandwidth at 2 V p-p meet the most exacting video demands. Figure 52 shows a typical noninverting video driver with a gain of +2.

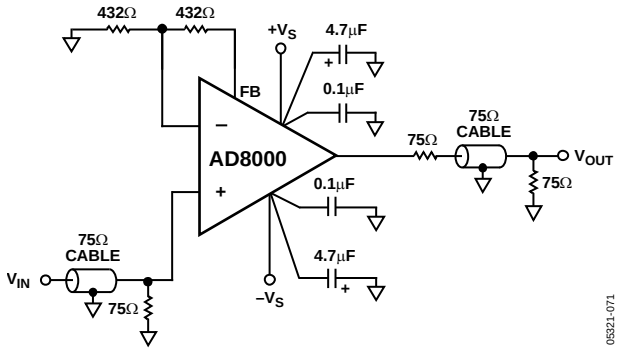

Figure 52. Video Line Driver

Table 5. Typical Values (LFCSP/SOIC)

Gain	Component Values (Ω)		−3 dB SS Bandwidth (MHz)		−3 dB LS Bandwidth (MHz)		Slew Rate (V/µs)	Output Noise (nV/√Hz)	Total Output Noise Including Resistors (nV/√Hz)
	R_F	R_G	LFCSP	SOIC	LFCSP	SOIC			
1	432		1380	1580	550	600	2200	10.9	11.2
2	432	432	600	650	610	650	3700	11.3	11.9
4	357	120	550	550	350	350	3800	10	12
10	357	40	350	365	370	370	3200	18.4	19.9

LOW DISTORTION PINOUT

The AD8000 LFCSP features Analog Devices low distortion pinout. The new pinout lowers the second harmonic distortion and simplifies the circuit layout. The close proximity of the non-inverting input and the negative supply pin creates a source of second harmonic distortion. Physical separation of the non-inverting input pin and the negative power supply pin reduces this distortion significantly, as seen in Figure 22.

By providing an additional output pin, the feedback resistor can be connected directly across Pin 2 and Pin 3. This greatly simplifies the routing of the feedback resistor and allows a more compact circuit layout, which reduces its size and helps to minimize parasitics and increase stability.

The SOIC also features a dedicated feedback pin. The feedback pin is brought out on Pin 1, which is typically a no connect on standard SOIC pinouts.

Existing applications that use the standard SOIC pinout can take full advantage of the performance offered by the AD8000. For drop-in replacements, ensure that Pin 1 is not connected to ground or to any other potential because this pin is connected internally to the output of the amplifier. For existing designs, Pin 6 can still be used for the feedback resistor.

EXPOSED PADDLE

The AD8000 features an exposed paddle, which can lower the thermal resistance by 25% compared to a standard SOIC plastic package. The paddle can be soldered directly to the ground plane of the board. Figure 53 shows a typical pad geometry for the LFCSP, the same type of pad geometry can be applied to the SOIC package.

Thermal vias or heat pipes can also be incorporated into the design of the mounting pad for the exposed paddle. These additional vias improve the thermal transfer from the package to the PCB. Using a heavier weight copper on the surface to which the exposed paddle of the amplifier is soldered also reduces the overall thermal resistance seen by the AD8000.

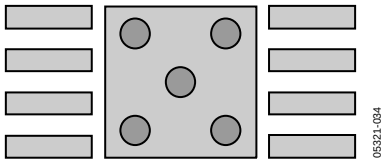

Figure 53. LFCSP Exposed Paddle Layout

PRINTED CIRCUIT BOARD LAYOUT

Laying out the printed circuit board (PCB) is usually the last step in the design process and often proves to be one of the most critical. A brilliant design can be rendered useless because of a poor or sloppy layout. Because the AD8000 can operate into the R_F frequency spectrum, high frequency board layout considerations must be taken into account. The PCB layout, signal routing, power supply bypassing, and grounding all must be addressed to ensure optimal performance.

SIGNAL ROUTING

The AD8000 LFCSP features the new low distortion pinout with a dedicated feedback pin and allows a compact layout. The dedicated feedback pin reduces the distance from the output to the inverting input, which greatly simplifies the routing of the feedback network.

To minimize parasitic inductances, use ground planes under high frequency signal traces. However, remove the ground plane from under the input and output pins to minimize the formation of parasitic capacitors, which degrades phase margin. Run signals that are susceptible to noise pickup on the internal layers of the PCB, which can provide maximum shielding.

POWER SUPPLY BYPASSING

Power supply bypassing is a critical aspect of the PCB design process. For best performance, the AD8000 power supply pins need to be properly bypassed.

A parallel connection of capacitors from each of the power supply pins to ground works best. Paralleling different values and sizes of capacitors helps to ensure that the power supply pins see a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier. Starting directly at the power supply pins, place the smallest value and sized component on the same side of the board as the amplifier, and as close as possible to the amplifier, and connected to the ground plane. Repeat this process for the next larger value capacitor. It is recommended for the AD8000 that a 0.1 µF ceramic 0508 case be used. The 0508 offers low series inductance and excellent high frequency performance. The 0.1 µF case provides low impedance at high frequencies. Place a 10 µF electrolytic capacitor in parallel with the 0.1 µF. The 10 µF capacitor provides low ac impedance at low frequencies. Smaller values of electrolytic capacitors can be used, depending on the circuit requirements. Additional smaller value capacitors help to provide a low impedance path for unwanted noise out to higher frequencies but are not always necessary.

Placement of the capacitor returns (grounds), where the capacitors enter into the ground plane, is also important. Returning the capacitors grounds close to the amplifier load is critical for distortion performance. Keeping the capacitors distance short, but equal from the load, is optimal for performance.

In some cases, bypassing between the two supplies can help to improve PSRR and to maintain distortion performance in crowded or difficult layouts. This is as another option to improve performance.

Minimizing the trace length and widening the trace from the capacitors to the amplifier reduce the trace inductance. A series inductance with the parallel capacitance can form a tank circuit, which can introduce high frequency ringing at the output. This additional inductance can also contribute to increased distortion due to high frequency compression at the output. Minimize the use of vias in the direct path to the amplifier power supply pins because vias can introduce parasitic inductance, which can lead to instability. When required, use multiple large diameter vias because this lowers the equivalent parasitic inductance.

GROUNDING

The use of ground and power planes is encouraged as a method of proving low impedance returns for power supply and signal currents. Ground and power planes can also help to reduce stray trace inductance and to provide a low thermal path for the amplifier. Do not use ground and power planes under any of the pins of the AD8000. The mounting pads and the ground or power planes can form a parasitic capacitance at the amplifiers input. Stray capacitance on the inverting input and the feedback resistor form a pole, which degrades the phase margin, leading to instability. Excessive stray capacitance on the output also forms a pole, which degrades phase margin.

OUTLINE DIMENSIONS

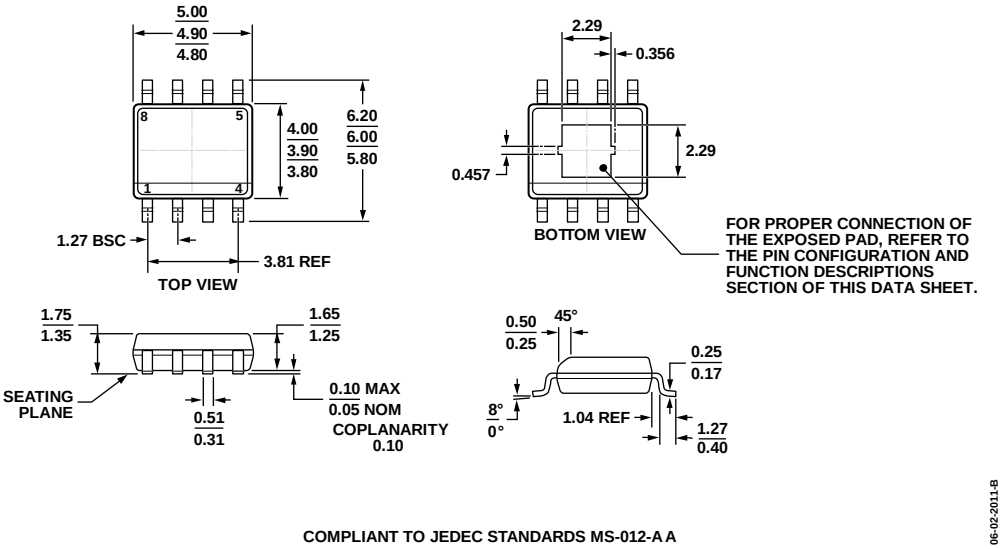

Figure 54. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters

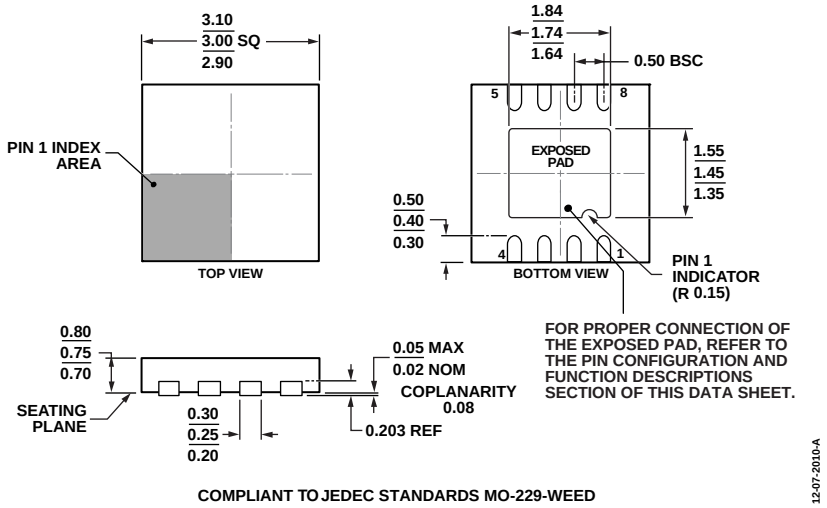

Figure 55. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
AD8000YRDZ	–40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1		1
AD8000YRDZ-REEL7	–40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1		1,000
AD8000YCPZ-R2	–40°C to +125°C	8-Lead LFCSP	CP-8-13	HNB	250
AD8000YCPZ-REEL	–40°C to +125°C	8-Lead LFCSP	CP-8-13	HNB	5,000
AD8000YCPZ-REEL7	–40°C to +125°C	8-Lead LFCSP	CP-8-13	HNB	1,500

[1] Z = RoHS Compliant Part.