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1/2016—Revision 0: Initial Version

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GENERAL DESCRIPTION

The AD7768/AD7768-4 are 8-channel and 4-channel, simultaneous sampling sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), respectively, with a Σ-Δ modulator and digital filter per channel, enabling synchronized sampling of ac and dc signals.

The AD7768/AD7768-4 achieve 108 dB dynamic range at a maximum input bandwidth of 110.8 kHz, combined with typical performance of ±2 ppm integral nonlinearity (INL), ±50 µV offset error, and ±30 ppm gain error.

The AD7768/AD7768-4 user can trade off input bandwidth, output data rate, and power dissipation, and select one of three power modes to optimize for noise targets and power consumption. The flexibility of the AD7768/AD7768-4 allows them to become reusable platforms for low power dc and high performance ac measurement modules.

The AD7768/AD7768-4 have three modes: fast mode (256 kSPS maximum, 110.8 kHz input bandwidth, 51.5 mW per channel), median mode (128 kSPS maximum, 55.4 kHz input bandwidth, 27.5 mW per channel) and low power mode (32 kSPS maximum, 13.8 kHz input bandwidth, 9.375 mW per channel).

The AD7768/AD7768-4 offer extensive digital filtering capabilities, such as a wideband, low ±0.005 dB pass-band ripple, antialiasing low-pass filter with sharp roll-off, and 105 dB attenuation at the Nyquist frequency.

Frequency domain measurements can use the wideband linear phase filter. This filter has a flat pass band (±0.005 dB ripple) from dc to 102.4 kHz at 256 kSPS, from dc to 51.2 kHz at 128 kSPS, or from dc to 12.8 kHz at 32 kSPS.

The AD7768/AD7768-4 also offer sinc response via a sinc5 filter, a low latency path for low bandwidth, and low noise measurements. The wideband and sinc5 filters can be selected and run on a per channel basis.

Within these filter options, the user can improve the dynamic range by selecting from decimation rates of ×32, ×64, ×128, ×256, ×512, and ×1024. The ability to vary the decimation filtering optimizes noise performance to the required input bandwidth.

Embedded analog functionality on each ADC channel makes design easier, such as a precharge buffer on each analog input that reduces analog input current and a precharge reference buffer per channel reduces input current and glitches on the reference input terminals.

The device operates with a 5 V AVDD1A and AVDD1B supply, a 2.25 V to 5.0 V AVDD2A and AVDD2B supply, and a 2.5 V to 3.3 V or 1.8 V IOVDD supply (see the 1.8 V IOVDD Operation section for specific requirements for operating at 1.8 V IOVDD).

The device requires an external reference; the absolute input reference voltage range is 1 V to AVDD1 − AVSS.

For the purposes of clarity in this data sheet, the AVDD1A and AVDD1B supplies are referred to as AVDD1 and the AVDD2A and AVDD2B supplies are referred to as AVDD2. For the negative supplies, AVSS refers to the AVSS1A, AVSS1B, AVSS2A, AVSS2B, and AVSS pins.

The specified operating temperature range is −40°C to +105°C. The device is housed in a 10 mm × 10 mm 64-lead LQFP package with a 12 mm × 12 mm printed circuit board (PCB) footprint.

Throughout this data sheet, multifunction pins, such as XTAL2/MCLK, are referred to either by the entire pin name or by a single function of the pin, for example MCLK, when only that function is relevant.

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SPECIFICATIONS

AVDD1A = AVDD1B = 4.5 V to 5.5 V, AVDD2A = AVDD2B = 2.0 V to 5.5 V, IOVDD = 2.25 V to 3.6 V, AVSS = DGND = 0 V, REFx+ = 4.096 V and REFx− = 0 V, MCLK = 32.768 MHz, analog input precharge buffers on, reference precharge buffers off, wideband filter, f_{CHOP} = $f_{MOD}/32$, T_A = −40°C to +105°C, unless otherwise noted. See Table 2 for specifications at 1.8 V IOVDD.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR), per Channel[1]	Fast mode	8		256	kSPS
	Median mode	4		128	kSPS
	Low power mode	1		32	kSPS
−3 dB Bandwidth (BW)	Fast mode, wideband filter			110.8	kHz
	Median mode, wideband filter			55.4	kHz
	Low power mode, wideband filter			13.8	kHz
Data Output Coding			Twos complement, MSB first		
No Missing Codes[2]		24			Bits
DYNAMIC PERFORMANCE					
Fast Mode	Decimation by 32, 256 kSPS ODR				
Dynamic Range	Shorted input, wideband filter	106.2	108		dB
Signal-to-Noise Ratio (SNR)	1 kHz, −0.5 dBFS, sine wave input				
	Sinc5 filter	109	111		dB
	Wideband filter	106	107.8		dB
Signal-to-Noise-and-Distortion Ratio (SINAD)	1 kHz, −0.5 dBFS, sine wave input	104.7	107.5		dB
Total Harmonic Distortion (THD)	1 kHz, −0.5 dBFS, sine wave input		−120	−107	dB
Spurious-Free Dynamic Range (SFDR)			128		dBc
Median Mode	Decimation by 32, 128 kHz ODR				
Dynamic Range	Shorted input, wideband filter	106.2	108		dB
SNR	Sinc5 filter, 1 kHz, −0.5 dBFS, sine wave input	109	111		dB
	Wideband filter, 1 kHz, −0.5 dBFS, sine wave input	106	107.8		dB
SINAD	1 kHz, −0.5 dBFS, sine wave input	105.8	107.5		dB
THD	1 kHz, −0.5 dBFS, sine wave input		−120	−113	dB
SFDR			128		dBc
Low Power Mode	Decimation by 32, 32 kHz ODR				
Dynamic Range	Shorted input, wideband filter	106.2	108		dB
SNR	Sinc5 filter, 1 kHz, −0.5 dBFS, sine wave input	109	111		dB
	Wideband filter, 1 kHz, −0.5 dBFS, sine wave input	106	107.8		dB
SINAD	1 kHz, −0.5 dBFS, sine wave input	105.8	107.5		dB
THD	1 kHz, −0.5 dBFS, sine wave input		−120	−113	dB
SFDR			128		dBc
INTERMODULATON DISTORTION (IMD)[3]	f_{INA} = 9.7 kHz, f_{INB} = 10.3 kHz				
	Second order		−125		dB
	Third order		−125		dB

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCURACY					
INL	Endpoint method		±2	±7	ppm of FSR
Offset Error[4]	DCLK frequency ≤ 24 MHz		±50	±115	µV
	24 MHz to 32.768 MHz DCLK frequency[2]		±75	±150	µV
Offset Error Drift	DCLK frequency ≤ 24 MHz		±250		nV/°C
	24 MHz to 32.768 MHz DCLK frequency		±750		nV/°C
Gain Error[4]	T_A = 25°C		±30	±70	ppm of FSR
Gain Drift vs. Temperature[2]			±0.5	±1	ppm/°C
VCM PIN					
Output	With respect to AVSS		(AVDD1 − AVSS)/2		V
Load Regulation	$\Delta V_{OUT}/\Delta I_L$		400		µV/mA
Voltage Regulation	Applies to the following VCM output options only: $V_{CM} = \Delta V_{OUT}/\Delta(AVDD1 - AVSS)/2$; V_{CM} = 1.65 V; and V_{CM} = 2.5 V		5		µV/V
Short-Circuit Current			30		mA
ANALOG INPUTS	See the Analog Inputs section				
Differential Input Voltage Range	$V_{REF} = (REFx+) - (REFx-)$	$-V_{REF}$		$+V_{REF}$	V
Input Common-Mode Range[2]		AVSS		AVDD1	V
Absolute Analog Input Voltage Limits[2]		AVSS		AVDD1	V
Analog Input Current					
Unbuffered	Differential component		±48		µA/V
	Common-mode component		±17		µA/V
Precharge Buffer On[5]			−20		µA
Input Current Drift					
Unbuffered			±5		nA/V/°C
Precharge Buffer On			±31		nA/°C
EXTERNAL REFERENCE					
Reference Voltage	$V_{REF} = (REFx+) - (REFx-)$	1		AVDD1 − AVSS	V
Absolute Reference Voltage Limits[2]	Precharge reference buffers off	AVSS − 0.05		AVDD1 + 0.05	V
	Precharge reference buffer on	AVSS		AVDD1	V
Average Reference Current	Fast mode; see Figure 63				
	Precharge reference buffers off		±72		µA/V/channel
	Precharge reference buffers on		±16		µA/V/channel
Average Reference Current Drift	Fast mode; see Figure 63				
	Precharge reference buffers off		±1.7		nA/V/°C
	Precharge reference buffers on		±49		nA/V/°C
Common-Mode Rejection			95		dB
DIGITAL FILTER RESPONSE					
Low Ripple Wideband Filter	FILTER = 0				
Decimation Rate	Up to six selectable decimation rates	32		1024	
Group Delay	Latency		34/ODR		sec
Settling Time	Complete settling		68/ODR		sec
Pass-Band Ripple[2]	From dc to 102.4 kHz at 256 kSPS			±0.005	dB
Pass Band	±0.005 dB bandwidth		0.4 × ODR		Hz
	−0.1 dB bandwidth		0.409 × ODR		Hz
	−3 dB bandwidth		0.433 × ODR		Hz
Stop Band Frequency	Attenuation > 105 dB		0.499 × ODR		Hz
Stop Band Attenuation			105		dB

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Sinc5 Filter	FILTER = 1				
Decimation Rate	Up to six selectable decimation rates	32		1024	
Group Delay	Latency		3/ODR		sec
Settling Time	Complete settling		7/ODR		sec
Pass Band	−3 dB bandwidth		0.204 × ODR		Hz
REJECTION					
AC Power Supply Rejection Ratio (PSRR)	V_{IN} = 0.1 V, AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 2.5 V				
AVDD1			90		dB
AVDD2			100		dB
IOVDD			75		dB
DC PSRR	V_{IN} = 1 V				
AVDD1			100		dB
AVDD2			118		dB
IOVDD			90		dB
Analog Input Common-Mode Rejection Ratio (CMRR)					
DC	V_{IN} = 0.1 V	95			dB
AC	Up to 10 kHz		95		dB
Crosstalk	−0.5 dBFS input on adjacent channels		−120		dB
CLOCK	See the Clocking Selections section for performance functionality				
Crystal Frequency		8	32.768	34	MHz
External Clock (MCLK)			32.768		MHz
Duty Cycle			50:50		%
MCLK Pulse Width[2]					
Logic Low		12.2			ns
Logic High		12.2			ns
CMOS Clock Input Voltage	See the Logic Inputs parameter				
High, V_{INH}					
Low, V_{INL}					
LVDS Clock[2]	R_L = 100 Ω				
Differential Input Voltage		100		650	mV
Common-Mode Input Voltage		800		1575	mV
Absolute Input Voltage				1.88	V
ADC RESET[2]					
ADC Start-Up Time After Reset[6]	Time to first $\overline{DRDY}$, fast mode, decimation by 32		1.58	1.66	ms
Minimum $\overline{RESET}$ Low Pulse Width	t_{MCLK} = 1/MCLK	2 × t_{MCLK}			
LOGIC INPUTS					
Input Voltage[2]					
High, V_{INH}		0.65 × IOVDD			V
Low, V_{INL}				0.7	V
Hysteresis[2]		0.04		0.09	V
Leakage Current		−10	+0.03	+10	µA
	$\overline{RESET}$ pin[7]	−10		+10	µA

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC OUTPUTS	See Table 2 for 1.8 V operation				
Output Voltage[2]					
High, V_{OH}	I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Low, V_{OL}	I_{SINK} = 400 µA			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
SYSTEM CALIBRATION[2]					
Full-Scale Calibration Limit				1.05 × V_{REF}	V
Zero-Scale Calibration Limit		−1.05 × V_{REF}			V
Input Span		0.4 × V_{REF}		2.1 × V_{REF}	V
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD1 − AVSS		4.5	5.0	5.5	V
AVDD2 − AVSS		2.0	2.25 to 5.0	5.5	V
AVSS − DGND		−2.75		0	V
IOVDD − DGND	See Table 2 for 1.8 V operation	2.25	2.5 to 3.3	3.6	V
POWER SUPPLY CURRENTS	Maximum output data rate, CMOS MCLK, eight DOUTx signals, all supplies at maximum voltages, all channels in Channel Mode A				
AD7768	Eight channels active				
Fast Mode					
AVDD1 Current	Precharge reference buffers off/on		36/57.5	40/64	mA
AVDD2 Current			37.5	40	mA
IOVDD Current	Wideband filter		63	67	mA
	Sinc5 filter		27	29	mA
Median Mode					
AVDD1 Current	Precharge reference buffers off/on		18.5/29	20.5/32.5	mA
AVDD2 Current			21.3	23	mA
IOVDD Current	Wideband filter		34	37	mA
	Sinc5 filter		16	18	mA
Low Power Mode					
AVDD1 Current	Precharge reference buffers off/on		5.1/8	5.8/9	mA
AVDD2 Current			9.3	10.1	mA
IOVDD Current	Wideband filter		12.5	13.7	mA
	Sinc5 filter		8	9	mA
AD7768-4	Four channels active				
Fast Mode					
AVDD1 Current	Precharge reference buffers off/on		18.2/28.8	20.3/32.5	mA
AVDD2 Current			18.8	20.3	mA
IOVDD Current	Wideband filter[2]		43.5	46.8	mA
	Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[8]		37	40	mA
	Sinc5 filter[2]		17	18.6	mA
Median Mode					
AVDD1 Current	Reference precharge buffers off/on		9.3/14.7	10.5/16.6	mA
AVDD2 Current			10.7	11.7	mA
IOVDD Current	Wideband filter[2]		24.4	26.4	mA
	Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[8]		21	23	mA
	Sinc5 filter[2]		11	12.3	mA

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Low Power Mode					
AVDD1 Current	Precharge reference buffers off/on		2.7/4.1	3.1/4.7	mA
AVDD2 Current			4.7	5.3	mA
IOVDD Current	Wideband filter[2]		10	11.1	mA
	Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[8]		9	10	mA
	Sinc5 filter[2]		6.5	7.6	mA
AD7768 and AD7768-4—Two Channels Active[2]	Serial peripheral interface (SPI) control mode only; see the Channel Standby section for details on disabling channels				
Fast Mode					
AVDD1 Current	Precharge reference buffers off/on		9.3/14.7	10.5/16.6	mA
AVDD2 Current			9.5	10.5	mA
IOVDD Current	Wideband filter		33.7	36.3	mA
	Wideband filter; disabled channels in Channel Mode A, and set to sinc5 filter mode[8]		23.4	25.5	mA
	Sinc5 filter		11.9	13.3	mA
Median Mode					
AVDD1 Current	Precharge reference buffers off/on		4.8/7.5	5.5/8.6	mA
AVDD2 Current			5.5	6.2	mA
IOVDD Current	Wideband filter		19.4	21.1	mA
	Wideband filter; disabled channels in Channel Mode A, and set to sinc5 filter mode[8]		14.1	15.5	mA
	Sinc5 filter		8.5	9.6	mA
Low Power Mode					
AVDD1 Current	Precharge reference buffers off/on		1.52/2.2	1.77/2.6	mA
AVDD2 Current			2.4	3	mA
IOVDD Current	Wideband filter		8.6	9.7	mA
	Wideband filter; disabled channels in Channel Mode A, and set to sinc5 filter mode[8]		7.2	8	mA
	Sinc5 filter		5.8	6.7	mA
Standby Mode	All channels disabled (sinc5 filter enabled)		6.5	8	mA
Sleep Mode[2]	Full power-down (SPI control mode only)		0.73	1.2	mA
Crystal Excitation Current	Extra current in IOVDD when using an external crystal compared to using the CMOS MCLK		540		µA
POWER DISSIPATION	External CMOS MCLK, all channels active, MCLK = 32.768 MHz, all channels in Channel Mode A except where otherwise specified				
Full Operating Mode	Analog precharge buffers on				
AD7768					
Wideband Filter					
Fast Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2]		412	446	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2]		600	645	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		631	681	mW

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Median Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2]		220	240	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2]		320	345	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		341	372	mW
Low Power Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2]		75	85	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2]		107	118	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		124	137	mW
Sinc5 Filter					
Fast Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2]		325	355	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2]		475	525	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		501	545	mW
Median Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2]		175	195	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2]		260	285	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		277	304	mW
Low Power Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off[2]		65	72	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on[2]		95	105	mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		108	120	mW
AD7768-4					
Wideband Filter					
Fast Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		235		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		336		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off[2]		360	392	mW
	SPI mode only; AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off, Channel Mode A set to sinc5 filter[8]		337	368	mW
Median Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		127		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		181		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off[2]		198	218	mW
	SPI mode only; AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off, Channel Mode A set to sinc5 filter[8]		186	205	mW

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Low Power Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		49		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		66		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off[2]		77	87	mW
	SPI mode only; AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off, Channel Mode A set to sinc5 filter[8]		73	83	mW
Sinc5 Filter					
Fast Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		168		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		248		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		265	291	mW
Median Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		94		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		137		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		150	167	mW
Low Power Mode	AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, precharge reference buffers off		40		mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V, precharge reference buffers on		55		mW
	AVDD1 = 5.5 V, AVDD2 = 5.5 V, IOVDD = 3.6 V, precharge reference buffers off		64	74	mW
Standby Mode	All channels disabled (sinc5 filter enabled), AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V[2]			18	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V[2]			26	mW
	AVDD1 = AVDD2 = 5.5 V, IOVDD = 3.6 V			29	mW
Sleep Mode[2]	Full power-down (SPI control mode), AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V		1.8	4	mW
	AVDD1 = 5 V, AVDD2 = IOVDD = 3.3 V		2.5	5	mW
	AVDD1 = AVDD2 = 5.5 V, IOVDD = 3.6 V		2.7	6.5	mW

[1] The output data rate ranges refer to the programmable decimation rates available on the AD7768/AD7668-4 for a fixed MCLK rate of 32.768 MHz. Varying MCLK rates allow users a wider variation of ODR.
[2] These specifications are not production tested but are supported by characterization data at initial product release.
[3] See the Terminology section for more information about the fa and fb input frequencies.
[4] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[5] −25 µA is measured when the analog input is close to either the AVDD1 or AVSS rail. The input current reduces as the common-mode voltage approaches (AVDD1 − AVSS)/2. The analog input current scales with the MCLK frequency and device power mode. See Figure 85 and Figure 86 for more details on how the analog input current scales with input voltage.
[6] For lower MCLK rates or higher decimation rates, use Table 28 and Table 29 to calculate any additional delay before the first $\overline{\text{DRDY}}$ pulse.
[7] The $\overline{\text{RESET}}$ pin has an internal pull-up device to IOVDD.
[8] Configuring Channel Mode A to the sinc5 filter and/or assigning disabled channels to Channel Mode A allows a lower power consumption to be achieved. To do this, the user must be operating in SPI control mode because it requires assigning channels to different channel modes (only possible in SPI control mode). If using pin control mode, all channels, whether active or in standby, are assigned to the same channel group and use the same filter type. This means that, in pin control mode, a higher current consumption is seen from disabled channels than can be achieved in SPI mode. See the Channel Modes section for more details.

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1.8 V IOVDD SPECIFICATIONS

AVDD1A = AVDD1B = 4.5 V to 5.5 V, AVDD2A = AVDD2B = 2.0 V to 5.5 V, IOVDD = 1.72 V to 1.88 V, AVSS = DGND = 0 V, REFx+ = 4.096 V and REFx− = 0 V, MCLK = 32.76 8 MHz, analog precharge buffers on, reference precharge buffers off, wideband filter, f_{CHOP} = $f_{MOD}/32$, T_A = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE	For dynamic range and SNR across all decimation rates, see Table 12 and Table 13				
Fast Mode	Decimation by 32, 256 kSPS ODR				
Dynamic Range	Shorted input, wideband filter	106.2	108		dB
SNR	Sinc5 filter, 1 kHz, −0.5 dBFS, sine wave input	109	111		dB
	Wideband filter, 1 kHz, −0.5 dBFS, sine wave input	106	107.8		dB
SINAD[1]	1 kHz, −0.5 dBFS, sine wave input	103.8	107.5		dB
THD	1 kHz, −0.5 dBFS, sine wave input		−120	−107	dB
SFDR			128		dBc
Median Mode	Decimation by 32, 128 kHz ODR				
Dynamic Range	Shorted input, wideband filter	106.2	108		dB
SNR	1 kHz, −0.5 dBFS, sine wave input				
	Sinc5 filter	109	111		dB
	Wideband filter	106	107.8		dB
SINAD	1 kHz, −0.5 dBFS, sine wave input	105.8	107.5		dB
THD	1 kHz, −0.5 dBFS, sine wave input		−120	−113	dB
SFDR			128		dBc
Low Power Mode	Decimation by 32, 32 kHz ODR				
Dynamic Range	Shorted input, wideband filter	106.2	108		dB
SNR	Sinc5 filter, 1 kHz, −0.5 dBFS, sine wave input	109	111		dB
	Wideband filter, 1 kHz, −0.5 dBFS, sine wave input	106	107.8		dB
SINAD	1 kHz, −0.5 dBFS, sine wave input	105.8	107.5		dB
THD	1 kHz, −0.5 dBFS, sine wave input		−120	−113	dB
SFDR			128		dBc
ACCURACY[1]					
INL	Endpoint method		±2	±7	ppm of FSR
Offset Error[2]	DCLK frequency ≤ 24 MHz		±50	±115	µV
	24 MHz to 32.768 MHz DCLK frequency		±75	±170	µV
Offset Error Drift	DCLK frequency ≤ 24 MHz		±250		nV/°C
	24 MHz to 32.768 MHz DCLK frequency		±750		nV/°C
Gain Error[2]	T_A = 25°C		±60	±120	ppm/FSR
Gain Drift vs. Temperature			±0.5	±2	ppm/°C
LOGIC INPUTS					
Input Voltage[1]					
High, V_{INH}		0.65 × IOVDD			V
Low, V_{INL}				0.4	V
Hysteresis[1]		0.04		0.2	V
Leakage Current		−10	+0.03	+10	µA
	$\overline{\text{RESET}}$ pin	−10		+10	µA
LOGIC OUTPUTS					
Output Voltage[1]					
High, V_{OH}	I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Low, V_{OL}	I_{SINK} = 400 µA			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD1 – AVSS		4.5	5.0	5.5	V
AVDD2 – AVSS		2.0	2.25 to 5.0	5.5	V
AVSS – DGND		−2.75		0	V
IOVDD – DGND	DREGCAP shorted to IOVDD	1.72	1.8	1.88	V
POWER SUPPLY CURRENTS[1]	Maximum output data rate, CMOS MCLK, eight DOUTx signals, all supplies at maximum voltages, all channels in Channel Mode A except where otherwise specified				
AD7768	Eight channels active				
Fast Mode					
AVDD1 Current	Reference precharge buffers off/on		36/57.5	40/64	mA
AVDD2 Current			37.5	40	mA
IOVDD Current	Wideband filter		63	69	mA
	Sinc5 filter		26	28.4	mA
Median Mode					
AVDD1 Current	Reference precharge buffers off/on		18.5/29	20.5/32.5	mA
AVDD2 Current			21.3	23	mA
IOVDD Current	Wideband filter		34	36.8	mA
	Sinc5 filter		15	16.8	mA
Low Power Mode					
AVDD1 Current	Reference precharge buffers off/on		5.1/8	5.8/9	mA
AVDD2 Current			9.3	10.1	mA
IOVDD Current	Wideband filter		11.6	12.9	mA
	Sinc5 filter		7	8.1	mA
AD7768-4	Four channels active				
Fast Mode					
AVDD1 Current	Reference precharge buffers off/on		18.2/28.8	20.3/32.5	mA
AVDD2 Current			18.8	20.3	mA
IOVDD Current	Wideband filter		43.9	47.7	mA
	Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[3]		36.8	41	mA
	Sinc5 filter		16	17.7	mA
Median Mode					
AVDD1 Current	Reference precharge buffers off/on		9.3/14.7	10.5/16.6	mA
AVDD2 Current			10.7	11.7	mA
IOVDD Current	Wideband filter		24	26.1	mA
	Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[3]		20.4	22.7	mA
	Sinc5 filter		10	11.3	mA
Low Power Mode					
AVDD1 Current	Reference precharge buffers off/on		2.7/4.1	3.1/4.7	mA
AVDD2 Current			4.7	5.3	mA
IOVDD Current	Wideband filter		9	10.2	mA
	Wideband filter, SPI mode only; Channel Mode A set to sinc5 filter[3]		8.1	9.2	mA
	Sinc5 filter		5.5	6.5	mA

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AD7768 and AD7768-4—Two Channels Active	SPI control mode only; see the Channel Standby section for details on disabling channels				
Fast Mode					
AVDD1 Current	Reference precharge buffers off/on		9.3/14.7	10.5/16.6	mA
AVDD2 Current			9.5	10.5	mA
IOVDD Current	Wideband filter		33.8	36.7	mA
	Wideband filter, SPI mode only; disabled channels in Channel Mode A, and set to sinc5 filter[3]		23.1	25.6	mA
	Sinc5 filter		11	12.3	mA
Median Mode					
AVDD1 Current	Reference precharge buffers off/on		4.8/7.5	5.5/8.6	mA
AVDD2 Current			5.5	6.2	mA
IOVDD Current	Wideband filter		18.9	20.6	mA
	Wideband filter, SPI mode only; disabled channels in Channel Mode A, and set to sinc5 filter[3]		13.4	15.1	mA
	Sinc5 filter		7.4	8.6	mA
Low Power Mode					
AVDD1 Current	Precharge reference buffers off/on		1.52/2.2	1.77/2.6	mA
AVDD2 Current			2.4	3	mA
IOVDD Current	Wideband filter		7.6	8.8	mA
	Wideband filter, SPI mode only; disabled channels in Channel Mode A, and set to sinc5 filter[3]		6.3	7.2	mA
	Sinc5 filter		4.8	5.8	mA
Standby Mode	All channels disabled (sinc5 filter enabled)		6.5	8	mA
Sleep Mode	Full power-down (SPI control mode)		0.73	1.2	mA
Crystal Excitation Current	Extra current in IOVDD when using an external crystal compared to using the CMOS MCLK		540		µA
POWER DISSIPATION[1]	External CMOS MCLK, all channels active, AVDD1 = AVDD2 = 5.5 V, IOVDD = 1.88 V, MCLK = 32.768 MHz, all channels in Channel Mode A except where otherwise noted				
Full Operating Mode	Analog precharge buffers on				
AD7768	Eight channels active				
Wideband Filter					
Fast Mode	Reference precharge buffers off		524	571	mW
	Reference precharge buffers on		638	704	mW
Median Mode	Reference precharge buffers off		284	309	mW
	Reference precharge buffers on		342	375	mW
Low Power Mode	Reference precharge buffers off		98.5	109	mW
	Reference precharge buffers on		118	130	mW
Sinc5 Filter					
Fast Mode	Reference precharge buffers off		455	495	mW
Median Mode	Reference precharge buffers off		248	271	mW
Low Power Mode	Reference precharge buffers off		94	105	mW

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Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
AD7768-4	Four channels active				
Wideband Filter					
Fast Mode	Reference precharge buffers off		287	314	mW
	Reference precharge buffers on		345	381	mW
Median Mode	Reference precharge buffers off		156	172	mW
	Reference precharge buffers on		185	206	mW
Low Power Mode	Reference precharge buffers off		58	66	mW
	Reference precharge buffers on		66	75	mW
Sinc5 Filter					
Fast Mode	Reference precharge buffers off		234	257	mW
Median Mode	Reference precharge buffers off		129	144	mW
Low Power Mode	Reference precharge buffers off		51	59	mW
Standby Mode	All channels disabled (sinc5 filter enabled)			17	mW
Sleep Mode	Full power-down (SPI control mode)		1.5	4.5	mW

[1] These specifications are not production tested but are supported by characterization data at initial product release.
[2] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[3] This configuration of setting Channel Mode A to the sinc5 filter and/or assigning disabled channels to Channel Mode A allows a lower power consumption to be achieved due to the disabling of internal clocks on the disabled only and sinc5 only channel modes. This configuration requires assigning sinc5 and wideband filters to different channels, or channel modes, and is only available in SPI control mode. In pin control mode, all channels, whether active or in standby, effectively use the same channel mode. See the Channel Modes section for more details.

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TIMING SPECIFICATIONS

AVDD1A = AVDD1B = 5 V, AVDD2A = AVDD2B = 5 V, IOVDD = 2.25 V to 3.6 V, Input Logic 0 = DGND, Input Logic 1 = IOVDD; C_{LOAD} = 10 pF on the DCLK pin, C_{LOAD} = 20 pF on the other digital outputs; REFx+ = 4.096 V, T_A = −40°C to +105°C. See Table 5 and Table 6 for timing specifications at 1.8 V IOVDD.

Table 3. Data Interface Timing[1]

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Master clock		1.15		34	MHz
f_{MOD}	Modulator frequency	Fast mode		MCLK/4		Hz
		Median mode		MCLK/8		Hz
		Low power mode		MCLK/32		Hz
t_1	$\overline{DRDY}$ high time	$t_{DCLK} = t_8 + t_9$	t_{DCLK} − 10%	28		ns
t_2	DCLK rising edge to $\overline{DRDY}$ rising edge				2	ns
t_3	DCLK rising to $\overline{DRDY}$ falling		−3.5		0	ns
t_4	DCLK rise to DOUTx valid				1.5	ns
t_5	DCLK rise to DOUTx invalid		−3			ns
t_6	DOUTx valid to DCLK falling		9.5	$t_{DCLK}/2$		ns
t_7	DCLK falling edge to DOUTx invalid		9.5	$t_{DCLK}/2$		ns
t_8	DCLK high time, DCLK = MCLK/1	50:50 CMOS clock	$t_{DCLK}/2$	$t_{DCLK}/2$	$(t_{DCLK}/2) + 5$	ns
	t_{8a} = DCLK = MCLK/2	t_{MCLK} = 1/MCLK		t_{MCLK}		ns
	t_{8b} = DCLK = MCLK/4			2 × t_{MCLK}		ns
	t_{8c} = DCLK = MCLK/8			4 × t_{MCLK}		ns
t_9	DCLK low time DCLK = MCLK/1	50:50 CMOS clock	$(t_{DCLK}/2) - 5$	$t_{MCLK}/2$	$t_{DCLK}/2$	ns
	t_{9a} = DCLK = MCLK/2			t_{MCLK}		ns
	t_{9b} = DCLK = MCLK/4			2 × t_{MCLK}		ns
	t_{9c} = DCLK = MCLK/8			4 × t_{MCLK}		ns
t_{10}	MCLK rising to DCLK rising	CMOS clock			30	ns
t_{11}	Setup time (daisy-chain inputs)	DOUT6 and DOUT7 on the AD7768, DIN on the AD7768-4	14			ns
t_{12}	Hold time (daisy-chain inputs)	DOUT6 and DOUT7 on the AD7768, DIN on the AD7768-4	0			ns
t_{13}	$\overline{START}$ low time		1 × t_{MCLK}			ns
t_{14}	MCLK to $\overline{SYNC_OUT}$ valid	CMOS clock				
		$\overline{SYNC_OUT}$ RETIME_EN bit disabled; measured from falling edge of MCLK	4.5		22	ns
		$\overline{SYNC_OUT}$ RETIME_EN bit enabled; measured from rising edge of MCLK	9.5		27.5	ns
t_{15}	$\overline{SYNC_IN}$ setup time	CMOS clock	0			ns
t_{16}	$\overline{SYNC_IN}$ hold time	CMOS clock	10			ns

[1] These specifications are not production tested but are supported by characterization data at initial product release.

Table 4. SPI Control Interface Timing[1]

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{17}	SCLK period		100			ns
t_{18}	$\overline{CS}$ falling edge to SCLK rising edge		26.5			ns
t_{19}	SCLK falling edge to $\overline{CS}$ rising edge		27			ns
t_{20}	$\overline{CS}$ falling edge to data output enable		22.5		40.5	ns
t_{21}	SCLK high time		20	50		ns
t_{22}	SCLK low time		20	50		ns
t_{23}	SCLK falling edge to SDO valid				15	ns
t_{24}	SDO hold time after SCLK falling		7			ns
t_{25}	SDI setup time		0			ns
t_{26}	SDI hold time		6			ns
t_{27}	SCLK enable time		0			ns

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Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{28}	SCLK disable time		0			ns
t_{29}	$\overline{CS}$ high time		10			ns
t_{30}	$\overline{CS}$ low time	f_{MOD} = MCLK/4	1.1 × t_{MCLK}			ns
		f_{MOD} = MCLK/8	2.2 × t_{MCLK}			ns
		f_{MOD} = MCLK/32	8.8 × t_{MCLK}			ns

[1] These specifications are not production tested but are supported by characterization data at initial product release.

1.8 V IOVDD TIMING SPECIFICATIONS

AVDD1A = AVDD1B = 5 V, AVDD2A = AVDD2B = 5 V, IOVDD = 1.72 V to 1.88 V (DREGCAP tied to IOVDD), Input Logic 0 = DGND, Input Logic 1 = IOVDD, C_{LOAD} = 10 pF on DCLK pin, C_{LOAD} = 20 pF on other digital outputs, T_A = −40°C to +105°C.

Table 5. Data Interface Timing[1]

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
MCLK	Master clock		1.15		34	MHz
f_{MOD}	Modulator frequency	Fast mode		MCLK/4		Hz
		Median mode		MCLK/8		Hz
		Low power mode		MCLK/32		Hz
t_1	$\overline{DRDY}$ high time		t_{DCLK} − 10%	28		ns
t_2	DCLK rising edge to $\overline{DRDY}$ rising edge				2	ns
t_3	DCLK rising to $\overline{DRDY}$ falling		−4.5		0	ns
t_4	DCLK rise to DOUTx valid				2.0	ns
t_5	DCLK rise to DOUTx invalid		−4			ns
t_6	DOUTx valid to DCLK falling		8.5	t_{DCLK}/2		ns
t_7	DCLK falling edge to DOUTx invalid		8.5	t_{DCLK}/2		ns
t_8	DCLK high time, DCLK = MCLK/1	50:50 CMOS clock	t_{DCLK}/2	t_{DCLK}/2	(t_{DCLK}/2) + 5	ns
	t_{8a} = DCLK = MCLK/2			t_{MCLK}		ns
	t_{8b} = DCLK = MCLK/4			2 × t_{MCLK}		ns
	t_{8c} = DCLK = MCLK/8			4 × t_{MCLK}		ns
t_9	DCLK low time DCLK=MCLK/1	50:50 CMOS clock	(t_{DCLK}/2) − 5	t_{MCLK}/2	(t_{DCLK}/2	ns
	t_{9a} = DCLK = MCLK/2			t_{MCLK}		ns
	t_{9b} = DCLK = MCLK/4			2 × t_{MCLK}		ns
	t_{9c} = DCLK = MCLK/8			4 × t_{MCLK}		ns
t_{10}	MCLK rising to DCLK rising	CMOS clock			37	ns
t_{11}	Setup time (daisy-chain inputs)	DOUT6 and DOUT7 on the AD7768, DIN on the AD7768-4	14			ns
t_{12}	Hold time (daisy-chain inputs)	DOUT6 and DOUT7 on the AD7768, DIN on the AD7768-4	0			ns
t_{13}	$\overline{START}$ low time		1 × t_{MCLK}			ns
t_{14}	MCLK to $\overline{SYNC_OUT}$ valid	CMOS clock				
		$\overline{SYNC_OUT}$ RETIME_EN bit disabled; measured from falling edge of MCLK	10		31	ns
		$\overline{SYNC_OUT}$ RETIME_EN bit enabled; measured from rising edge of MCLK	15		37	ns
t_{15}	$\overline{SYNC_IN}$ setup time	CMOS clock	0			ns
t_{16}	$\overline{SYNC_IN}$ hold time	CMOS clock	11			ns

[1] These specifications are not production tested but are supported by characterization data at initial product release.

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Table 6. SPI Control Interface Timing[1]

Parameter	Description	Test Conditions/Comments	Min	Typ	Max	Unit
t_{17}	SCLK period		100			ns
t_{18}	$\overline{CS}$ falling edge to SCLK rising edge		31.5			ns
t_{19}	SCLK falling edge to $\overline{CS}$ rising edge		30			ns
t_{20}	$\overline{CS}$ falling edge to data output enable		29		54	ns
t_{21}	SCLK high time		20	50		ns
t_{22}	SCLK low time		20	50		ns
t_{23}	SCLK falling edge to SDO valid				16	ns
t_{24}	SDO hold time after SCLK falling		7			ns
t_{25}	SDI setup time		0			ns
t_{26}	SDI hold time		10			ns
t_{27}	SCLK enable time		0			ns
t_{28}	SCLK disable time		0			ns
t_{29}	$\overline{CS}$ high time		10			ns
t_{30}	$\overline{CS}$ low time	f_{MOD} = MCLK/4	1.1 × t_{MCLK}			ns
		f_{MOD} = MCLK/8	2.2 × t_{MCLK}			ns
		f_{MOD} = MCLK/32	8.8 × t_{MCLK}			ns

[1] These specifications are not production tested but are supported by characterization data at initial product release.

Timing Diagrams

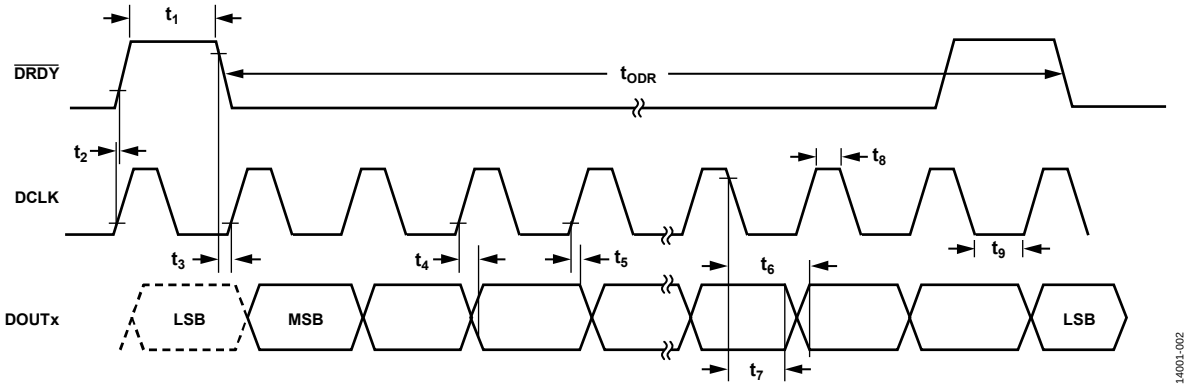

Figure 2. Data Interface Timing Diagram

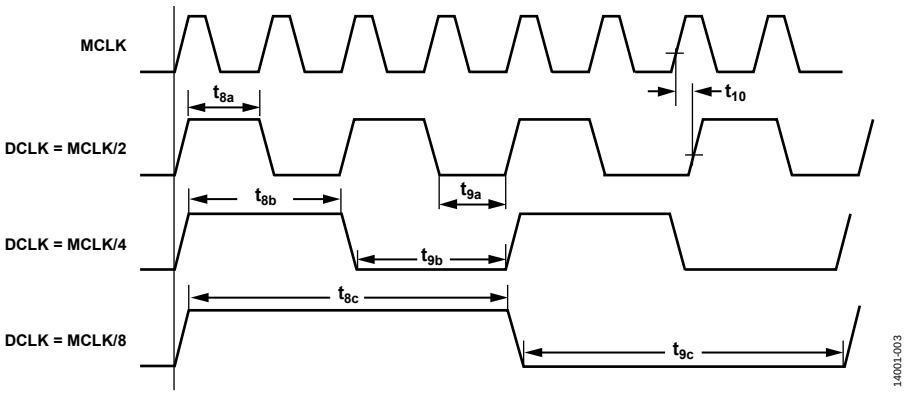

Figure 3. MCLK to DCLK Divider Timing Diagram

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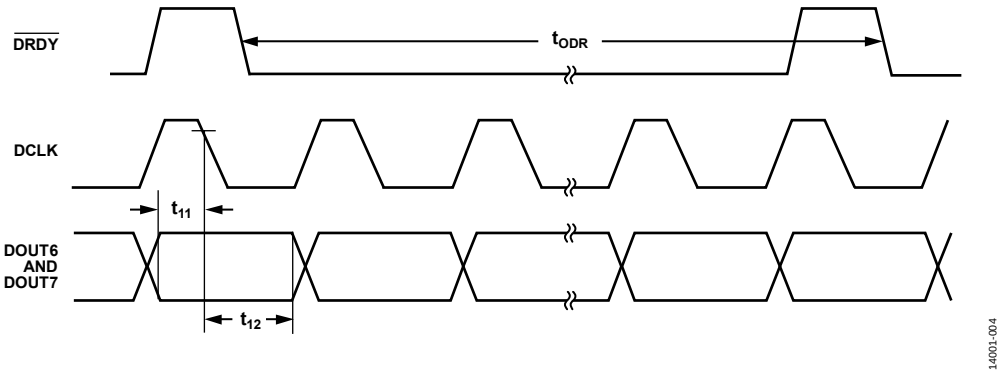

Figure 4. Daisy-Chain Setup and Hold Timing Diagram

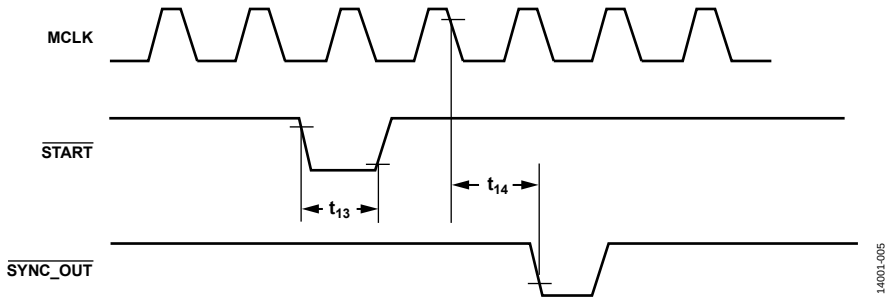

Figure 5. Asynchronous START and SYNC_OUT Timing Diagram

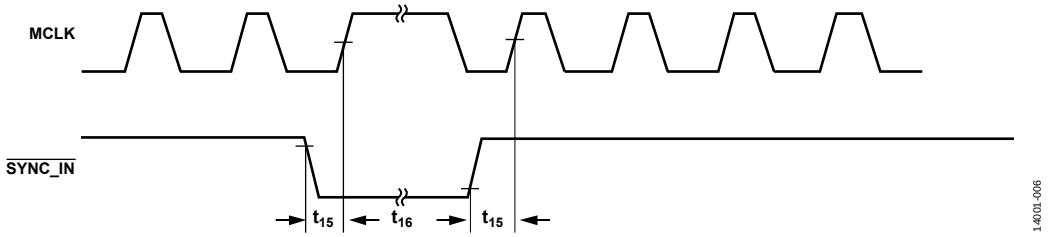

Figure 6. Synchronous SYNC_IN Pulse Timing Diagram

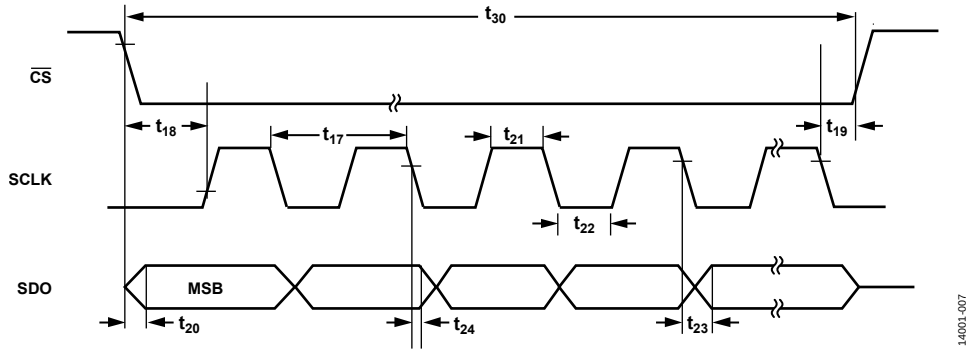

Figure 7. SPI Serial Read Timing Diagram

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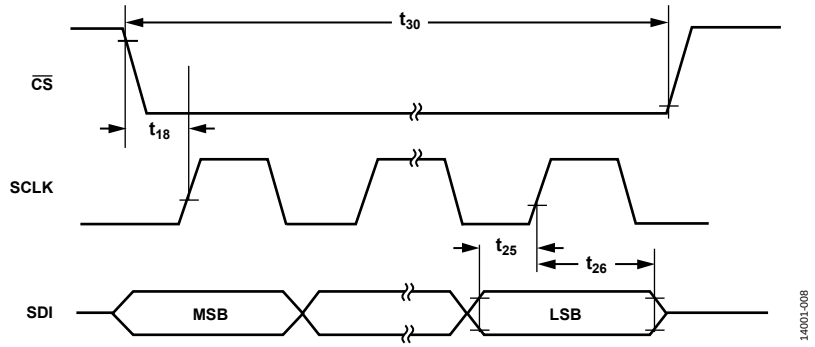

Figure 8. SPI Serial Write Timing Diagram

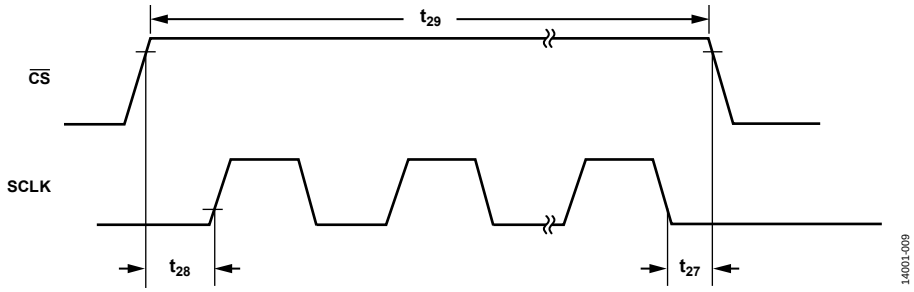

Figure 9. SCLK Enable and Disable Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD1, AVDD2 to AVSS[1]	−0.3 V to +6.5 V
AVDD1 to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
IOVDD, DREGCAP to DGND (IOVDD Tied to DREGCAP for 1.8 V Operation)	−0.3 V to +2.25 V
IOVDD to AVSS	−0.3 V to +7.5 V
AVSS to DGND	−3.25 V to +0.3 V
Analog Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Reference Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature, Soldering Reflow (10 sec to 30 sec)	260°C
Maximum Junction Temperature	150°C
Maximum Package Classification Temperature	260°C

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 8. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit	JEDEC Board Layers
ST-64-2	38	9.2	°C/W	2P2S[1]

[1] 2P2S is a JEDEC standard PCB configuration per JEDEC Standard JESD51-7.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

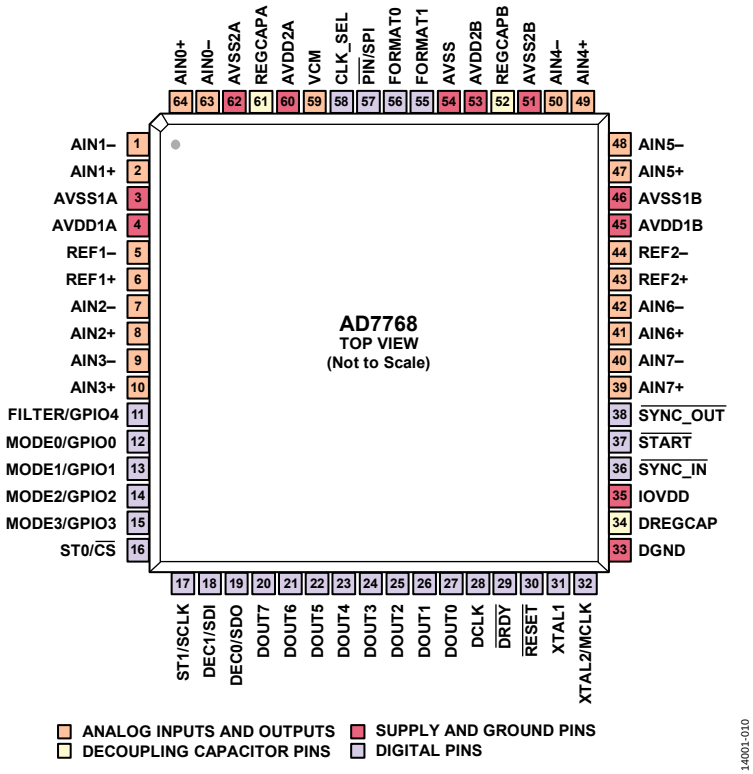

Figure 10. AD7768 Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	AIN1−	AI	Negative Analog Input to ADC Channel 1.
2	AIN1+	AI	Positive Analog Input to ADC Channel 1.
3	AVSS1A	P	Negative Analog Supply. This pin is nominally 0 V.
4	AVDD1A	P	Analog Supply Voltage, 5 V ± 10% with Respect to AVSS.
5	REF1−	AI	Reference Input, Negative. REF1− is the negative reference terminal for Channel 0 to Channel 3. The REF1− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3.
6	REF1+	AI	Reference Input, Positive. REF1+ is the positive reference terminal for Channel 0 to Channel 3. The REF1+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external differential reference voltage between REF1+ and REF1− in the range from 1 V to |AVDD1 − AVSS|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3.
7	AIN2−	AI	Negative Analog Input to ADC Channel 2.
8	AIN2+	AI	Positive Analog Input to ADC Channel 2.
9	AIN3−	AI	Negative Analog Input to ADC Channel 3.
10	AIN3+	AI	Positive Analog Input to ADC Channel 3.
11	FILTER/GPIO4	DI/O	Filter Select/General-Purpose Input/Output 4. In pin control mode, this pin selects the filter type. Set this pin to Logic 1 for the sinc5 filter. This sinc5 filter is a low latency filter, and is best for dc applications or when a user has specialized postfiltering implemented off chip. Set this pin to Logic 0 for the wideband low ripple filter response. This filter has a steep transition band and 105 dB stop band attenuation. Full attenuation at Nyquist (ODR/2) means that no aliasing occurs at ODR/2 out to the first chopping zone. In SPI control mode, this pin can be used as a general-purpose input/output (GPIO4). For further information on GPIO configuration, see the GPIO Functionality section. In SPI control mode, when not used as a GPIO pin and when a crystal is used as the clock source, this pin must be set to 1.

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Pin No.	Mnemonic	Type[1]	Description
12, 13, 14, 15	MODE0/GPIO0, MODE1/GPIO1, MODE2/GPIO2, MODE3/GPIO3	DI/DI/O	Mode Selection/General-Purpose Input/Output Pin 0 to Pin 3. In pin control mode, the MODEx pins set the mode of operation for all ADC channels, controlling power consumption, DCLK frequency, and the ADC conversion type, allowing one-shot conversion operation. In SPI control mode, the GPIOx pins, in addition to the FILTER/GPIO4 pin, form five general-purpose input/output pins (GPIO4 to GPIO0).
16	ST0/$\overline{CS}$	DI	Standby 0/Chip Select Input. In pin control mode, a Logic 1 places Channel 0 to Channel 3 into standby mode. In SPI control mode, this pin is the active low chip select input to the SPI control interface. The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768.
17	ST1/SCLK	DI	Standby 1/Serial Clock Input. In pin control mode, a Logic 1 on this pin places Channel 4 to Channel 7 into standby mode. The crystal excitation circuitry is associated with the Channel 4 circuitry. If Channel 4 is placed into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768. In SPI control mode, this pin is the serial clock input pin for the SPI control interface.
18	DEC1/SDI	DI	Decimation Rate Control Input 1/Serial Data Input. In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. See Table 17 in the Setting the Decimation Rate section for more information. In SPI control mode, this pin is the serial data input pin used to write data to the AD7768 register bank.
19	DEC0/SDO	DI/O	Decimation Rate Control Input 0/Serial Data Output. In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. See Table 17 in the Setting the Decimation Rate section for more information. In SPI control mode, this pin is the serial data output pin, allowing readback from the AD7768 registers.
20	DOUT7	DI/O	Conversion Data Output 7. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. This pin acts as a digital input from a separate AD7768 device if configured in a synchronized multidevice daisy chain when the FORMATx pins are configured as 01. To use the AD7768 in a daisy chain, hardwire the FORMATx pins as 01, 10, or 11, depending on the best interfacing format for the application. When FORMATx is set to 01, 10, or 11, and daisy-chaining is not used, connect this pin to ground through a pull-down resistor.
21	DOUT6	DI/O	Conversion Data Output 6. This pin is synchronous to DCLK and framed by $\overline{DRDY}$. This pin acts as a digital input from a separate AD7768 device if configured in a synchronized multidevice daisy chain. To use this pin in a daisy chain, hardwire the FORMATx pins as 01, 10, or 11, depending on the best interfacing format for the application. When FORMATx is set to 01, 10, or 11, and daisy chaining is not used, connect this pin to ground through a pull-down resistor.
22	DOUT5	DO	Conversion Data Output 5. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
23	DOUT4	DO	Conversion Data Output 4. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
24	DOUT3	DO	Conversion Data Output 3. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
25	DOUT2	DO	Conversion Data Output 2. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
26	DOUT1	DO	Conversion Data Output 1. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
27	DOUT0	DO	Conversion Data Output 0. This pin is synchronous to DCLK and framed by $\overline{DRDY}$
28	DCLK	DO	ADC Conversion Data Clock. This pin clocks conversion data out to the digital host (digital signal processor (DSP)/field-programmable gate array (FPGA)). This pin is synchronous with $\overline{DRDY}$ and any conversion data output on DOUT0 to DOUT7 and is derived from the MCLK signal. This pin is unrelated to the control SPI interface.
29	$\overline{DRDY}$	DO	Data Ready. $\overline{DRDY}$ is a periodic signal output framing the conversion results from the eight ADCs. This pin is synchronous to DCLK and DOUT0 to DOUT7.
30	$\overline{RESET}$	DI	Hardware Asynchronous Reset Input. After the device is fully powered up, it is recommended to perform a hard reset using this pin or, alternatively, to perform a soft reset by issuing a reset over the SPI control interface

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Pin No.	Mnemonic	Type[1]	Description
31	XTAL1	DI	Input 1 for Crystal or Connection to an LVDS Clock. When CLK_SEL is 0, connect XTAL1 to DGND. In SPI control mode, when using a crystal source, the FILTER pin must be set to Logic 1 for correct operation. The crystal excitation circuitry is associated with the Channel 4 circuitry. If Channel 4 is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768. When used with an LVDS clock, connect this pin to one trace of the LVDS signal pair. When used as an LVDS input, a rising edge on this pin is detected as a rising MCLK edge by the AD7768.
32	XTAL2/MCLK	DI	Input 2 for CMOS or Crystal/LVDS Sampling Clock. See the CLK_SEL pin for the details of this configuration. External crystal: XTAL2 is connected to the external crystal. In SPI control mode, when using a crystal source, the FILTER pin must be set to Logic 1 for correct operation. LVDS clock: when used with an LVDS clock, connect this pin to the second trace of the LVDS signal pair. CMOS clock: this pin operates as an MCLK input. This pin is a CMOS input with a logic level of IOVDD/DGND. When used as a CMOS clock input, a rising edge on this pin is detected as a rising MCLK edge by the AD7768. The crystal excitation circuitry is associated with the Channel 4 circuitry. If Channel 4 is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768.
33	DGND	P	Digital Ground. This pin is nominally 0 V.
34	DREGCAP	AO	Digital Low Dropout (LDO) Regulator Output. Decouple this pin to DGND with a high quality, low equivalent series resistance (ESR), 10 µF capacitor. For optimum performance, use a decoupling capacitor with an ESR specification of less than 400 mΩ. This pin is not for use in circuits external to the AD7768. For 1.8 V IOVDD operation, connect this pin to IOVDD via an external trace to provide power to the digital processing core.
35	IOVDD	P	Digital Supply. This pin sets the logic levels for all interface pins. IOVDD also powers the digital processing core via the digital LDO when IOVDD is at least 2.25 V. For 1.8 V IOVDD operation, connect this pin to DREGCAP via an external trace to provide power to the digital processing core.
36	$\overline{\text{SYNC_IN}}$	DI	Synchronization Input. $\overline{\text{SYNC_IN}}$ receives the synchronous signal from $\overline{\text{SYNC_OUT}}$. It is used in the synchronization of any AD7768 that requires simultaneous sampling or is in a daisy chain. Ignore the $\overline{\text{START}}$ and $\overline{\text{SYNC_OUT}}$ functions if the $\overline{\text{SYNC_IN}}$ pin is connected to the system synchronization pulse. This signal pulse must be synchronous to the MCLK clock domain. In a daisy-chained system of AD7768 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768 device sharing a single MCLK signal, where the $\overline{\text{DRDY}}$ pin of only one device is used to detect new data.
37	$\overline{\text{START}}$	DI	Start Signal. The $\overline{\text{START}}$ pulse synchronizes the AD7768 to other devices. The signal can be asynchronous. The AD7768 samples the input and then outputs a $\overline{\text{SYNC_OUT}}$ pulse. This $\overline{\text{SYNC_OUT}}$ pulse must be routed to the $\overline{\text{SYNC_IN}}$ pin of this device, and any other AD7768 devices that must be synchronized together. This means that the user does not need to run the ADCs and their digital host from the same clock domain, which is useful when there are long traces or back planes between the ADC and the controller. If this pin is not used, it must be tied to a Logic 1 through a pull-up resistor. In a daisy-chained system of AD7768 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768 device sharing a single MCLK signal, where the $\overline{\text{DRDY}}$ pin of only one device is used to detect new data.
38	$\overline{\text{SYNC_OUT}}$	DO	Synchronization Output. This pin operates only when the $\overline{\text{START}}$ input is used. When using the $\overline{\text{START}}$ input feature, the $\overline{\text{SYNC_OUT}}$ pin must be connected to $\overline{\text{SYNC_IN}}$ via an external trace. $\overline{\text{SYNC_OUT}}$ is a digital output that is synchronous to the MCLK signal; the synchronization signal driven in on $\overline{\text{START}}$ is internally synchronized to the MCLK signal and is driven out on $\overline{\text{SYNC_OUT}}$. $\overline{\text{SYNC_OUT}}$ can also be routed to other AD7768 devices requiring simultaneous sampling and/or daisy-chaining, ensuring synchronization of devices related to the MCLK clock domain. It must then be wired to drive the $\overline{\text{SYNC_IN}}$ pin on the same AD7768 and on the other AD7768 devices.
39	AIN7+	AI	Positive Analog Input to ADC Channel 7.
40	AIN7−	AI	Negative Analog Input to ADC Channel 7.
41	AIN6+	AI	Positive Analog Input to ADC Channel 6.
42	AIN6−	AI	Negative Analog Input to ADC Channel 6.

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Pin No.	Mnemonic	Type[1]	Description
43	REF2+	AI	Reference Input, Positive. REF2+ is the positive reference terminal for Channel 4 to Channel 7. The REF2+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external differential reference voltage between REF2+ and REF2− in the range from 1 V to |AVDD1 − AVSS|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 46.
44	REF2−	AI	Reference Input, Negative. REF2− is the negative reference terminal for Channel 4 to Channel 7. The REF2− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 46.
45	AVDD1B	P	Analog Supply Voltage. This pin is 5 V ± 10% with respect to AVSS.
46	AVSS1B	P	Negative Analog Supply. This pin is nominally 0 V.
47	AIN5+	AI	Positive Analog Input to ADC Channel 5.
48	AIN5−	AI	Negative Analog Input to ADC Channel 5.
49	AIN4+	AI	Positive Analog Input to ADC Channel 4.
50	AIN4−	AI	Negative Analog Input to ADC Channel 4.
51	AVSS2B	P	Negative Analog Supply. This pin is nominally 0 V.
52	REGCAPB	AO	Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor.
53	AVDD2B	P	Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS.
54	AVSS	P	Negative Analog Supply. This pin is nominally 0 V.
55, 56	FORMAT1, FORMAT0	DI	Format Selection Pins. Hardwire the FORMATx pins to the required values in pin control and SPI control mode. These pins set the number of DOUTx pins used to output ADC conversion data. The FORMATx pins are checked by the AD7768 on power-up; the AD7768 then remains in this data output configuration (see Table 33).
57	$\overline{\text{PIN}}$/SPI	DI	Pin Control/SPI Control. This pin sets the control method. Logic 0 = pin control mode for the AD7768. Pin control mode allows a pin strapped configuration of the AD7768 by tying logic input pins to required logic levels. Tie the logic pins (MODE0 to MODE4, DEC0 and DEC1, and FILTER) as required for the configuration. See the Pin Control section for more details. Logic 1 = SPI control mode for the AD7768. Use the SPI control interface signals ($\overline{\text{CS}}$, SCLK, SDI, and SDO) for reading and writing to the AD7768 memory map.
58	CLK_SEL	DI	Clock Select. Logic 0 = pull this pin low for the CMOS clock option. The clock is applied to Pin 32 (Connect Pin 31 to DGND). Logic 1 = pull this pin high for the crystal or LVDS clock option. The crystal or LVDS clock is applied to Pin 31 and Pin 32. The LVDS option is available only in SPI control mode. A write is required to enable the LVDS clock option.
59	VCM	AO	Common-Mode Voltage Output. This pin outputs (AVDD1 − AVSS)/2 V, which is 2.5 V by default in pin control mode. Configure this pin to (AVDD1 − AVSS)/2 V, 2.5 V, 2.14 V, or 1.65 V in SPI control mode. When driving capacitive loads larger than 0.1 µF, it is recommended to place a 50 Ω series resistor between this pin and the capacitive load for stability. The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768.
60	AVDD2A	P	Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS.
61	REGCAPA	AO	Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor.
62	AVSS2A	P	Negative Analog Supply. This pin is nominally 0 V.
63	AIN0−	AI	Negative Analog Input to ADC Channel 0.
64	AIN0+	AI	Positive Analog Input to ADC Channel 0.

[1] AI is analog input, P is power, DI/O is digital input/output, DI is digital input, DO is digital output, and AO is analog output.

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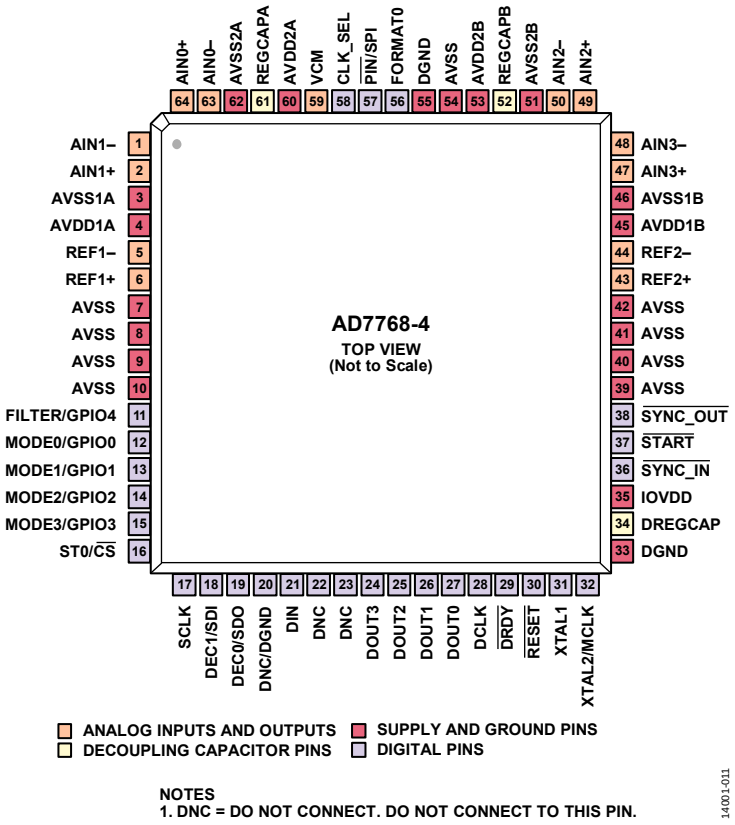

Figure 11. AD7768-4 Pin Configuration

Table 10. AD7768-4 Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	AIN1−	AI	Negative Analog Input to ADC Channel 1.
2	AIN1+	AI	Positive Analog Input to ADC Channel 1.
3	AVSS1A	P	Negative Analog Supply. This pin is nominally 0 V.
4	AVDD1A	P	Analog Supply Voltage, 5 V ± 10% with respect to AVSS.
5	REF1−	AI	Reference Input Negative. REF1− is the negative reference terminal for Channel 0 and Channel 1. The REF1− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3.
6	REF1+	AI	Reference Input Positive. REF1+ is the positive reference terminal for Channel 0 and Channel 1. The REF1+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external differential reference voltage between REF1+ and REF1− in the range from 1 V to |AVDD1 − AVSS|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3.
7 to 10, 39 to 42, 54	AVSS	AI	Negative Analog Supply. This pin is nominally 0 V.
11	FILTER/GPIO4	DI/O	Filter Select/General-Purpose Input/Output 4. In pin control mode, this pin selects the filter type. Set this pin to Logic 1 for the sinc5 filter. This sinc5 filter is a low latency filter, and is best for dc applications or where a user has specialized postfiltering implemented off chip. Set this pin to Logic 0 for the wideband low ripple filter response. This filter has a steep transition band and 105 dB stop band attenuation. Full attenuation at Nyquist (ODR/2) means that no aliasing occurs at ODR/2 out to the first chopping zone. In SPI control mode, this pin can be used as a general-purpose input/output (GPIO4). For further information on GPIO configuration, see the GPIO Functionality section. In SPI control mode, when not used as a GPIO pin, and when a crystal will be used as the clock source, this pin must be set to 1.

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Pin No.	Mnemonic	Type[1]	Description
12, 13, 14, 15	MODE0/GPIO0, MODE1/GPIO1, MODE2/GPIO2, MODE3/GPIO3	DI/DI/O	Mode Selection/General-Purpose Input/Output Pin 0 to Pin 3. In pin control mode, the MODEx pins set the mode of operation for all ADC channels, controlling power consumption, DCLK frequency, and the ADC conversion type, allowing one-shot conversion operation. In SPI control mode, the GPIOx pins, in addition to the FILTER/GPIO4 pin, form five general-purpose input/output pins (GPIO4 to GPIO0). See Table 75 for more details.
16	ST0/$\overline{CS}$	DI	Standby 0/Chip Select Input. In pin control mode, a Logic 1 on this pin places Channel 0 to Channel 3 into standby mode. In SPI control mode, this pin is the active low chip select input to the SPI control interface. The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel0 must be enabled while VCM is being used externally to the AD7768-4. The crystal excitation circuitry is associated with the Channel 2 circuitry. If Channel 2 is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 2 must be enabled while the external crystal is used on the AD7768-4.
17	SCLK	DI	Serial Clock Input. In SPI control mode, this pin is the serial clock input pin for the SPI control interface. In pin control mode, tie this pin to a Logic 0 or DGND.
18	DEC1/SDI	DI	Decimation Rate Control Input 1/Serial Data Input. In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. See Table 17 in the Setting the Decimation Rate section. In SPI control mode, this pin is the serial data input pin used to write data to the AD7768-4 register bank.
19	DEC0/SDO	DI/O	Decimation Rate Control Input 0/Serial Data Output. In pin control mode, the DEC0 and DEC1 pins configure the decimation rate for all ADC channels. See Table 17 in the Setting the Decimation Rate section. In SPI control mode, this pin is the serial data output pin, allowing readback from the AD7768-4 registers.
20	DNC/DGND	DO/DI	Do Not Connect/Digital Ground. This is an unused pin. Leave this pin floating if FORMAT0 is tied to logic low. If FORMAT0 is tied to logic high, connect this pin to DGND through a pull-down resistor.
21	DIN	DI	Data Input Daisy Chain. This pin acts as a digital input from a separate AD7768-4 device if configured in a synchronized multidevice daisy-chain. To use this pin in a daisy-chain, hardwire the FORMAT0 pin to logic high. If FORMAT0 is tied to logic low, or the daisy chaining input pin is not used, then tie this pin to DGND through a pull-down resistor.
22, 23	DNC	DO	Do Not Connect. Do not connect to this pin.
24	DOUT3	DO	Conversion Data Output 3. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
25	DOUT2	DO	Conversion Data Output 2. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
26	DOUT1	DO	Conversion Data Output 1. This pin is synchronous to DCLK and framed by $\overline{DRDY}$.
27	DOUT0	DO	Conversion Data Output 0. This pin is synchronous to DCLK and framed by $\overline{DRDY}$
28	DCLK	DO	ADC Conversion Data Clock. This pin clocks conversion data out to the digital host (DSP/FPGA). This pin is synchronous with $\overline{DRDY}$ and any conversion data output on DOUT0 to DOUT3 and is derived from the MCLK signal. This pin is unrelated to the control SPI interface.
29	$\overline{DRDY}$	DO	Data Ready. $\overline{DRDY}$ is a periodic signal output framing the conversion results from the four ADCs. This pin is synchronous to DCLK and DOUT0 to DOUT3.
30	$\overline{RESET}$	DI	Hardware Asynchronous Reset Input. After the device is fully powered up, it is recommended to perform a hard reset using this pin or, alternatively, to perform a soft reset by issuing a reset over the SPI control interface
31	XTAL1	DI	Input 1 for Crystal or Connection to an LVDS Clock. When CLK_SEL is 0, connect XTAL1 to DGND. In SPI control mode, when using a crystal source, the FILTER pin must be set to Logic 1 for correct operation. When used with an LVDS clock, it is recommended that this pin be connected to one trace of the LVDS signal pair. When used as an LVDS input, a rising edge on this pin is detected as a rising MCLK edge by the AD7768-4.

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Pin No.	Mnemonic	Type[1]	Description
32	XTAL2/MCLK	DI	Input 2 for CMOS/Crystal/LVDS Sampling Clock. See the CLK_SEL pin for the details of this configuration. External crystal: XTAL2 is connected to the external crystal. In SPI control mode, when using a crystal source, the FILTER pin must be set to Logic 1 for correct operation. LVDS: when used with an LVDS clock, connect this pin to the second trace of the LVDS signal pair. CMOS clock: this pin operates as an MCLK input. This pin is a CMOS input with logic level of IOVDD/DGND. When used as a CMOS clock input, a rising edge on this pin is detected as a rising MCLK edge by the AD7768-4.
33	DGND	P	Digital Ground. Nominally GND (0 V).
34	DREGCAP	AO	Digital LDO Regulator Output. Decouple this pin to DGND with a high quality, low ESR, 10 µF capacitor. For optimum performance, use a decoupling capacitor with an ESR specification of less than 400 mΩ. This pin is not for use in circuits external to the AD7768-4. For 1.8 V IOVDD operation, connect this pin to IOVDD via an external trace to provide power to the digital processing core.
35	IOVDD	P	Digital Supply. This pin sets the logic levels for all interface pins. IOVDD also powers the digital processing core, via the digital LDO, when IOVDD is at least 2.25 V. For 1.8 V IOVDD operation, connect this pin to DREGCAP via an external trace to provide power to the digital processing core.
36	$\overline{\text{SYNC_IN}}$	DI	Synchronization Input. $\overline{\text{SYNC_IN}}$ receives the synchronous signal from $\overline{\text{SYNC_OUT}}$. It is used in the synchronization of any AD7768-4 that requires simultaneous sampling or is in a daisy chain. The user can ignore the $\overline{\text{START}}$ and $\overline{\text{SYNC_OUT}}$ function if the AD7768-4 $\overline{\text{SYNC_IN}}$ pin is connected to the system synchronization pulse. This signal pulse must be synchronous to the MCLK clock domain.
37	$\overline{\text{START}}$	DI	Start Signal. The $\overline{\text{START}}$ pulse acts to synchronize the AD7768-4 to other devices. The signal can be asynchronous. The AD7768-4 samples the input and then outputs a $\overline{\text{SYNC_OUT}}$ pulse. This $\overline{\text{SYNC_OUT}}$ pulse must be routed to the $\overline{\text{SYNC_IN}}$ pin of this device, and any other AD7768-4 devices that must be synchronized together. This means that the user does not need to run the ADCs and their digital host from the same clock domain, which is useful when there are long traces or back planes between the ADC and the controller. If this pin is not used, it must be tied to a Logic 1 through a pull-up resistor. In a daisy-chained system of AD7768-4 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768-4 device sharing a single MCLK signal, where the $\overline{\text{DRDY}}$ pin of only one device is used to detect new data.
38	$\overline{\text{SYNC_OUT}}$	DO	Synchronization Output. This pin operates only when the $\overline{\text{START}}$ input is used. When using the $\overline{\text{START}}$ input feature, the $\overline{\text{SYNC_OUT}}$ must be connected to $\overline{\text{SYNC_IN}}$ via an external trace. $\overline{\text{SYNC_OUT}}$ is a digital output that is synchronous to the MCLK signal; the synchronization signal driven in on $\overline{\text{START}}$ is internally synchronized to the MCLK signal and is driven out on $\overline{\text{SYNC_OUT}}$. $\overline{\text{SYNC_OUT}}$ can also be routed to other AD7768-4 devices requiring simultaneous sampling and/or daisy-chaining, ensuring synchronization of devices related to the MCLK clock domain. It must then be wired to drive the $\overline{\text{SYNC_IN}}$ pin on the same AD7768-4 and on the other AD7768-4 devices.
43	REF2+	AI	Reference Input Positive. REF2+ is the positive reference terminal for Channel 2 and Channel 3. The REF2+ voltage range is from (AVSS + 1 V) to AVDD1. Apply an external differential reference voltage between REF2+ and REF2− in the range from 1 V to |AVDD1 − AVSS|. Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3.
44	REF2−	AI	Reference Input Negative. REF2− is the negative reference terminal for Channel 2 and Channel 3. The REF2− voltage range is from AVSS to (AVDD1 − 1 V). Decouple this pin to AVSS with a high quality capacitor, and maintain a low impedance between this capacitor and Pin 3.
45	AVDD1B	P	Analog Supply Voltage. This pin is 5 V ± 10% with respect to AVSS.
46	AVSS1B	P	Negative Analog Supply. This pin is nominally 0 V.
47	AIN3+	AI	Positive Analog Input to ADC Channel 3.
48	AIN3−	AI	Negative Analog Input to ADC Channel 3.
49	AIN2+	AI	Positive Analog Input to ADC Channel 2.
50	AIN2−	AI	Negative Analog Input to ADC Channel 2.
51	AVSS2B	P	Negative Analog Supply. This pin is nominally 0 V.

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Pin No.	Mnemonic	Type[1]	Description
52	REGCAPB	AO	Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor.
53	AVDD2B	P	Analog Supply Voltage. 2 V to 5.5 V with respect to AVSS.
55	DGND	P	Digital Ground. This pin is nominally 0 V.
56	FORMAT0	DI	Format Selection. Hardwire the FORMAT0 pin to the required value in pin and SPI control mode. This pin sets the number of DOUTx pins used to output ADC conversion data. The FORMAT0 pin is checked by the AD7768-4 on power-up, the AD7768-4 then remains in this data output configuration. See Table 34.
57	$\overline{\text{PIN}}$/SPI	DI	Pin Control/SPI Control. This pin sets the AD7768-4 control method. Logic 0 = pin control mode for the AD7768-4. Pin control mode allows pin strapped configuration of the AD7768-4 by tying logic input pins to required logic levels. Tie logic pins MODE0 to MODE4, DEC0 and DEC1, and FILTER as required for the configuration. See the Pin Control section for more details. Logic 1 = SPI control mode for the AD7768-4. Use the SPI control interface signals ($\overline{\text{CS}}$, SCLK, SDI, and SDO) for reading and writing to the AD7768-4 memory map.
58	CLK_SEL	DI	Clock Select. Logic 0 = pull this pin low for the CMOS clock option. The clock is applied to Pin 32 (Connect Pin 31 to DGND). Logic 1 = pull this pin high for the crystal or LVDS clock option. The crystal or LVDS clock is applied to Pin 31 and Pin 32. The LVDS option is available only in SPI control mode. A write is required to enable the LVDS clock option.
59	VCM	AO	Common-Mode Voltage Output. This pin outputs (AVDD1 − AVSS)/2 V, which is 2.5 V by default in pin control mode. Configure this pin to (AVDD1 − AVSS)/2 V, 2.5 V, 2.14 V, or 1.65 V in SP control mode. When driving capacitive loads larger than 0.1 µF, it is recommended to place a 50 Ω series resistor between the pin and the capacitive load for stability. The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768-4.
60	AVDD2A	P	Analog Supply Voltage. This pin is 2 V to 5.5 V with respect to AVSS.
61	REGCAPA	AO	Analog LDO Regulator Output. Decouple this pin to AVSS with a 1 µF capacitor.
62	AVSS2A	P	Negative Analog Supply. This pin is nominally 0 V.
63	AIN0−	AI	Negative Analog Input to ADC Channel 0.
64	AIN0+	AI	Positive Analog Input to ADC Channel 0.

[1] AI is analog input, P is power, DI/O is digital input/output, DI is digital input, DO is digital output, and AO is analog output.

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TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 2.5 V, AVSS = 0 V, IOVDD = 2.5 V, V_{REF} = 4.096 V, T_A = 25°C, wideband filter, decimation = ×32, MCLK = 32.768 MHz, analog input precharge buffers on, precharge reference buffers off, unless otherwise noted.

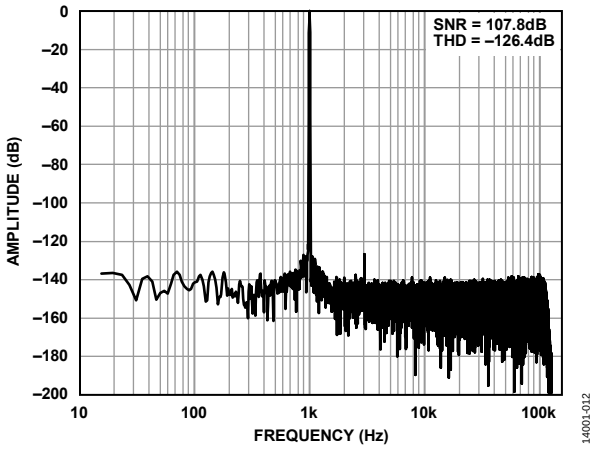

Figure 12. FFT, Fast Mode, Wideband Filter, –0.5 dBFS

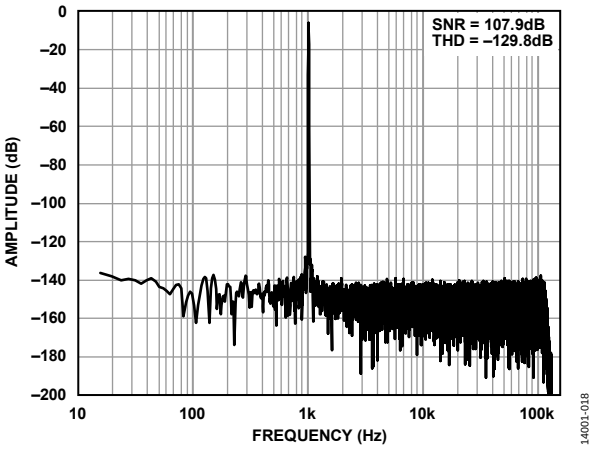

Figure 15. FFT, Fast Mode, Wideband Filter, –6 dBFS

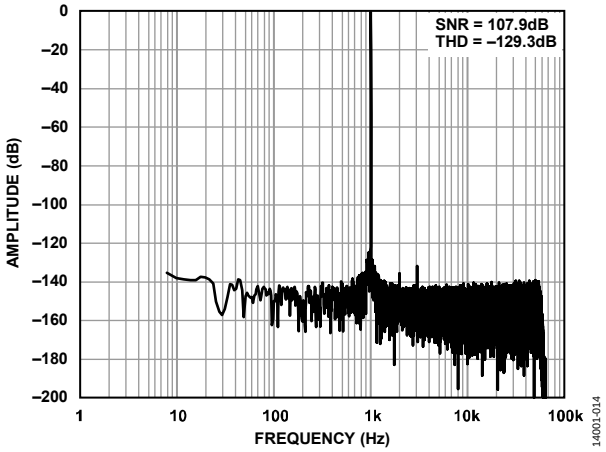

Figure 13. FFT, Median Mode, Wideband Filter, –0.5 dBFS

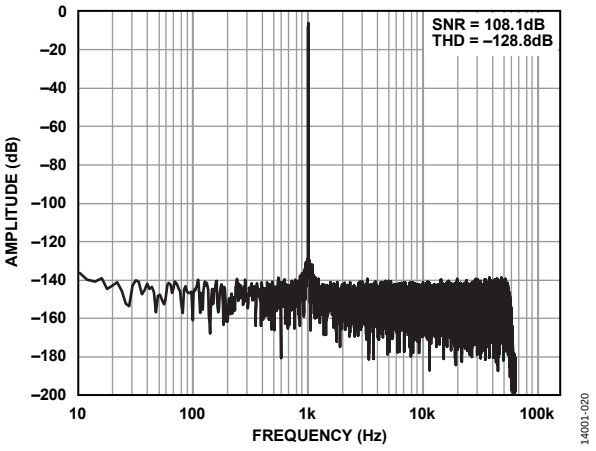

Figure 16. FFT, Median Mode, Wideband Filter, –6 dBFS

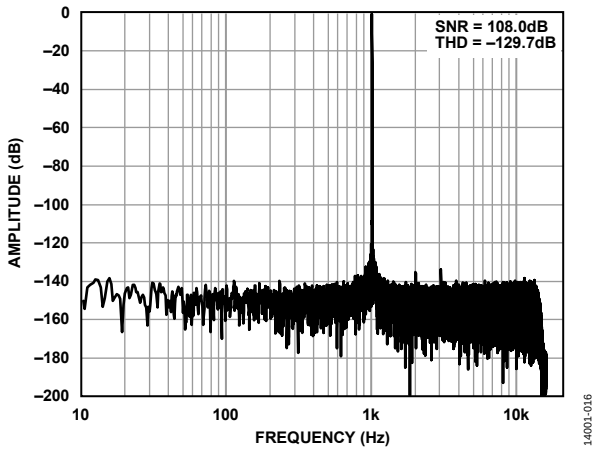

Figure 14. FFT, Low Power Mode, Wideband Filter, –0.5 dBFS

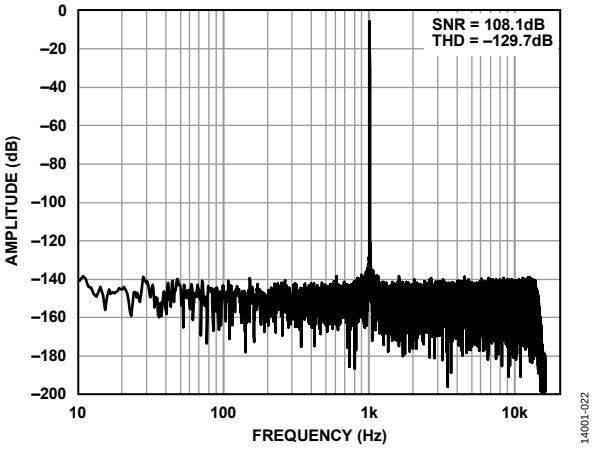

Figure 17. FFT, Low Power Mode, Wideband Filter, –6 dBFS

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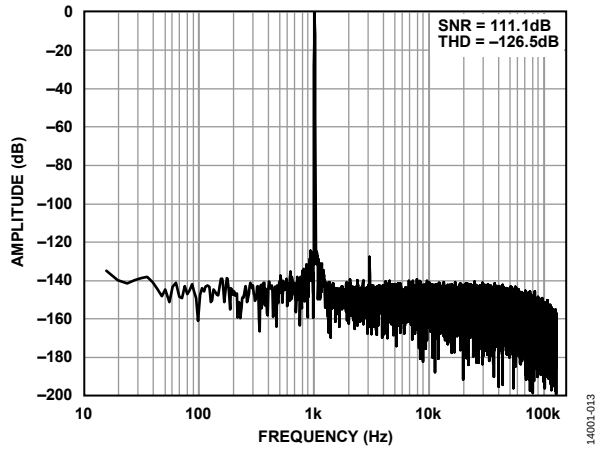

Figure 18. FFT, Fast Mode, Sinc5 Filter, –0.5 dBFS

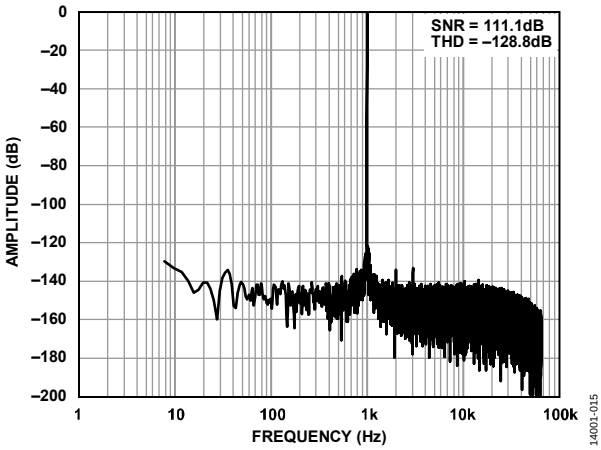

Figure 19. FFT, Median Mode, Sinc5 Filter, –0.5 dBFS

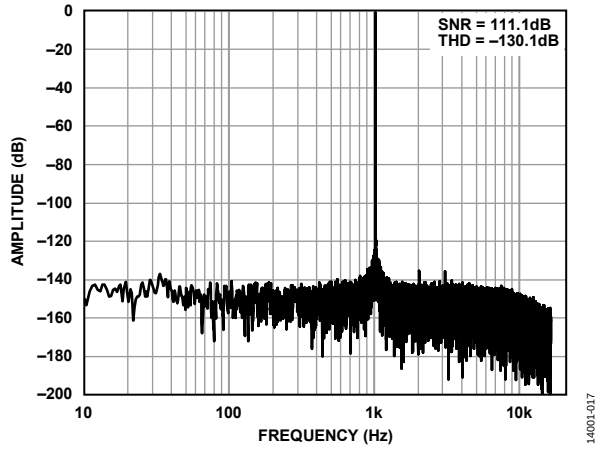

Figure 20. FFT, Low Power Mode, Sinc5 Filter, –0.5 dBFS

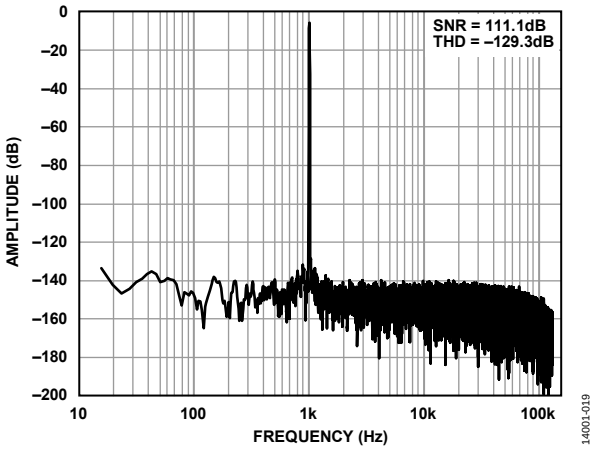

Figure 21. FFT, Fast Mode, Sinc5 Filter, –6 dBFS

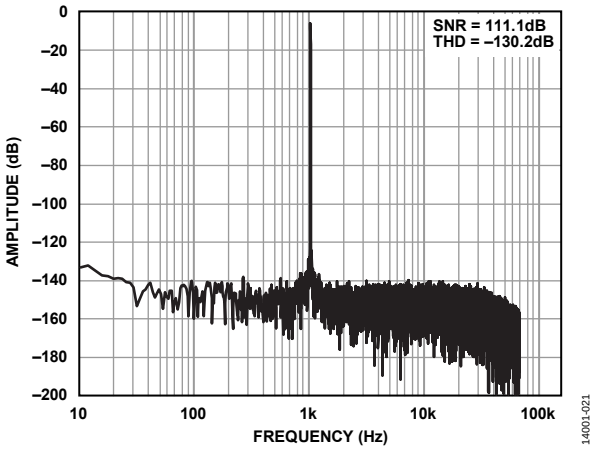

Figure 22. FFT, Median Mode, Sinc5 Filter, –6 dBFS

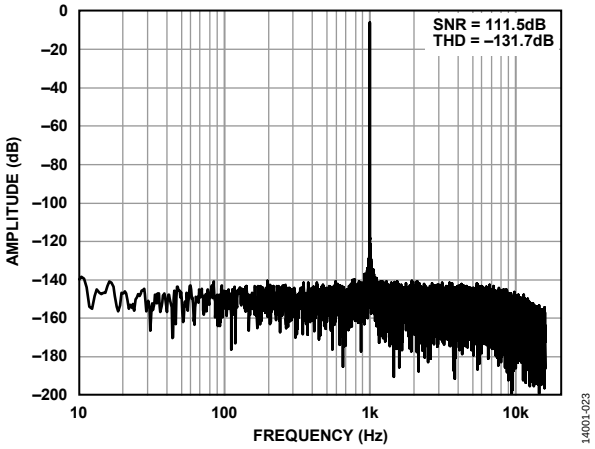

Figure 23. FFT, Low Power Mode, Sinc5 Filter, –6 dBFS

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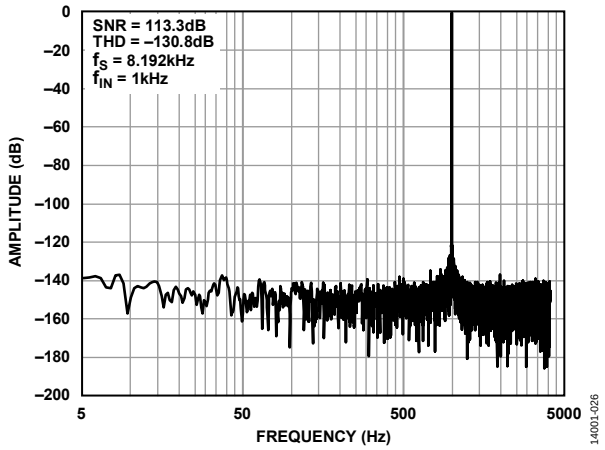

Figure 24. FFT One-Shot-Mode, Sinc5 Filter, Median Mode, Decimation = ×64, −0.5 dBFS, $\overline{SYNC_IN}$ Frequency = MCLK/4000

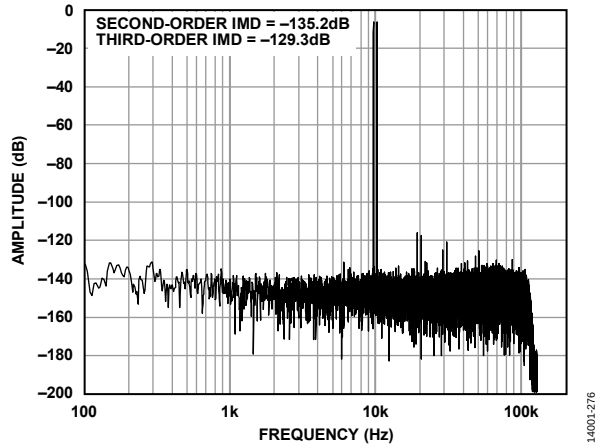

Figure 25. IMD with Input Signals at 9.7 kHz and 10.3 kHz

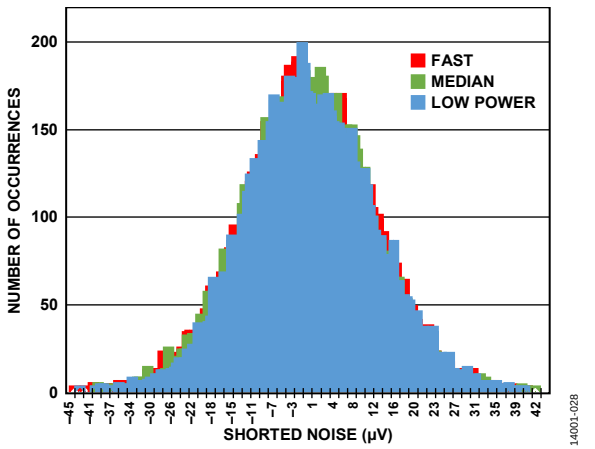

Figure 26. Shorted Noise, Wideband Filter

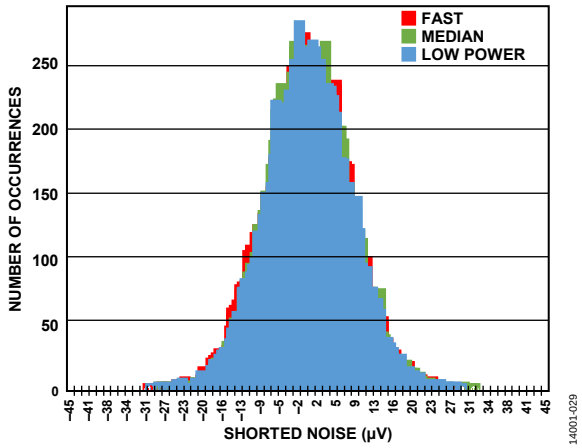

Figure 27. Shorted Noise, Sinc5 Filter

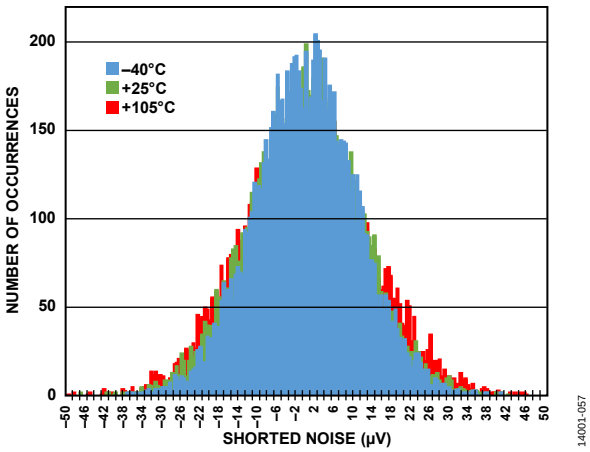

Figure 28. Shorted Noise vs. Temperature, Wideband Filter

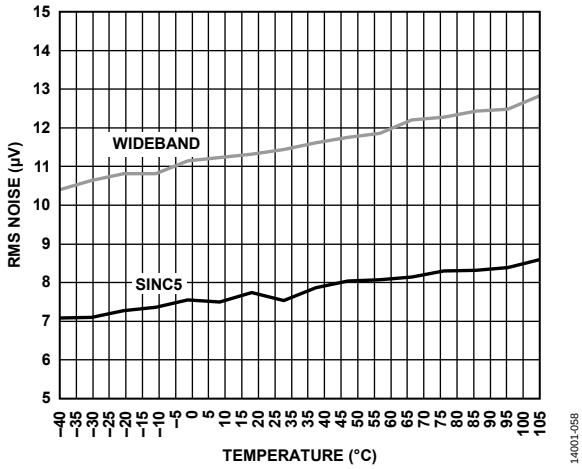

Figure 29. RMS Noise vs. Temperature, Fast Mode

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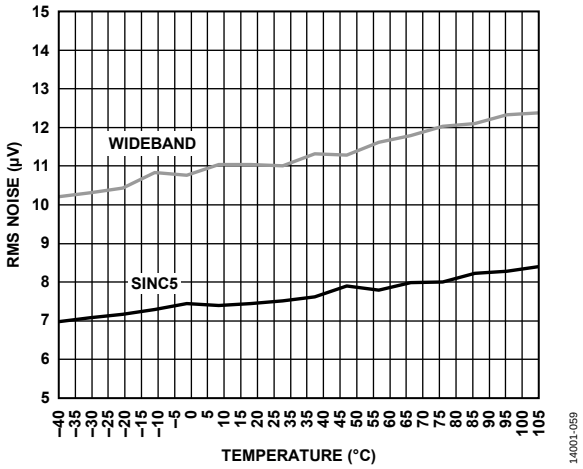

Figure 30. RMS Noise vs. Temperature, Median Mode

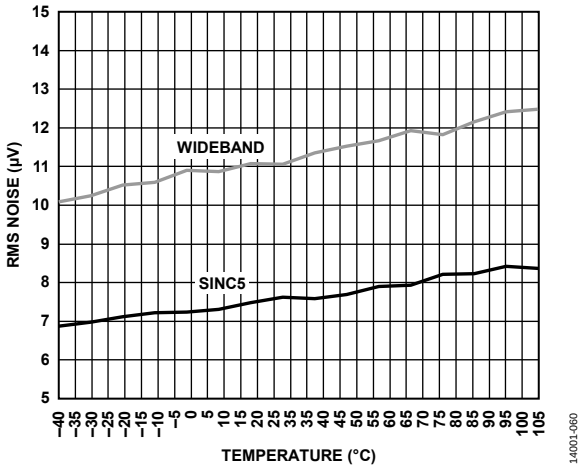

Figure 31. RMS Noise vs. Temperature, Low Power Mode

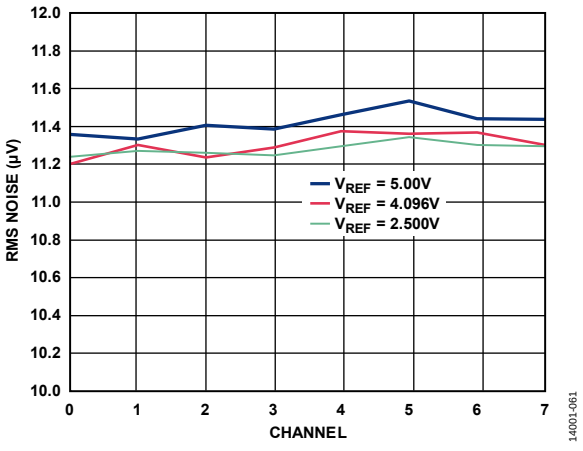

Figure 32. RMS Noise per Channel for Various V_{REF} Values

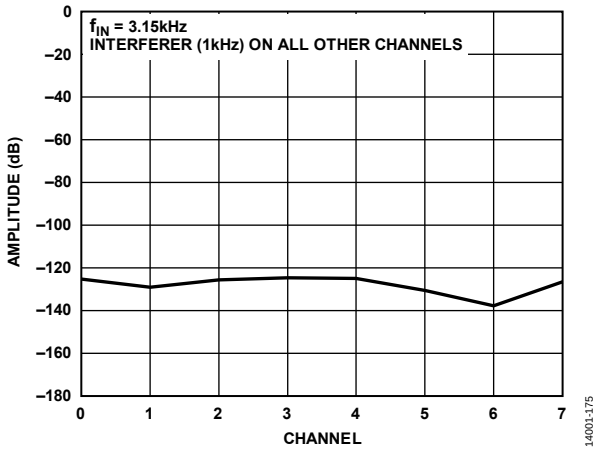

Figure 33. Crosstalk

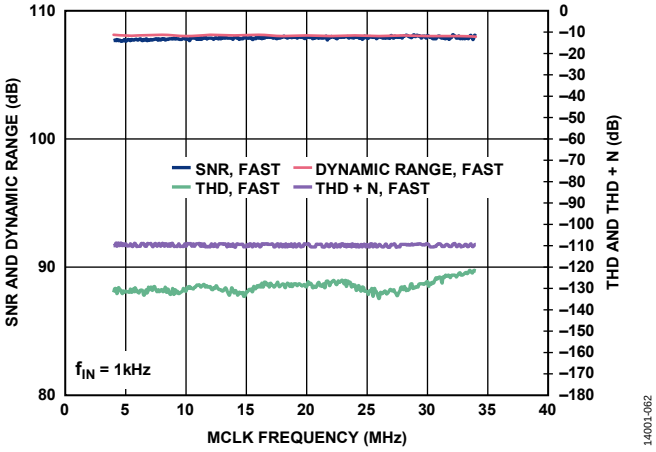

Figure 34. SNR, Dynamic Range, THD, and THD +N vs. MCLK Frequency

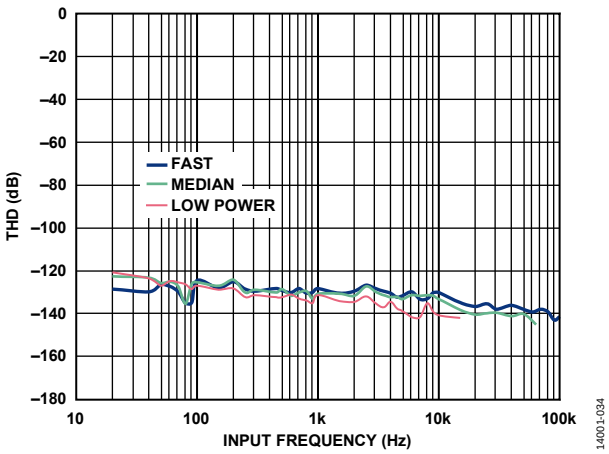

Figure 35. THD vs. Input Frequency, Three Power Modes, Wideband Filter

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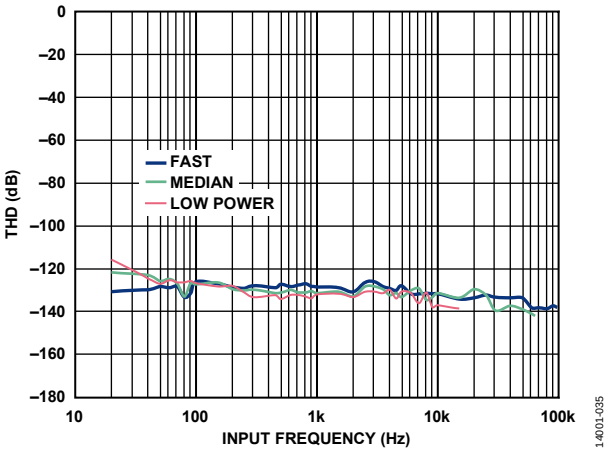

Figure 36. THD vs. Input Frequency, Three Power Modes, Sinc5 Filter

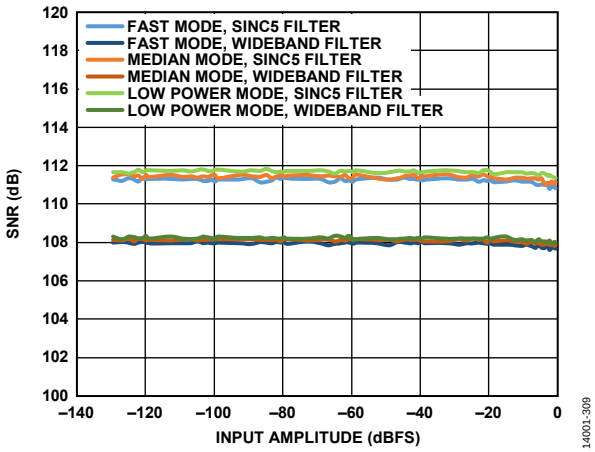

Figure 39. SNR vs. Input Amplitude

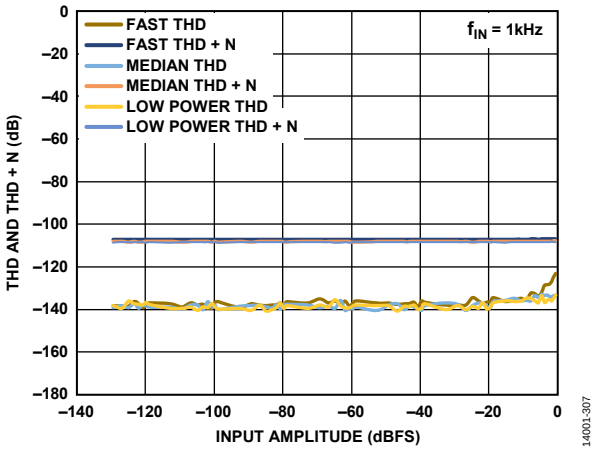

Figure 37. THD and THD + N vs. Input Amplitude, Wideband Filter

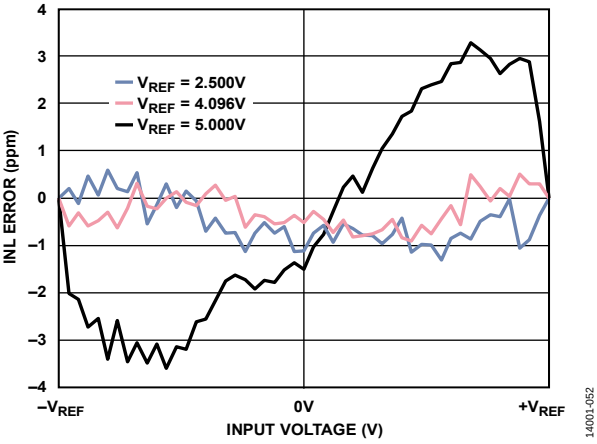

Figure 40. INL Error vs. Input Voltage for Various Voltage Reference (V_{REF}) Levels, Fast Mode

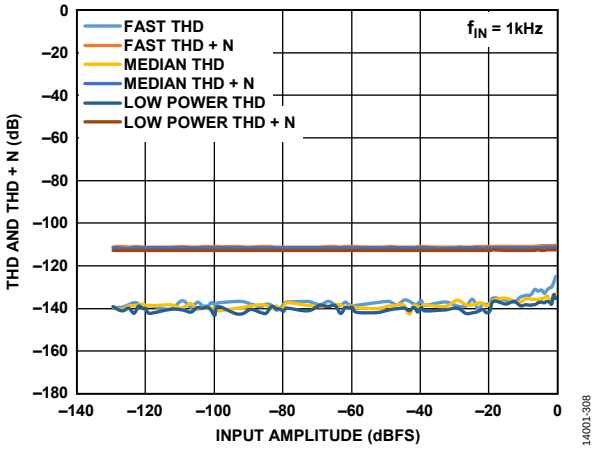

Figure 38. THD and THD + N vs. Input Amplitude, Sinc5 Filter

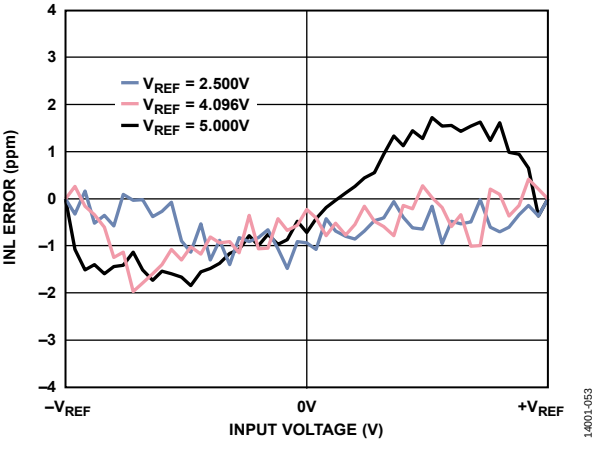

Figure 41. INL Error vs. Input Voltage for Various Voltage Reference (V_{REF}) Levels, Median Mode

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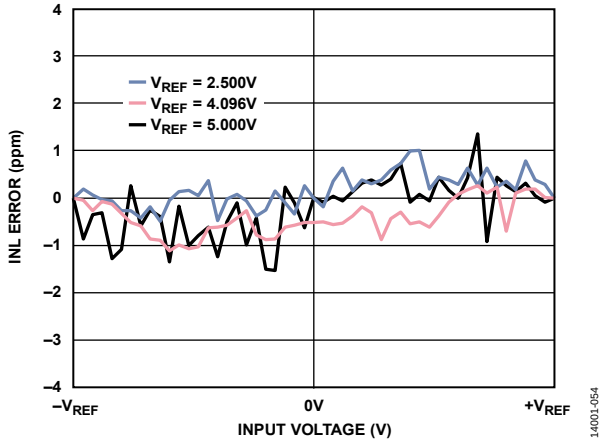

Figure 42. INL Error vs. Input Voltage for Various Voltage Reference (V_{REF}) Levels, Low Power Mode

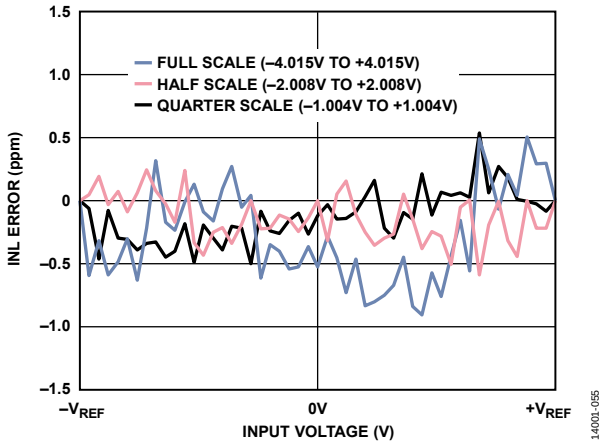

Figure 43. INL Error vs. Input Voltage, Full-Scale, Half-Scale, and Quarter-Scale Inputs

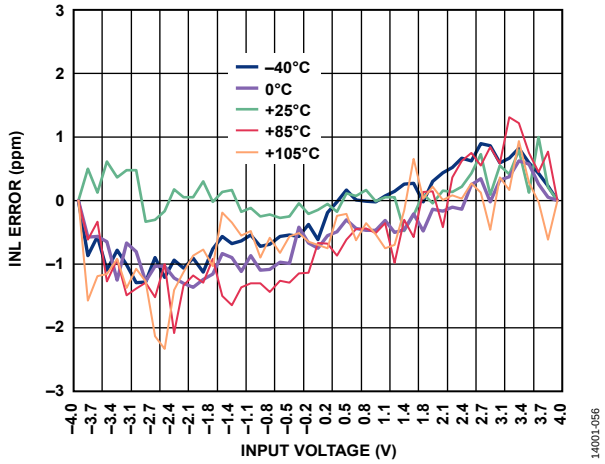

Figure 44. INL Error vs. Input Voltage for Various Temperatures, Fast Mode

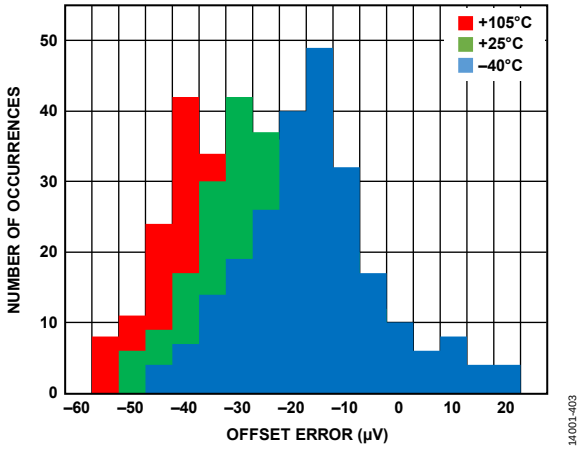

Figure 45. Offset Error Distribution, DCLK = 24 MHz

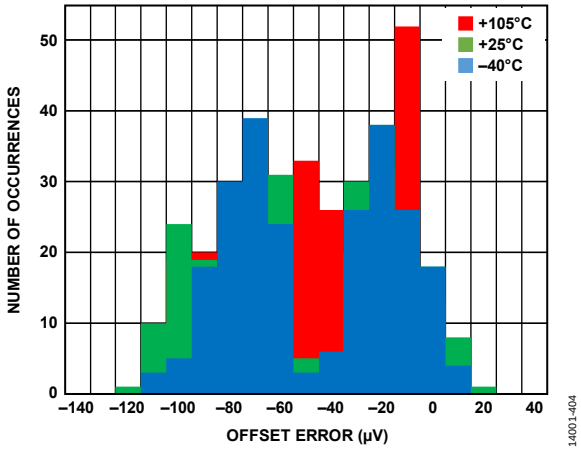

Figure 46. Offset Error Distribution, DCLK = 32 MHz

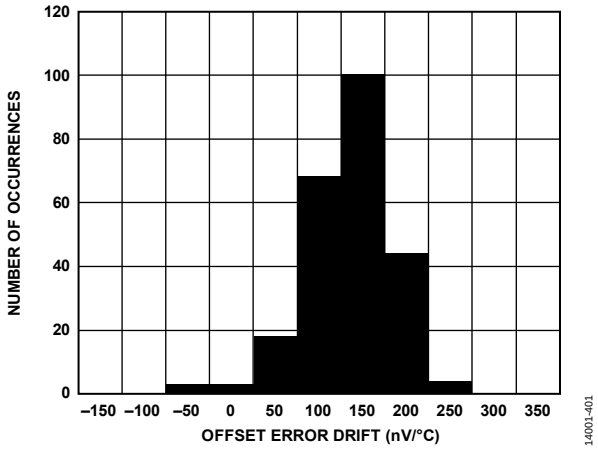

Figure 47. Offset Error Drift, DCLK = 24 MHz

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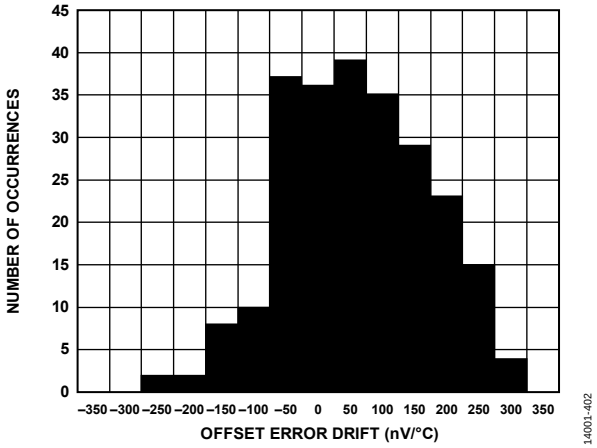

Figure 48. Offset Error Drift, DCLK = 32 MHz

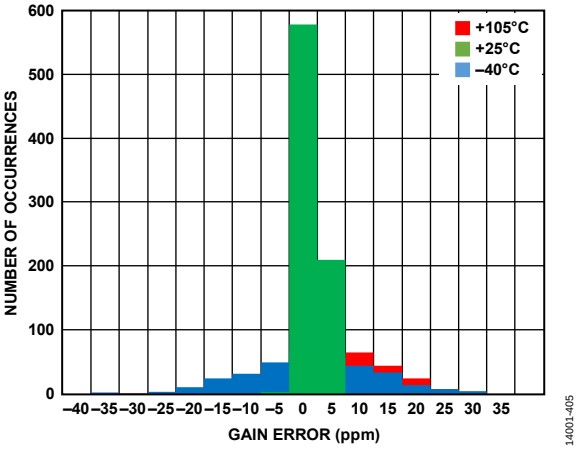

Figure 51. Gain Error Distribution

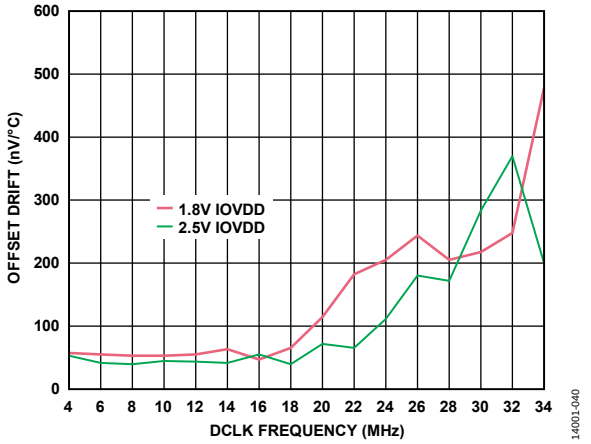

Figure 49. Offset Drift vs. DCLK Frequency

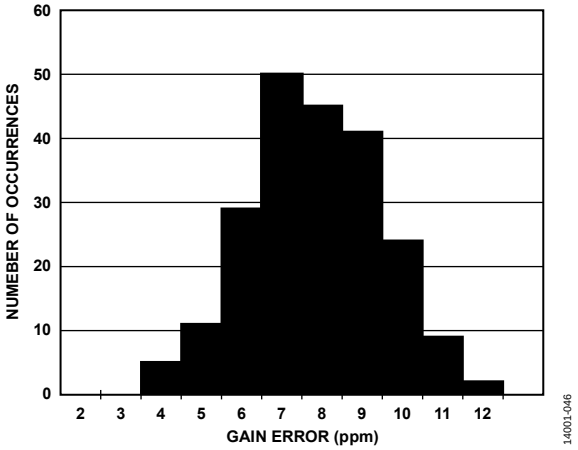

Figure 52. Channel to Channel Gain Error Matching

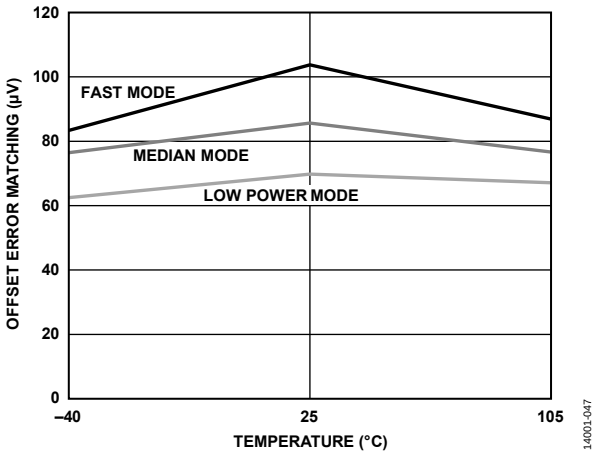

Figure 50. Channel Offset Error Matching

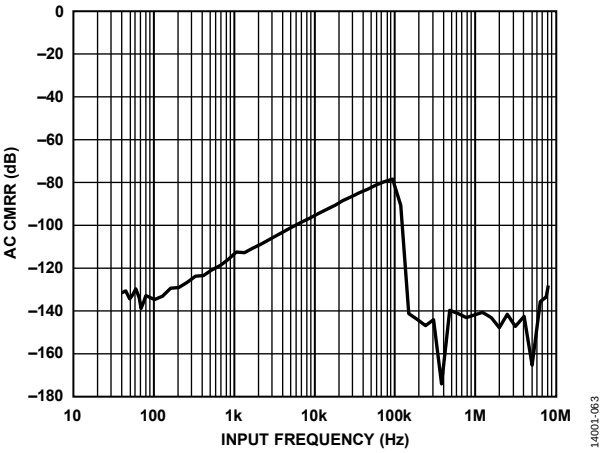

Figure 53. AC CMRR vs. Input Frequency

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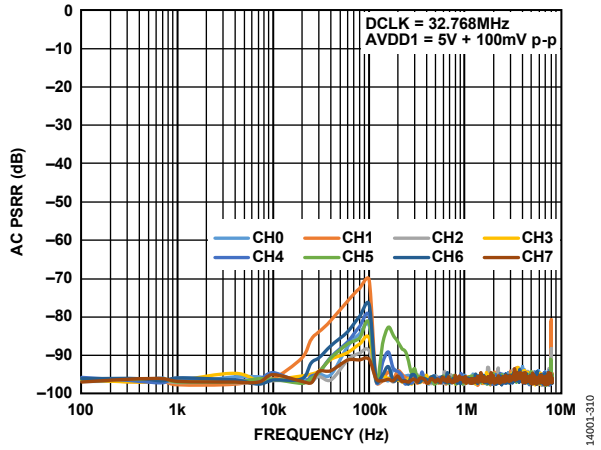

Figure 54. AC PSRR vs. Frequency, AVDD1

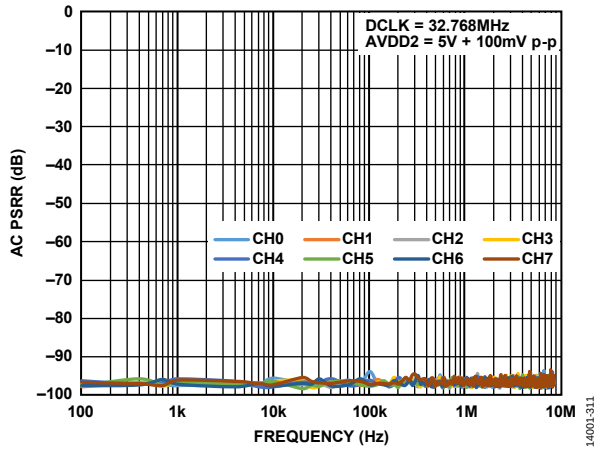

Figure 55. AC PSRR vs. Frequency, AVDD2

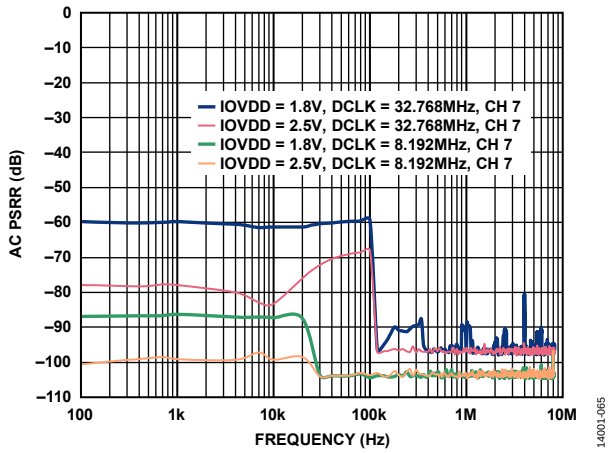

Figure 56. AC PSRR vs. Frequency, IOVDD

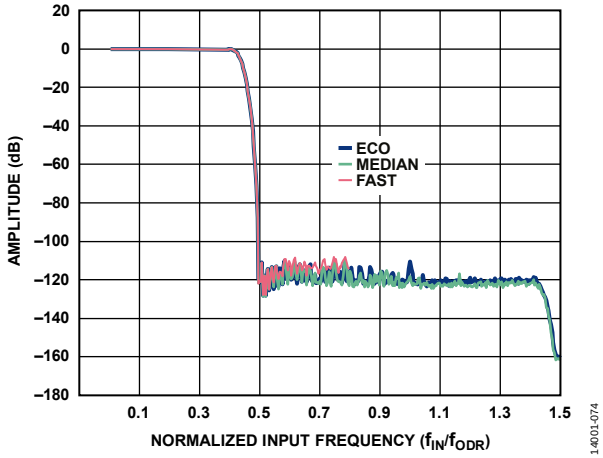

Figure 57. Wideband Filter Profile, Amplitude vs. f_{IN}/f_{ODR}

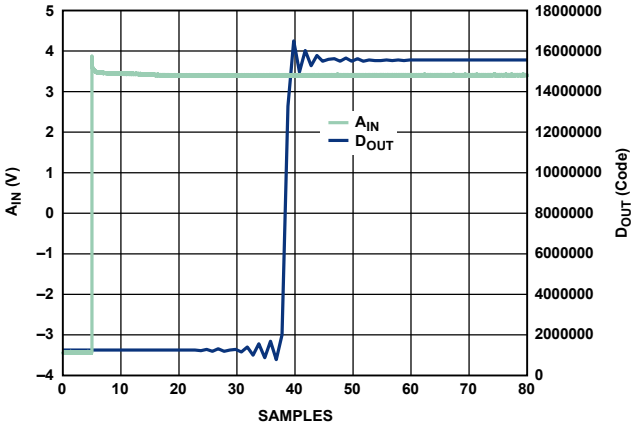

Figure 58. Step Response, Wideband Filter

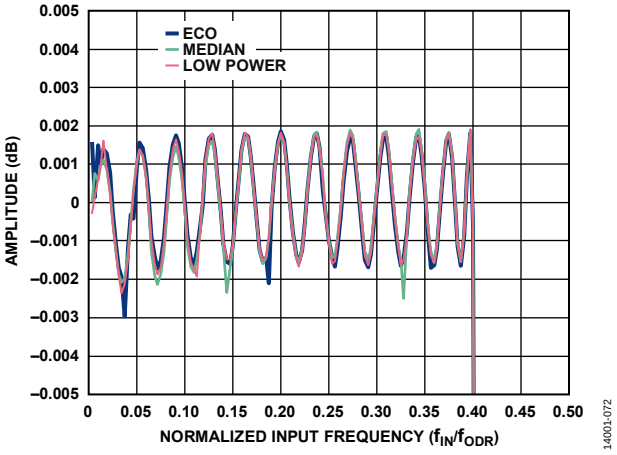

Figure 59. Wideband Filter Ripple

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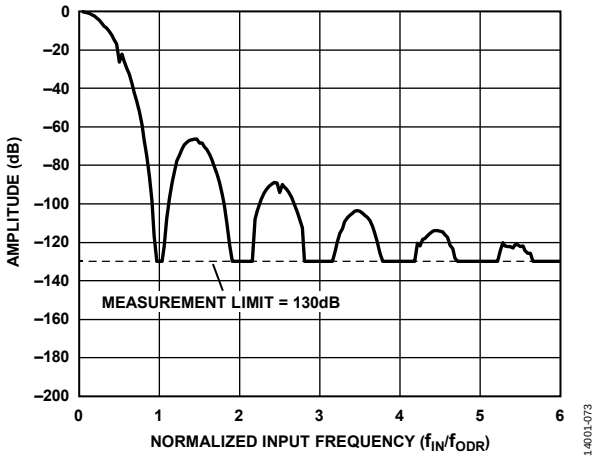

Figure 60. Sinc5 Filter Profile, Amplitude vs. f_{IN}/f_{ODR}

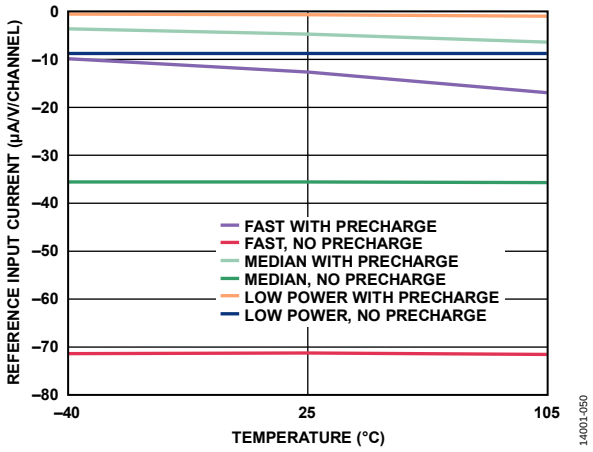

Figure 63. Reference Input Current vs. Temperature, Reference Precharge Buffers On/Off

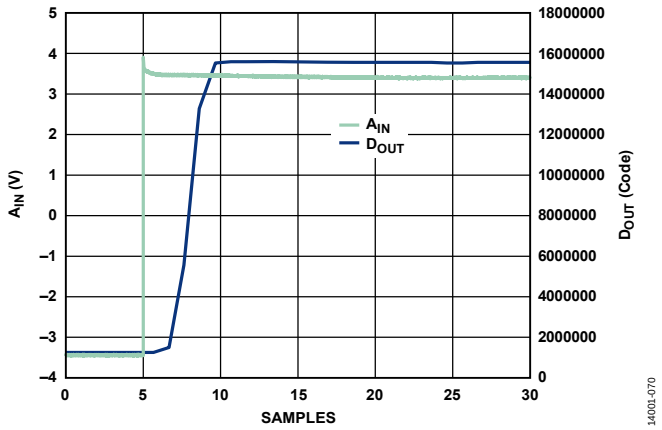

Figure 61. Step Response, Sinc5 Filter

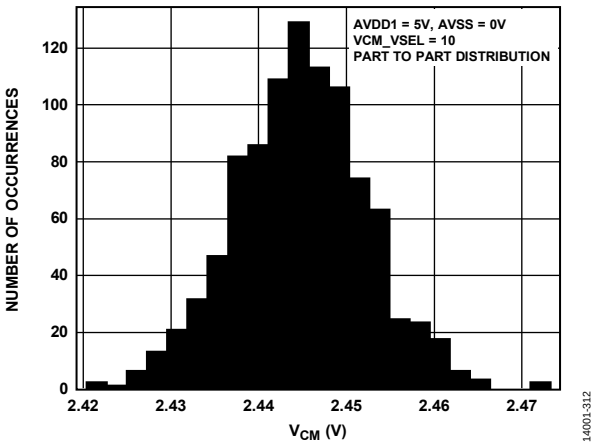

Figure 64. VCM Output Voltage Distribution

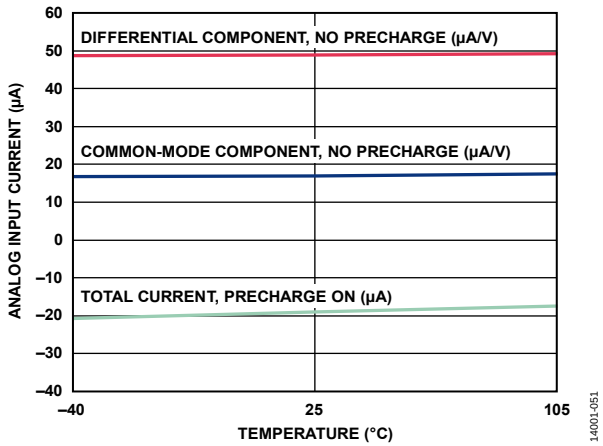

Figure 62. Analog Input Current vs. Temperature, Analog Input Precharge Buffers On/Off

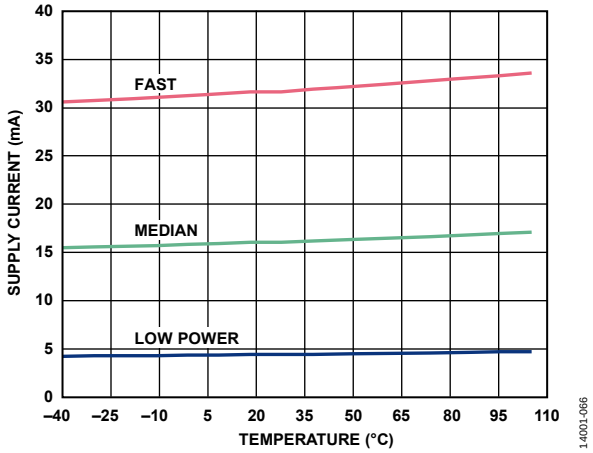

Figure 65. Supply Current vs. Temperature, AVDD1

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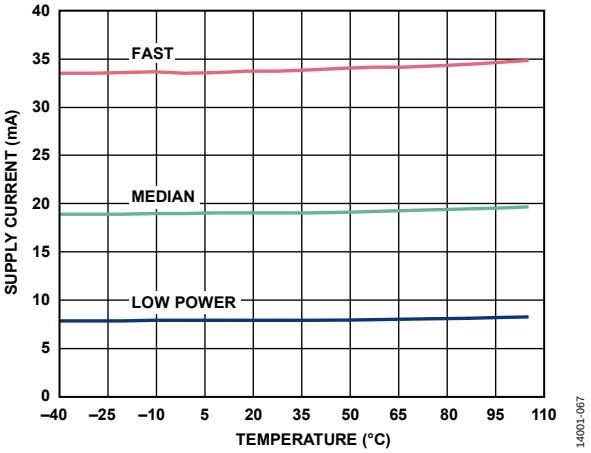

Figure 66. Supply Current vs. Temperature, AVDD2

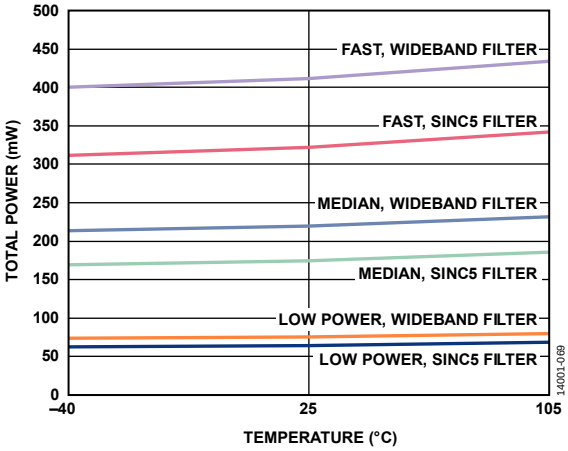

Figure 68. Total Power vs. Temperature

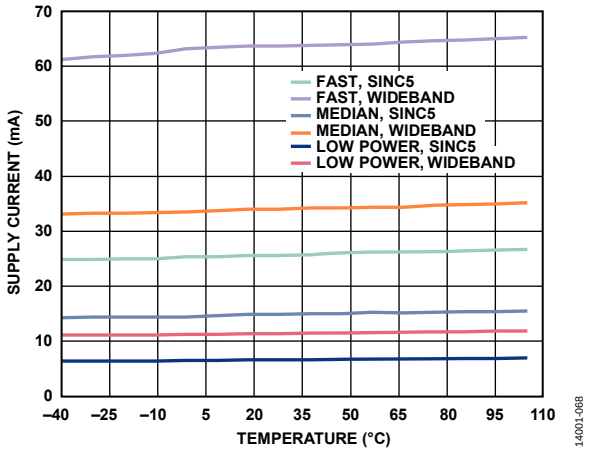

Figure 67. Supply Current vs. Temperature, IOVDD

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TERMINOLOGY

AC Common-Mode Rejection Ratio (AC CMRR)
AC CMRR is defined as the ratio of the power in the ADC output at frequency, f, to the power of a sine wave applied to the common-mode voltage of AINx+ and AINx− at frequency, f_S.

$$AC\ CMRR\ (\text{dB}) = 10\log(Pf/Pf_S)$$

where:
Pf is the power at frequency, *f*, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Gain Error
The first transition (from 100 … 000 to 100 … 001) occurs at a level ½ LSB above nominal negative full scale (−4.0959375 V for the ±4.096 V range). The last transition (from 011 … 110 to 011 … 111) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.0959375 V for the ±4.096 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Drift
Gain error drift is the gain error change due to a temperature change of 1°C. It is expressed in parts per million per degree Celsius.

Integral Nonlinearity (INL) Error
INL error refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at the sum and difference frequencies of mfa and nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m or n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7768/AD7768-4 are tested using the CCIF standard, where two input frequencies near to each other are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second-order and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in decibels.

Least Significant Bit (LSB)
The least significant bit, or LSB, is the smallest increment that can be represented by a converter. For a fully differential input ADC with N bits of resolution, the LSB expressed in volts is as follows:

$$LSB\ (\text{V}) = (2 \times V_{REF})/2^N$$

For the AD7768/AD7768-4, V_{REF} is the difference voltage between the REFx+ and REFx− pins, and N = 24.

Offset Error
Offset error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Power Supply Rejection Ratio (PSRR)
Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the full-scale transition point due to a change in the power supply voltage from the nominal value.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal (excluding the first five harmonics).

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

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THEORY OF OPERATION

The AD7768 and AD7768-4 are 8-channel and 4-channel, simultaneously sampled, low noise, 24-bit Σ-Δ ADCs, respectively.

Each ADC within the AD7768/AD7768-4 employs a Σ-Δ modulator whose clock runs at a frequency of f_{MOD}. The modulator samples the inputs at a rate of $2 \times f_{MOD}$ to convert the analog input into an equivalent digital representation. These samples therefore represent a quantized version of the analog input signal.

The Σ-Δ conversion technique is an oversampled architecture. This oversampled approach spreads the quantization noise over a wide frequency band (see Figure 69). To reduce the quantization noise in the signal band, the high order modulator shapes the noise spectrum so that most of the noise energy is shifted out of the band of interest (see Figure 70). The digital filter that follows the modulator removes the large out of band quantization noise (see Figure 71).

For further information on the basics as well as more advanced concepts of Σ-Δ ADCs, see the MT-022 Tutorial and the MT-023 Tutorial.

Digital filtering has certain advantages over analog filtering. First, it is insensitive to component tolerances and the variation of component parameters over time and temperature. Because digital filtering on the AD7768/AD7768-4 occurs after the analog to digital conversion, it can remove some of the noise injected during the conversion process; analog filtering cannot remove noise injected during conversion. Second, the digital filter combines low pass-band ripple with a steep roll-off, and high stop band attenuation, while also maintaining a linear phase response, which is difficult to achieve in an analog filter implementation.

Figure 69. Σ-Δ ADC Quantization Noise (Linear Scale X-Axis)

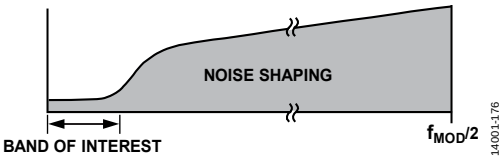

Figure 70. Σ-Δ ADC Noise Shaping (Linear Scale X-Axis)

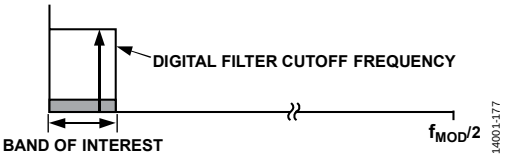

Figure 71. Σ-Δ ADC Digital Filter Cutoff Frequency (Linear Scale X-Axis)

CLOCKING, SAMPLING TREE, AND POWER SCALING

The AD7768/AD7768-4 include multiple ADC cores. Each of these ADCs receives the same master clock signal, MCLK. The MCLK signal can be sourced from one of three options: a CMOS clock, a crystal connected between the XTAL1 and XTAL2 pins, or in the form of an LVDS signal. The MCLK signal received by the AD7768/AD7768-4 defines the modulator clock rate, f_{MOD}, and, in turn, the sampling frequency of the modulator of $2 \times f_{MOD}$. The same MCLK signal is also used to define the digital output clock, DCLK. The f_{MOD} and DCLK internal signals are synchronous with MCLK.

Figure 72 illustrates the clock tree from the MCLK input to the modulator, the digital filter, and the DCLK output. There are divider settings for MCLK and DCLK. These dividers in conjunction with the power mode and digital filter decimation settings are key to AD7768/AD7768-4 operation.

The AD7768/AD7768-4 have the ability to scale power consumption vs. the input bandwidth or noise desired. The user controls two parameters to achieve this: MCLK division and power mode. Combined, these two settings determine the clock frequency of the modulator (f_{MOD}) and the bias current supplied to each modulator. The power mode (fast, median, or low power) sets the noise, speed capability, and current consumption of the modulator. The power mode is the dominant control for scaling the power consumption of the ADC. All settings of MCLK division and power mode apply to all ADC channels.

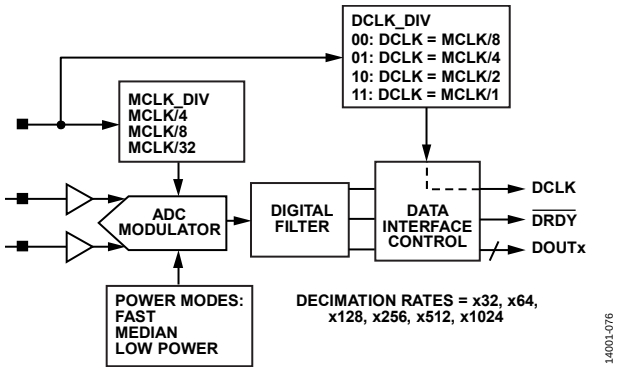

Figure 72. Sampling Structure, Defined by MCLK, DCLK_DIV, and MCLK_DIV Settings

The modulator clock frequency (f_{MOD}) is determined by selecting one of three clock divider settings: MCLK/4, MCLK/8, or MCLK/32.

Although the MCLK division and power modes are independent settings, there are restrictions that must be adhered to. A valid range of modulator frequencies exists for each power mode. Table 11 describes this recommended range, which allows the device to achieve the best performance while minimizing power consumption. The AD7768/AD7768-4 specifications do not cover the performance and function beyond the maximum f_{MOD} for a given power mode.

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For example, in fast mode, to maximize the speed of conversion or input bandwidth, an MCLK of 32.768 MHz is required and MCLK_DIV = 4 must be selected for a modulator frequency of 8.192 MHz.

Table 11. Recommended f_{MOD} Range for Each Power Mode

Power Mode	Recommended f_{MOD} (MHz) Range, MCLK = 32.768 MHz
Low Power	0.036 to 1.024
Median	1.024 to 4.096
Fast	4.096 to 8.192

Control of the settings for power mode, the modulator frequency and the data clock frequency differs in pin control mode vs. SPI control mode.

In SPI control mode, the user can program the power mode, MCLK divider (MCLK_DIV), and DCLK frequency using Register 0x04 and Register 0x07 (see Table 42 and Table 45 for register information for the AD7768 or Table 68 and Table 71 for the AD7768-4). Independent selection of the power mode and MCLK_DIV allows full freedom in the MCLK speed selection to achieve a target modulator frequency.

In pin control mode, the MODEx pins determine the power mode, modulator frequency, and DCLK frequency. The modulator frequency tracks the power mode. This means that f_{MOD} is fixed at MCLK/32 for low power mode, MCLK/8 for median mode, and MCLK/4 for fast mode (see Table 20).

Example of Power vs. Noise Performance Optimization

Depending on the bandwidth of interest for the measurement, the user can choose a strategy of either lowest current consumption or highest resolution. This choice is due to an overlap in the coverage of each power mode. The devices offer the ability to balance the MCLK division ratio with the rate of decimation (averaging) set in the digital filter. Lower power can be achieved by using lower modulator clock frequencies. Conversely, the highest resolution can be achieved by using higher modulator clock frequencies and maximizing the amount of oversampling.

As an example, consider a system constraint with a maximum available MCLK of 16 MHz. The system is targeting a measurement bandwidth of approximately 25 kHz with the wideband filter, setting the output data rate of the AD7768/AD7768-4 to 62.5 kHz. Because of the low MCLK frequency available and system power budget, median power mode is used.

In median power mode, this 25 kHz input bandwidth can be achieved by setting the MCLK division and decimation ratio to balance, using two configurations. This flexibility is possible in SPI control mode only.

Configuration A

To maximize the dynamic range, use the following settings:

- MCLK = 16 MHz
- Median power
- f_{MOD} = MCLK/4
- Decimation = ×64 (digital filter setting)
- ODR = 62.5 kHz

This configuration maximizes the available decimation rate (or oversampling ratio) for the bandwidth required and MCLK rate available. The decimation averages the noise from the modulator, maximizing the dynamic range.

Configuration B

To minimize power, use the following settings:

- MCLK = 16 MHz
- Median power
- f_{MOD} = MCLK/8
- Decimation = ×32 (digital filter setting)
- ODR = 62.5 kHz

This configuration reduces the clocking speed of the modulator and the digital filter.

Compared to Configuration A, Configuration B saves 48 mW of power. The trade-off in the case of Configuration B is that the digital filter must run at a 2× lower decimation rate. This 2× reduction in decimation rate (or oversampling ratio) results in a 3 dB reduction in the dynamic range vs. Configuration A.

Clocking Out the ADC Conversion Results (DCLK)

The AD7768/AD7768-4 DCLK is a divided version of the master clock input. As shown in Figure 72, the DCLK_DIV setting determines the speed of the DCLK. DCLK is a continuous clock.

The user can set the DCLK frequency rate to one of four divisions of MCLK: MCLK/1, MCLK/2, MCLK/4, and MCLK/8. Because there are eight channels and 32 bits of data per conversion, the conversion time and the setting of DCLK directly determine the number of data output lines that are required via the FORMAT0 and FORMAT1 pin settings on the AD7768, or the FORMAT0 pin on the AD7768-4. Thus, the intended minimum decimation and desired DCLK_DIV setting must be understood prior to choosing the setting of the FORMATx pins.

NOISE PERFORMANCE AND RESOLUTION

Table 12 and Table 13 show the noise performance for the wideband and sinc5 digital filters of the AD7768/AD7768-4 for various output data rates and power modes. The noise values and dynamic range specified are typical for the bipolar input range with an external 4.096 V reference (V_{REF}). The rms noise is measured with shorted analog inputs, which are driven to (AVDD1 − AVSS)/2 using the on-board VCM buffer output.

The dynamic range is calculated as the ratio of the rms shorted input noise to the rms full-scale input signal range.

$$Dynamic\ Range\ (\text{dB}) = 20\log_{10}((2 \times V_{REF}/2\sqrt{2})/(RMS\ Noise)$$

The LSB size with 4.096 V reference is 488 nV, and is calculated as follows:

$$LSB\ (\text{V}) = (2 \times V_{REF})/2^{24}$$

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Table 12. Wideband Filter Noise: Performance vs. Output Data Rate (V_{REF} = 4.096 V)

Output Data Rate (kSPS)	−3 dB Bandwidth (kHz)	Shorted Input Dynamic Range (dB)	RMS Noise (µV)
Fast Mode			
256	110.8	107.96	11.58
128	55.4	111.43	7.77
64	27.7	114.55	5.42
32	13.9	117.58	3.82
16	6.9	120.56	2.72
8	3.5	123.5	1.94
Median Mode			
128	55.4	108.13	11.36
64	27.7	111.62	7.6
32	13.9	114.75	5.3
16	6.9	117.79	3.74
8	3.5	120.8	2.64
4	1.7	123.81	1.87
Low Power Mode			
32	13.9	108.19	11.28
16	6.9	111.69	7.54
8	3.5	114.83	5.25
4	1.7	117.26	3.71
2	0.87	120.88	2.62
1	0.43	123.88	1.85

Table 13. Sinc5 Filter Noise: Performance vs. Output Data Rate (V_{REF} = 4.096 V)

Output Data Rate (kSPS)	−3 dB Bandwidth (kHz)	Shorted Input Dynamic Range (dB)	RMS Noise (µV)
Fast Mode			
256	52.224	111.36	7.83
128	26.112	114.55	5.43
64	13.056	117.61	3.82
32	6.528	120.61	2.71
16	3.264	123.52	1.93
8	1.632	126.39	1.39
Median Mode			
128	26.112	111.53	7.68
64	13.056	114.75	5.3
32	6.528	117.81	3.72
16	3.264	120.82	2.64
8	1.632	123.82	1.87
4	0.816	126.79	1.33
Low Power Mode			
32	6.528	111.57	7.65
16	3.264	114.82	5.26
8	1.632	117.88	3.7
4	0.816	120.9	2.61
2	0.408	123.91	1.85
1	0.204	126.89	1.31

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APPLICATIONS INFORMATION

The AD7768/AD7768-4 offer users a multichannel platform measurement solution for ac and dc signal processing.

Flexible filtering allows the AD7768/AD7768-4 to be configured to simultaneously sample ac and dc signals on a per channel basis. Power scaling allows users to trade off the input bandwidth of the measurement vs. the current consumption. This ability, coupled with the flexibility of the digital filtering, allows the user to optimize the energy efficiency of the measurement, while still meeting power, bandwidth, and performance targets.

Key capabilities that allow users to choose the AD7768/AD7768-4 as their platform high resolution ADC are highlighted as follows:

- Eight fully differential or pseudo differential analog inputs on the AD7768 (four channels on the AD7768-4).
- Fast throughput simultaneous sampling ADCs catering for input signals up to 110.8 kHz.
- Three selectable power modes (fast, median, and low power) for scaling the current consumption and input bandwidth of the ADC for optimal measurement efficiency.
- Analog input precharge and reference precharge buffers reduce the drive requirements of external amplifiers.
- Control of reference and analog input precharge buffers on a per channel basis.
- Wideband, low ripple, digital filter for ac measurement.
- Fast sinc5 filter for precision low frequency measurement.
- Two channel modes, defined by the user selected filter choice, and decimation ratios, can be defined for use on different ADC channels. This enables optimization of the input bandwidth versus the signal of interest.
- Option of SPI or pin strapped control and configuration.
- Offset, gain, and phase calibration registers per channel.
- Common-mode voltage output buffer for use by driver amplifier.
- On-board AVDD2 and IOVDD LDOs for the low power, 1.8 V, internal circuitry.

Refer to Figure 73 and Table 14 for the typical connections and minimum requirements to get started using the AD7768/AD7768-4.

Table 15 shows the typical power and performance of the AD7768/AD7768-4 for the available power modes, for each filter type.

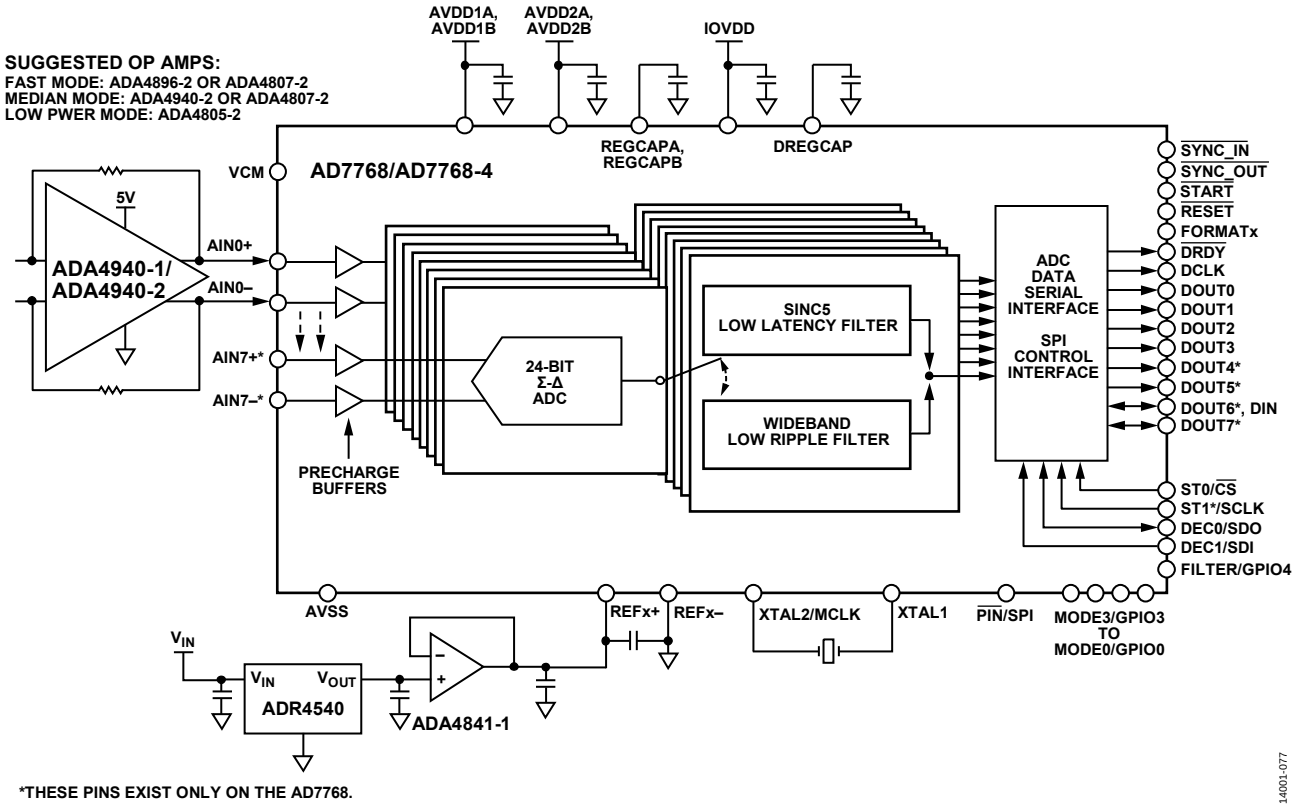

Figure 73. Typical Connection Diagram

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Table 14. Requirements to Operate the AD7768/AD7768-4

Requirement	Description
Power Supplies	5 V AVDD1 supply, 2.25 V to 5 V AVDD2 supply, 1.8 V or 2.5 V to 3.3 V IOVDD supply (ADP7104/ADP7118)
External Reference	2.5 V, 4.096 V, or 5 V (ADR4525, ADR4540, or ADR4550)
External Driver Amplifiers	The ADA4896-2, the ADA4940-1/ADA4940-2, the ADA4805-2, and the ADA4807-2
External Clock	Crystal or a CMOS/LVDS clock for the ADC modulator sampling
FPGA or DSP	Input/output voltage of 2.5 V to 3.6 V, or 1.8 V (see the 1.8 V IOVDD Operation section)

Table 15. Speed, Dynamic Range, THD, and Power Overview; Eight Channels Active, Decimate by 32[1]

			Sinc5 Filter			Wideband Filter		
Power Mode	Output Data Rate (kSPS)	THD (dB)	Dynamic Range (dB)	Bandwidth (kHz)	Power Dissipation (mW per channel)	Dynamic Range (dB)	Bandwidth (kHz)	Power Dissipation (mW per channel)
Fast	256	−115	111	52.224	41	108	110.8	52
Median	128	−120	111	26.112	22	108	55.4	28
Low Power	32	−120	111	6.528	8.5	108	13.9	9.5

[1] Analog precharge buffers on, reference precharge buffers and VCM disabled, typical values, AVDD1 = 5 V, AVDD2 = IOVDD = 2.5 V, V_{REF} = 4.096 V, MCLK = 32.768 MHz, DCLK = MCLK/4, T_A = 25°C.

POWER SUPPLIES

The AD7768/AD7768-4 have three independent power supplies: AVDD1 (AVDD1A and AVDD2A), AVDD2 (AVDD2A and AVDD2B), and IOVDD.

The reference potentials for these supplies are AVSS and DGND. Tie all the AVSS supply pins (AVSS1A, AVSS1B, AVSS2A, AVSS2B, and AVSS) to the same potential with respect to DGND. AVDD1A, AVDD1B, AVDD2A, and AVDD2B are referenced to this AVSS rail. IOVDD is referenced to DGND.

The supplies can be powered within the following ranges:

- AVDD1 = 5 V ± 10%, relative to AVSS
- AVDD2 = 2 V to 5.5 V, relative to AVSS
- IOVDD (with internal regulator) = 2.25 V to 3.6 V, relative to DGND
- IOVDD (bypassing regulator) = 1.72 V to 1.88 V, relative to DGND
- AVSS = −2.75 V to 0 V, relative to DGND

The AVDD1A and AVDD1B (AVDD1) supplies power the analog front end, reference input, and common-mode output circuitry. AVDD1 is referenced to AVSS, and all AVDD1 supplies must be tied to the same potential with respect to AVSS. If AVDD1 supplies are used in a ±2.5 V split supply configuration, the ADC inputs are truly bipolar. When using split supplies, reference the absolute maximum ratings, which apply to the voltage allowed between AVSS and IOVDD supplies.

The AVDD2A and AVDD2B (AVDD2) supplies connect to internal 1.8 V analog LDO regulators. The regulators power the ADC core. AVDD2 is referenced to AVSS, and all AVDD2 supplies must be tied to the same potential with respect to AVSS. The voltage on AVDD2 can range from 2 V (minimum) to 5.5 V (maximum), with respect to AVSS.

IOVDD powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. IOVDD also sets the voltage levels for the SPI interface of the ADC. IOVDD is referenced to DGND, and the voltage on IOVDD can vary from 2.25 V (minimum) to 3.6 V (maximum), with respect to DGND. IOVDD can also be configured to run at 1.8 V. In this case, IOVDD and DREGCAP must be tied together and must be within the range of 1.72 V (minimum) to 1.88 V (maximum), with respect to DGND. See the 1.8 V IOVDD Operation section for more information on operating the AD7768/AD7768-4 at 1.8 V IOVDD.

Recommended Power Supply Configuration

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a power solution that uses the ADP7118 is shown in Figure 74. The ADP7118 provides positive supply rails for optimal converter performance, creating either a single 5 V, 3.3 V, or dual AVDD1x and AVDD2x/IOVDD, depending on the required supply configuration. The ADP7118 can operate from input voltages of up to 20 V.

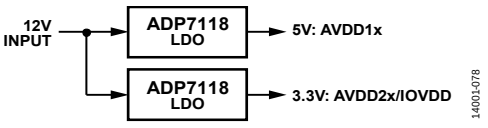

Figure 74. Power Supply Configuration

Alternatively, the ADP7112 or ADP7104 can be selected for powering the AD7768/AD7768-4. Refer to the AN-1120 Application Note for more information regarding low noise LDO performance and power supply filtering.

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1.8 V IOVDD Operation

The AD7768/AD7768-4 contain an internal 1.8 V LDO on the IOVDD supply to regulate the IOVDD down to the operating voltage of the digital core. This internal LDO allows the internal logic to operate efficiently at 1.8 V and the input/output logic to operate at the level set by IOVDD. The IOVDD supply is rated from 2.25 V to 3.6 V for normal operation, and 1.8 V for LDO bypass setup.

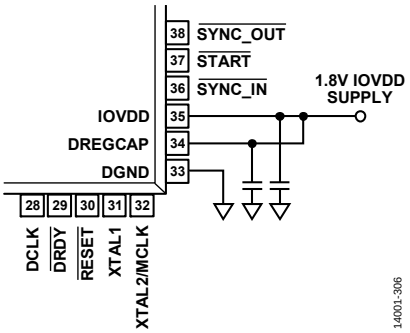

Figure 75. DREGCAP and IOVDD Connection Diagram for 1.8 V IOVDD Operation

Users can bypass the LDO by shorting the DREGCAP pin to IOVDD (see Figure 75), which pulls the internal LDO out of regulation and sets the internal core voltage and input/output logic levels to the IOVDD level. When bypassing the internal LDO, the maximum operating voltage of the IOVDD supply is equal to the maximum operating voltage of the internal digital core, which is 1.72 V to 1.88 V.

There are a number of performance differences to consider when operating at 1.8 V IOVDD. See the 1.8 V IOVDD Specifications section for detailed specifications while operating at 1.8 V IOVDD.

Analog Supply Internal Connectivity

The AD7768/AD7768-4 have two analog supply rails, AVDD1 and AVDD2, which are both referred to AVSS. These supplies are completely separate from the digital pins IOVDD, DREGCAP, and DGND. To achieve optimal performance and isolation of the ADCs, more than one device pin supplies these analog rails to the internal ADCs.

- AVSS1A (Pin 3) and AVSS2A (Pin 62) are internally connected.
- AVSS (Pin 54) is connected to the substrate, and is connected internally to AVSS1B (Pin 46) and AVSS2B (Pin 51).
- The following supply and reference input pins are separate on chip: AVDD1A, AVDD1B, AVDD2A, AVDD2B, REF1+, REF1−, REF2+, and REF2−.
- On the AD7768-4, the following AVSS pins are separate on chip: Pin 7, Pin 8, Pin 9, Pin 10, Pin 39, Pin 40, Pin 41, and Pin 42.

The details of which individual supplies are shorted internally are given in this section for information purposes. In general, connect the supplies as described in the Power Supplies section.

DEVICE CONFIGURATION

The AD7768/AD7768-4 have independent paths for reading data from the ADC conversions and for controlling the device functionality.

For control, the device can be configured in either of two modes. The two modes of configuration are

- Pin control mode: pin strapped digital logic inputs (which allows a subset of the configurability options)
- SPI control mode: over a 3-wire or 4-wire SPI interface (complete configurability)

On power-up, the state of the $\overline{\text{PIN}}$/SPI pin determines the mode used. Immediately after power-up, the user must apply a soft or hard reset to the device when using either control mode.

Interface Data Format

When operating the device, the data format of the serial interface is determined by the FORMAT0 and FORMAT1 pin settings on the AD7768, or the FORMAT0 pin on the AD7768-4. Table 33 shows that each ADC can be assigned a DOUTx pin, or, alternatively, the data can be arranged to share the DOUTx pins in a time division multiplexed manner. For more details, see the Data Interface section.

PIN CONTROL

Pin control mode eliminates the need for an SPI communication interface. When a single known configuration is required by the user, or when only limited reconfiguration is required, the number of signals that require routing to the digital host can be reduced using this mode. Pin control mode is useful in digitally isolated applications where minimal adjustment of the configuration is needed. Pin control offers a subset of the core functionality and ensures a known state of operation after power-up, reset, or a fault condition on the power supply. In pin control mode, the analog input precharge buffers are enabled by default for best performance. The reference input precharge buffers are disabled in pin control mode.

After any change to the configuration in pin control mode, the user must provide a sync signal to the AD7768/AD7768-4 by applying the appropriate pulse to the $\overline{\text{START}}$ pin or $\overline{\text{SYNC_IN}}$ pin to ensure that the configuration changes are applied correctly to the ADC and digital filters.

Setting the Filter

The filter function chooses between the two filter settings. In pin control mode, all ADC channels use the same filter type, which is selected by the FILTER pin, as shown in Table 16.

Table 16. FILTER Control Pin

Logic Level	Function
1	Sinc5 filter selected
0	Wideband filter selected

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Setting the Decimation Rate

Pin control mode allows selection from four possible decimation rates. The decimation rate is selected via the DEC1 and DEC0 pins. The chosen decimation rate is used on all ADC channels. Table 17 shows the truth table for the DECx pins.

Table 17. Decimation Rate Control Pins Truth Table

DEC1	DEC0	Decimation Rate
0	0	×32
0	1	×64
1	0	×128
1	1	×1024

Operating Mode

The MODE3 to MODE0 pins determine the configuration of all channels when using pin control mode. The variables controlled by the MODEx pins are shown in Table 18. The user selects how much current the device consumes, the sampling speed of the ADC (power mode), how fast the ADC result is received by the digital host (DCLK_DIV), and how the ADC conversion is initiated (conversion operation). Figure 76 illustrates the inputs used to configure the AD7768 in pin control mode, and Figure 77 illustrates the inputs used to configure the AD7768-4 in pin control mode.

Table 18. MODEx Pins: Variables for Control

Control Variable	Possible Settings
Sampling Speed/Power Consumption Power Mode	Fast mode Median mode Low Power mode
Data Clock Output Frequency (DCLK_DIV)	DCLK = MCLK/1 DCLK = MCLK/2 DCLK = MCLK/4 DCLK = MCLK/8
Conversion Operation	Standard conversion One-shot conversion

The MODEx pins map to 16 distinct settings. The settings are selected to optimize the use cases of the AD7768/AD7768-4, allowing the user to reduce the DCLK frequency for lower, less demanding power modes and selecting either the one-shot or standard conversion modes.

See Table 20 for the complete selection of operating modes that are available via the MODEx pins in pin control mode.

The power mode setting automatically scales the bias currents of the ADC and divides the applied MCLK signal to the correct setting for that mode. Note that this is not the same as using SPI control, where separate bit fields exist to control the bias currents of the ADC and MCLK division.

In pin control mode, the modulator rate is fixed for each power mode to achieve the best performance. Table 19 shows the modulator division for each power mode.

Table 19. Modulator Rate, Pin Control Mode

Power Mode	Modulator Rate, f_{MOD}
Fast	MCLK/4
Median	MCLK/8
Low Power	MCLK/32

Diagnostics

Pin control mode offers a subset of diagnostics features. Internal errors are reported in the status header output with the data conversion results for each channel.

Internal cyclical redundancy check (CRC) errors, memory map flipped bits, and external clocks not detected are reported by Bit 7 of the status header and indicate that a reset is required. The status header also reports filter not settled, filter type, and filter saturated signals. Users can determine when to ignore data by monitoring these error flags. For more information on the status header, see the ADC Conversion Output: Header and Data section.

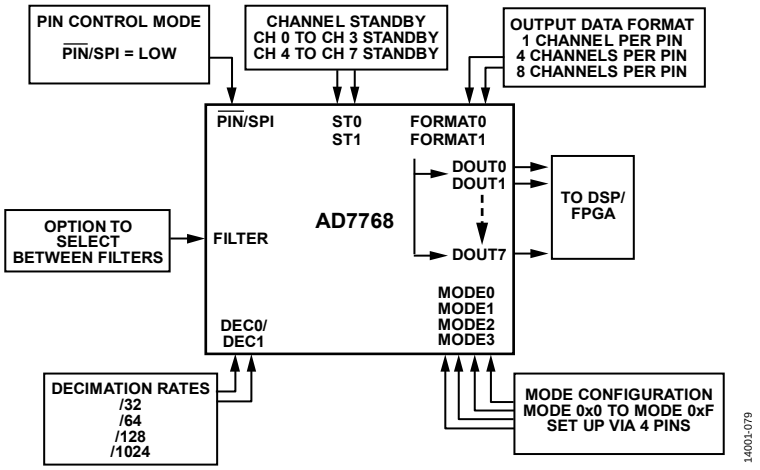

Figure 76. AD7768 Pin Configurable Functions

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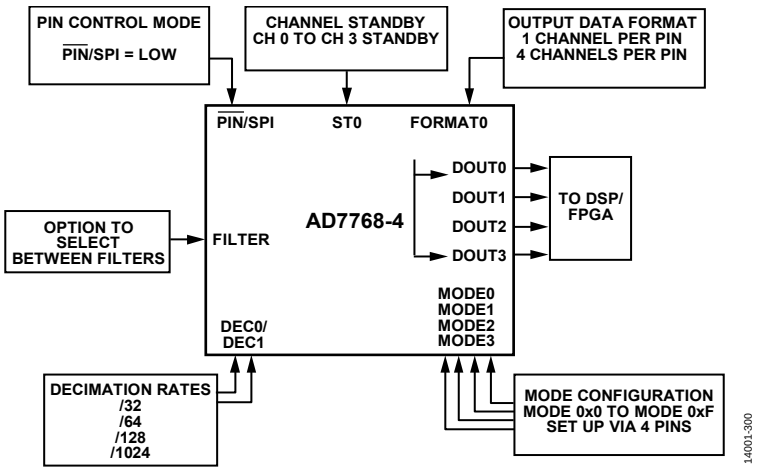

Figure 77. AD7768-4 Pin Configurable Functions

Table 20. MODEx Selection Details: Pin Control Mode

Mode Hex.	MODE3	MODE2	MODE1	MODE0	Power Mode	DCLK Frequency	Data Conversion
0x0	0	0	0	0	Low power	MCLK/1	Standard
0x1	0	0	0	1	Low power	MCLK/2	Standard
0x2	0	0	1	0	Low power	MCLK/4	Standard
0x3	0	0	1	1	Low power	MCLK/8	Standard
0x4	0	1	0	0	Median	MCLK/1	Standard
0x5	0	1	0	1	Median	MCLK/2	Standard
0x6	0	1	1	0	Median	MCLK/4	Standard
0x7	0	1	1	1	Median	MCLK/8	Standard
0x8	1	0	0	0	Fast	MCLK/1	Standard
0x9	1	0	0	1	Fast	MCLK/2	Standard
0xA	1	0	1	0	Fast	MCLK/4	Standard
0xB	1	0	1	1	Fast	MCLK/8	Standard
0xC	1	1	0	0	Low power	MCLK/1	One-shot
0xD	1	1	0	1	Median	MCLK/1	One-shot
0xE	1	1	1	0	Fast	MCLK/2	One-shot
0xF	1	1	1	1	Fast	MCLK/1	One-shot

Configuration Example

In the example shown in Table 23, the lowest current consumption is used, and the AD7768/AD7768-4 are connected to an FPGA. The FORMATx pins are set such that all eight data outputs, DOUT0 to DOUT7, connect to the FPGA. For the lowest power, the lowest DCLK frequency is used. The input bandwidth is set through the combination of selecting decimation by 64 and selecting the wideband filter.

$$ODR = f_{MOD} \div Decimation\ Ratio$$

where:
MCLK = 32.768 MHz.
f_{MOD} is MCLK/32 for low power mode (see Table 19).
Decimation Ratio = 64.

Thus, for this example, where MCLK = 32.768 MHz,

$$ODR = (32.768\ MHz/32) \div 64 = 16\ kHz$$

Minimizing the DCLK frequency means selecting DCLK = MCLK/8, which results in a 4 MHz DCLK signal. The period of DCLK in this case is 1/4 MHz = 250 ns. The data conversion on each DOUTx pin is 32 bits long. The conversion data takes 32 × 250 ns = 8 µs to be output. All 32 bits must be output within the ODR period of 1/16 kHz, which is approximately 64 µs. In this case, the 8 µs required to read out the conversion data is well within the 64 µs between conversion outputs. Therefore, this combination, which is summarized in Table 23, is viable for use.

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Channel Standby

Table 21 and Table 23 show how the user can put channels into standby mode. Set either ST0 or ST1 to Logic 1 to place banks of four channels into standby mode. When in standby mode, the channels are disabled but still hold their position in the output data stream. The 8-bit header and 24-bit conversion result are set to all zeros when the ADC channels are set to standby.

The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768/AD7768-4.

The crystal excitation circuitry is associated with the Channel 4 (Channel 2 on the AD7768-4) circuitry. If Channel 4 (Channel 2 on the AD7768-4) is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768. Channel 2 must be enabled while the external crystal is used on the AD7768-4.

Table 21. Truth Table for the AD7768 ST0 and ST1 Pins

ST1	ST0	Function
0	0	All channels operational.
0	1	Channel 0 to Channel 3 in standby. Channel 4 to Channel 7 operational.
1	0	Channel 4 to Channel 7 in standby. Channel 0 to Channel 3 operational.
1	1	All channels in standby.

Table 22. Truth Table for the AD7768-4 ST0 Pin

ST0	Function
0	All channels operational.
1	Channel 0 to Channel 3 in standby.

SPI CONTROL

The AD7768/AD7768-4 have a 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 0. In SPI Mode 0, SCLK idles low, the falling edge of $\overline{CS}$ clocks out the MSB, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

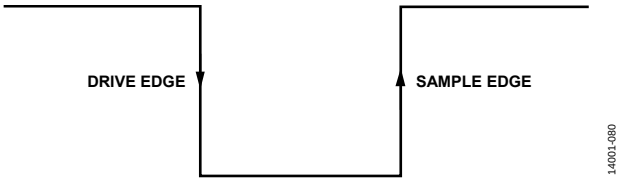

Figure 78. SPI Mode 0 SCLK Edges

Accessing the ADC Register Map

To use SPI control mode, set the $\overline{PIN}$/SPI pin to logic high. The SPI control operates as a 16-bit, 4-wire interface, allowing read and write access. Figure 80 shows the interface format between the AD7768/AD7768-4 and the digital host.

The SPI serial control interface of the AD7768 is an independent path for controlling and monitoring the AD7768. There is no direct link to the data interface. The timing of MCLK and DCLK is not directly related to the timing of the SPI control interface. However, the user must ensure that the SPI reads and writes satisfy the minimum t_{30} specification (see Table 4 and Table 6) so that the AD7768/AD7768-4 can detect changes to the register map.

SPI access is ignored during the period immediately after a reset. Allow the full ADC start-up time after reset (see Table 1) to elapse before accessing the AD7768/AD7768-4 over the SPI interface.

Table 23. MODEx Example Selection

Mode Hex	MODE3	MODE2	MODE1	MODE0	Power Mode	DCLK Frequency	Data Conversion
0x3	0	0	1	1	Low power	MCLK/8	Standard

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SPI Interface Details

Each SPI access frame is 16 bits long. The MSB (Bit 15) of the SDI command is the R/$\overline{W}$ bit; 1 = read and 0 = write. Bits[14:8] of the SDI command are the address bits.

The SPI control interface uses an off frame protocol. This means that the master (FPGA/DSP) communicates with the AD7768/AD7768-4 in two frames. The first frame sends a 16-bit instruction (R/$\overline{W}$, address, and data) and the second frame is the response where the AD7768/AD7768-4 send 16 bits back to the master.

During the master write command, the SDO output contains eight leading zeros, followed by eight bits of data, as shown in Figure 80.

Figure 79 illustrates the off frame protocol. Register access responses are always offset by one $\overline{CS}$ frame. In Figure 79, the response (read RESP 1) to the first command (CMD 1) is output by the AD7768/AD7768-4 during the following $\overline{CS}$ frame at the same time as the second command (CMD 2) is being sent.

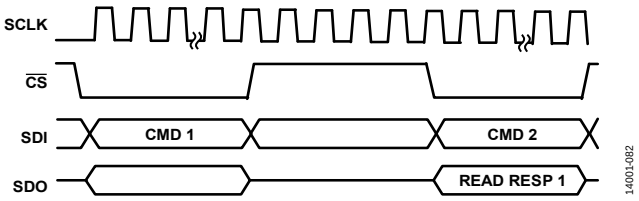

Figure 79. Off Frame Protocol

SPI Control Interface Error Handling

The AD7768/AD7768-4 SPI control interface detects whether it has received an illegal command. An illegal command is a write to a read only register, a write to a register address that does not exist, or a read from a register address that does not exist. If any of these illegal commands are received by the AD7768/AD7768-4, the AD7768/AD7768-4 responds with an error output of 0x0E00.

SPI Reset Configuration

After a power-on or reset, the AD7768/AD7768-4 default configuration is set to the following low current consumption settings:

- Low power mode with f_{MOD} = MCLK/32.
- Interface configuration of DCLK = MCLK/8, header output enabled, and CRC disabled.
- Filter configuration of Channel Mode A and Channel Mode B is set to sinc5 and decimation = ×1024.
- Channel mode select is set to 0x00, and all channels are assigned to Channel Mode A.
- The analog input precharge buffers are enabled and the reference precharge buffers are disabled on all channels.
- The offset, gain, and phase calibration are set to the zero position.
- Continuous conversion mode is enabled.

SPI CONTROL FUNCTIONALITY

SPI control offers the superset of flexibility and diagnostics to the user. The following sections highlight the functionality and diagnostics offered when SPI control is used.

After any change to these configuration register settings, the user must provide a sync signal to the AD7768/AD7768-4 through either the SPI_SYNC command, or by applying the appropriate pulse to the $\overline{START}$ pin or $\overline{SYNC_IN}$ pin to ensure that the configuration changes are applied correctly to the ADC and digital filters.

Channel Configuration

The AD7768 has eight fully differential analog input channels. The AD7768-4 has four fully differential analog input channels. The channel configuration registers allow the channel to be individually configured to adapt to the measurement required on that channel. Channels can be enabled or disabled using the channel standby register, Register 0x00. Analog input and reference precharge buffers can be assigned per input terminal. Gain, offset, and phase calibration can be controlled on a per channel basis using the calibration registers. See the Per Channel Calibration Gain, Offset, and Sync Phase section for more information.

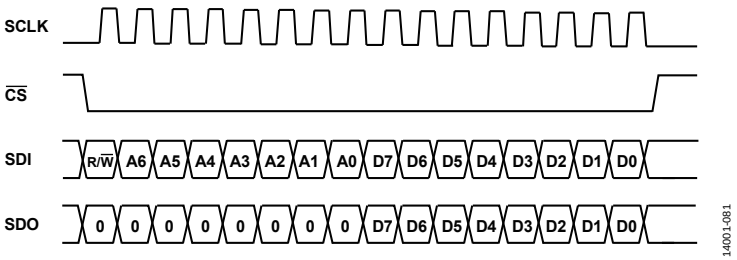

Figure 80. Write/Read Command

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Channel Modes

In SPI control mode, the user can set up two channel modes, Channel Mode A (Register 0x01), and Channel Mode B (Register 0x02). Each channel mode register can have a specific filter type and decimation ratio. Using the channel mode select register (Register 0x03), the user can assign each channel to either Channel Mode A or Channel Mode B, which maps that mode to the required ADC channels. These modes allow different filter types and decimation rates to be selected and mapped to any of the ADC channels.

When different decimation rates are selected on different channels, the AD7768/AD7768-4 output a data ready signal at the fastest selected decimation rate. Any channel that runs at a lower output data rate is updated only at that slower rate. In between valid result data, the data for that channel is set to zero and the repeated data bit is set in the header status bits to distinguish it from a real conversion result (see the ADC Conversion Output: Header and Data section).

On the AD7768, consider Channel Mode A as the primary group. In this respect, it is recommended that there always be at least one channel assigned to Channel Mode A. If all eight channels of the AD7768 are assigned to Channel Mode B, conversion data is not output on the data interface for any of the channels. This consideration does not affect the AD7768-4.

On the AD7768-4, it is recommended that Channel Mode A be set to the sinc5 filter whenever possible. There is a small power saving in IOVDD current when Channel Mode A is set to the sinc5 filter compared to setting Channel Mode A to the wideband filter.

For example, to assign two channels of the AD7768-4 to the wideband filter, and the remaining two channels to the sinc5 filter, it is recommended to assign the two sinc5 filter channels to Channel Mode A. Set Channel Mode A to the sinc5 filter, set Channel Mode B to the wideband filter, and assign the two wideband filter channels to Channel Mode B. Similarly, to assign all four channels of the AD7768-4 to wideband filter, assign all four channels to Channel Mode B. Set Channel Mode B to the wideband filter, and keep Channel Mode A set to the sinc5 filter. Assigning the channels in this way ensures that the lowest IOVDD current is achieved.

Table 24. Channel Mode A/Channel Mode B, Register 0x01 and Register 0x02

Bits	Bit Name	Setting	Description	Reset	Access
3	FILTER_TYPE_x		Filter output	0x1	RW
		0	Wideband filter		
		1	Sinc5 filter		
[2:0]	DEC_RATE_x		Decimation rate	0x5	RW
		000 to 101	×32 to ×1024		

Table 25. Channel Mode Selection, Register 0x03

Bits	Bit Name	Setting	Description	Reset	Access
[7:0]	CH_x_MODE		Channel x	0x0	RW
		0	Mode A		
		1	Mode B		

Reset over SPI Control Interface

Two successive commands must be written to the AD7768/AD7768-4 data control register to initiate a full reset of the device over the SPI interface. This action fully resets all registers to the default conditions. Details of the commands and their sequence are shown in Table 44 for the AD7768 or Table 70 for the AD7768-4.

After a reset over the SPI control interface, the AD7768/AD7768-4 respond to the first command sent to them with 0x0E00. This response, in addition to the fact that all registers have assumed their default values, indicates that the software reset succeeded.

Sleep Mode

Sleep mode puts the AD7768/AD7768-4 into their lowest power mode. In sleep mode, all ADCs are disabled and a large portion of the digital core is inactive.

The AD7768/AD7768-4 SPI remains active and is available to the user when in sleep mode. Write to Register 0x04, Bit 7 to exit sleep mode. For the lowest power consumption, select the sinc5 filter before entering sleep mode.

Channel Standby

For efficient power usage, users can place the selected channels into standby mode, effectively disabling them, when not in use. Setting the bits in Register 0x00 disables the corresponding channel (see Table 38 for the AD7768 or Table 64 for the AD7768-4). For maximum power savings, switch disabled channels to the sinc5 filter using the channel mode configurations, which disables some clocks associated with the wideband filters of those channels.

For highest power savings when disabling channels on the AD7768-4, set Channel Mode A to the sinc5 filter, and assign the disabled channels to Channel Mode A, while keeping any active channels in Channel Mode B.

The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768/AD7768-4.

The crystal excitation circuitry is associated with the Channel 4 (Channel 2 on the AD7768-4) circuitry. If Channel 4 (Channel 2 on the AD7768-4) is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768. Channel 2 must be enabled while the external crystal is used on the AD7768-4.

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Clocking Selections

The internal modulator frequency (f_{MOD}) that is used by each of the ADCs in the AD7768/AD7768-4 is derived from the externally applied MCLK signal. The MCLK division bits allow the user to control the ratio between the MCLK frequency and the internal modulator clock frequency. This control allows the user to select the division ratio that is best for their configuration.

The appropriate clock configuration depends on the power mode, the decimation rate, and the base MCLK frequency available in the system. See the Clocking, Sampling Tree section for further information on setting MCLK_DIV correctly.

MCLK Source Selection

The following clocking options are available as the MCLK input source in SPI control mode:

- LVDS
- External crystal
- CMOS input MCLK

Setting CLK_SEL to logic low configures the AD7768/AD7768-4 for correct operation using a CMOS clock. Setting CLK_SEL to logic high enables the use of an external crystal. In SPI control mode, the FILTER pin must also be set to Logic 1 for operation of the external crystal.

If CLK_SEL is set to logic high and Bit 3 of Register 0x04 is also set, the application of an LVDS clock signal to the MCLK pin is enabled. LVDS clocking is exclusive to SPI control mode and requires the register selection for operation (see Table 42 for the AD7768 or Table 68 for the AD7768-4).

The DCLK rate is derived from MCLK. DCLK division (the ratio between MCLK and DCLK) is controlled in the interface configuration selection register, Register 0x07 (see Table 45 for the AD7768 or Table 71 for the AD7768-4).

Interface Configuration

The data interface is a master output interface, where ADC conversion results are output by the AD7768/AD7768-4 at a rate based on the mode selected. The interface consists of a data clock (DCLK), the data ready ($\overline{DRDY}$) framing output, and the data output pins (DOUT0 to DOUT7 for the AD7768, DOUT0 to DOUT3 for the AD7768-4).

On the AD7768, the interface can be configured to output conversion data on one, two, or eight of the DOUTx pins. The DOUTx configuration for the AD7768 is selected using the FORMATx pins (see Table 33).

On the AD7768-4, the interface can be configured to output conversion data on one or four of the DOUTx pins. The DOUTx configuration for the AD7768-4 is selected using the FORMAT0 pin (see Table 34).

The DCLK rate is a direct division of the MCLK input and can be controlled using Bits[1:0] of Register 0x07. The minimum DCLK rate can be calculated as

$$DCLK\ (minimum) = Output\ Data\ Rate \times Channels\ per\ DOUTx \times 32\ bits$$

where $MCLK \geq DCLK$.

With eight ADCs enabled, an MCLK rate of 32.768 MHz, an ODR of 256 kSPS, and two DOUTx channels, DCLK (minimum) is

$$256\ kSPS \times 4\ channels\ per\ DOUTx \times 32\ bits = 32.768\ MHz$$

where $DCLK = MCLK/1$.

For more information on the status header, CRC, and interface configuration, see the Data Interface section.

CRC Protection

The AD7768/AD7768-4 can be configured to output a CRC message per channel every 4 or 16 samples. This function is available only with SPI control. CRC is enabled in the interface control register, Register 0x07 (see the CRC Check on Data Interface section).

ADC Synchronization over SPI

The ADC synchronization over SPI allows the user to request a synchronization pulse to the ADCs over the SPI interface. To initiate the synchronization in this manner, write to Bit 7 in Register 0x06 twice.

First, the user must write a 0, which sets $\overline{SYNC_OUT}$ low, and then write a 1 to set the $\overline{SYNC_OUT}$ logic high again.

The SPI_SYNC command is recognized after the last rising edge of SCLK in the SPI instruction, where the SPI_SYNC bit is changed from low to high. The SPI_SYNC command is then output synchronously to the AD7768/AD7768-4 MCLK signal on the $\overline{SYNC_OUT}$ pin. The user must connect the $\overline{SYNC_OUT}$ signal to the $\overline{SYNC_IN}$ pin on the PCB.

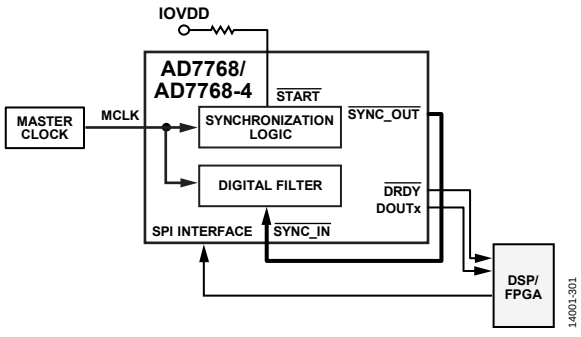

Figure 81. Connection Diagram for Synchronization Using SPI_SYNC

The $\overline{SYNC_OUT}$ pin can also be routed to the $\overline{SYNC_IN}$ pins of other AD7768/AD7768-4 devices, allowing simultaneous sampling to occur across larger channel count systems. Any daisy-chained system of AD7768/AD7768-4 devices requires that all ADCs be synchronized.

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In a daisy-chained system of AD7768/AD7768-4 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768/AD7768-4 device sharing a single MCLK signal, where the $\overline{\text{DRDY}}$ pin of only one device is used to detect new data.

As per any synchronization pulse present on the $\overline{\text{SYNC_IN}}$ pin, the digital filters of the AD7768/AD7768-4 are reset by the SPI_SYNC command. The full settling time of the filters must then elapse before valid data is output on the data interface.

Analog Input Precharge Buffers

The AD7768/AD7768-4 contain precharge buffers on each analog input to ease the drive requirements on the external amplifier. Each analog input precharge buffer can be enabled or disabled using the analog input precharge buffer registers (see Table 52 and Table 53 for the AD7768 or Table 78 and Table 79 for the AD7768-4). When writing to these registers, the user must write the inverse of the required bit settings. For example, to clear Bit 1 of this register, the user must write 0x01 to the register. This clears Bit 1 and sets all other bits. If the user reads the register again after writing 0x01, the data read is 0xFE, as required.

Reference Precharge Buffers

The AD7768/AD7768-4 contain reference precharge buffers on each reference input to ease the drive requirements on the external reference and help to settle any nonlinearity on the reference inputs. Each reference precharge buffer can be enabled or disabled using the reference precharge buffer registers (see Table 54 and Table 55 for the AD7768 or Table 80 and Table 81 for the AD7768-4).

Per Channel Calibration Gain, Offset, and Sync Phase

The user can adjust the gain, offset, and sync phase of the AD7768/AD7768-4. These options are available only in SPI control mode. Further register information and calibration instructions are available in the Offset Registers section, the Gain Registers section, and the Sync Phase Offset Registers section. See the Calibration section for information on calibration equations.

GPIOs

The AD7768/AD7768-4 have five general-purpose input/output (GPIO) pins available when operating in SPI control mode. For further information on GPIO configuration, see the GPIO Functionality section.

SPI CONTROL MODE EXTRA DIAGNOSTIC FEATURES

RAM Built In Self Test

The RAM built in self test (BIST) is a coefficient check for the digital filters. The AD7768/AD7768-4 DSP path uses some internal memories for storing data associated with filtering and calibration. A user may, if desired, initiate a built in self test (BIST) of these memories. Normal conversions are not possible while BIST is running. The test is started by writing to the BIST control register, Register 0x08. The results and status of the test are available in the status register, Register 0x09 (see Table 47 for the AD7768 or Table 73 for the AD7768-4).

Normal ADC conversion is disrupted when this test is run. A synchronization pulse is required after this test is complete to resume normal ADC operation.

Revision Identification Number

The AD7768/AD7768-4 contain an identification register that can be accessed in SPI control mode, the revision identification register. This register is an excellent way to verify the correct operation of the serial control interface. Register information is available in the Revision Identification Register section.

Diagnostic Meter Mode

The diagnostic metering mode can be used to verify the functionality of each ADC by internally passing a positive full-scale, midscale, or negative full-scale voltage to the ADC. The user can then read the resulting ADC conversion result to determine that the ADC is operating correctly. To configure ADC conversion diagnostics, see the ADC Diagnostic Receive Select Register section and the ADC Diagnostic Control Register section.

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CIRCUIT INFORMATION

CORE SIGNAL CHAIN

Each ADC channel on the AD7768/AD7768-4 has an identical signal path from the analog input pins to the data interface. Figure 83 shows a top level implementation of the core signal chain. Each ADC channel has its own Σ-Δ modulator that oversamples the analog input and passes the digital representation to the digital filter block. The modulator sampling frequency (f_{MOD}) ranges are explained in the Clocking, Sampling Tree, and Power Scaling section. The data is filtered, scaled for gain and offset (depending on user settings), and then output on the data interface. Control of the flexible settings for the signal chain is provided by either using the pin control or the SPI control set at power-up by the state of the $\overline{PIN}$/SPI input pin.

The AD7768/AD7768-4 can use up to a 5 V reference and converts the differential voltage between the analog inputs (AINx+ and AINx−) into a digital output. The analog inputs can be configured as either differential or pseudo differential inputs. As a pseudo differential input, either AINx+ or AINx− can be connected to a constant input voltage (such as 0 V, GND, AVSS, or some other reference voltage). The ADC converts the voltage difference between the analog input pins into a digital code on the output. Using a common-mode voltage of AVDD1/2 for the analog inputs, AINx+ and AINx−, maximizes the ADC input range. The 24-bit conversion result is in twos complement, MSB first, format. Figure 82 shows the ideal transfer functions for the AD7768/AD7768-4.

ADC Power Modes

The AD7768/AD7768-4 have three selectable power modes. In pin control mode, the modulator rate and power mode are tied together for best performance. In SPI control mode, the user can select the power mode and modulator MCLK divider settings. The choice of power modes gives more flexibility to control the bandwidth and power dissipation for the AD7768/AD7768-4.

Table 11 shows the recommended f_{MOD} frequencies for each power mode, and Table 42 shows the register information for the AD7768, and Table 68 shows the register information for the AD7768-4.

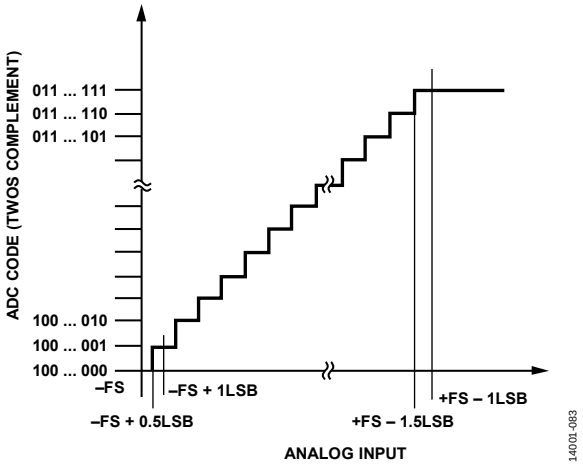

Figure 82. ADC Ideal Transfer Functions (FS is Full Scale)

Table 26. Output Codes and Ideal Input Voltages

Description	Analog Input (AINx+ – (AINx–)) V_{REF} = 4.096 V	Digital Output Code, Twos Complement (Hex.)
FS – 1 LSB	+4.095999512 V	0x7FFFFF
Midscale + 1 LSB	+488 nV	0x000001
Midscale	0 V	0x000000
Midscale – 1 LSB	−488 nV	0xFFFFFF
−FS + 1 LSB	−4.095999512 V	0x800001
−FS	−4.096 V	0x800000

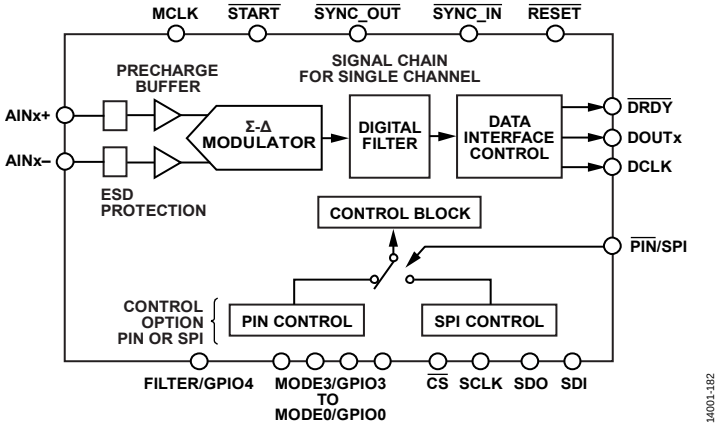

Figure 83. Top Level Core Signal Chain and Control

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ANALOG INPUTS

Figure 84 shows the AD7768/AD7768-4 analog front end. The ESD protection diodes that are designed to protect the ADC from some short duration overvoltage and ESD events are shown on the signal path. The analog input is sampled at twice the modulator sampling frequency, f_{MOD}, which is derived from MCLK. By default, the ADC internal sampling capacitors, CS1 and CS2, are driven by a per channel analog input precharge buffer to ease the driving requirement of the external network.

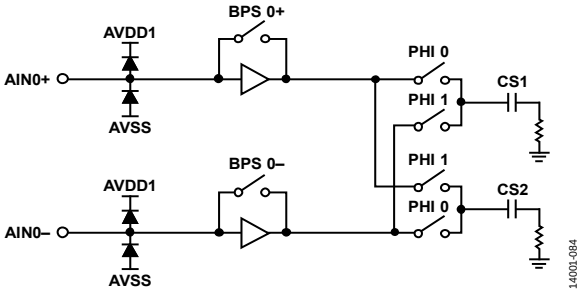

Figure 84. Analog Front End

The analog input precharge buffers, if enabled, will be enabled for a set period of time for each Fmod cycle. The period of time is dependent on the power mode of the AD7761. The precharge buffer is on for approximately 15 ns in fast mode, 29 ns in median mode, and 116 ns in low mode. For the initial rough charging of the switched capacitor network, the bypass switches, BPS 0+ and BPS 0–, remain open during this first phase. For the remaining phase, the bypass switches are closed, and the fine accuracy settling charge is provided by the external source. PHI 0 and PHI 1 represent the modulator clock sampling phases that switch the input signals onto the sampling capacitors, CS1 and CS2.

The analog input precharge buffers reduce the switching kickback from the sampling stage to the external circuitry. The precharge buffer reduces the average input current by a factor of eight, and makes the input current more signal independent, to reduce the effects of sampling distortion. This reduction in drive requirements allows pairing of the AD7768/AD7768-4 with lower power, lower bandwidth front end driver amplifiers such as the ADA4940-1/ ADA4940-2.

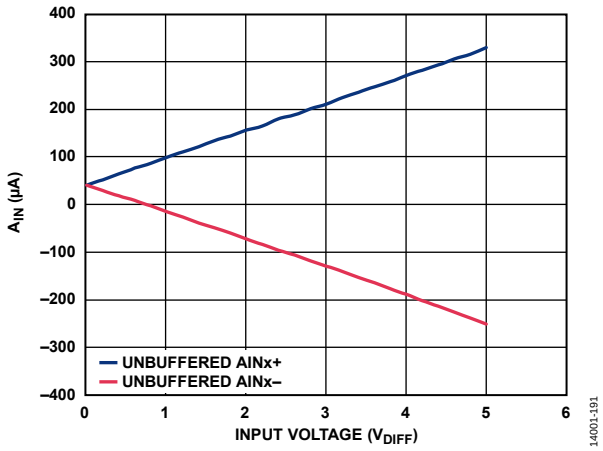

Figure 85. Analog Input Current (A_{IN}) vs. Input Voltage, Analog Input Precharge Buffer Off, V_{CM} = 2.5 V, f_{MOD} = 8.192 MHz

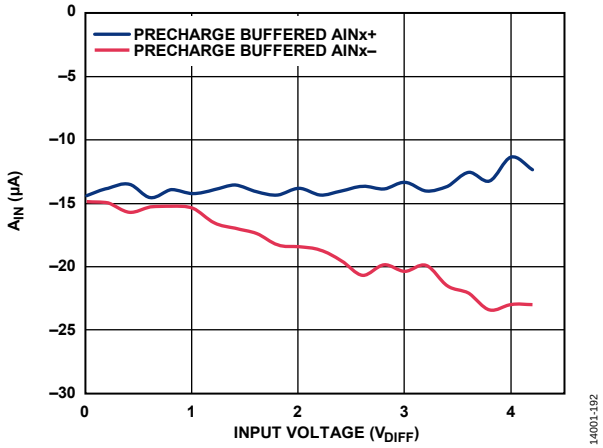

Figure 86. Analog Input Current (A_{IN}) vs. Input Voltage, Analog Input Precharge Buffer On, V_{CM} = 2.5 V, f_{MOD} = 8.192 MHz

The analog input precharge buffers can be turned on/off by means of a register write to Register 0x11 and Register 0x12 (Precharge Buffer Register 1 and Precharge Buffer Register 2). When writing to these registers, the user must write the inverse of the required bit settings. For example, to clear Bit 1 of this register, the user must write 0x01 to the register. This clears Bit 1 and sets all other bits. If the user reads the register again after writing 0x01, the data read is 0xFE, as required. Each analog input precharge buffer is selectable per channel. In pin control mode, the analog input precharge buffers are always enabled for optimum performance.

When the analog input precharge buffers are disabled, the analog input current is sourced completely from the analog input source. The unbuffered analog input current is calculated from two components: the differential input voltage on the analog input pair, and the analog input voltage with respect to AVSS. With the precharge buffers disabled, for 32.768 MHz MCLK in fast mode with f_{MOD} = MCLK/4, the differential input current is approximately 48 µA/V and the current with respect to ground is approximately 17 µA/V.

For example, if the precharge buffers are off, with AIN1+= 5 V, and AIN1– = 0 V, estimate the current in each input pin as follows:

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$AIN1+ = 5\ V \times 48\ \mu A/V + 5\ V \times 17\ \mu A/V = 325\ \mu A$

$AIN1- = -5\ V \times 48\ \mu A/V + 0\ V \times 17\ \mu A/V = -240\ \mu A$

When the precharge buffers are enabled, the absolute voltage with respect to AVSS determines the majority of the current. The maximum input current of approximately −25 µA is measured when the analog input is close to either the AVDD1 or AVSS rails.

With either precharge buffers enabled or disabled, the analog input current scales linearly with the modulator clock rate. The analog input current versus input voltage is shown in Figure 85.

Full settling of the analog inputs to the ADC requires the use of an external amplifier. Pair amplifiers such as the ADA4805-2 for low power mode, the ADA4807-2 or ADA4940-1/ADA4940-2 for median mode, and the ADA4807-2 or ADA4896-2 for fast mode with the AD7768/AD7768-4 (see Figure 87 for details). Running the AD7768/AD7768-4 in median and low power modes or reducing the MCLK rate reduces the load and speed requirements of the amplifier; therefore, lower power amplifiers can be paired with the analog inputs to achieve the optimum signal chain efficiency.

There is a resistor/capacitor (RC) network between the amplifier output and the ADC input. Figure 87 shows a typical RC network used for the AD7768/AD7768-4 for most amplifier pairings. The RC network performs a variety of tasks. C1 and C2 are charge reservoirs to the ADC, providing the ADC with fast charge current to the sampling capacitors. Capacitor C3 removes common-mode errors between the AINx+ and AINx− inputs. These capacitors, in combination with RIN, form a low-pass filter to filter out glitches related to the input switching. The input resistance also stabilizes the amplifier when driving large capacitor loads and prevents the amplifier from oscillating.

The optimum driver amplifiers for each of these power, performance, and supply requirements are as follows:

- The ADA4805-2 is suited for low power, particularly in low power mode.
- The ADA4940-1 is suited for single-supply operation and is also the recommended fully differential amplifier to drive the AD7768/AD7768-4.
- For optimum performance in fast power mode, the ADA4896-2 performs best, although the device does not consume the same power as the ADA4899-1. The ADA4896-2 is also suitable for a general-purpose DAQ module, which can be configured for all three power modes.

For more details, refer to the AN-1384 Application Note.

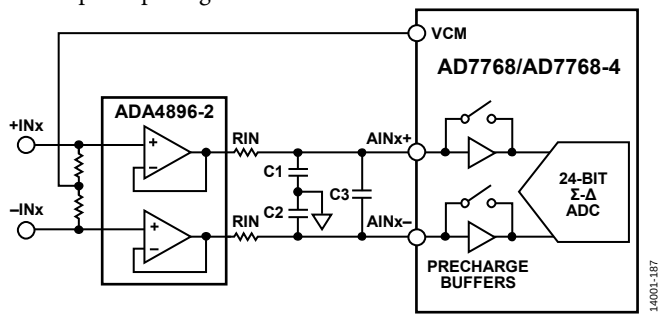

Figure 87. Typical Input Structure for an RC Network

Table 27. Amplifier Pairing Options

Power Mode	Amplifier	Amplifier Power (mW/channel)[1]	Analog Input Precharge Buffer	Total Power (Amplifier + AD7768) (mW/channel)[1]
Fast	ADA4896-2	40.6	On	87.9
Fast	ADA4940-2	13.4	On	64.9
Median	ADA4805-2	6.9	On	34.4
Low Power	ADA4805-2	6.5	On	15.9

[1] Typical power at 25°C.

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VCM

The AD7768/AD7768-4 provide a buffered common-mode voltage output on Pin 59. This output can bias up analog input signals. By incorporating the VCM buffer into the ADC, the AD7768/AD7768-4 reduce component count and board space. In pin control mode, the VCM potential is fixed to (AVDD1 − AVSS)/2, and is enabled by default.

In SPI control mode, configure the VCM potential using the general configuration register (Register 0x05). The output can be enabled or disabled, and set to (AVDD1 − AVSS)/2, 1.65 V, 2.14 V, or 2.5 V, with respect to AVSS.

The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768/AD7768-4.

REFERENCE INPUT

The AD7768/AD7768-4 have two differential reference input pairs. On the AD7768 REF1+ and REF1− are the reference inputs for Channel 0 to Channel 3, and REF2+ and REF2− are for Channel 4 to Channel 7. On the AD7768-4 REF1+ and REF1− are the reference inputs for Channel 0 and Channel 1, and REF2+ and REF2− are for Channel 2 and Channel 3. The absolute input reference voltage range is 1 V to AVDD1 − AVSS.

Like the analog inputs, the reference inputs have a precharge buffer option. Each ADC has an individual buffer for each REFx+ and REFx−. The precharge buffers help reduce the burden on the external reference circuitry.

In pin control mode, the reference precharge buffers are off by default. In SPI control mode, the user can enable or disable the reference precharge buffers. In the case of unipolar analog supplies, in SPI control mode, the user can achieve the best performance and power efficiency by enabling only the REFx+ buffers. The reference input current scales linearly with the modulator clock rate.

For 32 MHz MCLK and MCLK/4 fast mode, the differential input current is ~72 µA/V per channel unbuffered, and ~16 µA/V per channel with the precharge buffers enabled.

With the precharge buffers off, REFx+ = 5 V, and REFx− = 0 V,

$$REFx\pm = 5\ V \times 72\ \mu A/V = 360\ \mu A$$

With the precharge buffers on, REFx+ = 5 V, and REFx− = 0 V,

$$REFx\pm = 5\ V \times 16\ \mu A/V = 80\ \mu A$$

For the best performance and headroom, it is recommended to use a 4.096 V reference such as the ADR444 or the ADR4540.

For the best performance at high sampling rates, it is recommended to use an external reference drive amplifier such as the ADA4841-1 or the AD8031. See Figure 88 for the configuration diagram of the reference connection.

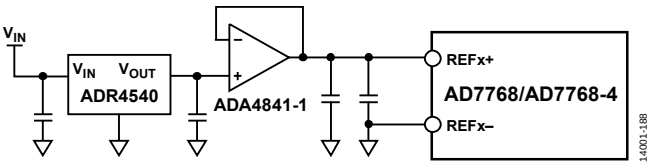

Figure 88. Typical Reference Input Configuration Diagram

CLOCK SELECTION

The AD7768/AD7768-4 have an internal oscillator that is used for initial power-up of the device. After the AD7768/AD7768-4 have completed their start-up routine, the devices normally transfer control of the internal clocking to the externally applied MCLK. The AD7768/AD7768-4 count the falling edges of the external MCLK over a given number of internal clock cycles to determine if the clock is valid and at least a frequency of 1.15 MHz. If there is a fault with the external MCLK, the transfer of control does not occur, the AD7768/AD7768-4 output an error in the status header, and the clock error bit is set in the device status register. No conversion data is output and a reset is required to exit this error state.

Three clock source input options are available to the AD7768/AD7768-4: external CMOS, crystal oscillator, or LVDS. The clock is selected on power-up and is determined by the state of the CLK_SEL pin.

If CLK_SEL = 0, the CMOS clock option is selected and the clock is applied to Pin 32 (Pin 31 is tied to DGND).

If CLK_SEL = 1, the crystal or LVDS option is selected and the crystal or LVDS is applied to Pin 31 and Pin 32. The LVDS option is available only in SPI control mode. An SPI write to Bit 3 of Register 0x04 enables the LVDS clock option.

DIGITAL FILTERING

The AD7768/AD7768-4 offer two types of digital filters. In SPI control mode, these filters can be chosen on a per channel basis. In pin control mode, only one filter can be selected for all channels. The digital filters available on the AD7768/AD7768-4 are

- Sinc5 low latency filter, −3 dB at 0.204 × ODR
- Wideband low ripple filter, −3 dB at 0.433 × ODR

Both filters can be operated in one of six different decimation rates, allowing the user to choose the optimal input bandwidth and speed of the conversion versus the desired power mode or resolution.

Sinc5 Filter

Most precision Σ-Δ ADCs use a sinc filter. The sinc5 filter offered in the AD7768/AD7768-4 enables a low latency signal path useful for dc inputs, for control loops, or where other specific postprocessing is required. The sinc5 filter path offers the lowest noise and power consumption. The sinc5 filter has a −3 dB BW of 0.204 × ODR. Table 13 contains the noise performance for the sinc5 filter across power modes and decimation ratios.

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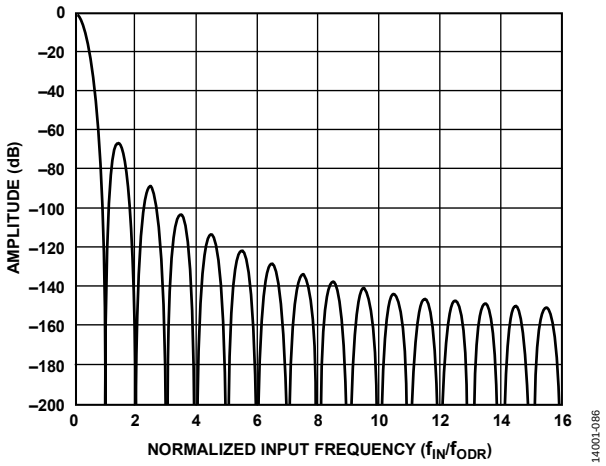

Figure 89. Sinc5 Filter Frequency Response (Decimation = ×32)

The settling times for the AD7768/AD7768-4 when using the sinc5 filter are shown in Figure 89.

Wideband Low Ripple Filter

The wideband filter has a low ripple pass band, within ±0.005 dB of ripple, of 0.4 × ODR. The wideband filter has full attenuation at 0.499 × ODR (Nyquist), maximizing antialias protection. The wideband filter has a pass-band ripple of ±0.005 dB and a stop band attenuation of 105 dB from Nyquist out to f_{CHOP}. For more information on antialiasing and f_{CHOP} aliasing, see the Antialiasing section.

The wideband filter is a very high order digital filter with a group delay of approximately 34/ODR. After a synchronization pulse, there is an additional delay from the $\overline{\text{SYNC_IN}}$ rising edge to fully settled data. The settling times for the AD7768/AD7768-4 when using the wideband filter are shown in Figure 90. See Table 12 for the noise performance of the wideband filter across power modes and decimation rates.

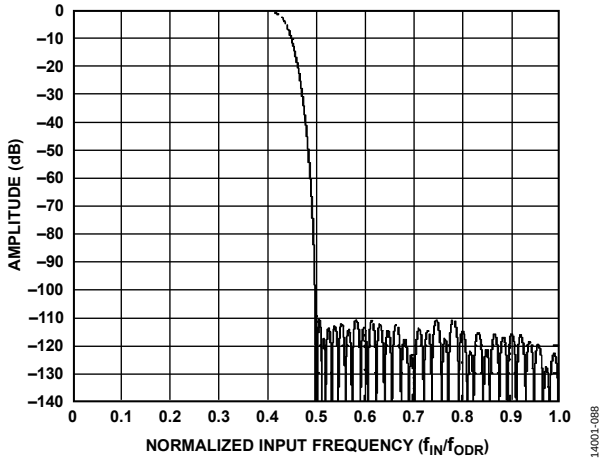

Figure 90. Wideband Filter Frequency Response

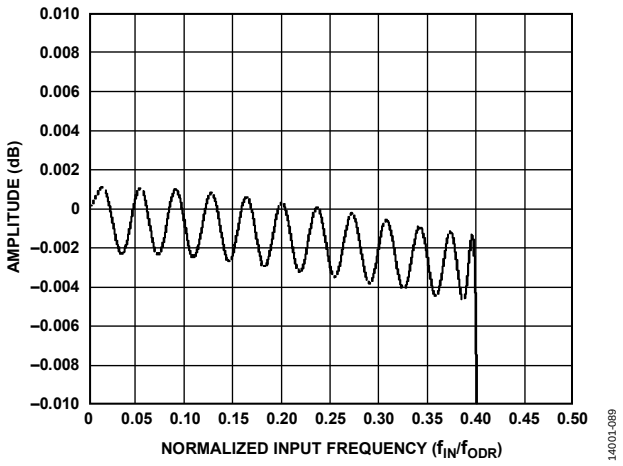

Figure 91. Wideband Filter Pass-Band Ripple

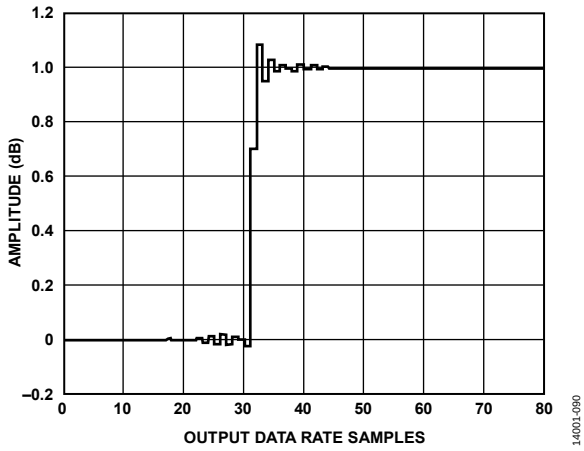

Figure 92. Wideband Filter Step Response

Filter Settling Time

The AD7768/AD7768-4 digital filters are resynchronized on the rising edge of the $\overline{\text{SYNC_IN}}$ signal. Provide this resynchronization after power-up in pin control mode or SPI control mode, and after any reconfiguration of the device in SPI control mode, prior to capturing ADC samples. After the $\overline{\text{SYNC_IN}}$ rising edge is provided, there is a deterministic delay until the first new conversion result is available, and until the first settled data is available. Table 28 and Table 29 provide these delays, measured in MCLK cycles, for the wideband and sinc5 filters, respectively, for each possible setting of MCLK_DIV. Each table provides the delays for configurations where all channels are using the exact same configuration (Group B unused), and for configurations where one or more channels have a different decimation rate applied (Group B is used).

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For example, when the channels are configured with the wideband filter and MCLK_DIV = MCLK/4, with some channels are assigned to Group A with decimate by 32 and other channels to Group B with decimate by 64, then the delay until the first $\overline{\text{DRDY}}$ signal after the $\overline{\text{SYNC_IN}}$ signal is 758 MCLK periods. All active channels output the first data after 758 MCLK periods. However, due to differing decimation rates across channels, in this case, the first settled data is available for the Group A channels 8822 MCLK periods after the $\overline{\text{SYNC_IN}}$ signal, and after 17,014 MCLK periods for the Group B channels.

Table 28. Wideband Filter $\overline{\text{SYNC_IN}}$ to Settled Data

MCLK_DIV Setting	Filter Type		Decimation Factor		Delay from First MCLK Rise After $\overline{\text{SYNC_IN}}$ Rise to First $\overline{\text{DRDY}}$ Rise	Delay from First MCLK Rise After $\overline{\text{SYNC_IN}}$ Rise to Earliest Settled Data $\overline{\text{DRDY}}$ Rise	
						MCLK Periods	
	Group A	Group B	Group A	Group B	MCLK Periods	Group A	Group B
MCLK/4	Wideband	Wideband	32	Unused	336	8400	Not applicable
	Wideband	Wideband	64	Unused	620	16,748	Not applicable
	Wideband	Wideband	128	Unused	1187	33,443	Not applicable
	Wideband	Wideband	256	Unused	2325	66,837	Not applicable
	Wideband	Wideband	512	Unused	4601	133,625	Not applicable
	Wideband	Wideband	1024	Unused	9153	267,201	Not applicable
	Wideband	Wideband	32	32	758	8822	8822
	Wideband	Wideband	32	64	758	8822	17,014
	Wideband	Wideband	32	128	758	8822	33,526
	Wideband	Wideband	32	256	758	8822	66,934
	Wideband	Wideband	32	512	758	8822	133,622
	Wideband	Wideband	32	1024	758	8822	267,253
	Wideband	Wideband	64	32	759	17,015	8823
	Wideband	Wideband	128	32	760	33,528	8824
	Wideband	Wideband	256	32	762	66,938	8826
	Wideband	Wideband	512	32	782	133,646	8846
	Wideband	Wideband	1024	32	806	267,302	8870
MCLK/8	Wideband	Wideband	32	Unused	656	16,784	Not applicable
	Wideband	Wideband	64	Unused	1225	33,481	Not applicable
	Wideband	Wideband	128	Unused	2359	66,871	Not applicable
	Wideband	Wideband	256	Unused	4635	133,659	Not applicable
	Wideband	Wideband	512	Unused	9187	267,235	Not applicable
	Wideband	Wideband	1024	Unused	18,291	534,387	Not applicable
	Wideband	Wideband	32	32	820	16,948	16,948
	Wideband	Wideband	32	64	820	16,948	33,588
	Wideband	Wideband	32	128	820	16,948	66,868
	Wideband	Wideband	32	256	820	16,948	133,684
	Wideband	Wideband	32	512	820	16,948	267,316
	Wideband	Wideband	32	1024	820	16,948	534,580
	Wideband	Wideband	64	32	822	33,590	16,950
	Wideband	Wideband	128	32	824	66,872	16,952
	Wideband	Wideband	256	32	844	133,708	16,972
	Wideband	Wideband	512	32	836	267,332	16,964
	Wideband	Wideband	1024	32	852	534,612	16,980

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MCLK_DIV Setting	Filter Type		Decimation Factor		Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise	Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled Data DRDY Rise	
						MCLK Periods	
	Group A	Group B	Group A	Group B	MCLK Periods	Group A	Group B
MCLK/32	Wideband	Wideband	32	Unused	2587	67,099	Not applicable
	Wideband	Wideband	64	Unused	4855	133,879	Not applicable
	Wideband	Wideband	128	Unused	9391	267,439	Not applicable
	Wideband	Wideband	256	Unused	18,495	534,591	Not applicable
	Wideband	Wideband	512	Unused	36,703	1,068,895	Not applicable
	Wideband	Wideband	1024	Unused	73,119	2,137,503	Not applicable
	Wideband	Wideband	32	32	2587	67,099	67,099
	Wideband	Wideband	32	64	2587	67,099	134,683
	Wideband	Wideband	32	128	2587	67,099	267,803
	Wideband	Wideband	32	256	2587	67,099	535,067
	Wideband	Wideband	32	512	2587	67,099	1,069,595
	Wideband	Wideband	32	1024	2587	67,099	2,137,627
	Wideband	Wideband	64	32	2587	134,683	67,099
	Wideband	Wideband	128	32	2587	267,803	67,099
	Wideband	Wideband	256	32	2587	535,067	67,099
	Wideband	Wideband	512	32	2587	1,069,595	67,099
	Wideband	Wideband	1024	32	2587	2,137,627	67,099

Table 29. Sinc5 Filter SYNC_IN to Settled Data

MCLK_DIV Setting	Filter Type		Decimation Factor		Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise	Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled Data DRDY Rise	
						Group A	Group B
	Group A	Group B	Group A	Group B	MCLK Periods	MCLK Periods	MCLK Periods
MCLK/4	Sinc5	Sinc5	32	Unused	199	839	Not applicable
	Sinc5	Sinc5	64	Unused	327	1607	Not applicable
	Sinc5	Sinc5	128	Unused	583	3143	Not applicable
	Sinc5	Sinc5	256	Unused	1095	6215	Not applicable
	Sinc5	Sinc5	512	Unused	2119	12359	Not applicable
	Sinc5	Sinc5	1024	Unused	4167	24,647	Not applicable
	Sinc5	Sinc5	32	32	199	839	839
	Sinc5	Sinc5	32	64	199	839	1607
	Sinc5	Sinc5	32	128	199	839	3143
	Sinc5	Sinc5	32	256	199	839	6215
	Sinc5	Sinc5	32	512	199	839	12,359
	Sinc5	Sinc5	32	1024	199	839	24,647
	Sinc5	Sinc5	64	32	199	1607	839
	Sinc5	Sinc5	1024	32	199	24,647	839
MCLK/8	Sinc5	Sinc5	32	Unused	383	1663	Not applicable
	Sinc5	Sinc5	64	Unused	639	3199	Not applicable
	Sinc5	Sinc5	128	Unused	1151	6271	Not applicable
	Sinc5	Sinc5	256	Unused	2175	12,415	Not applicable
	Sinc5	Sinc5	512	Unused	4223	24,703	Not applicable
	Sinc5	Sinc5	1024	Unused	8319	49,279	Not applicable
	Sinc5	Sinc5	32	32	383	1663	1663
	Sinc5	Sinc5	32	64	383	1663	3199
	Sinc5	Sinc5	32	128	383	1663	6271
	Sinc5	Sinc5	32	256	398	1663	12,415
	Sinc5	Sinc5	32	512	398	1663	24,703
	Sinc5	Sinc5	32	1024	398	1663	49,279
	Sinc5	Sinc5	64	32	383	3199	1663
	Sinc5	Sinc5	1024	32	398	49,279	1663

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MCLK_DIV Setting	Filter Type		Decimation Factor		Delay from First MCLK Rise After SYNC_IN Rise to First DRDY Rise	Delay from First MCLK Rise After SYNC_IN Rise to Earliest Settled Data DRDY Rise	
	Group A	Group B	Group A	Group B		Group A	Group B
					MCLK Periods	MCLK Periods	MCLK Periods
MCLK/32	Sinc5	Sinc5	32	Unused	1487	6607	Not applicable
	Sinc5	Sinc5	64	Unused	2511	12,751	Not applicable
	Sinc5	Sinc5	128	Unused	4559	25,039	Not applicable
	Sinc5	Sinc5	256	Unused	8655	49,615	Not applicable
	Sinc5	Sinc5	512	Unused	16,847	98,767	Not applicable
	Sinc5	Sinc5	1024	Unused	33,231	197,071	Not applicable
	Sinc5	Sinc5	32	32	1487	6607	6607
	Sinc5	Sinc5	32	64	1487	6607	12,751
	Sinc5	Sinc5	32	128	1487	6607	25,039
	Sinc5	Sinc5	32	256	1487	6607	49,615
	Sinc5	Sinc5	32	512	1487	6607	98,767
	Sinc5	Sinc5	32	1024	1487	6607	197,071
	Sinc5	Sinc5	64	32	1487	12,751	6607
	Sinc5	Sinc5	1024	32	1487	197,071	6607

DECIMATION RATE CONTROL

The AD7768/AD7768-4 have programmable decimation rates for the digital filters. The decimation rates allow the user to reduce the measurement bandwidth, reducing the speed but increasing the resolution. When using the SPI control, control the decimation rate on the AD7768/AD7768-4 through the channel mode registers. These registers set two separate channel modes with a given decimation rate and filter type. Each ADC is mapped to one of these modes via the channel mode select register. Table 30 details both the decimation rates available, and the filter types for selection, within Mode A and Mode B.

In pin control mode, the decimation ratio is controlled by the DEC0 and DEC1 pins; see Table 17 for decimation configuration in pin control mode.

Table 30. Channel x Mode Registers, Register 0x01 and Register 0x02

Bits	Name	Logic Value	Decimation Rate
3	FILTER_TYPE_x	0	Wideband filter
		1	Sinc5 filter
[2:0]	DEC_RATE_x	000	32
		001	64
		010	128
		011	256
		100	512
		101	1024
		110	1024
		111	1024

ANTIALIASING

Because the AD7768/AD7768-4 are switched capacitor, discrete time ADCs, the user may wish to employ external analog antialiasing filters to protect against fold back of out of band tones.

Within this section, an out of band tone refers to an input frequency greater than the pass band frequency specification of the digital filter that is applied at the analog input.

When designing an antialiasing filter for the AD7768/AD7768-4, three main aliasing regions must be taken into account. After the alias requirements of each zone are understood, the user can design an antialiasing filter to meet the needs of the specific application. The three zones for consideration are related to the modulator sampling frequency, the modulator chopping frequency, and the modulator saturation point.

Modulator Sampling Frequency

The AD7768/AD7768-4 modulator signal transfer function includes a notch, at odd multiples of f_{MOD}, to reject tones or harmonics related to the modulator clock. The modulator itself attenuate signals at frequencies of f_{MOD}, $3 \times f_{MOD}$., $5 \times f_{MOD}$, and so on. For an MCLK frequency of 32.768 MHz, the attenuation is approximately 35 dB in fast mode, 41 dB in median mode, and 53 dB in low power mode. Attenuation is increased by 6 dB across each power mode, with every halving of the MCLK frequency, for example, when reducing the clock from 32.768 MHz to 16.384 MHz.

The modulator has no rejection to signals that are at frequencies in zones around $2 \times f_{MOD}$ and all even multiples of f_{MOD}. Signals at these frequencies are aliased by the AD7768/AD7768-4. For the AD7768/AD7768-4, the first of these zones that requires protection is at $2 \times f_{MOD}$. Because typical switch capacitor, discrete time Σ-Δ modulators provide no protection to aliasing at the frequency, f_{MOD}, the AD7768/AD7768-4 provide a distinct advantage in this regard.

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Figure 93 shows the frequency response of the modulator and wideband digital filter to out of band tones at the analog input. Figure 93 shows the magnitude of an alias that is seen in band vs. the frequency of the signal sampled at the analog input. The relationship between the input signal and the modulator frequency is expressed in a normalized manner as a ratio of the input signal (f_{IN}) to the modulator frequency (f_{MOD}). This data demonstrates the ADC frequency response relative to out of band tones when using the wideband filter. The input frequency (f_{IN}) is swept from dc to 20 MHz. In fast mode, using an 8.192MHz f_{MOD} frequency, the x-axis spans ratios of f_{IN}/f_{MOD} from 0 to 2.44 (equivalent to f_{IN} of 0 Hz to 20 MHz). A similar characteristic occurs in median mode and low power mode.

The notch appears in Figure 93 with the input frequency (f_{IN}) at f_{MOD} (designated at f_{IN}/f_{MOD} = 1.00 on the x-axis). An input at this frequency is attenuated by 35 dB, which adds to the attenuation of any external antialiasing filter, thus reducing the frequency roll-off requirement of the external filter. If the plot is swept further in frequency, the notch is seen to recur at f_{IN}/f_{MOD} = 3.00.

The point where $f_{IN} = 2 \times f_{MOD}$ (designated on the x-axis at 2.00) offers 0 dB attenuation, indicating that all signals falling at this frequency alias directly back into the ADC conversion results, in accordance with sampling theory.

The AD7768/AD7768-4 wideband digital filter also offers an added protection against aliasing. Because the wideband filter has full attenuation at the Nyquist frequency ($f_{ODR}/2$, where f_{ODR} = f_{MOD}/Decimation Rate), input frequencies, and in particular harmonics of input frequencies, that may fall close to $f_{ODR}/2$, do not fold back into the pass-band of the AD7768/AD7768-4.

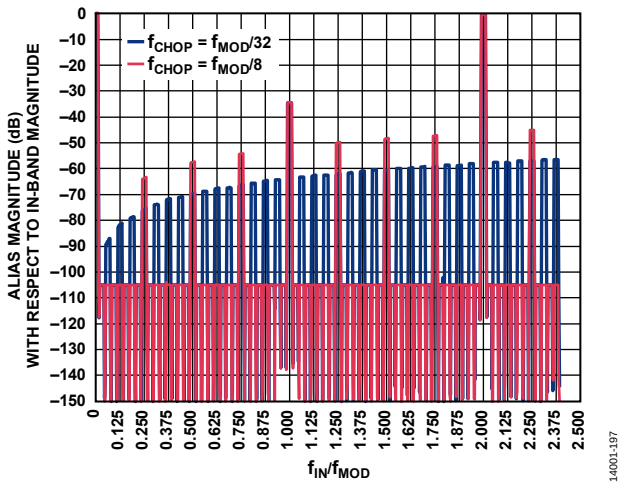

Figure 93. AD7768/AD7768-4 Rejection of Out of Band Input Tones, Wideband Filter, Decimation = ×32, f_{MOD} = 8.192 MHz, Analog Input Sweep from DC to 20 MHz

Modulator Chopping Frequency

Figure 93 plots two scenarios that relate to the chopping frequency of the AD7768/AD7768-4 modulators.

The AD7768/AD7768-4 use a chopping technique in the modulator similar to that of a chopped amplifier to remove offset, offset drift, and 1/f noise. The AD7768/AD7768-4 default chopping rate is $f_{MOD}/32$. In pin control mode, the chop frequency is hardwired to $f_{MOD}/32$. In SPI control mode, the user can select the chop frequency to be either $f_{MOD}/32$ or $f_{MOD}/8$.

As shown in Figure 93, the stop band rejection of the digital filter is reduced at frequencies that relate to even multiples of the chopping frequency (f_{CHOP}). All other out of band frequencies (excluding those already discussed relating to the modulator clock frequency f_{MOD}) are rejected by the stop band attenuation of the digital filter. An out of band tone with a frequency in the range of $(2 \times f_{CHOP}) \pm f_{3dB}$, where f_{3dB} is the filter bandwidth employed, is attenuated to the envelope determined by the chop frequency setting (see Figure 93), and aliased into the pass band. Out of band tones near additional even multiples of f_{CHOP} (that is, N × f_{CHOP}, where N is an even integer), are attenuated and aliased in the same way.

Chopping at $f_{MOD}/32$ offers the best performance for noise, offset, and offset drift for the AD7768/AD7768-4.

For ac performance it may be useful to select chopping at $f_{MOD}/8$ as this moves the first chopping tone to a higher frequency. However, chopping at $f_{MOD}/8$ may lead to slightly degraded noise (approximately 1 dB loss in dynamic range) and offset performance compared to the default chop rate of $f_{MOD}/32$.

Table 31 shows the aliasing achieved by different order antialiasing filter options at the critical frequencies of $f_{MOD}/32$ and $f_{MOD}/8$ for chop aliasing, $f_{MOD}/16$ for modulator saturation, and $2 \times f_{MOD}$ for the first zone with 0 dB attenuation. It assumes the corner frequency of the antialiasing filter is at $f_{MOD}/64$, which is just above the maximum input bandwidth that the AD7768/AD7768-4 digital filter can pass when using a decimate by 32 filter setting.

Table 31. External Antialiasing Filter Attenuation

RC Filter	$f_{MOD}/32$ (dB)	$f_{MOD}/16$ (dB)	$f_{MOD}/8$ (dB)	$2 \times f_{MOD}$ (dB)
First Order	−6	−12	−18	−42
Second Order	−12	−24	−36	−84
Third Order	−18	−36	−54	−126

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Modulator Saturation Point

A Σ-Δ modulator can be considered a standard control loop, employing negative feedback. The control loop works to ensure that the average processed error signal is very small over time. It uses an integrator to remember preceding errors and force the mean error to be zero. As the input signal rate of change increases with respect to the modulator clock, f_{MOD}, a larger voltage feedback error is processed. Above a certain frequency, the error begins to saturate the modulator.

For theAD7768/AD7768-4, the modulator may saturate for full-scale input frequencies greater than $f_{MOD}/16$ (see Figure 94), depending on the rate of change of input signal, input signal amplitude, and reference input level. A half power input tone at $f_{MOD}/8$ may also cause the modulator to saturate. In applications where there may be high amplitude and frequency out of band tones, a first-order antialiasing filter is required with a −3 dB corner frequency set at $f_{MOD}/16$ to protect against modulator saturation. For example, if operating the AD7768/AD7768-4 at full speed and using a decimation rate of ×32 to achieve an output data rate of 256 kSPS, the modulator rate is equal to 8.192 MHz. In this instance, to protect against saturation, set the antialiasing filter −3 dB corner frequency to 512 kHz.

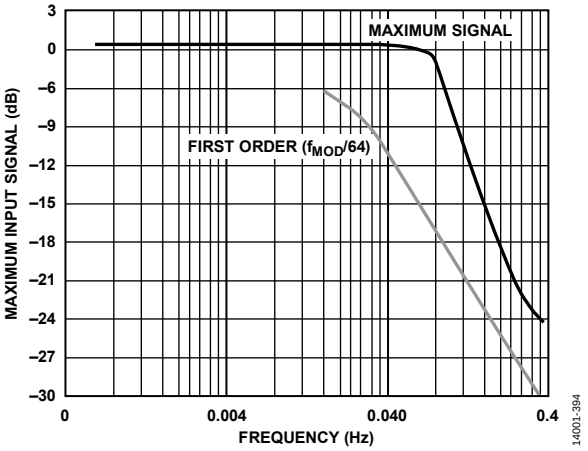

Figure 94. Maximum Input Signal vs. Frequency

CALIBRATION

In SPI control mode, the AD7768/AD7768-4 offer users the ability to adjust offset, gain, and phase delay on a per channel basis.

Offset Adjustment

The CHx_OFFSET_MSB, CHx_OFFSET_MID, and CHx_OFFSET_LSB registers are 24-bit, signed twos complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. Because offset calibration occurs before gain calibration, the ratio of 4/3 changes linearly with gain adjustment via the Channel x gain registers (see Table 56 and Table 57 for the AD7768, or Table 82 and Table 83 for the AD7768-4). After a reset or power cycle, the offset register values revert to the default factory setting.

Gain Adjustment

Each ADC channel has an associated gain coefficient. The coefficient is stored in three single-byte registers split up as MSB, MID, and LSB. Each of the gain registers are factory programmed. Nominally, this gain is around the value 0x555555 (for an ADC channel). The user may overwrite the gain register setting. However, after a reset or power cycle, the gain register values revert to the hard coded programmed factory setting.

Calculate the approximate result that is output using the following formula:

$$Data = \left(\frac{3 \times V_{IN}}{V_{REF}} \times 2^{21} - (Offset) \right) \times \frac{Gain}{4} \times \frac{4{,}194{,}300}{2^{42}}$$

where:
Offset is the offset register setting.
Gain is the gain register setting.

Sync Phase Offset Adjustment

The AD7768/AD7768-4 have one synchronization signal for all channels. The sync phase offset register allows the user to vary the phase delay on each of the channels relative to the synchronization edge received on the $\overline{\text{SYNC_IN}}$ pin.

By default, all ADC channels react simultaneously to the $\overline{\text{SYNC_IN}}$ pulse. The sync phase registers can be programmed to equalize known external phase differences on ADC input channels, relative to one another. The range of phase compensation is limited to a maximum of one conversion cycle, and the resolution of the correction depends on the decimation rate in use.

Table 32 displays the resolution and register bits used for phase offset for each decimation ratio.

Table 32. Phase Delay Resolution

Decimation Ratio	Resolution	Steps	Phase Register Bits
×32	$1/f_{MOD}$	32	[7:3]
×64	$1/f_{MOD}$	64	[7:2]
×128	$1/f_{MOD}$	128	[7:1]
×256	$1/f_{MOD}$	256	[7:0]
×512	$2/f_{MOD}$	256	[7:0]
×1024	$4/f_{MOD}$	256	[7:0]

Adjusting the sync phase of channels can affect the time to the first $\overline{\text{DRDY}}$ pulse after the sync pulse, as well as the time to Bit 6 of the header status (filter not settled data bit) being cleared, that is, the time to settled data.

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If all channels are using the Sinc5 filter, the time to the first $\overline{\text{DRDY}}$ pulse is not affected by the adjustment of the sync phase offset, assuming that at least one channel has zero sync phase offset adjustment. If all channels have a nonzero sync phase offset setting, the time to the first $\overline{\text{DRDY}}$ pulse is delayed according to the channel that has the least offset applied. Channels with a sync offset adjustment setting that delays the internal sync signal, relative to other channels, may not output settled data until after the next $\overline{\text{DRDY}}$ pulse. In other words, there may be a delay of one ODR period between the settled data being output by the AD7768/AD7768-4 for the channels with added phase delay.

If all channels are using the wideband filter, the time to the first $\overline{\text{DRDY}}$ pulse and the time to settled data is delayed according to the channel with the maximum phase delay setting. In this case, the interface waits for the latest channel and outputs data for all channels when that channel is ready.

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DATA INTERFACE

SETTING THE FORMAT OF DATA OUTPUT

The data interface format is determined by setting the FORMATx pins. The logic state of the FORMATx pins are read on power-up and determine how many data lines (DOUTx) the ADC conversions are output on.

Because the FORMATx pins are read on power-up of the AD7768 and the device remains in this output configuration, this function must always be hardwired and cannot be altered dynamically. Table 33, Figure 95, Figure 96, and Figure 98 show the formatting configuration for the digital output pins on the AD7768.

Calculate the minimum required DCLK rate for a given data interface configuration as follows:

DCLK (minimum) = *Output Data Rate* × *Channels per DOUTx* × 32

where MCLK ≥ DCLK.

For example, if MCLK = 32.768 MHz, with two DOUTx lines,

DCLK (minimum) = 256 kSPS × 4 channels per DOUTx × 32 = 32.768 Mbps

Therefore, *DCLK* = *MCLK*/1.

Alternatively, if MCLK = 32.768 MHz, with eight DOUTx lines,

DCLK (minimum) = 256 kSPS × 1 channel per DOUTx × 32 = 8.192 Mbps

Therefore, DCLK = MCLK/4.

Higher DCLK rates make it easier to receive the conversion data from the AD7768/AD7768-4 with a lower number of DOUTx lines; however, there is a trade-off against ADC offset performance with higher DCLK frequencies. For the best offset and offset drift performance, use the lowest DCLK frequency possible. The user can choose to reduce the DCLK frequency by an appropriate selection of MCLK frequency, DCLK divider, and/or the number of DOUTx lines used. Table 1 and Table 2 give the offset and offset drift specifications for ranges of DCLK frequency, and Figure 49 shows the typical offset drift over a range of DCLK frequencies.

Table 33. FORMATx Truth Table for the AD7768

FORMAT1	FORMAT0	Description
0	0	Each ADC channel outputs on its own dedicated pin. DOUT0 to DOUT7 are in use.
0	1	The ADCs share the DOUT0 and DOUT1 pins: Channel 0 to Channel 3 output on DOUT0. Channel 4 to Channel 7 output on DOUT1. The ADC channels share data pins in time division multiplexed (TDM) output. DOUT0 and DOUT1 are in use.
1	X	All channels output on the DOUT0 pin, in TDM output. Only DOUT0 is in use.

Table 34. FORMAT0 Truth Table for the AD7768-4

FORMAT0	Description
0	Each ADC channel outputs on its own dedicated pin. DOUT0 to DOUT3 are in use.
1	All channels output on the DOUT0 pin, in TDM output. Only DOUT0 is in use.

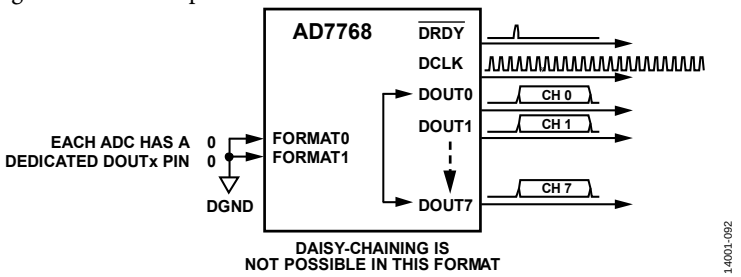

Figure 95. AD7768 FORMATx = 00, Eight Data Output Pins

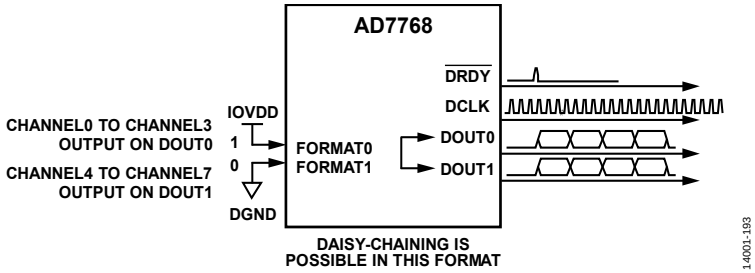

Figure 96. AD7768 FORMATx = 01, Two Data Output Pins

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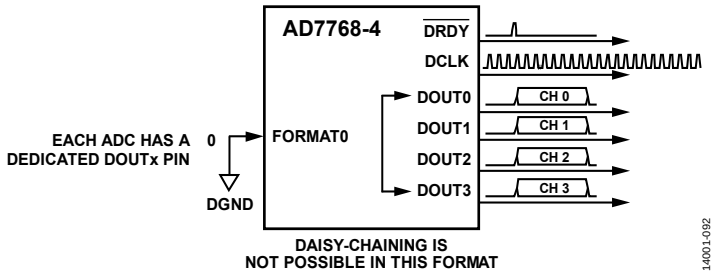

Figure 97. AD7768-4 FORMAT0 = 0, Four Data Output Pins

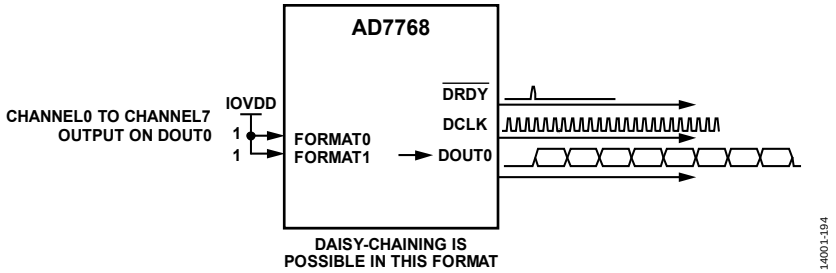

Figure 98. AD7768 FORMATx = 10 or 11, or AD7768-4 FORMAT0 = 1, One Data Output Pin

ADC CONVERSION OUTPUT: HEADER AND DATA

The AD7768 data is output on the DOUT0 to DOUT7 pins, depending on the FORMATx pins. The AD7768-4 data is output on the DOUT0 to DOUT3 pins, depending on the FORMAT0 pin. The actual structure of the data output for each ADC result is shown in Figure 99. Each ADC result comprises 32 bits. The first eight bits are the header status bits, which contain status information and the channel number. The names of each of the header status bits are shown in Table 35, and their functions are explained in the subsequent sections. This header is followed by a 24-bit ADC output in twos complement coding, MSB first.

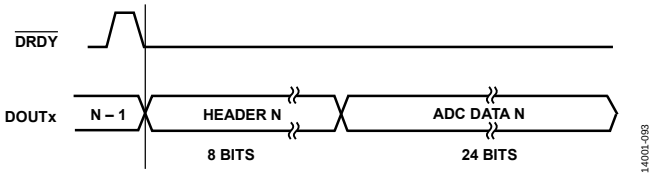

Figure 99. ADC Output: 8-Bit Header, 24-Bit ADC Conversion Data

Table 35. Header Status Bits

Bit	Bit Name
7	ERROR_FLAGGED
6	Filter not settled
5	Repeated data
4	Filter type
3	Filter saturated
[2:0]	Channel ID[2:0]

ERROR_FLAGGED

The error flagged bit indicates that a serious error has occurred. If this bit is set, a reset is required to clear this bit. This bit indicates that the external clock is not detected, a memory map bit has unexpectedly changed state, or an internal CRC error has been detected.

In the case where an external clock is not detected, the conversion results are output as all zeros regardless of the analog input voltages applied to the ADC channels.

Filter Not Settled

After power-up, reset, or synchronization, the AD7768/AD7768-4 clear the digital filters and begins conversion. Due to the weighting of the digital filters, there is a delay from the first conversion to fully settled data. The settling times for the AD7768/AD7768-4 when using the wideband and sinc5 filters are shown in Table 28 and Table 29, respectively. This bit is set if this settling delay has not yet elapsed.

Repeated Data

If different channels use different decimation rates, data outputs are repeated for the slower speed channels. In these cases, the header is output as normal with the repeated data bit set to 1, and the following repeated ADC result is output as all zeros. This bit indicates that the conversion result of all zeros is not real; it indicates that there is a repeated data condition because two different decimation rates are selected. This condition can only occur during SPI control of the AD7768/AD7768-4.

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Filter Type

In pin control mode, all channels operate using one filter selection. The filter selected in pin control mode is determined by the logic level of the FILTER pin. In SPI control mode, the digital filters can be selected on a per channel basis, using the mode registers. This header bit is 0 for channels using the wideband filter, and 1 for channels using the sinc5 filter.

Filter Saturated

The filter saturated bit indicates that the filter output is clipping at either positive or negative full scale. The digital filter clips if the signal goes beyond the specification of the filter; it does not wrap. The clipping may be caused by the analog input exceeding the analog input range, or by a step change in the input, which may cause overshoot in the digital filter. Clipping may also occur when the combination of the analog input signal and the channel gain register setting cause the signal seen by the filter to be higher than the analog input range.

Channel ID

The channel ID bits indicate the ADC channel from which the succeeding conversion data originates (see Table 36).

Table 36. Channel ID vs. Channel Number

Channel	Channel ID 2	Channel ID 1	Channel ID 0
Channel 0	0	0	0
Channel 1	0	0	1
Channel 2	0	1	0
Channel 3	0	1	1
Channel 4	1	0	0
Channel 5	1	0	1
Channel 6	1	1	0
Channel 7	1	1	1

Data Interface: Standard Conversion Operation

In standard mode operation, the AD7768/AD7768-4 operate as the master and stream data to the DSP or FPGA. The AD7768/AD7768-4 supply the data, the data clock (DCLK), and a falling edge framing signal ($\overline{\text{DRDY}}$) to the slave device. All of these signals are synchronous. The data interface connections to DSP/FPGA are shown in Figure 107. The FORMATx pins determine how the data is output from the AD7768/AD7768-4.

Figure 100 through Figure 103 show the data interface operating in standard mode at the maximum data rate. In all instances, $\overline{\text{DRDY}}$ is asserted one clock cycle before the MSB of the data conversion is made available on the data pin.

Each $\overline{\text{DRDY}}$ falling edge starts the output of the new ADC conversion data. The first eight bits output after the $\overline{\text{DRDY}}$ falling edge are the header bits; the last 24 bits are the ADC conversion result.

Figure 100, Figure 101, Figure 102, and Figure 103, are distinct examples of the impact of the FORMATx pins on the AD7768 output operating in standard conversion operation. Figure 104, Figure 105, and Figure 106show examples of the AD7768-4 interface configuration.

Figure 100 to Figure 103 represent running the AD7768 at maximum data rate for the three FORMATx options.

Figure 100 shows FORMATx = 00 each ADC has its own data out pin running at the MCLK/4 bit rate. In pin control mode, this is achieved by selecting Mode 0xA (fast mode, DCLK = MCLK/4, standard conversion, see Table 20) with the decimation rate set as ×32.

Figure 101 shows FORMATx = 01 share DOUT1 at the maximum bit rate. In pin control mode, this is achieved by selecting Mode 0x8 (fast mode, DCLK = MCLK/1, standard conversion) with a decimation rate of ×32.

If running in pin control mode, the example shown in Figure 103 represents Mode 0x4 (median mode, DCLK = MCLK/1, standard conversion) with a decimation rate of ×32, giving the maximum output data capacity possible on one DOUTx pin.

Figure 102 (AD7768) and Figure 106 (AD7768-4) show examples of one configuration where there can be long periods in which no data is output by the AD7768. This configuration depends on the FORMATx, MCLK, and decimation settings. In Figure 102, FORMATx = 01, meaning the channels share DOUT0 and DOUT1. In Figure 106, FORMAT0 = 1, meaning all channels share the DOUT0 pin. For both Figure 102 and Figure 106, DCLK = MCLK/4 and the decimation rate is 512.In pin control mode, this setup is achieved by selecting Mode 0x0A (fast mode, DCLK = MCLK/4, standard conversion mode). With a decimation rate of 512, the ratio of ODR to DCLK rate is high enough to show that only ¼ of the DRDY or ODR period is used with output data, and the other ¾ of the period DOUTx is low.

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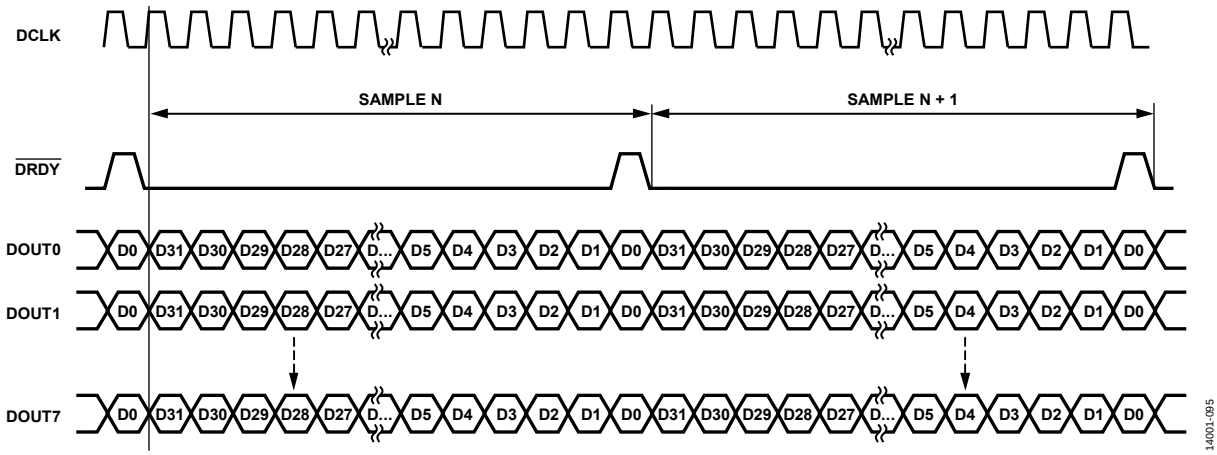

Figure 100. AD7768 FORMATx = 00: Each ADC Has a Dedicated Data Output Pin, Maximum Data Rate

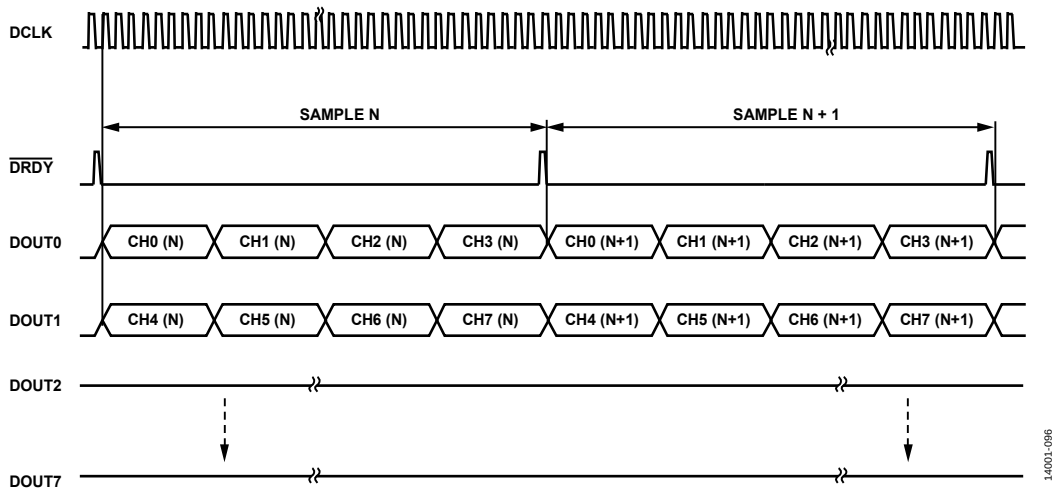

Figure 101. AD7768 FORMATx = 01: Channel 0 to Channel 3 Share DOUT0, and Channel 4 to Channel 7 Share DOUT1, Maximum Data Rate

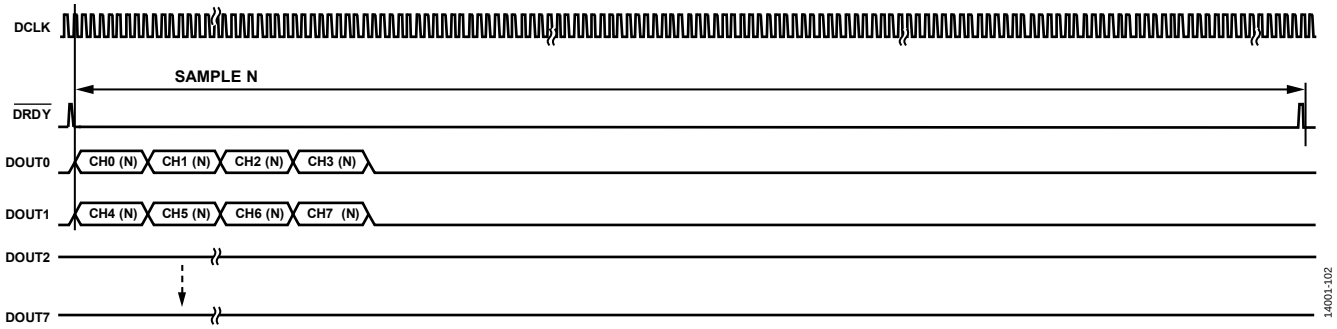

Figure 102. AD7768 FORMATx = 01: Channel 0 to Channel 3 Share DOUT0, and Channel 4 to Channel 7 Share DOUT1, Decimation=512

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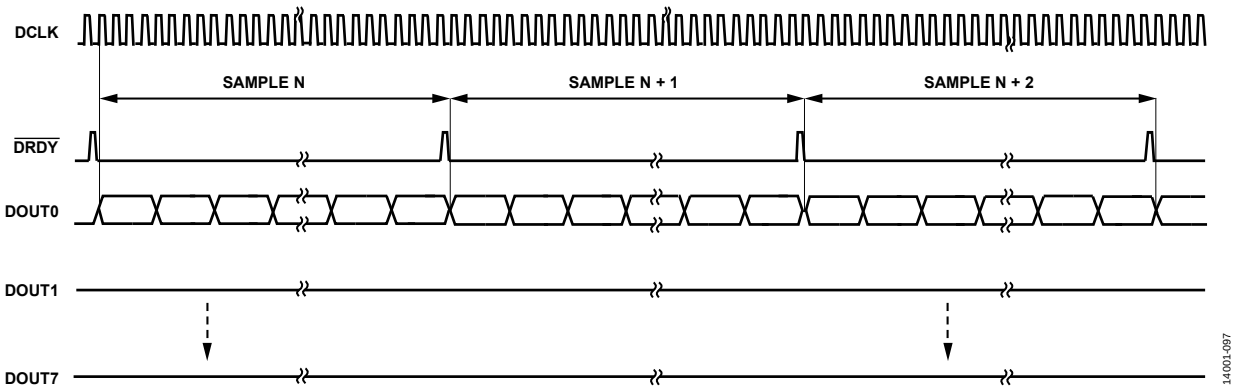

Figure 103. AD7768 FORMATx = 11 or 10: Channel 0 to Channel 7 Output on DOUT0 Only, Maximum Data Rate

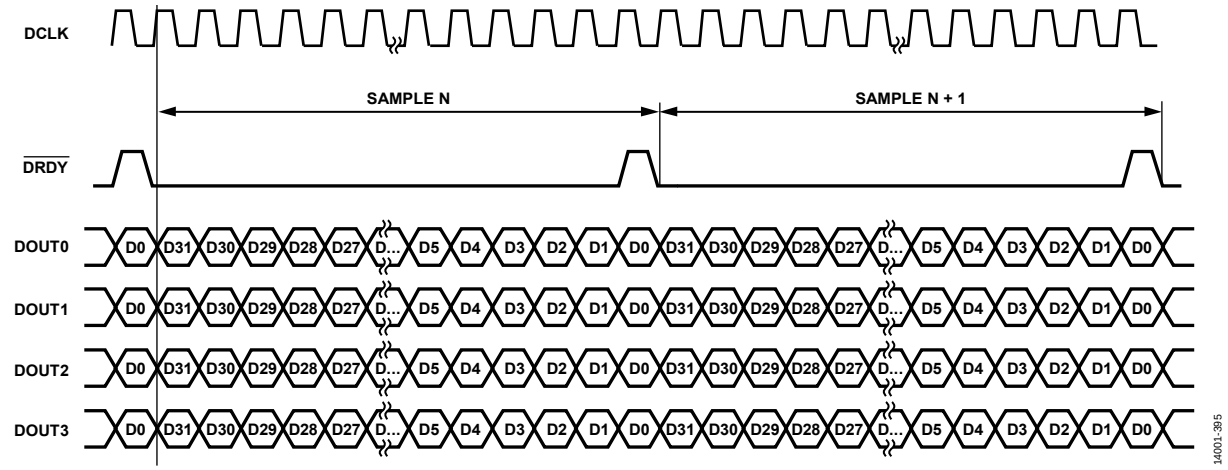

Figure 104. AD7768-4 FORMAT0 = 0: Each ADC Has a Dedicated Data Output Pin, Maximum Data Rate

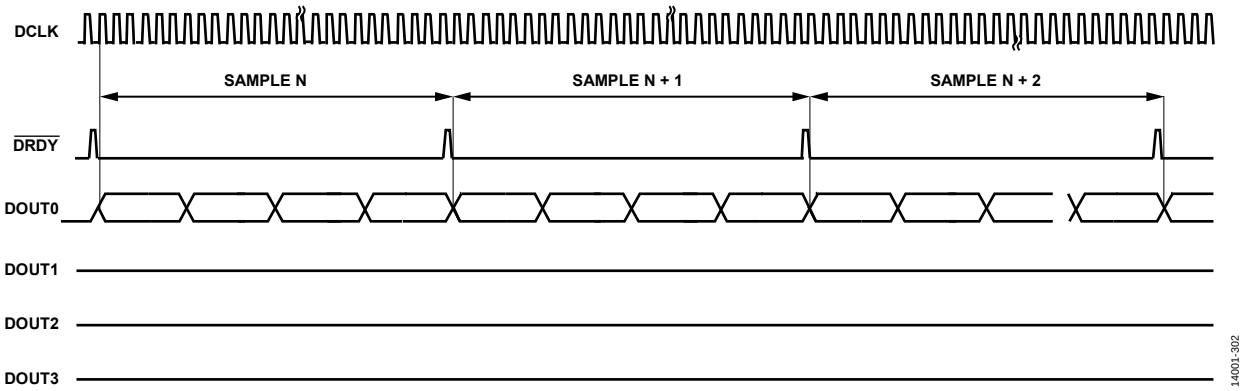

Figure 105. AD7768-4 FORMAT0 = 1: Channel 0 to Channel 3 Output on DOUT0 Only, Maximum Data Rate

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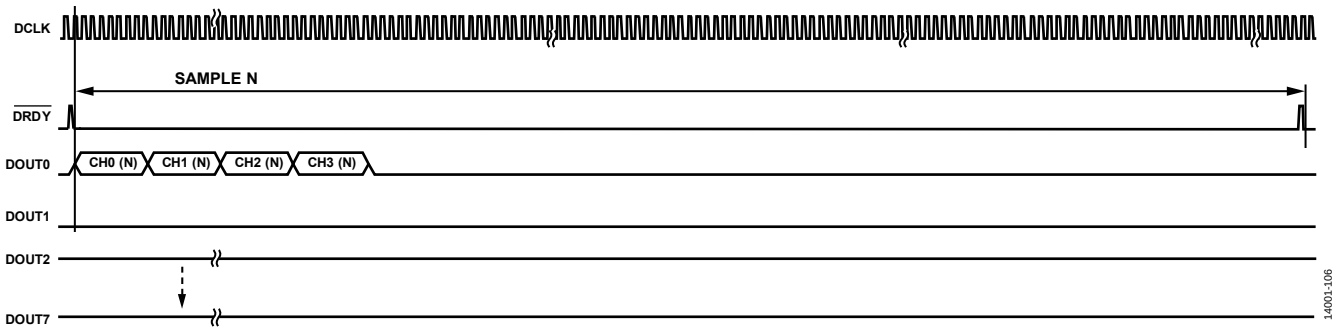

Figure 106. AD7768-4 FORMAT0 = 1: Channel 0 to Channel 3 Output on DOUT0 Only, Decimation =512

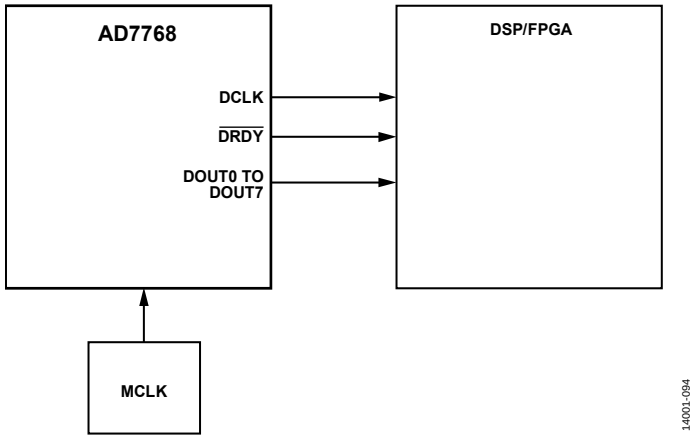

Figure 107. Data Interface: Standard Conversion Operation, AD7768 = Master, DSP/FPGA = Slave

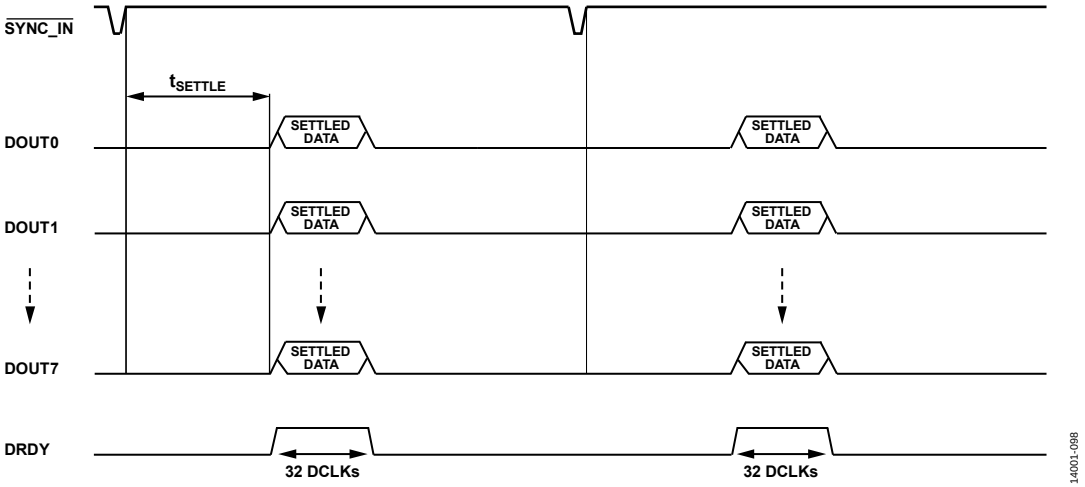

Figure 108. AD7768 One-Shot Mode

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Data Interface: One-Shot Conversion Operation

One-shot mode is available in both SPI and pin control modes. This conversion mode is available by selecting one of Mode 0xC to Mode 0xF when in pin control mode. In SPI control mode, set Bit 4 (one shot) of Register 0x06, the data control register. Figure 108 shows the device operating in one-shot mode.

In one-shot mode, the AD7768/AD7768-4 are pseudo slaves. Conversions occur on request by the master device, for example, the DSP or FPGA. The $\overline{\text{SYNC_IN}}$ pin initiates the conversion request. In one-shot mode, all ADCs run continuously; however, the rising edge of the $\overline{\text{SYNC_IN}}$ pin controls the point in time from which data is output.

To receive data, the master must pulse the $\overline{\text{SYNC_IN}}$ pin to reset the filter and force $\overline{\text{DRDY}}$ low. $\overline{\text{DRDY}}$ subsequently goes high to indicate to the master device that the device has valid settled data available. Unlike standard mode, $\overline{\text{DRDY}}$ remains high for the number of clock periods of valid data before it goes low again; thus, in this conversion mode, it is an active high frame of the data.

When the master pulses $\overline{\text{SYNC_IN}}$ and the AD7768/AD7768-4 receive the rising edge of this signal, the digital filter is reset and the full settling time of the filter elapses before the data is available. The duration of the settling time depends on the filter path and decimation rate. Running one-shot mode with the sinc5 filter allows the fastest throughput, because this filter has a lower settling time than the wideband filter.

As soon as settled data is available on any channel, the device outputs data from all channels. The contents of Bit 6 of the channel header status bits indicates whether the data is fully settled.

The period before the data is settled on all channels (t_{SETTLE}) is shown in Figure 108. . The settling (t_{SETTLE}) time for the AD7768 in one-shot mode is equivalent to the number of clock cycles specified as "Delay from the First MCLK Rise after SYNC_IN Rise to Earliest Settled Data, DRDY Rise" in Table 30. After the data has settled on all channels, $\overline{\text{DRDY}}$ is asserted high and the device outputs the required settled data on all channels before $\overline{\text{DRDY}}$ is asserted low. If the user configures the same filter and decimation rate on each ADC, the data is settled for all channels on the first $\overline{\text{DRDY}}$ output frame, which avoids a period of unsettled data prior to the settled data and ensures that all data is output at the same time on all ADCs. The device then waits for another $\overline{\text{SYNC_IN}}$ signal before outputting more data.

Because all the ADCs are sampling continuously, one-shot mode affects the sampling theory of the AD7768/AD7768-4. Particularly, a user periodically sending a $\overline{\text{SYNC_IN}}$ pulse to the device is a form of subsampling of the ADC output. The subsampling occurs at the rate of the $\overline{\text{SYNC_IN}}$ pulses. The $\overline{\text{SYNC_IN}}$ pulse must be synchronous with the master clock to ensure coherent sampling and to reduce the effects of jitter on the frequency response.

Daisy-Chaining

Daisy-chaining devices allows numerous devices to use the same data interface lines by cascading the outputs of multiple ADCs from separate AD7768/AD7768-4 devices. Only one ADC device has its data interface in direct connection with the digital host.

For the AD7768/AD7768-4, this connection can be implemented by cascading DOUT0 and DOUT1 through a number of devices, or just using DOUT0; whether two data output pins or only one data output pin is enabled depends on the FORMATx pins. The ability to daisy-chain devices and the limit on the number of devices that can be handled by the chain is dependent on the power mode, DCLK, and the decimation rate employed.

The maximum usable DCLK frequency allowed when daisy-chaining devices is limited by the combination of timing specifications in Table 3 or Table 5, as well as by the propagation delay of the data between devices and any skew between the MCLK signals at each AD7768/AD7768-4 device. The propagation delay and MCLK skew are dependent on the PCB layout and trace lengths.

This feature is especially useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity.

When daisy-chaining, on the AD7768, DOUT6 and DOUT7 become serial data inputs, and DOUT0 and DOUT1 remain as serial data outputs under the control of the FORMATx pins. For the AD7768-4 the DIN pin is the daisy chain serial data input pin and DOUT0 is the serial data output pin.

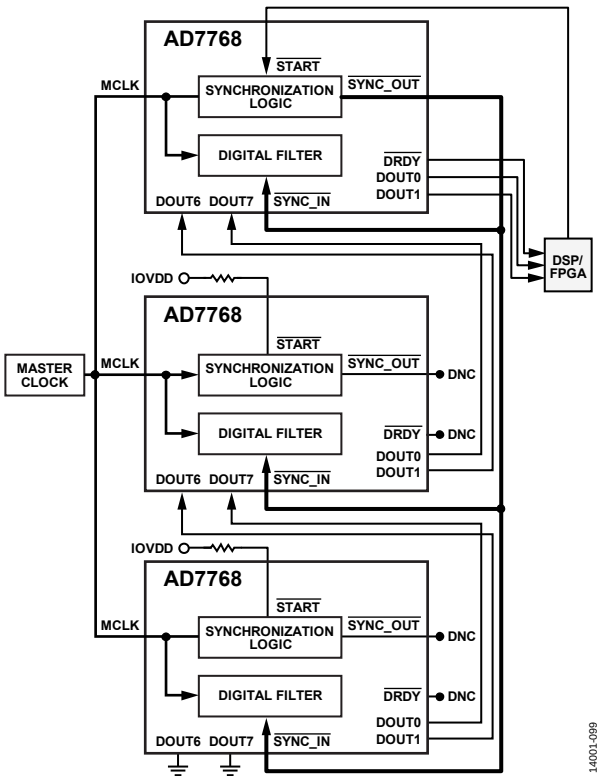

Figure 109. Daisy-Chaining Multiple AD7768 Devices

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Figure 109 shows an example of daisy-chaining AD7768 devices, when FORMATx = 01. In this case, the DOUT0 and DOUT1 pins of the AD7768 devices are cascaded to the DOUT6 and DOUT7 pins, respectively, of the next device in the chain. Data readback is analogous to clocking a shift register where data is clocked on the rising edge of DCLK.

The scheme operates by passing the output data of the DOUT0 and DOUT1 pins of an AD7768 upstream device to the DOUT6 and DOUT7 inputs, respectively, of the next AD7768 device downstream in the chain. The data then continues through the chain until it is clocked onto the DOUT0 and DOUT1 pins of the final downstream device in the chain.

The devices in the chain must be synchronized by using one of the following methods:

- Applying a synchronous signal to the $\overline{\text{SYNC_IN}}$ pin of all devices in the chain
- By routing the $\overline{\text{SYNC_OUT}}$ pin of the first device to the $\overline{\text{SYNC_IN}}$ pin of that same device and to the $\overline{\text{SYNC_IN}}$ pins of all other devices in the chain and applying an asynchronous signal to the $\overline{\text{START}}$ input.
- Issuing an SPI_SYNC command over the SPI control interface.

Figure 109 shows the configuration where an asynchronous signal is applied to the $\overline{\text{START}}$ pin, and the $\overline{\text{SYNC_OUT}}$ pin of the first device is connected to the $\overline{\text{SYNC_IN}}$ pins of all devices in the chain

Daisy chaining can be achieved in a similar manner on the AD7768 and AD7768-4 when using only the DOUT0 pin. In this case, only Pin 21 of the AD7768/AD7768-4 is used as the serial data input pin.

In a daisy-chained system of AD7768/AD7768-4 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768/AD7768-4 device sharing a single MCLK signal, where the $\overline{\text{DRDY}}$ pin of only one device is used to detect new data.

The maximum DCLK frequency that can be used when daisy-chaining devices is a function of the AD7768/AD7768-4 timing specifications (t_4 and t_{11} in Table 3 and Table 5) and any timing differences between the AD7768/AD7768-4 devices due to layout and spacing of devices on the PCB.

Use the following formula to aid in determining the maximum operating frequency of the interface:

$$f_{MAX} = \frac{1}{2 \times (t_{11} + t_4 + t_P + t_{SKEW})}$$

where:
f_{MAX} is the maximum useable DCLK frequency.
t_{11} and t_4 are the AD7768/AD7768-4 timing specifications (see Table 3 and Table 5).
t_P is the maximum propagation delay of the data between successive AD7768/AD7768-4 devices in the chain.
t_{SKEW} is the maximum skew in the MCLK signal seen by any pair of AD7768/AD7768-4 devices in the chain.

Synchronization

The basic provision for synchronizing multiple devices is that each device is clocked with the same base MCLK signal and that the user can provide a synchronization signal to at least one of the devices by one of the methods described in this section.

The AD7768/AD7768-4 offer three options to allow ease of system synchronization. Choosing between the options depends on the system, but is determined by whether the user can supply a synchronization pulse that is truly synchronous with the base MCLK signal.

Two synchronization pulses are required in a system of more than one AD7768/AD7768-4 device sharing a single MCLK signal, to ensure that all devices are in close phase alignment, or where the DRDY pin of only one device is used to detect new data.

If the user cannot provide a signal that is synchronous to the base MCLK signal, one of the following two methods can be employed:

- Apply a $\overline{\text{START}}$ pulse to the first AD7768 or AD7768-4 device. The first AD7768 or AD7768-4 device samples the asynchronous $\overline{\text{START}}$ pulse and generates a pulse on $\overline{\text{SYNC_OUT}}$ of the first device related to the base MCLK signal for distribution locally.
- Use synchronization over SPI (only available in SPI control mode) to write a synchronization command to the first AD7768 or AD7768-4 device. Similarly to the $\overline{\text{START}}$ pin method, the SPI sync generates a pulse on $\overline{\text{SYNC_OUT}}$ of the first device related to the base MCLK signal for distribution locally.

In both cases, route the $\overline{\text{SYNC_OUT}}$ pin of the first device to the $\overline{\text{SYNC_IN}}$ pin of that same device and to the $\overline{\text{SYNC_IN}}$ pins of all other devices that are to be synchronized (see Figure 110). The $\overline{\text{SYNC_OUT}}$ pins of the other devices must remain open circuit. Tie all unused $\overline{\text{START}}$ pins to a Logic 1 through pull-up resistors.

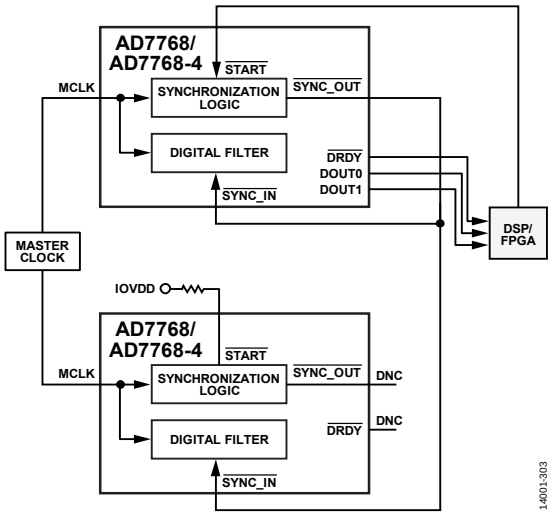

Figure 110. Synchronizing Multiple AD7768/AD7768-4 Devices Using $\overline{\text{SYNC_OUT}}$

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If the user can provide a signal that is synchronous to the base MCLK, this signal can be applied directly to the SYNC_IN pin. Route the signal from a star point and connect it directly to the SYNC_IN pin of each AD7768/AD7768-4 device (see Figure 111). The signal is sampled on the rising MCLK edge; setup and hold times are associated with the SYNC_IN input are relative to the AD7768/AD7768-4 MCLK rising edge.

In this case, tie the START pin to Logic 1 through a pull-up resistor; SYNC_OUT is not used and can remain open circuit.

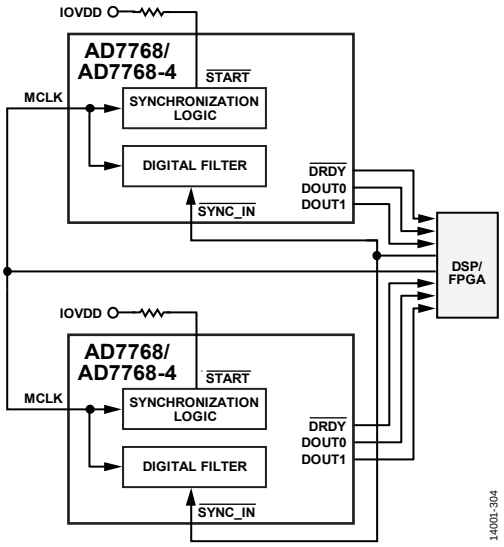

Figure 111. Synchronizing Multiple AD7768/AD7768-4 Devices Using Only SYNC_IN

CRC Check on Data Interface

The AD7768/AD7768-4 deliver 32 bits per channel as standard, which by default consists of 8 status header bits and 24 bits of data.

The header bits default per the description in Table 35. However, there is also the option to employ a CRC check on the ADC conversion data. This functionality is available only when operating in SPI control mode. The function is controlled by CRC_SELECT in the interface configuration register (Register 0x07). When employed, the CRC message is calculated internally by the AD7768/AD7768-4 on a per channel basis. The CRC then replaces the 8-bit header every four samples or every 16 samples.

The following is an example of how the CRC works for four-sample mode (see Figure 112):

1. After a synchronization pulse is applied to the AD7768/AD7768-4, the CRC register is cleared to 0xFF.
2. The next four 24-bit conversion data samples (N to N + 3) for a given channel stream into the CRC calculation.
3. For the first three samples that are output after the synchronization pulse (N to N + 2), the header contains the normal status bits.
4. For the fourth sample after the synchronization pulse (N + 3), the 8-bit CRC is sent out instead of the normal header status bits, followed by the sample conversion data. This CRC calculation includes the conversion data that is output immediately after the CRC header.
5. The CRC register is then cleared back to 0xFF and the cycle begins again for the fifth to eighth samples after the synchronization pulse.

It is possible to have channels outputting at different rates (for example decimation by 32 on Channel 0 and decimation by 64 on Channel 1). In such cases, the CRC header still appears across all channels at the same time, that is, at every fourth DRDY pulse after a synchronization. For the channels operating at a relatively slower ODR, the CRC is still calculated and emitted every 4 or 16 DRDY cycles, even if this means that the nulled data is included. Therefore, a CRC is calculated for only nulled samples or for a combination of nulled samples and actual conversion data.

The AD7768/AD7768-4 use a CRC polynomial to calculate the CRC message. The 8-bit CRC polynomial used is $x^8 + x^2 + x + 1$.

The following code is a snippet of the C code which shows how the CRC value can be calculated for a given set of ADC conversion results. Running this code on sets of 4 or 16 conversion results gives the CRC value that the AD7768 generatse, per channel. The user can then compare the computed value from this code to the actual CRC value read from the AD7768, and so confirm that the data was read without error.

```
#include <stdio.h>
  FILE *fi1;
  FILE *fo1;
main(){
int num_data_bits=24;  // 24 or 16
int num_data_words=4; //4 or 16

int data;
int crc[8],crc_new[8];
int i,j,n,k,num,bit,result;
const int num_crc_bits=8;
int bit_sel[num_data_bits];

bit_sel[23] = 0x800000;
bit_sel[22] = 0x400000;
bit_sel[21] = 0x200000;
bit_sel[20] = 0x100000;
bit_sel[19] = 0x080000;
bit_sel[18] = 0x040000;
bit_sel[17] = 0x020000;
bit_sel[16] = 0x010000;
bit_sel[15] = 0x008000;
bit_sel[14] = 0x004000;
```


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```
bit_sel[13] = 0x002000;
bit_sel[12] = 0x001000;
bit_sel[11] = 0x000800;
bit_sel[10] = 0x000400;
bit_sel[9] = 0x000200;
bit_sel[8] = 0x000100;
bit_sel[7] = 0x000080;
bit_sel[6] = 0x000040;
bit_sel[5] = 0x000020;
bit_sel[4] = 0x000010;
bit_sel[3] = 0x000008;
bit_sel[2] = 0x000004;
bit_sel[1] = 0x000002;
bit_sel[0] = 0x000001;

fi1 = fopen("adcdata.txt", "r");
fo1 = fopen("crc_out.txt", "w");
j = 1;

//initialise CRC to FF
for (i=0;i<num_crc_bits;i++) crc[i]=1;

      result = ((crc[7]<<7) & 0x0080)
        | ((crc[6]<<6) & 0x0040)
        | ((crc[5]<<5) & 0x0020)
        | ((crc[4]<<4) & 0x0010)
        | ((crc[3]<<3) & 0x0008)
        | ((crc[2]<<2) & 0x0004)
        | ((crc[1]<<1) & 0x0002)
        | ((crc[0]<<0) & 0x0001);

printf("CRC Initialised to 0x%.02X \n",result);
fprintf(fo1,"--------------------------------\n");
fprintf(fo1,"CRC Initialised to 0x%.02X \n",result);

//run CRC on  data

for (n = 0; n < num_data_words; n++){

    fprintf(fo1,"--------------------------------\n");
    fprintf(fo1,"Loop %d start\n",n+1);

fprintf(fo1,"--------------------------------\n");
fprintf(fo1,"ADC Data values\n");
fprintf(fo1,"--------------------------------\n");
fscanf(fi1,"%x\n",&num);
fprintf(fo1,"0x%.06X\n",num);
fprintf(fo1,"--------------------------------\n");
fprintf(fo1,"CRC values\n");
fprintf(fo1,"--------------------------------\n");
for (k=num_data_bits-1;k>=0;k--){
  //for (i=7;i>=0;i--){
  //   printf("%1d",crc[i]);
  //}
  bit = (num & bit_sel[k]); // msb first
  data = bit>>(k);
  printf(" bit_sel is: %.06X - data is : %X   ",bit_sel[k], data);
  crc_new[0]=data^crc[7];
  //debug printf(" qq(0) = %1d ",qq[0]);
  crc_new[1]=data^crc[7]^crc[0];
  crc_new[2]=data^crc[7]^crc[1];
  crc_new[3]=crc[2];
  crc_new[4]=crc[3];
  crc_new[5]=crc[4];
  crc_new[6]=crc[5];
  crc_new[7]=crc[6];
  //debug    printf("%8d   ",j);
  for (i=num_crc_bits-1;i>=0;i--){
     crc[i]=crc_new[i];
     printf("%1d",crc[i]);
     }
  //debug    printf("\n");
  result = ((crc[7]<<7) & 0x0080)
    | ((crc[6]<<6) & 0x0040)
    | ((crc[5]<<5) & 0x0020)
    | ((crc[4]<<4) & 0x0010)
    | ((crc[3]<<3) & 0x0008)
    | ((crc[2]<<2) & 0x0004)
    | ((crc[1]<<1) & 0x0002)
    | ((crc[0]<<0) & 0x0001);
     printf(" intermediate res is 0x%.02X\n",result);
     fprintf(fo1,"intermediate res is 0x%.02X\n",result);
```


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```
if (k == 0) {
        printf("loop %d:res is 0x%.02X\n",n,result);
        }

    }
  }
```

```
        fprintf(fo1,"--------------------------------\n");
        printf("Final CRC value = 0x%.02X\n",result);
        fprintf(fo1,"CRC value  = 0x%.02X\n",result);
}
```

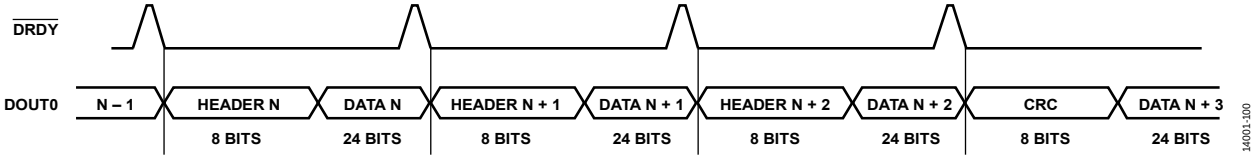

Figure 112. CRC 4-Bit Stream

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FUNCTIONALITY

GPIO FUNCTIONALITY

The AD7768/AD7768-4 have additional GPIO functionality when operated in SPI mode. This fully configurable mode allows the device to operate five GPIOs. The GPIOx pins can be set as inputs or outputs (read or write) on a per pin basis.

In write mode, these GPIO pins can be used to control other circuits such as switches, multiplexers, buffers, over the same SPI interface as the AD7768/AD7768-4. Sharing the SPI interface in this way allows the user to use a lower overall number of data lines from the controller compared to a system where multiple control signals are required. This sharing is especially useful in systems where reducing the number of control lines across an isolation barrier is important. See Figure 113 and Figure 114 for details of the GPIO pin options available on the AD7768 and AD7768-4, respectively.

Similarly, a GPIO read is a useful feature because it allows a peripheral device to send information to the input GPIO and then this information can be read from the SPI interface of the AD7768/AD7768-4.

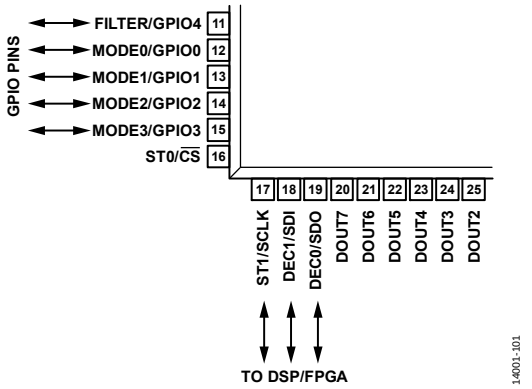

Figure 113. AD7768 GPIO Functionality

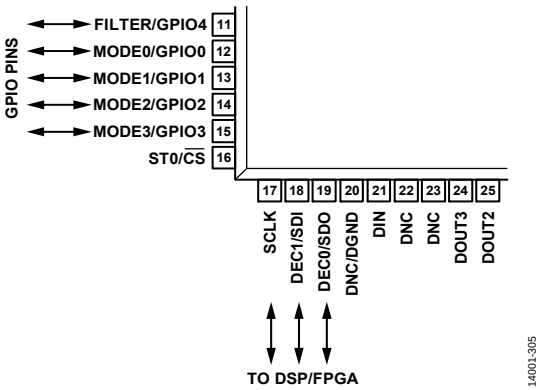

Figure 114. AD7768-4 GPIO Functionality

Configuration control and readback of the GPIOx pins are set in Register 0x0E, Register 0x0F, and Register 0x10 (see Table 49, Table 50, and Table 51 for more information for the AD7768, and Table 75, Table 76, and Table 77 for the AD7768-4).

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AD7768 REGISTER MAP DETAILS (SPI CONTROL)

AD7768 REGISTER MAP

See Table 63 and the AD7768-4 Register Map Details (SPI Control) section for the AD7768-4 register map and register functions.

Table 37. Detailed AD7768 Register Map

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	Channel standby	CH_7	CH_6	CH_5	CH_4	CH_3	CH_2	CH_1	CH_0	0x00	RW
0x01	Channel Mode A	Unused				FILTER_TYPE_A	DEC_RATE_A			0x0D	RW
0x02	Channel Mode B	Unused				FILTER_TYPE_B	DEC_RATE_B			0x0D	RW
0x03	Channel mode select	CH_7_MODE	CH_6_MODE	CH_5_MODE	CH_4_MODE	CH_3_MODE	CH_2_MODE	CH_1_MODE	CH_0_MODE	0x00	RW
0x04	POWER_MODE	SLEEP_MODE	Unused	POWER_MODE		LVDS_ENABLE	Unused	MCLK_DIV		0x00	RW
0x05	General configuration	Unused	Reserved	RETIME_EN	VCM_PD	Reserved	Unused	VCM_VSEL		0x08	RW
0x06	Data control	SPI_SYNC	Unused		SINGLE_SHOT_EN	Unused		SPI_RESET		0x80	RW
0x07	Interface configuration	Unused				CRC_SELECT		DCLK_DIV		0x0	RW
0x08	BIST control	Unused							RAM_BIST_START	0x0	RW
0x09	Device status	Unused				CHIP_ERROR	NO_CLOCK_ERROR	RAM_BIST_PASS	RAM_BIST_RUNNING	0x0	R
0x0A	Revision ID	REVISION_ID								0x06	R
0x0B	Reserved	Reserved								0x00	R
0x0C	Reserved	Reserved								0x00	R
0x0D	Reserved	Reserved								0x00	R
0x0E	GPIO control	UGPIO_ENABLE	Unused		GPIOE4_FILTER	GPIOE3_MODE3	GPIOE2_MODE2	GPIOE1_MODE1	GPIO0_MODE0	0x00	RW
0x0F	GPIO write data	Unused			GPIO4_WRITE	GPIO3_WRITE	GPIO2_WRITE	GPIO1_WRITE	GPIO0_WRITE	0x00	RW
0x10	GPIO read data	Unused			GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ	GPIO0_READ	0x00	R
0x11	Precharge Buffer 1	CH3_PREBUF_NEG_EN	CH3_PREBUF_POS_EN	CH2_PREBUF_NEG_EN	CH2_PREBUF_POS_EN	CH1_PREBUF_NEG_EN	CH1_PREBUF_POS_EN	CH0_PREBUF_NEG_EN	CH0_PREBUF_POS_EN	0xFF	RW
0x12	Precharge Buffer 2	CH7_PREBUF_NEG_EN	CH7_PREBUF_POS_EN	CH6_PREBUF_NEG_EN	CH6_PREBUF_POS_EN	CH5_PREBUF_NEG_EN	CH5_PREBUF_POS_EN	CH4_PREBUF_NEG_EN	CH4_PREBUF_POS_EN	0xFF	RW
0x13	Positive reference precharge buffer	CH7_REFP_BUF	CH6_REFP_BUF	CH5_REFP_BUF	CH4_REFP_BUF	CH3_REFP_BUF	CH2_REFP_BUF	CH1_REFP_BUF	CH0_REFP_BUF	0x00	RW
0x14	Negative reference precharge buffer	CH7_REFN_BUF	CH6_REFN_BUF	CH5_REFN_BUF	CH4_REFN_BUF	CH3_REFN_BUF	CH2_REFN_BUF	CH1_REFN_BUF	CH0_REFN_BUF	0x00	RW
0x1E	Channel 0 offset	CH0_OFFSET_MSB								0x00	RW
0x1F		CH0_OFFSET_MID									
0x20		CH0_OFFSET_LSB									
0x21	Channel 1 offset	CH1_OFFSET_MSB								0x00	RW
0x22		CH1_OFFSET_MID									
0x23		CH1_OFFSET_LSB									
0x24	Channel 2 offset	CH2_OFFSET_MSB								0x00	RW
0x25		CH2_OFFSET_MID									
0x26		CH2_OFFSET_LSB									
0x27	Channel 3 offset	CH3_OFFSET_MSB								0x00	RW
0x28		CH3_OFFSET_MID									
0x29		CH3_OFFSET_LSB									
0x2A	Channel 4 offset	CH4_OFFSET_MSB								0x00	RW
0x2B		CH4_OFFSET_MID									
0x2C		CH4_OFFSET_LSB									
0x2D	Channel 5 offset	CH5_OFFSET_MSB								0x00	RW
0x2E		CH5_OFFSET_MID									
0x2F		CH5_OFFSET_LSB									
0x30	Channel 6 offset	CH6_OFFSET_MSB								0x00	RW
0x31		CH6_OFFSET_MID									
0x32		CH6_OFFSET_LSB									
0x33	Channel 7 offset	CH7_OFFSET_MSB								0x00	RW
0x34		CH7_OFFSET_MID									
0x35		CH7_OFFSET_LSB									

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Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x36	Channel 0 gain	CH0_GAIN_MSB								0xXX	RW
0x37		CH0_GAIN_MID									
0x38		CH0_GAIN_LSB									
0x39	Channel 1 gain	CH1_GAIN_MSB								0xXX	RW
0x3A		CH1_GAIN_MID									
0x3B		CH1_GAIN_LSB									
0x3C	Channel 2 gain	CH2_GAIN_MSB								0xXX	RW
0x3D		CH2_GAIN_MID									
0x3E		CH2_GAIN_LSB									
0x3F	Channel 3 gain	CH3_GAIN_MSB								0xXX	RW
0x40		CH3_GAIN_MID									
0x41		CH3_GAIN_LSB									
0x42	Channel 4 gain	CH4_GAIN_MSB								0xXX	RW
0x43		CH4_GAIN_MID									
0x44		CH4_GAIN_LSB									
0x45	Channel 5 gain	CH5_GAIN_MSB								0xXX	RW
0x46		CH5_GAIN_MID									
0x47		CH5_GAIN_LSB									
0x48	Channel 6 gain	CH6_GAIN_MSB								0xXX	RW
0x49		CH6_GAIN_MID									
0x4A		CH6_GAIN_LSB									
0x4B	Channel 7 gain	CH7_GAIN_MSB								0xXX	RW
0x4C		CH7_GAIN_MID									
0x4D		CH7_GAIN_LSB									
0x4E	Channel 0 sync offset	CH0_SYNC_OFFSET								0x00	RW
0x4F	Channel 1 sync offset	CH1_SYNC_OFFSET								0x00	RW
0x50	Channel 2 sync offset	CH2_SYNC_OFFSET								0x00	RW
0x51	Channel 3 sync offset	CH3_SYNC_OFFSET								0x00	RW
0x52	Channel 4 sync offset	CH4_SYNC_OFFSET								0x00	RW
0x53	Channel 5 sync offset	CH5_SYNC_OFFSET								0x00	RW
0x54	Channel 6 sync offset	CH6_SYNC_OFFSET								0x00	RW
0x55	Channel 7 sync offset	CH7_SYNC_OFFSET								0x00	RW
0x56	Diagnostic receiver (Rx)	CH7_RX	CH6_RX	CH5_RX	CH4_RX	CH3_RX	CH2_RX	CH1_RX	CH0_RX	0x00	RW
0x57	Diagnostic mux control	Unused	GRPB_SEL			Unused	GRPA_SEL			0x00	RW
0x58	Modulator delay control	Unused				CLK_MOD_DEL_EN		Reserved		0x02	RW
0x59	Chop control	Unused				GRPA_CHOP		GRPB_CHOP		0x0A	RW

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CHANNEL STANDBY REGISTER

Address: 0x00, Reset: 0x00, Name: Channel Standby

Each of the ADC channels can be put into standby mode independently by setting the appropriate bit in the channel standby register. When a channel is in standby mode, its position in the data output stream is held. The 8-bit header is all zeros, as is the conversion result output of 24 zeros.

The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768.

The crystal excitation circuitry is associated with the Channel 4 circuitry. If Channel 4 is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 4 must be enabled while the external crystal is used on the AD7768.

Table 38. Bit Descriptions for Channel Standby

Bits	Bit Name	Settings	Description	Reset	Access
7	CH_7		Channel 7	0x0	RW
		0	Enabled		
		1	Standby		
6	CH_6		Channel 6	0x0	RW
		0	Enabled		
		1	Standby		
5	CH_5		Channel 5	0x0	RW
		0	Enabled		
		1	Standby		
4	CH_4		Channel 4	0x0	RW
		0	Enabled		
		1	Standby		
3	CH_3		Channel 3	0x0	RW
		0	Enabled		
		1	Standby		
2	CH_2		Channel 2	0x0	RW
		0	Enabled		
		1	Standby		
1	CH_1		Channel 1	0x0	RW
		0	Enabled		
		1	Standby		
0	CH_0		Channel 0	0x0	RW
		0	Enabled		
		1	Standby		

CHANNEL MODE A REGISTER

Address: 0x01, Reset: 0x0D, Name: Channel Mode A

Two mode options are available on the AD7768 ADCs. The channel modes are defined by the contents of the Channel Mode A and Channel Mode B registers. Each mode is then mapped as desired to the required ADC channel. Channel Mode A and Channel Mode B allow different filter types and decimation rates to be selected and mapped to any of the ADC channels.

When different decimation rates are selected, the AD7768 output a data ready signal at the fastest selected decimation rate. Any channel that runs at a lower output data rate is updated only at that slower rate. In between valid result data, the data for that channel is set to zero and the repeated data bit is set in the header status bits to distinguish it from a real conversion result (see the ADC Conversion Output: Header and Data section).

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Table 39. Bit Descriptions for Channel Mode A

Bits	Bit Name	Settings	Description	Reset	Access
3	FILTER_TYPE_A		Filter selection	0x1	RW
		0	Wideband filter		
		1	Sinc5 filter		
[2:0]	DEC_RATE_A		Decimation rate selection	0x5	RW
		000	×32		
		001	×64		
		010	×128		
		011	×256		
		100	×512		
		101	×1024		
		110	×1024		
		111	×1024		

CHANNEL MODE B REGISTER

Address: 0x02, Reset: 0x0D, Name: Channel Mode B

Table 40. Bit Descriptions for Channel Mode B

Bits	Bit Name	Settings	Description	Reset	Access
3	FILTER_TYPE_B		Filter selection	0x1	RW
		0	Wideband filter		
		1	Sinc5 filter		
[2:0]	DEC_RATE_B		Decimation rate selection	0x5	RW
		000	×32		
		001	×64		
		010	×128		
		011	×256		
		100	×512		
		101	×1024		
		110	×1024		
		111	×1024		

CHANNEL MODE SELECT REGISTER

Address: 0x03, Reset: 0x00, Name: Channel Mode Select

This register selects the mapping of each ADC channel to either Channel Mode A or Channel Mode B.

Table 41. Bit Descriptions for Channel Mode Select

Bits	Bit Name	Settings	Description	Reset	Access
7	CH_7_MODE		Channel 7	0x0	RW
		0	Mode A		
		1	Mode B		
6	CH_6_MODE		Channel 6	0x0	RW
		0	Mode A		
		1	Mode B		
5	CH_5_MODE		Channel 5	0x0	RW
		0	Mode A		
		1	Mode B		
4	CH_4_MODE		Channel 4	0x0	RW
		0	Mode A		
		1	Mode B		
3	CH_3_MODE		Channel 3	0x0	RW
		0	Mode A		
		1	Mode B		

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Bits	Bit Name	Settings	Description	Reset	Access
2	CH_2_MODE		Channel 2	0x0	RW
		0	Mode A		
		1	Mode B		
1	CH_1_MODE		Channel 1	0x0	RW
		0	Mode A		
		1	Mode B		
0	CH_0_MODE		Channel 0	0x0	RW
		0	Mode A		
		1	Mode B		

POWER MODE SELECT REGISTER

Address: 0x04, Reset: 0x00, Name: POWER_MODE

Table 42. Bit Descriptions for POWER_MODE

Bits	Bit Name	Settings	Description	Reset	Access
7	SLEEP_MODE		In sleep mode, many of the digital clocks are disabled and all of the ADCs are disabled. The analog LDOs are not disabled. The AD7768 SPI is live and is available to the user. Writing to this bit brings the AD7768 out of sleep mode again.	0x0	RW
		0	Normal operation.		
		1	Sleep mode.		
[5:4]	POWER_MODE		Power mode. The power mode bits control the power mode setting for the bias currents used on all ADCs on the AD7768. The user can select the current consumption target to meet the application. The power modes of fast, median, and low power give optimum performance when mapped to the correct MCLK division setting. These power mode bits do not control the MCLK division of the ADCs. See the MCLK_DIV bits for control of the division of the MCLK input.	0x0	RW
		00	Low Power mode.		
		10	Median mode.		
		11	Fast mode.		
3	LVDS_ENABLE		LVDS clock.	0x0	RW
		0	LVDS input clock disabled.		
		1	LVDS input clock enabled.		
[1:0]	MCLK_DIV		MCLK division. The MCLK division bits control the divided ratio between the MCLK applied at the input to the AD7768 and the clock used by each of the ADC modulators. The appropriate division ratio depends on the following factors: power mode, decimation rate, and the base MCLK available in the system. See the Clocking, Sampling Tree, and Power Scaling section for more information on setting MCLK_DIV correctly.	0x0	RW
		00	MCLK/32: with a base MCLK of 32.768 MHz, set to MCLK/32 for low power mode.		
		10	MCLK/8: with a base MCLK of 32.768 MHz, set to MCLK/8 for median mode.		
		11	MCLK/4: with a base MCLK of 32.768 MHz, set to MCLK/4 for fast mode.		

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GENERAL DEVICE CONFIGURATION REGISTER

Address: 0x05, Reset: 0x08, Name: General Configuration

Table 43. Bit Descriptions for General Configuration

Bits	Bit Name	Settings	Description	Reset	Access
6	CLK_QUAL_DIS		Clock qualification disable bit. Allows the user to disable the external clock source qualification. After reset, the external MCLK frequency is checked to be at least approximately 1.15 MHz, before being accepted as valid and before the AD7768 hands control over to the external clock source. If this qualification check fails, the NO_CLOCK_ERROR bit is set and the AD7768 continues to run using the internal startup clock. Users can disable this qualification check to force the AD7768 to accept and hand control over to an external clock source with a lower frequency.	0x0	RW
		0	Enabled. Clock qualification check is performed.		
		1	Disabled. Clock qualification check is not performed.		
5	RETIME_EN		$\overline{\text{SYNC_OUT}}$ signal retime enable bit.	0x0	RW
		0	Disabled: normal timing of $\overline{\text{SYNC_OUT}}$.		
		1	Enabled: $\overline{\text{SYNC_OUT}}$ signal derived from alternate MCLK edge.		
4	VCM_PD		VCM buffer power-down.	0x0	RW
		0	Enabled: VCM buffer normal mode.		
		1	Powered down: VCM buffer powered down.		
[1:0]	VCM_VSEL		VCM voltage. These bits select the output voltage of the VCM pin. This voltage is derived from the AVDD1 supply and can be output as half of that AVDD1 voltage, or other fixed voltages, with respect to AVSS. The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768.	0x0	RW
		00	(AVDD1 − AVSS)/2 V.		
		01	1.65 V.		
		10	2.5 V.		
		11	2.14 V.		

DATA CONTROL: SOFT RESET, SYNC, AND SINGLE-SHOT CONTROL REGISTER

Address: 0x06, Reset: 0x80, Name: Data Control

Table 44. Bit Descriptions for Data Control

Bits	Bit Name	Settings	Description	Reset	Access
7	SPI_SYNC		Software synchronization of the AD7768. This command has the same effect as sending a signal pulse to the $\overline{\text{START}}$ pin. To operate the SPI_SYNC, the user must write to this bit two separate times. First, write a zero, putting SPI_SYNC low, and then write a 1 to set SPI_SYNC logic high again. The SPI_SYNC command is recognized after the last rising edge of SCLK in the SPI instruction where the SPI_SYNC bit is changed from low to high. The SPI_SYNC command is then output synchronous to the AD7768 MCLK on the $\overline{\text{SYNC_OUT}}$ pin. The user must connect the $\overline{\text{SYNC_OUT}}$ signal to the $\overline{\text{SYNC_IN}}$ pin on the PCB. The $\overline{\text{SYNC_OUT}}$ pin can also be routed to the $\overline{\text{SYNC_IN}}$ pins of other AD7768 devices, allowing larger channel count simultaneous sampling systems. As per any synchronization pulse seen by the $\overline{\text{SYNC_IN}}$ pin, the digital filters of the AD7768 are reset. The full settling time of the filters must elapse before data is output on the data interface. In a daisy-chained system of AD7768 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768 device sharing a single MCLK signal, where the $\overline{\text{DRDY}}$ pin of only one device is used to detect new data.	0x1	RW

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Bits	Bit Name	Settings	Description	Reset	Access
		0	Change to SPI_SYNC low.		
		1	Change to SPI_SYNC high.		
4	SINGLE_SHOT_EN		One-shot mode. Enables one-shot mode. In one-shot mode, the AD7768 output a conversion result in response to a $\overline{\text{SYNC_IN}}$ rising edge.	0x0	RW
		0	Disabled.		
		1	Enabled.		
[1:0]	SPI_RESET		Soft reset. These bits allow a full device reset over the SPI port. Two successive commands must be received in the correct order to generate a reset: first, write 0x03 to the soft reset register, and then write 0x02 to the soft reset register. This sequence causes the digital core to reset and all registers return to their default values. Following a soft reset, if the SPI master sends a command to the AD7768, the devices respond on the next frame to that command with an output of 0x0E00.	0x0	RW
		00	No effect.		
		01	No effect.		
		10	Second reset command.		
		11	First reset command.		

INTERFACE CONFIGURATION REGISTER

Address: 0x07, Reset: 0x0, Name: Interface Configuration

Table 45. Bit Descriptions for Interface Configuration

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	CRC_SELECT		CRC select. These bits allow the user to implement a CRC on the data interface. When selected, the CRC replaces the header every fourth or 16th output sample depending on the CRC option chosen. There are two options for the CRC; both use the same polynomial: $x^8 + x^2 + x + 1$. The options offer the user the ability to reduce the duty cycle of the CRC calculation by performing it less often: in the case of having it every 16th sample or more often in the case of every fourth conversion. The CRC is calculated on a per channel basis and it includes conversion data only.	0x0	RW
		00	No CRC. Status bits with every conversion.		
		01	Replace the header with CRC message every 4 samples.		
		10	Replace the header with CRC message every 16 samples.		
		11	Replace the header with CRC message every 16 samples.		
[1:0]	DCLK_DIV		DCLK divider. These bits control division of the DCLK clock used to clock out conversion data on the DOUTx pins. The DCLK signal is derived from the MCLK applied to the AD7768. The DCLK divide mode allows the user to optimize the DCLK output to fit the application. Optimizing the DCLK per application depends on the requirements of the user. When the AD7768 are using the highest capacity output on the fewest DOUTx pins, for example, running in decimate by 32 using the DOUT0 and DOUT1 pins, the DCLK must equal the MCLK; thus, in this case, choosing the no division setting is the only way the user can output all the data within the conversion period. There are other cases, however, when the ADC may be running in fast mode with high decimation rates, or in median or low power mode where the DCLK does not need to run at the same speed as MCLK. In these cases, the DCLK divide allows the user to reduce the clock speed and makes routing and isolating such signals easier.	0x0	RW
		00	Divide by 8.		
		01	Divide by 4.		
		10	Divide by 2.		
		11	No division.		

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DIGITAL FILTER RAM BUILT IN SELF TEST (BIST) REGISTER

Address: 0x08, Reset: 0x0, Name: BIST Control

Table 46. Bit Descriptions for BIST Control

Bits	Bit Name	Settings	Description	Reset	Access
0	RAM_BIST_START		RAM BIST. Filter RAM BIST is a built in self test of the internal RAM. Normal ADC conversion is disrupted when this test is run. A synchronization pulse is required after this test is complete to resume normal ADC operation. The test can be run at intervals depending on user preference. The status and result of the RAM BIST is available in the device status register; see the RAM_BIST_PASS and RAM_BIST_RUNNING bits in Table 47.	0x0	RW
		0	Off.		
		1	Begin RAM BIST.		

STATUS REGISTER

Address: 0x09, Reset: 0x0, Name: Device Status

Table 47. Bit Descriptions for Device Status

Bits	Bit Name	Settings	Description	Reset	Access
3	CHIP_ERROR		Chip error. Chip error is a global error flag that is output within the status byte of each ADC conversion output. The following bits lead to the chip error bit being set to logic high: CRC check on internally hard coded settings after power-up does not pass; XOR check on the internal memory does not pass (this check runs continuously in the background); and clock error is detected on power-up.	0x0	R
		0	No error present.		
		1	Error has occurred.		
2	NO_CLOCK_ERROR		External clock check. This bit indicates whether the externally applied MCLK is detected correctly. If the MCLK is not applied correctly to the ADC at power-up, this bit is set and the DCLK frequency is approximately 16 MHz. If this bit is set, the chip error bit is set to logic high in the status bits of the data output headers, and the conversion results are output as all zeros regardless of the analog input voltages applied to the ADC channels.	0x0	R
		0	MCLK detected.		
		1	No MCLK detected.		
1	RAM_BIST_PASS		BIST pass/fail. RAM BIST result status. This bit indicates the result of the most recent RAM BIST. The result is latched to this register and is only cleared by a device reset.	0x0	R
		0	BIST failed or not run.		
		1	BIST passed.		
0	RAM_BIST_RUNNING		BIST status. Reading back the value of this bit allows the user to poll when the BIST test has finished.	0x0	R
		0	BIST not running.		
		1	BIST running.		

REVISION IDENTIFICATION REGISTER

Address: 0x0A, Reset: 0x06, Name: Revision ID

Table 48. Bit Descriptions for Revision ID

Bits	Bit Name	Description	Reset	Access
[7:0]	REVISION_ID	ASIC revision. 8-bit ID for revision details.	0x06	R

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GPIO CONTROL REGISTER

Address: 0x0E, Reset: 0x00, Name: GPIO Control

Table 49. Bit Descriptions for GPIO Control

Bits	Bit Name	Setting	Description	Reset	Access
7	UGPIO_ENABLE		User GPIO enable. The GPIOx pins are dual-purpose and can be operated only when the device is in SPI control mode. By default, when the AD7768 are powered up in SPI control mode, the GPIOx pins are disabled. This bit is a universal enable/disable for all GPIOx input/outputs. The direction of each general-purpose pin is determined by Bits[4:0] of this register.	0x0	RW
		0	GPIO Disabled.		
		1	GPIO Enabled.		
4	GPIOE4_FILTER		GPIO4 Direction. This bit assigns the direction of GPIO4 as either an input or an output. For SPI control, GPIO4 maps to Pin 11, which is the FILTER/GPIO4 pin.	0x0	RW
		0	Input.		
		1	Output.		
3	GPIOE3_MODE3		GPIO3 Direction. This bit assigns the direction of GPIO3 as either an input or an output. For SPI control, GPIO3 maps to Pin 15, which is the MODE3/GPIO3 pin.	0x0	RW
		0	Input.		
		1	Output.		
2	GPIOE2_MODE2		GPIO2 Direction. This bit assigns the direction of GPIO2 as either an input or an output. For SPI control, GPIO2 maps to Pin 14, which is the MODE2/GPIO2 pin.	0x0	RW
		0	Input.		
		1	Output.		
1	GPIOE1_MODE1		GPIO1 Direction. This bit assigns the direction of GPIO1 as either an input or an output. For SPI control, GPIO1 maps to Pin 13, which is the MODE1/GPIO1 pin.	0x0	RW
		0	Input.		
		1	Output.		
0	GPIO0_MODE0		GPIO0 Direction. This bit assigns the direction of GPIO0 as either an input or an output. For SPI control, GPIO0 maps to Pin 12, which is the MODE0/GPIO0 pin.	0x0	RW
		0	Input.		
		1	Output.		

GPIO WRITE DATA REGISTER

Address: 0x0F, Reset: 0x00, Name: GPIO Write Data

This register writes the values to be set on each of the general-purpose pins when selected as general-purpose outputs. Each bit, from Bits[4:0], maps directly to the GPIOx pins.

Table 50. Bit Descriptions for GPIO Write Data

Bits	Bit Name	Description	Reset	Access
4	GPIO4_WRITE	GPIO4/FILTER	0x0	RW
3	GPIO3_WRITE	GPIO3/MODE3	0x0	RW
2	GPIO2_WRITE	GPIO2/MODE2	0x0	RW
1	GPIO1_WRITE	GPIO1/MODE1	0x0	RW
0	GPIO0_WRITE	GPIO0/MODE0	0x0	RW

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GPIO READ DATA REGISTER

Address: 0x10, Reset: 0x00, Name: GPIO Read Data

This register reads back the value of the logic input level at the general-purpose pins when selected to operate as general-purpose inputs. Each bit, from Bits[4:0], maps directly to the GPIO0 to GPIO4 pins.

Table 51. Bit Descriptions for GPIO Read Data

Bits	Bit Name	Description	Reset	Access
4	GPIO4_READ	GPIO4/FILTER	0x0	R
3	GPIO3_READ	GPIO3/MODE3	0x0	R
2	GPIO2_READ	GPIO2/MODE2	0x0	R
1	GPIO1_READ	GPIO1/MODE1	0x0	R
0	GPIO0_READ	GPIO0/MODE0	0x00	R

ANALOG INPUT PRECHARGE BUFFER ENABLE REGISTER CHANNEL 0 TO CHANNEL 3

Address: 0x11, Reset: 0xFF, Name: Precharge Buffer 1

This register turns on or off the precharge buffers on the analog inputs. When writing to these registers, the user must write the inverse of the required bit settings. For example, to clear Bit 1 of this register, the user must write 0x01 to the register. This clears Bit 1 and sets all other bits. If the user reads the register again after writing 0x01, the data read is 0xFE, as required.

Table 52. Bit Descriptions for Precharge Buffer 1

Bits	Bit Name	Settings	Description	Reset
7	CH3_PREBUF_NEG_EN	0	Off	0x1
		1	On	
6	CH3_PREBUF_POS_EN	0	Off	0x1
		1	On	
5	CH2_PREBUF_NEG_EN	0	Off	0x1
		1	On	
4	CH2_PREBUF_POS_EN	0	Off	0x1
		1	On	
3	CH1_PREBUF_NEG_EN	0	Off	0x1
		1	On	
2	CH1_PREBUF_POS_EN	0	Off	0x1
		1	On	
1	CH0_PREBUF_NEG_EN	0	Off	0x1
		1	On	
0	CH0_PREBUF_POS_EN	0	Off	0x1
		1	On	

ANALOG INPUT PRECHARGE BUFFER ENABLE REGISTER CHANNEL 4 TO CHANNEL 7

Address: 0x12, Reset: 0xFF, Name: Precharge Buffer 2

This register turns on or off the precharge buffers on the analog inputs. When writing to these registers, the user must write the inverse of the required bit settings. For example, to clear Bit 1 of this register, the user must write 0x01 to the register. This clears Bit 1 and sets all other bits. If the user reads the register again after writing 0x01, the data read is 0xFE, as required.

Table 53. Bit Descriptions for Precharge Buffer 2

Bits	Bit Name	Settings	Description	Reset
7	CH7_PREBUF_NEG_EN	0	Off	0x1
		1	On	
6	CH7_PREBUF_POS_EN	0	Off	0x1
		1	On	
5	CH6_PREBUF_NEG_EN	0	Off	0x1
		1	On	

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Bits	Bit Name	Settings	Description	Reset
4	CH6_PREBUF_POS_EN	0	Off	0x1
		1	On	
3	CH5_PREBUF_NEG_EN	0	Off	0x1
		1	On	
2	CH5_PREBUF_POS_EN	0	Off	0x1
		1	On	
1	CH4_PREBUF_NEG_EN	0	Off	0x1
		1	On	
0	CH4_PREBUF_POS_EN	0	Off	0x1
		1	On	

POSITIVE REFERENCE PRECHARGE BUFFER ENABLE REGISTER

Address: 0x13, Reset: 0x00, Name: Positive Reference Precharge Buffer

This register turns on or off the precharge buffers on the reference positive input to each of the ADCs from Channel 0 to Channel 7.

Table 54. Bit Descriptions for Positive Reference Precharge Buffer

Bits	Bit Name	Settings	Description	Reset
7	CH7_REFP_BUF	0	Off	0x0
		1	On	
6	CH6_REFP_BUF	0	Off	0x0
		1	On	
5	CH5_REFP_BUF	0	Off	0x0
		1	On	
4	CH4_REFP_BUF	0	Off	0x0
		1	On	
3	CH3_REFP_BUF	0	Off	0x0
		1	On	
2	CH2_REFP_BUF	0	Off	0x0
		1	On	
1	CH1_REFP_BUF	0	Off	0x0
		1	On	
0	CH0_REFP_BUF	0	Off	0x0
		1	On	

NEGATIVE REFERENCE PRECHARGE BUFFER ENABLE REGISTER

Address: 0x14, Reset: 0x00, Name: Negative Reference Precharge Buffer

This register turns on or off the precharge buffers on the reference negative input to each of the ADCs from Channel 0 to Channel 7.

Table 55. Bit Descriptions for Negative Reference Precharge Buffer

Bits	Bit Name	Settings	Description	Reset
7	CH7_REFN_BUF	0	Off	0x0
		1	On	
6	CH6_REFN_BUF	0	Off	0x0
		1	On	
5	CH5_REFN_BUF	0	Off	0x0
		1	On	
4	CH4_REFN_BUF	0	Off	0x0
		1	On	
3	CH3_REFN_BUF	0	Off	0x0
		1	On	
2	CH2_REFN_BUF	0	Off	0x0
		1	On	

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Bits	Bit Name	Settings	Description	Reset
1	CH1_REFN_BUF	0	Off	0x0
		1	On	
0	CH0_REFN_BUF	0	Off	0x0
		1	On	

OFFSET REGISTERS

The CHx_OFFSET_MSB, CHx_OFFSET_MID, and CHx_OFFSET_LSB registers are 24-bit, signed twos complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. As offset adjustment occurs before gain adjustment, the ratio of 4/3 changes linearly with gain adjustment via the CHx_GAIN_x registers. After a reset or power cycle, the register values revert to the default factory setting.

Table 56. Per Channel 24-Bit Offset Registers, Three 8-Bit Registers for Each Channel, Split Up as MSB, MID, and LSB

Address					Reset			
MSB	Mid	LSB	Name	Description	MSB	Mid	LSB	Access
0x1E	0x1F	0x20	Channel 0 offset	Channel 0 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x21	0x22	0x23	Channel 1 offset	Channel 1 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x24	0x25	0x26	Channel 2 offset	Channel 2 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x27	0x28	0x29	Channel 3 offset	Channel 3 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x2A	0x2B	0x2C	Channel 4 offset	Channel 4 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x2D	0x2E	0x2F	Channel 5 offset	Channel 5 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x30	0x31	0x32	Channel 6 offset	Channel 6 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x33	0x34	0x35	Channel 7 offset	Channel 7 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW

GAIN REGISTERS

Each ADC channel has an associated gain coefficient. The coefficient is stored in three single-byte registers split up as MSB, MID, and LSB. Each of the gain registers are factory programmed. Nominally, this gain is around the value 0x555555 (for an ADC channel). The user may overwrite the gain register setting however, after a reset or power cycle, the gain register values revert to the hard coded programmed factory setting.

Table 57. Per Channel 24-Bit Gain Registers, 3 8-Bit Registers for Each Channel, Split Up as MSB, MID, and LSB

Address					Reset			
MSB	Mid	LSB	Name	Description	MSB	Mid	LSB	Access
0x36	0x37	0x38	Channel 0 gain	Channel 0 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x39	0x3A	0x3B	Channel 1 gain	Channel 1 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x3C	0x3D	0x3E	Channel 2 gain	Channel 2 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x3F	0x40	0x41	Channel 3 gain	Channel 3 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x42	0x43	0x44	Channel 4 gain	Channel 4 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x45	0x46	0x47	Channel 5 gain	Channel 5 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x48	0x49	0x4A	Channel 6 gain	Channel 6 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x4B	0x4C	0x4D	Channel 7 gain	Channel 7 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW

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SYNC PHASE OFFSET REGISTERS

The AD7768 have one synchronization signal for all channels. The sync phase offset register allows the user to vary the phase delay on each of the channels relative to the synchronization edge received on the SYNC_IN pin. See the Sync Phase Offset Adjustment section for details on the use of this function.

Table 58. Per Channel 8-Bit Sync Phase Offset Registers

Address	Name	Description	Reset	Access
0x4E	Channel 0 sync offset	Channel 0 sync phase offset register	0x00	RW
0x4F	Channel 1 sync offset	Channel 1 sync phase offset register	0x00	RW
0x50	Channel 2 sync offset	Channel 2 sync phase offset register	0x00	RW
0x51	Channel 3 sync offset	Channel 3 sync phase offset register	0x00	RW
0x52	Channel 4 sync offset	Channel 4 sync phase offset register	0x00	RW
0x53	Channel 5 sync offset	Channel 5 sync phase offset register	0x00	RW
0x54	Channel 6 sync offset	Channel 6 sync phase offset register	0x00	RW
0x55	Channel 7 sync offset	Channel 7 sync phase offset register	0x00	RW

ADC DIAGNOSTIC RECEIVE SELECT REGISTER

Address: 0x56, Reset: 0x00, Name: Diagnostic Rx

The AD7768 ADC diagnostic allows the user to select a zero-scale, positive full-scale, or negative full-scale input to the ADC, which can be converted to verify the correct operation of the ADC channel. This register enables the diagnostic. Enable the receive (Rx) for each channel and set each bit in this register to 1. The diagnostic requires the analog input pins to be disconnected from external drive/sources to accurately measure the internal nodes.

The ADC diagnostic feature depends on some features of the analog input precharge buffers. The user must ensure that the analog input precharge buffers are enabled on the channels that are selected to receive the diagnostic voltages internally.

Table 59. Bit Descriptions for Diagnostic Rx

Bits	Bit Name	Settings	Description	Reset	Access
7	CH7_RX		Channel 7	0x0	RW
		0	Not in use		
		1	Receive		
6	CH6_RX		Channel 6	0x0	RW
		0	Not in use		
		1	Receive		
5	CH5_RX		Channel 5	0x0	RW
		0	Not in use		
		1	Receive		
4	CH4_RX		Channel 4	0x0	RW
		0	Not in use		
		1	Receive		
3	CH3_RX		Channel 3	0x0	RW
		0	Not in use		
		1	Receive		
2	CH2_RX		Channel 2	0x0	RW
		0	Not in use		
		1	Receive		
1	CH1_RX		Channel 1	0x0	RW
		0	Not in use		
		1	Receive		
0	CH0_RX		Channel 0	0x0	RW
		0	Not in use		
		1	Receive		

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ADC DIAGNOSTIC CONTROL REGISTER

Address: 0x57, Reset: 0x00, Name: Diagnostic Mux Control

The AD7768 ADC diagnostic allows the user to select a zero-scale, positive full-scale, or negative full-scale input to the ADC, which can be converted to verify the correct operation of the ADC channel. This register controls the voltage that is applied to each of the ADC channels for the diagnostic. There are three input voltage options that the user can select. The voltage selected is mapped to the channels based on which mode (Mode A or Mode B) they belong to, which is set according to the channel mode select register (Register 0x03).

Set Bits[7:0] to 1 in the ADC diagnostic receive select register, then select the voltage check desired for the channels on Mode A and the channels on Mode B through Bits[2:0] and Bits[6:4], respectively.

Table 60. Bit Descriptions for Diagnostic Mux Control

Bits	Bit Name	Settings	Description	Reset	Access
[6:4]	GRPB_SEL		Mux B.	0x0	RW
		000	Off.		
		011	Positive full-scale ADC check. A voltage close to positive full scale is applied internally to the ADC channel.		
		100	Negative full-scale ADC check. A voltage close to negative (or minus) full scale is applied internally to the ADC channel.		
		101	Zero-scale ADC check. A voltage close to 0 V is applied internally to the ADC channel.		
[2:0]	GRPA_SEL		Mux A.	0x0	RW
		000	Off.		
		011	Positive full-scale ADC check. A voltage close to positive full scale is applied internally to the ADC channel.		
		100	Negative full-scale ADC check. A voltage close to negative (or minus) full scale is applied internally to the ADC channel.		
		101	Zero-scale ADC check. A voltage close to 0 V is applied internally to the ADC channel.		

MODULATOR DELAY CONTROL REGISTER

Address: 0x58, Reset: 0x02, Name: Modulator Delay Control

Table 61. Bit Descriptions for Modulator Delay Control

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	CLK_MOD_DEL_EN		Enable delayed modulator clock.	0x0	RW
		00	Disabled delayed clock for all channels.		
		01	Enable delayed clock for Channel 0 to Channel 3 only on the AD7768.		
		10	Enable delayed clock for Channel 4 to Channel 7 only on AD7768.		
		11	Enable delayed clock for all channels.		
[1:0]	Reserved	10	Not a user option. Must be set to 0x2.	0x2	RW

CHOPPING CONTROL REGISTER

Address: 0x59, Reset: 0x0A, Name: Chop Control

Table 62. Bit Descriptions for Chop Control

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	GRPA_CHOP		Group A chopping	0x2	RW
		01	Chop at $f_{MOD}/8$		
		10	Chop at $f_{MOD}/32$		
[1:0]	GRPB_CHOP		Group B chopping	0x2	RW
		01	Chop at $f_{MOD}/8$		
		10	Chop at $f_{MOD}/32$		

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AD7768-4 REGISTER MAP DETAILS (SPI CONTROL)

AD7768-4 REGISTER MAP

Table 63. Detailed AD7768-4 Register Map

Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	Channel standby	Unused				CH_3	CH_2	CH_1	CH_0	0x00	RW
0x01	Channel Mode A	Unused				FILTER_TYPE_A	DEC_RATE_A			0x0D	RW
0x02	Channel Mode B	Unused				FILTER_TYPE_B	DEC_RATE_B			0x0D	RW
0x03	Channel mode select	Reserved		CH_3_MODE	CH_2_MODE	Reserved		CH_1_MODE	CH_0_MODE	0x00	RW
0x04	POWER_MODE	SLEEP_MODE	Unused	POWER_MODE		LVDS_ENABLE	Unused	MCLK_DIV		0x00	RW
0x05	General configuration	Unused	Reserved	RETIME_EN	VCM_PD	Reserved	Unused	VCM_VSEL		0x08	RW
0x06	Data control	SPI_SYNC	Unused		SINGLE_SHOT_EN	Unused		SPI_RESET		0x80	RW
0x07	Interface configuration	Unused				CRC_SELECT		DCLK_DIV		0x0	RW
0x08	BIST control	Unused							RAM_BIST_START	0x0	RW
0x09	Device status	Unused				CHIP_ERROR	NO_CLOCK_ERROR	RAM_BIST_PASS	RAM_BIST_RUNNING	0x0	R
0x0A	Revision ID	REVISION_ID								0x06	R
0x0B	Reserved	Reserved								0x00	R
0x0C	Reserved	Reserved								0x00	R
0x0D	Reserved	Reserved								0x00	R
0x0E	GPIO control	UGPIO_ENABLE	Unused		GPIOE4_FILTER	GPIOE3_MODE3	GPIOE2_MODE2	GPIOE1_MODE1	GPIO0_MODE0	0x00	RW
0x0F	GPIO write data	Unused			GPIO4_WRITE	GPIO3_WRITE	GPIO2_WRITE	GPIO1_WRITE	GPIO0_WRITE	0x00	RW
0x10	GPIO read data	Unused			GPIO4_READ	GPIO3_READ	GPIO2_READ	GPIO1_READ	GPIO0_READ	0x00	R
0x11	Precharge Buffer 1	Reserved				CH1_PREBUF_NEG_EN	CH1_PREBUF_POS_EN	CH0_PREBUF_NEG_EN	CH0_PREBUF_POS_EN	0xFF	RW
0x12	Precharge Buffer 2	Reserved				CH3_PREBUF_NEG_EN	CH3_PREBUF_POS_EN	CH2_PREBUF_NEG_EN	CH2_PREBUF_POS_EN	0xFF	RW
0x13	Positive reference precharge buffer	Reserved		CH3_REFP_BUF	CH2_REFP_BUF	Reserved		CH1_REFP_BUF	CH0_REFP_BUF	0x00	RW
0x14	Negative reference precharge buffer	Reserved		CH3_REFN_BUF	CH2_REFN_BUF	Reserved		CH1_REFN_BUF	CH0_REFN_BUF	0x00	RW
0x1E	Channel 0 offset	CH0_OFFSET_MSB								0x00	RW
0x1F		CH0_OFFSET_MID									
0x20		CH0_OFFSET_LSB									
0x21	Channel 1 offset	CH1_OFFSET_MSB								0x00	RW
0x22		CH1_OFFSET_MID									
0x23		CH1_OFFSET_LSB									
0x24	Reserved	Reserved								0x00	RW
0x25		Reserved									
0x26		Reserved									
0x27	Reserved	Reserved								0x00	RW
0x28		Reserved									
0x29		Reserved									
0x2A	Channel 2 offset	CH2_OFFSET_MSB								0x00	RW
0x2B		CH2_OFFSET_MID									
0x2C		CH2_OFFSET_LSB									
0x2D	Channel 3 offset	CH3_OFFSET_MSB								0x00	RW
0x2E		CH3_OFFSET_MID									
0x2F		CH3_OFFSET_LSB									
0x30	Reserved	Reserved								0x00	RW
0x31		Reserved									
0x32		Reserved									
0x33	Reserved	Reserved								0x00	RW
0x34		Reserved									
0x35		Reserved									
0x36	Channel 0 gain	CH0_GAIN_MSB								0xXX	RW
0x37		CH0_GAIN_MID									
0x38		CH0_GAIN_LSB									

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Reg.	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x39	Channel 1 gain	CH1_GAIN_MSB								0xXX	RW
0x3A		CH1_GAIN_MID									
0x3B		CH1_GAIN_LSB									
0x3C	Reserved	Reserved								0xXX	RW
0x3D		Reserved									
0x3E		Reserved									
0x3F	Reserved	Reserved								0xXX	RW
0x40		Reserved									
0x41		Reserved									
0x42	Channel 2 gain	CH2_GAIN_MSB								0xXX	RW
0x43		CH2_GAIN_MID									
0x44		CH2_GAIN_LSB									
0x45	Channel 3 gain	CH3_GAIN_MSB								0xXX	RW
0x46		CH3_GAIN_MID									
0x47		CH3_GAIN_LSB									
0x48	Reserved	Reserved								0xXX	RW
0x49		Reserved									
0x4A		Reserved									
0x4B	Reserved	Reserved								0xXX	RW
0x4C		Reserved									
0x4D		Reserved									
0x4E	Channel 0 sync offset	CH0_SYNC_OFFSET								0x00	RW
0x4F	Channel 1 sync offset	CH1_SYNC_OFFSET								0x00	RW
0x50	Reserved	Reserved								0x00	RW
0x51	Reserved	Reserved								0x00	RW
0x52	Channel 2 sync offset	CH2_SYNC_OFFSET								0x00	RW
0x53	Channel 3 sync offset	CH3_SYNC_OFFSET								0x00	RW
0x54	Reserved	Reserved								0x00	RW
0x55	Reserved	Reserved								0x00	RW
0x56	Diagnostic Rx	Reserved			CH3_RX	CH2_RX	Reserved		CH1_RX	CH0_RX	0x00	RW
0x57	Diagnostic mux control	Unused	GRPB_SEL			Unused	GRPA_SEL			0x00	RW
0x58	Modulator delay control	Unused				CLK_MOD_DEL_EN		Reserved		0x02	RW
0x59	Chop control	Unused				GRPA_CHOP		GRPB_CHOP		0x0A	RW

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CHANNEL STANDBY REGISTER

Address: 0x00, Reset: 0x00, Name: Channel Standby

Each of the ADC channels can be put into standby mode independently by setting the appropriate bit in the channel standby register. When a channel is in standby mode, its position in the data output stream is held. The 8-bit header is all zeros, as is the conversion result output of 24 zeros.

The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768-4.

The crystal excitation circuitry is associated with the Channel 2 circuitry. If Channel 2 is put into standby mode, the crystal circuitry is also disabled for maximum power savings. Channel 2 must be enabled while the external crystal is used on the AD7768-4.

Table 64. Bit Descriptions for Channel Standby

Bits	Bit Name	Settings	Description	Reset	Access
3	CH_3		Channel 3	0x0	RW
		0	Enabled		
		1	Standby		
2	CH_2		Channel 2	0x0	RW
		0	Enabled		
		1	Standby		
1	CH_1		Channel 1	0x0	RW
		0	Enabled		
		1	Standby		
0	CH_0		Channel 0	0x0	RW
		0	Enabled		
		1	Standby		

CHANNEL MODE A REGISTER

Address: 0x01, Reset: 0x0D, Name: Channel Mode A

Two mode options are available on the AD7768-4 ADCs. The channel modes are defined by the contents of the Channel Mode A and Channel Mode B registers. Each mode is then mapped as desired to the required ADC channel. Mode A and Mode B allow different filter types and decimation rates to be selected and mapped to any of the ADC channels.

When different decimation rates are selected, the AD7768-4 output a data ready signal at the fastest selected decimation rate. Any channel that runs at a lower output data rate is updated only at that slower rate. In between valid result data, the data for that channel is set to zero and the repeated data bit is set in the header status bits to distinguish it from a real conversion result (see the ADC Conversion Output: Header and Data section).

Table 65. Bit Descriptions for Channel Mode A

Bits	Bit Name	Settings	Description	Reset	Access
3	FILTER_TYPE_A		Filter selection	0x1	RW
		0	Wideband filter		
		1	Sinc5 filter		
[2:0]	DEC_RATE_A		Decimation rate selection	0x5	RW
		000	×32		
		001	×64		
		010	×128		
		011	×256		
		100	×512		
		101	×1024		
		110	×1024		
		111	×1024		

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CHANNEL MODE B REGISTER

Address: 0x02, Reset: 0x0D, Name: Channel Mode B

Table 66. Bit Descriptions for Channel Mode B

Bits	Bit Name	Settings	Description	Reset	Access
3	FILTER_TYPE_B		Filter selection	0x1	RW
		0	Wideband filter		
		1	Sinc5 filter		
[2:0]	DEC_RATE_B		Decimation rate selection	0x5	RW
		000	×32		
		001	×64		
		010	×128		
		011	×256		
		100	×512		
		101	×1024		
		110	×1024		
		111	×1024		

CHANNEL MODE SELECT REGISTER

Address: 0x03, Reset: 0x00, Name: Channel Mode Select

This register selects the mapping of each ADC channel to either Channel Mode A or Channel Mode B.

Table 67. Bit Descriptions for Channel Mode Select

Bits	Bit Name	Settings	Description	Reset	Access
5	CH_3_MODE		Channel 3	0x0	RW
		0	Mode A		
		1	Mode B		
4	CH_2_MODE		Channel 2	0x0	RW
		0	Mode A		
		1	Mode B		
1	CH_1_MODE		Channel 1	0x0	RW
		0	Mode A		
		1	Mode B		
0	CH_0_MODE		Channel 0	0x0	RW
		0	Mode A		
		1	Mode B		

POWER MODE SELECT REGISTER

Address: 0x04, Reset: 0x00, Name: POWER_MODE

Table 68. Bit Descriptions for POWER_MODE

Bits	Bit Name	Settings	Description	Reset	Access
7	SLEEP_MODE		In sleep mode, many of the digital clocks are disabled and all of the ADCs are disabled. The analog LDOs are not disabled. The AD7768-4 SPI is live and is available to the user. Writing to this bit brings the AD7768-4 out of sleep mode again.	0x0	RW
		0	Normal operation.		
		1	Sleep mode.		

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Bits	Bit Name	Settings	Description	Reset	Access
[5:4]	POWER_MODE		Power mode. The power mode bits control the power mode setting for the bias currents used on all ADCs on the AD7768-4. The user can select the current consumption target to meet the application. The power modes of fast, median, and low power give optimum performance when mapped to the correct MCLK division setting. These power mode bits do not control the MCLK division of the ADCs. See the MCLK_DIV bits for control of the division of the MCLK input.	0x0	RW
		00	Low power.		
		10	Median.		
		11	Fast.		
3	LVDS_ENABLE		LVDS clock.	0x0	RW
		0	LVDS input clock disabled.		
		1	LVDS input clock enabled.		
[1:0]	MCLK_DIV		MCLK division. The MCLK division bits control the divided ratio between the MCLK applied at the input to the AD7768-4 and the clock used by each of the ADC modulators. The appropriate division ratio depends on the following factors: power mode, decimation rate, and the base MCLK available in the system. See the Clocking, Sampling Tree, and Power Scaling section for more information on setting MCLK_DIV correctly.	0x0	RW
		00	MCLK/32: with a base MCLK of 32.768 MHz, set to MCLK/32 for low power mode.		
		10	MCLK/8: with a base MCLK of 32.768 MHz, set to MCLK/8 for median mode.		
		11	MCLK/4: with a base MCLK of 32.768 MHz, set to MCLK/4 for fast mode.		

GENERAL DEVICE CONFIGURATION REGISTER

Address: 0x05, Reset: 0x08, Name: General Configuration

Table 69. Bit Descriptions for General Configuration

Bits	Bit Name	Settings	Description	Reset	Access
5	RETIME_EN		$\overline{\text{SYNC_OUT}}$signal retime enable bit.	0x0	RW
		0	Disabled: normal timing of $\overline{\text{SYNC_OUT}}$.		
		1	Enabled: $\overline{\text{SYNC_OUT}}$ signal derived from alternate MCLK edge.		
4	VCM_PD		VCM buffer power-down.	0x0	RW
		0	Enabled: VCM buffer normal mode.		
		1	Powered down: VCM buffer powered down.		
3	Reserved	1	Not a user option. This bit must be set to 1.	0x1	RW
[1:0]	VCM_VSEL		VCM voltage. These bits select the output voltage of the VCM pin. This voltage is derived from the AVDD1 supply and can be output as half of that AVDD1 voltage, or other fixed voltages, with respect to AVSS. The VCM voltage output is associated with the Channel 0 circuitry. If Channel 0 is put into standby mode, the VCM voltage output is also disabled for maximum power savings. Channel 0 must be enabled while VCM is being used externally to the AD7768-4.	0x0	RW
		00	(AVDD1 − AVSS)/2 V.		
		01	1.65 V.		
		10	2.5 V.		
		11	2.14 V.		

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DATA CONTROL: SOFT RESET, SYNC, AND SINGLE-SHOT CONTROL REGISTER

Address: 0x06, Reset: 0x80, Name: Data Control

Table 70. Bit Descriptions for Data Control

Bits	Bit Name	Settings	Description	Reset	Access
7	SPI_SYNC		Software synchronization of the AD7768-4. This command has the same effect as sending a signal pulse to the $\overline{START}$ pin. To operate the SPI_SYNC, the user must write to this bit two separate times. First, write a zero, putting SPI_SYNC low, and then write a 1 to set SPI_SYNC logic high again. The SPI_SYNC command is recognized after the last rising edge of SCLK in the SPI instruction where the SPI_SYNC bit is changed from low to high. The SPI_SYNC command is then output synchronous to the AD7768-4 MCLK on the $\overline{SYNC_OUT}$ pin. The user must connect the $\overline{SYNC_OUT}$ signal to the $\overline{SYNC_IN}$ pin on the PCB. The $\overline{SYNC_OUT}$ pin can also be routed to the $\overline{SYNC_IN}$ pins of other AD7768-4 devices, allowing larger channel count simultaneous sampling systems. As per any synchronization pulse seen by the $\overline{SYNC_IN}$ pin, the digital filters of the AD7768-4 are reset. The full settling time of the filters must elapse before data is output on the data interface. In a daisy-chained system of AD7768-4 devices, two successive synchronization pulses must be applied to guarantee that all ADCs are synchronized. Two synchronization pulses are also required in a system of more than one AD7768-4 device sharing a single MCLK signal, where the $\overline{DRDY}$ pin of only one device is used to detect new data.	0x1	RW
		0	Change to SPI_SYNC low.		
		1	Change to SPI_SYNC high.		
4	SINGLE_SHOT_EN		One-shot mode. Enables one-shot mode. In one-shot mode, the AD7768-4 output a conversion result in response to a $\overline{SYNC_IN}$ rising edge.	0x0	RW
		0	Disabled.		
		1	Enabled.		
[1:0]	SPI_RESET		Soft reset. These bits allow a full device reset over the SPI port. Two successive commands must be received in the correct order to generate a reset: first, write 0x03 to the soft reset register, and then write 0x02 to the soft reset register. This sequence causes the digital core to reset and all registers return to their default values. Following a soft reset, if the SPI master sends a command to the AD7768-4, the devices respond on the next frame to that command with an output of 0x0E00.	0x0	RW
		00	No effect.		
		01	No effect.		
		10	Second reset command.		
		11	First reset command.		

INTERFACE CONFIGURATION REGISTER

Address: 0x07, Reset: 0x0, Name: Interface Configuration

Table 71. Bit Descriptions for Interface Configuration

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	CRC_SELECT		CRC select. These bits allow the user to implement a CRC on the data interface. When selected, the CRC replaces the header every fourth or 16th output sample depending on the CRC option chosen. There are two options for the CRC; both use the same polynomial: $x^8 + x^2 + x + 1$. The options offer the user the ability to reduce the duty cycle of the CRC calculation by performing it less often: in the case of having it every 16th sample or more often in the case of every fourth conversion. The CRC is calculated on a per channel basis and it includes conversion data only.	0x0	RW
		00	No CRC. Status bits with every conversion.		
		01	Replace the header with CRC message every 4 samples.		
		10	Replace the header with CRC message every 16 samples.		
		11	Replace the header with CRC message every 16 samples.		

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Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	DCLK_DIV		DCLK divider. These bits control division of the DCLK clock used to clock out conversion data on the DOUTx pins. The DCLK signal is derived from the MCLK applied to the AD7768-4. The DCLK divide mode allows the user to optimize the DCLK output to fit the application. Optimizing the DCLK per application depends on the requirements of the user. When the AD7768-4 are using the highest capacity output on the fewest DOUTx pins, for example, running in decimate by 32 using the DOUT0 and DOUT1 pins, the DCLK must equal the MCLK; thus, in this case, choosing the no division setting is the only way the user can output all the data within the conversion period. There are other cases, however, when the ADC may be running in fast mode with high decimation rates, or in median or low power mode where the DCLK does not need to run at the same speed as MCLK. In these cases, the DCLK divide allows the user to reduce the clock speed and makes routing and isolating such signals easier.	0x0	RW
		00	Divide by 8.		
		01	Divide by 4.		
		10	Divide by 2.		
		11	No division.		

DIGITAL FILTER RAM BUILT IN SELF TEST (BIST) REGISTER

Address: 0x08, Reset: 0x0, Name: BIST Control

Table 72. Bit Descriptions for BIST Control

Bits	Bit Name	Settings	Description	Reset	Access
0	RAM_BIST_START		RAM BIST. Filter RAM BIST is a built in self test of the RAM storage of the coefficients used by the digital filter. Normal ADC conversion is disrupted when this test is run. A synchronization pulse is required after this test is complete to resume normal ADC operation. The test can be run at intervals depending on user preference. The status and result of the RAM BIST is available in the device status register; see the RAM_BIST_PASS and RAM_BIST_RUNNING bits in Table 73.	0x0	RW
		0	Off.		
		1	Begin RAM BIST.		

STATUS REGISTER

Address: 0x09, Reset: 0x0, Name: Device Status

Table 73. Bit Descriptions for Device Status

Bits	Bit Name	Settings	Description	Reset	Access
3	CHIP_ERROR		Chip error. Chip error is a global error flag that is output within the status byte of each ADC conversion output. The following bits lead to the chip error bit being set to logic high: CRC check on internally hard coded settings after power-up does not pass; XOR check on the memory map does not pass (this check runs continuously in the background); and clock error is detected on power-up.	0x0	R
		0	No error present.		
		1	Error has occurred.		
2	NO_CLOCK_ERROR		External clock check. This bit indicates whether the externally applied MCLK is detected correctly. If the MCLK is not applied correctly to the ADC at power-up, this bit is set and the DCLK frequency is approximately 16 MHz. If this bit is set, the chip error bit is set to logic high in the status bits of the data output headers, and the conversion results are output as all zeros regardless of the analog input voltages applied to the ADC channels.	0x0	R
		0	MCLK detected.		
		1	No MCLK detected.		

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Bits	Bit Name	Settings	Description	Reset	Access
1	RAM_BIST_PASS		BIST pass/fail. RAM BIST result status. This bit indicates the result of the most recent RAM BIST. The result is latched to this register and is only cleared by a device reset.	0x0	R
		0	BIST failed or not run.		
		1	BIST passed.		
0	RAM_BIST_RUNNING		BIST status. Reading back the value of this bit allows the user to poll when the BIST test has finished.	0x0	R
		0	BIST not running.		
		1	BIST running.		

REVISION IDENTIFICATION REGISTER

Address: 0x0A, Reset: 0x06, Name: Revision ID

Table 74. Bit Descriptions for Revision ID

Bits	Bit Name	Description	Reset	Access
[7:0]	REVISION_ID	ASIC revision. 8-bit ID for revision details.	0x06	R

GPIO CONTROL REGISTER

Address: 0x0E, Reset: 0x00, Name: GPIO Control

Table 75. Bit Descriptions for GPIO Control

Bits	Bit Name	Setting	Description	Reset	Access
7	UGPIO_ENABLE		User GPIO enable. The GPIOx pins are dual-purpose and can be operated only when the device is in SPI control mode. By default, when the AD7768-4 are powered up in SPI control mode, the GPIOx pins are disabled. This bit is a universal enable/ disable for all GPIOx input/outputs. The direction of each general-purpose pin is determined by Bits[4:0] of this register.	0x0	RW
		0	GPIO Disabled.		
		1	GPIO Enabled.		
4	GPIOE4_FILTER		GPIO4 Direction. This bit assigns the direction of GPIO4 as either an input or an output. For SPI control, GPIO4 maps to Pin 11, which is the FILTER/GPIO4 pin.	0x0	RW
		0	Input.		
		1	Output.		
3	GPIOE3_MODE3		GPIO3 Direction. This bit assigns the direction of GPIO3 as either an input or an output. For SPI control, GPIO3 maps to Pin 15, which is the MODE3/GPIO3 pin.	0x0	RW
		0	Input.		
		1	Output.		
2	GPIOE2_MODE2		GPIO2 Direction. This bit assigns the direction of GPIO2 as either an input or an output. For SPI control, GPIO2 maps to Pin 14, which is the MODE2/GPIO2 pin.	0x0	RW
		0	Input.		
		1	Output.		
1	GPIOE1_MODE1		GPIO1 Direction. This bit assigns the direction of GPIO1 as either an input or an output. For SPI control, GPIO1 maps to Pin 13, which is the MODE1/GPIO1 pin.	0x0	RW
		0	Input.		
		1	Output.		
0	GPIO0_MODE0		GPIO0 Direction. This bit assigns the direction of GPIO0 as either an input or an output. For SPI control, GPIO0 maps to Pin 12, which is the MODE0/GPIO0 pin.	0x0	RW
		0	Input.		
		1	Output.		

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GPIO WRITE DATA REGISTER

Address: 0x0F, Reset: 0x00, Name: GPIO Write Data

This register writes the values to be set on each of the general-purpose pins when selected as general-purpose outputs. Each bit, from Bits[4:0], maps directly to the GPIOx pins.

Table 76. Bit Descriptions for GPIO Write Data

Bits	Bit Name	Description	Reset	Access
4	GPIO4_WRITE	GPIO4/FILTER	0x0	RW
3	GPIO3_WRITE	GPIO3/MODE3	0x0	RW
2	GPIO2_WRITE	GPIO2/MODE2	0x0	RW
1	GPIO1_WRITE	GPIO1/MODE1	0x0	RW
0	GPIO0_WRITE	GPIO0/MODE0	0x0	RW

GPIO READ DATA REGISTER

Address: 0x10, Reset: 0x00, Name: GPIO Read Data

This register reads back the value of the logic input level at the general-purpose pins when selected to operate as general-purpose inputs. Each bit, from Bits[4:0], maps directly to the GPIO0 to GPIO4 pins.

Table 77. Bit Descriptions for GPIO Read Data

Bits	Bit Name	Description	Reset	Access
4	GPIO4_READ	GPIO4/FILTER	0x0	R
3	GPIO3_READ	GPIO3/MODE3	0x0	R
2	GPIO2_READ	GPIO2/MODE2	0x0	R
1	GPIO1_READ	GPIO1/MODE1	0x0	R
0	GPIO0_READ	GPIO0/MODE0	0x00	R

ANALOG INPUT PRECHARGE BUFFER ENABLE REGISTER CHANNEL 0 AND CHANNEL 1

Address: 0x11, Reset: 0xFF, Name: Precharge Buffer 1

This register turns on or off the precharge buffers on the analog inputs. When writing to these registers, the user must write the inverse of the required bit settings. For example, to clear Bit 1 of this register, the user must write 0x01 to the register. This clears Bit 1 and sets all other bits. If the user reads the register again after writing 0x01, the data read is 0xFE, as required.

Table 78. Bit Descriptions for Precharge Buffer 1

Bits	Bit Name	Settings	Description	Reset
3	CH1_PREBUF_NEG_EN	0	Off	0x1
		1	On	
2	CH1_PREBUF_POS_EN	0	Off	0x1
		1	On	
1	CH0_PREBUF_NEG_EN	0	Off	0x1
		1	On	
0	CH0_PREBUF_POS_EN	0	Off	0x1
		1	On	

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ANALOG INPUT PRECHARGE BUFFER ENABLE REGISTER CHANNEL 2 AND CHANNEL 3

Address: 0x12, Reset: 0xFF, Name: Precharge Buffer 2

This register turns on or off the precharge buffers on the analog inputs. When writing to these registers, the user must write the inverse of the required bit settings. For example, to clear Bit 1 of this register, the user must write 0x01 to the register. This clears Bit 1 and sets all other bits. If the user reads the register again after writing 0x01, the data read is 0xFE, as required.

Table 79. Bit Descriptions for Precharge Buffer 2

Bits	Bit Name	Settings	Description	Reset
3	CH3_PREBUF_NEG_EN	0	Off	0x1
		1	On	
2	CH3_PREBUF_POS_EN	0	Off	0x1
		1	On	
1	CH2_PREBUF_NEG_EN	0	Off	0x1
		1	On	
0	CH2_PREBUF_POS_EN	0	Off	0x1
		1	On	

POSITIVE REFERENCE PRECHARGE BUFFER ENABLE REGISTER

Address: 0x13, Reset: 0x00, Name: Positive Reference Precharge Buffer

This register turns on or off the precharge buffers on the reference positive input to each of the ADCs from Channel 0 to Channel 3.

Table 80. Bit Descriptions for Positive Reference Precharge Buffer

Bits	Bit Name	Settings	Description	Reset
5	CH3_REFP_BUF	0	Off	0x0
		1	On	
4	CH2_REFP_BUF	0	Off	0x0
		1	On	
1	CH1_REFP_BUF	0	Off	0x0
		1	On	
0	CH0_REFP_BUF	0	Off	0x0
		1	On	

NEGATIVE REFERENCE PRECHARGE BUFFER ENABLE REGISTER

Address: 0x14, Reset: 0x00, Name: Negative Reference Precharge Buffer

This register turns on or off the precharge buffers on the reference negative input to each of the ADCs from Channel 0 to Channel 3.

Table 81. Bit Descriptions for Negative Reference Precharge Buffer

Bits	Bit Name	Settings	Description	Reset
5	CH3_REFN_BUF	0	Off	0x0
		1	On	
4	CH2_REFN_BUF	0	Off	0x0
		1	On	
1	CH1_REFN_BUF	0	Off	0x0
		1	On	
0	CH0_REFN_BUF	0	Off	0x0
		1	On	

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OFFSET REGISTERS

The CHx_OFFSET_MSB, CHx_OFFSET_MID, and CHx_OFFSET_LSB registers are 24-bit, signed twos complement registers for channel offset adjustment. If the channel gain setting is at its ideal nominal value of 0x555555, an LSB of offset register adjustment changes the digital output by −4/3 LSBs. For example, changing the offset register from 0 to 100 changes the digital output by −133 LSBs. As offset adjustment occurs before gain adjustment, the ratio of 4/3 changes linearly with gain adjustment via the CHx_GAIN_x registers. After a reset or power cycle, the register values revert to the default factory setting.

Table 82. Per Channel 24-Bit Offset Registers, Three 8-Bit Registers for Each Channel, Split Up as MSB, MID, and LSB

Address					Reset			
MSB	Mid	LSB	Name	Description	MSB	Mid	LSB	Access
0x1E	0x1F	0x20	Channel 0 offset	Channel 0 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x21	0x22	0x23	Channel 1 offset	Channel 1 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x2A	0x2B	0x2C	Channel 2 offset	Channel 2 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW
0x2D	0x2E	0x2F	Channel 3 offset	Channel 3 offset registers: upper, middle, and lower bytes (24 bits in total)	0x00	0x00	0x00	RW

GAIN REGISTERS

Each ADC channel has an associated gain coefficient. The coefficient is stored in three single-byte registers split up as MSB, MID, and LSB. Each of the gain registers are factory programmed. Nominally, this gain is around the value 0x555555 (for an ADC channel). The user may overwrite the gain register setting however, after a reset or power cycle, the gain register values revert to the hard coded programmed factory setting.

Table 83. Per Channel 24-Bit Gain Registers, 3 8-Bit Registers for Each Channel, Split Up as MSB, MID, and LSB

Address					Reset			
MSB	Mid	LSB	Name	Description	MSB	Mid	LSB	Access
0x36	0x37	0x38	Channel 0 gain	Channel 0 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x39	0x3A	0x3B	Channel 1 gain	Channel 1 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x42	0x43	0x44	Channel 2 gain	Channel 2 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW
0x45	0x46	0x47	Channel 3 gain	Channel 3 gain registers: upper, middle, and lower bytes (24 bits in total)	0xXX	0xXX	0xXX	RW

SYNC PHASE OFFSET REGISTERS

The AD7768-4 have one synchronization signal for all channels. The sync phase offset register allows the user to vary the phase delay on each of the channels relative to the synchronization edge received on the $\overline{\text{SYNC_IN}}$ pin. See the Sync Phase Offset Adjustment section for details on the use of this function.

Table 84. Per Channel 8-Bit Sync Phase Offset Registers

Address	Name	Description	Reset	Access
0x4E	Channel 0 sync offset	Channel 0 sync phase offset register	0x00	RW
0x4F	Channel 1 sync offset	Channel 1 sync phase offset register	0x00	RW
0x52	Channel 2 sync offset	Channel 2 sync phase offset register	0x00	RW
0x53	Channel 3 sync offset	Channel 3 sync phase offset register	0x00	RW

ADC DIAGNOSTIC RECEIVE SELECT REGISTER

Address: 0x56, Reset: 0x00, Name: Diagnostic Rx

The AD7768-4 ADC diagnostic allows the user to select a zero-scale, positive full-scale, or negative full-scale input to the ADC, which can be converted to verify the correct operation of the ADC channel. This register enables the diagnostic. Enable the receive (Rx) for each channel and set each bit in this register to 1. The diagnostic requires the analog input pins to be disconnected from external drive/sources to accurately measure the internal nodes.

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The ADC diagnostic feature depends on some features of the analog input precharge buffers. The user must ensure that the analog input precharge buffers are enabled on the channels that are selected to receive the diagnostic voltages internally.

Table 85. Bit Descriptions for Diagnostic Rx

Bits	Bit Name	Settings	Description	Reset	Access
5	CH3_RX		Channel 3	0x0	RW
		0	Not in use		
		1	Receive		
4	CH2_RX		Channel 2	0x0	RW
		0	Not in use		
		1	Receive		
1	CH1_RX		Channel 1	0x0	RW
		0	Not in use		
		1	Receive		
0	CH0_RX		Channel 0	0x0	RW
		0	Not in use		
		1	Receive		

ADC DIAGNOSTIC CONTROL REGISTER

Address: 0x57, Reset: 0x00, Name: Diagnostic Mux Control

The AD7768-4 ADC diagnostic allows the user to select a zero-scale, positive full-scale, or negative full-scale input to the ADC, which can be converted to verify the correct operation of the ADC channel. This register controls the voltage that is applied to each of the ADC channels for the diagnostic. There are three input voltage options that the user can select. The voltage selected is mapped to the channels based on which mode (Mode A or Mode B) they belong to, which is set according to the channel mode select register (Register 0x03).

Set Bits[7:0] to 1 in the ADC diagnostic receive select register, then select the voltage check desired for the channels on Mode A and the channels on Mode B through Bits[2:0] and Bits[6:4], respectively.

Table 86. Bit Descriptions for Diagnostic Mux Control

Bits	Bit Name	Settings	Description	Reset	Access
[6:4]	GRPB_SEL		Mux B.	0x0	RW
		000	Off.		
		011	Positive full-scale ADC check. A voltage close to positive full scale is applied internally to the ADC channel.		
		100	Negative full-scale ADC check. A voltage close to negative (or minus) full scale is applied internally to the ADC channel.		
		101	Zero-scale ADC check. A voltage close to 0 V is applied internally to the ADC channel.		
[2:0]	GRPA_SEL		Mux A.	0x0	RW
		000	Off.		
		011	Positive full-scale ADC check. A voltage close to positive full scale is applied internally to the ADC channel.		
		100	Negative full-scale ADC check. A voltage close to negative (or minus) full scale is applied internally to the ADC channel.		
		101	Zero-scale ADC check. A voltage close to 0 V is applied internally to the ADC channel.		

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MODULATOR DELAY CONTROL REGISTER

Address: 0x58, Reset: 0x02, Name: Modulator Delay Control

Table 87. Bit Descriptions for Modulator Delay Control

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	CLK_MOD_DEL_EN		Enable delayed modulator clock.	0x0	RW
		00	Disabled delayed clock for all channels.		
		01	Enable delayed clock for Channel 0 and Channel 1 only on the AD7768-4.		
		10	Enable delayed clock for Channel 2 and Channel 3 only on the AD7768-4.		
		11	Enable delayed clock for all channels.		
[1:0]	Reserved	10	Not a user option. Must be set to 0x2.	0x2	RW

CHOPPING CONTROL REGISTER

Address: 0x59, Reset: 0x0A, Name: Chop Control

Table 88. Bit Descriptions for Chop Control

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	GRPA_CHOP		Group A chopping	0x2	RW
		01	Chop at $f_{MOD}/8$		
		10	Chop at $f_{MOD}/32$		
[1:0]	GRPB_CHOP		Group B chopping	0x2	RW
		01	Chop at $f_{MOD}/8$		
		10	Chop at $f_{MOD}/32$		

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OUTLINE DIMENSIONS

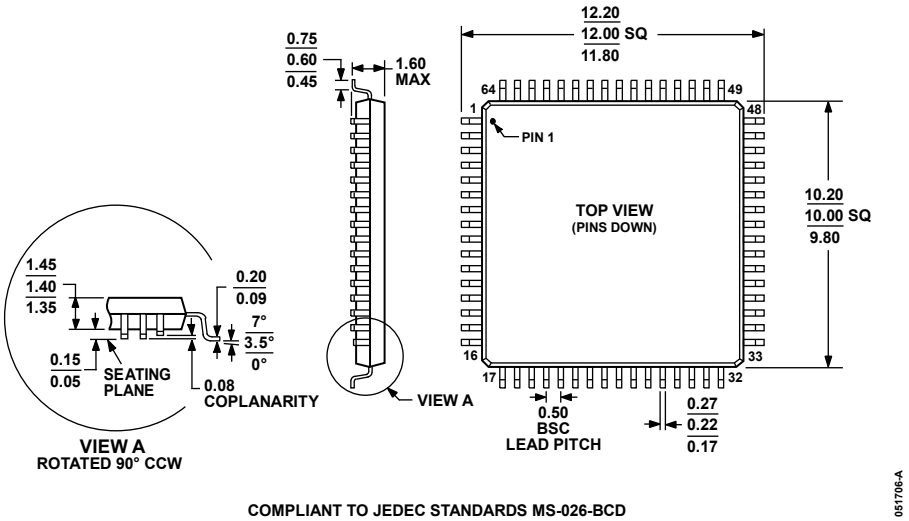

Figure 115. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7768BSTZ	−40°C to +105°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7768BSTZ-RL7	−40°C to +105°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7768BSTZ-RL	−40°C to +105°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7768-4BSTZ	−40°C to +105°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7768-4BSTZ-RL7	−40°C to +105°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
AD7768-4BSTZ-RL	−40°C to +105°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-AD7768FMCZ		Evaluation Board	
EVAL-AD7768-4FMCZ		AD7768-4 Evaluation Board	
EVAL-SDP-CH1Z		Controller Board	

[1] Z = RoHS Compliant Part.

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