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3/07—Rev. 0 to Rev. A

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4/06—Revision 0: Initial Version

SPECIFICATIONS

VDD = 4.75 V to 5.25 V, VIO = 2.3 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RESOLUTION		18			Bits
ANALOG INPUT					
Voltage Range	IN+ to IN−	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Voltage	IN+, IN−	−0.1		V_{REF} + 0.1	V
Common-Mode Input Range	IN+, IN−	$V_{REF}/2 - 0.1$	$V_{REF}/2$	$V_{REF}/2 + 0.1$	V
Analog Input CMRR	f_{IN} = 250 kHz		65		dB
Leakage Current at 25°C	Acquisition phase		1		nA
Input Impedance[1]					
THROUGHPUT					
Conversion Rate		0		400	kSPS
Transient Response	Full-scale step			400	ns
ACCURACY					
No Missing Codes		18			Bits
Integral Linearity Error		−1.5	±0.75	+1.5	LSB[2]
Differential Linearity Error		−1	±0.5	+1.25	LSB
Transition Noise	REF = VDD = 5 V		0.75		LSB
Gain Error[3]		−40	±2	+40	LSB
Gain Error Temperature Drift			±0.3		ppm/°C
Zero Error[3]		−0.8		+0.8	mV
Zero Temperature Drift			±0.3		ppm/°C
Power Supply Sensitivity	VDD = 5 V ± 5%		±0.25		LSB
AC ACCURACY					
Dynamic Range	V_{REF} = 5 V	101	102		dB[4]
Oversampled Dynamic Range[5]	f_{IN}= 1 kSPS		125		dB
Signal-to-Noise	f_{IN} = 1 kHz, V_{REF} = 5 V	100	101.5		dB
	f_{IN} = 1 kHz, V_{REF} = 2.5 V	94.5	96		dB
Spurious-Free Dynamic Range	f_{IN} = 1 kHz, V_{REF} = 5 V		−125		dB
Total Harmonic Distortion	f_{IN} = 1 kHz, V_{REF} = 5 V		−125		dB
Signal-to-(Noise + Distortion)	f_{IN} = 1 kHz, V_{REF} = 5 V	100	101.5		dB
Intermodulation Distortion[6]			115		dB

[1] See the Analog Inputs section.
[2] LSB means least significant bit. With the ±5 V input range, one LSB is 38.15 µV.
[3] See the Terminology section. These specifications include full temperature range variation but not the error contribution from the external reference.
[4] All specifications in dB are referred to a full-scale input FSR. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[5] Dynamic range obtained by oversampling the ADC running at a throughput f_S of 400 kSPS, followed by postdigital filtering with an output word rate f_O.
[6] f_{IN1} = 21.4 kHz and f_{IN2} = 18.9 kHz, with each tone at −7 dB below full scale.

VDD = 4.75 V to 5.25 V, VIO = 2.3 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
REFERENCE					
Voltage Range		0.5		VDD + 0.3	V
Load Current	400 kSPS, REF = 5 V		100		µA
SAMPLING DYNAMICS					
−3 dB Input Bandwidth			9		MHz
Aperture Delay	VDD = 5 V		2.5		ns
DIGITAL INPUTS					
Logic Levels					
V_{IL}		−0.3		+0.3 × VIO	V
V_{IH}		0.7 × VIO		VIO + 0.3	V
I_{IL}		−1		+1	µA
I_{IH}		−1		+1	µA
DIGITAL OUTPUTS					
Data Format		Serial 18 bits, twos complement			
Pipeline Delay		Conversion results available immediately after completed conversion			
V_{OL}	I_{SINK} = +500 µA			0.4	V
V_{OH}	I_{SOURCE} = −500 µA	VIO − 0.3			V
POWER SUPPLIES					
VDD	Specified performance	4.75		5.25	V
VIO	Specified performance	2.3		VDD + 0.3	V
VIO Range		1.8		VDD + 0.3	V
Standby Current[1, 2]	VDD and VIO = 5 V, 25°C		1	50	nA
Power Dissipation	VDD = 5 V, 100 SPS throughput		4.25		µW
	VDD = 5 V, 100 kSPS throughput		4.25	5	mW
	VDD = 5 V, 400 kSPS throughput		17	20	mW
Energy per Conversion			50		nJ/sample
TEMPERATURE RANGE[3]					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] With all digital inputs forced to VIO or GND as required.
[2] During acquisition phase.
[3] Contact an Analog Devices, Inc., sales representative for the extended temperature range.

TIMING SPECIFICATIONS

VDD = 4.75 V to 5.25 V, VIO = 2.3 V to VDD, V_{REF} = VDD, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.[1]

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time: CNV Rising Edge to Data Available	t_{CONV}	0.5		2.1	µs
Acquisition Time	t_{ACQ}	400			ns
Time Between Conversions	t_{CYC}	2.5			µs
CNV Pulse Width ($\overline{CS}$ Mode)	t_{CNVH}	10			ns
SCK Period ($\overline{CS}$ Mode)	t_{SCK}	15			ns
SCK Period (Chain Mode)	t_{SCK}				
VIO Above 4.5 V		17			ns
VIO Above 3 V		18			ns
VIO Above 2.7 V		19			ns
VIO Above 2.3 V		20			ns
SCK Low Time	t_{SCKL}	7			ns
SCK High Time	t_{SCKH}	7			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	4			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}				
VIO Above 4.5 V				14	ns
VIO Above 3 V				15	ns
VIO Above 2.7 V				16	ns
VIO Above 2.3 V				17	ns
CNV or SDI Low to SDO D17 MSB Valid ($\overline{CS}$ Mode)	t_{EN}				
VIO Above 4.5 V				15	ns
VIO Above 2.7 V				18	ns
VIO Above 2.3 V				22	ns
CNV or SDI High or Last SCK Falling Edge to SDO High Impedance ($\overline{CS}$ Mode)	t_{DIS}			25	ns
SDI Valid Setup Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{SSDICNV}$	15			ns
SDI Valid Hold Time from CNV Rising Edge ($\overline{CS}$ Mode)	$t_{HSDICNV}$	0			ns
SCK Valid Setup Time from CNV Rising Edge (Chain Mode)	$t_{SSCKCNV}$	5			ns
SCK Valid Hold Time from CNV Rising Edge (Chain Mode)	$t_{HSCKCNV}$	10			ns
SDI Valid Setup Time from SCK Falling Edge (Chain Mode)	$t_{SSDISCK}$	3			ns
SDI Valid Hold Time from SCK Falling Edge (Chain Mode)	$t_{HSDISCK}$	4			ns
SDI High to SDO High (Chain Mode with BUSY Indicator)	$t_{DSDOSDI}$				
VIO Above 4.5 V				15	ns
VIO Above 2.3 V				26	ns

[1] See Figure 3 and Figure 4 for load conditions.

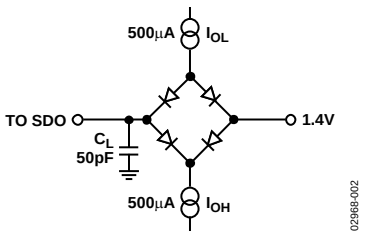


Figure 3. Load Circuit for Digital Interface Timing

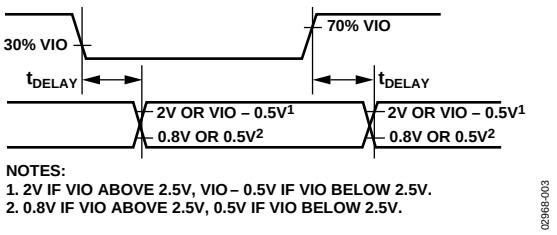


Figure 4. Voltage Levels for Timing

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Analog Inputs	
IN+,[1] IN–[1]	GND – 0.3 V to VDD + 0.3 V or ±130 mA
REF	GND – 0.3 V to VDD + 0.3 V
Supply Voltages	
VDD, VIO to GND	−0.3 V to +7 V
VDD to VIO	±7 V
Digital Inputs to GND	−0.3 V to VIO + 0.3 V
Digital Outputs to GND	−0.3 V to VIO + 0.3 V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance (10-Lead MSOP)	200°C/W
θ_{JC} Thermal Impedance (10-Lead MSOP)	44°C/W
Lead Temperature Range	JEDEC J-STD-20

[1] See the Analog Inputs section.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

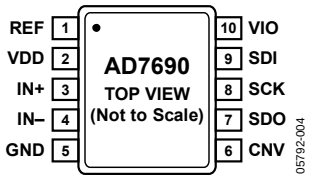


Figure 5. 10-Lead MSOP Pin Configuration

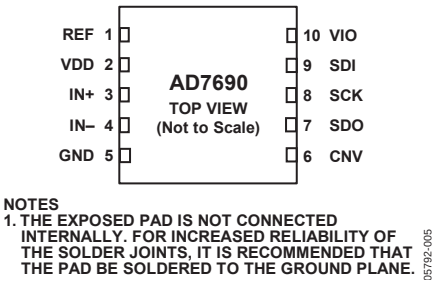


Figure 6. 10-Lead LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	REF	AI	Reference Input Voltage. The REF range is from 0.5 V to VDD. It is referred to the GND pin. This pin should be decoupled closely to the pin with a 10 µF capacitor.
2	VDD	P	Power Supply.
3	IN+	AI	Differential Positive Analog Input.
4	IN−	AI	Differential Negative Analog Input.
5	GND	P	Power Supply Ground.
6	CNV	DI	Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the part, chain or $\overline{CS}$ mode. In $\overline{CS}$ mode, the SDO pin is enabled when CNV is low. In chain mode, the data should be read when CNV is high.
7	SDO	DO	Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.
8	SCK	DI	Serial Data Clock Input. When the part is selected, the conversion result is shifted out by this clock.
9	SDI	DI	Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 18 SCK cycles. $\overline{CS}$ mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled.
10	VIO	P	Input/Output Interface Digital Power. Nominally at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V).
	EPAD		Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the ground plane.

[1]AI = analog input, DI = digital input, DO = digital output, and P = power.

TERMINOLOGY

Integral Nonlinearity Error (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 25).

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Zero Error
Zero error is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

Gain Error
The first transition (from 100 ... 00 to 100 ... 01) should occur at a level ½ LSB above nominal negative full scale (−4.999981 V for the ±5 V range). The last transition (from 011 … 10 to 011 … 11) should occur for an analog voltage 1½ LSB below the nominal full scale (+4.999943 V for the ±5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Spurious-Free Dynamic Range (SFDR)
SFDR is the difference, in decibels, between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD by the following formula:

$$ENOB = (SINAD_{dB} - 1.76)/6.02$$

and is expressed in bits.

Noise-Free Code Resolution
Noise-free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as:

$$Noise\text{-}Free\ Code\ Resolution = \log_2(2^N/Peak\text{-}to\text{-}Peak\ Noise)$$

and is expressed in bits.

Effective Resolution
Effective resolution is calculated as

$$Effective\ Resolution = \log_2(2^N/RMS\ Input\ Noise)$$

and is expressed in bits.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured with the inputs shorted together. The value for dynamic range is expressed in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that is less than the Nyquist frequency, excluding harmonics and dc. The value of SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Aperture Delay
Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

Transient Response
Transient response is the time required for the ADC to accurately acquire its input after a full-scale step function is applied.

TYPICAL PERFORMANCE CHARACTERISTICS

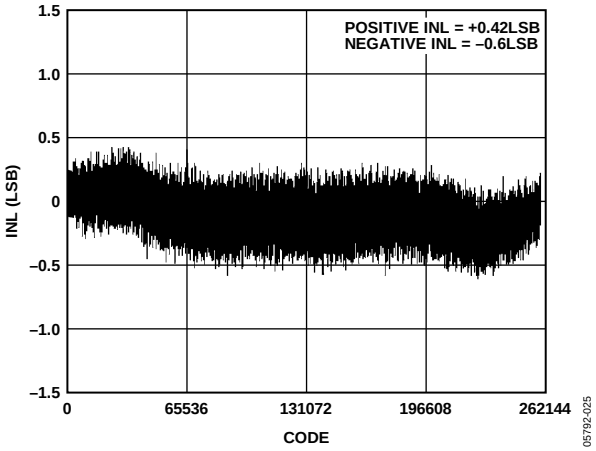


Figure 7. Integral Nonlinearity vs. Code

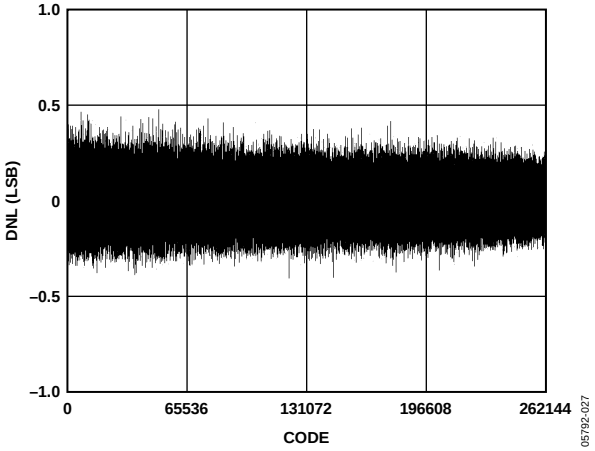


Figure 10. Differential Nonlinearity vs. Code

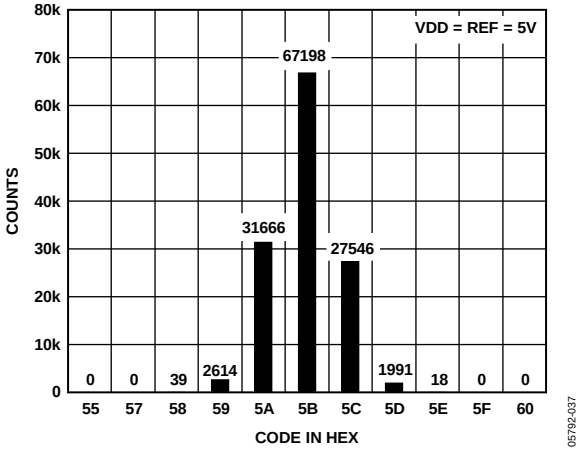


Figure 8. Histogram of a DC Input at the Code Center

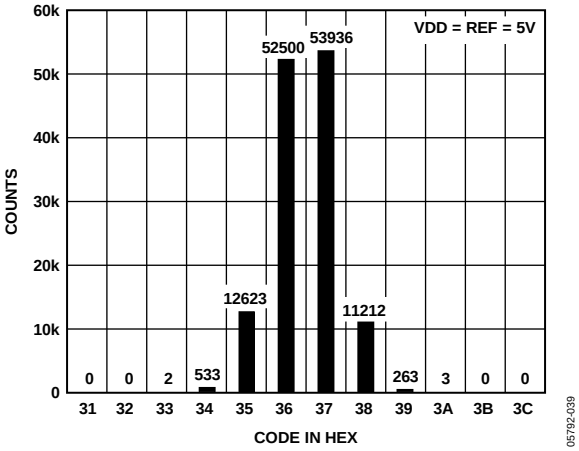


Figure 11. Histogram of a DC Input at the Code Transition

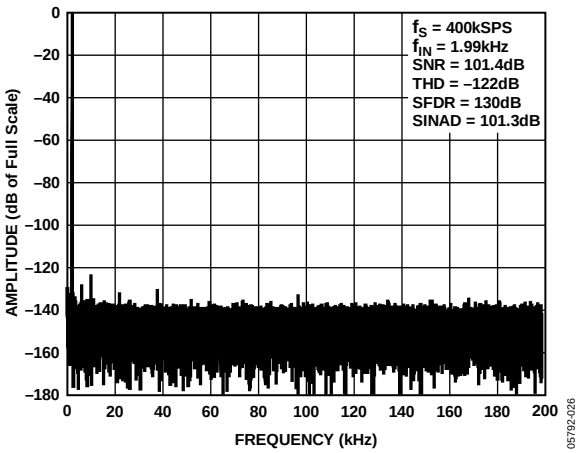


Figure 9. Fast Fourier Transform Plot

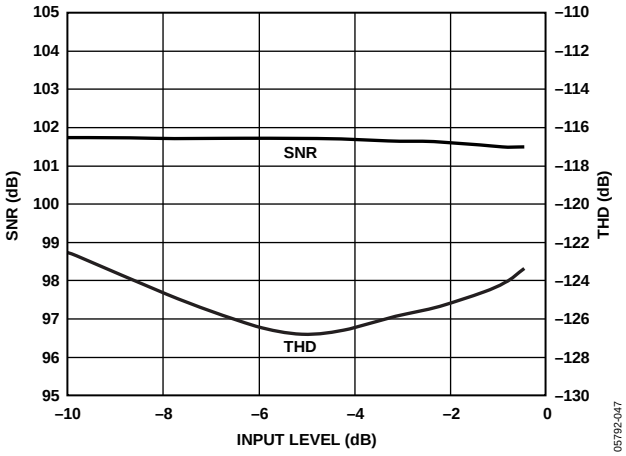


Figure 12. SNR, THD vs. Input Level

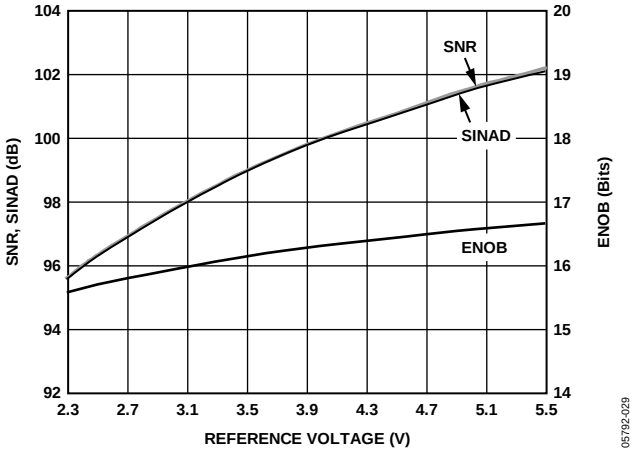


Figure 13. SNR, SINAD, and ENOB vs. Reference Voltage

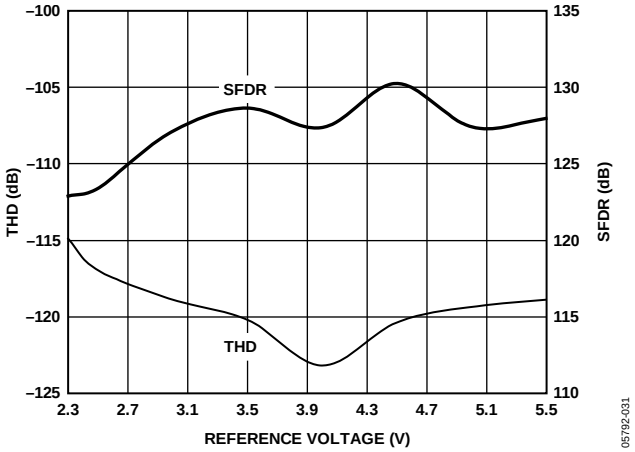


Figure 16. THD, SFDR vs. Reference Voltage

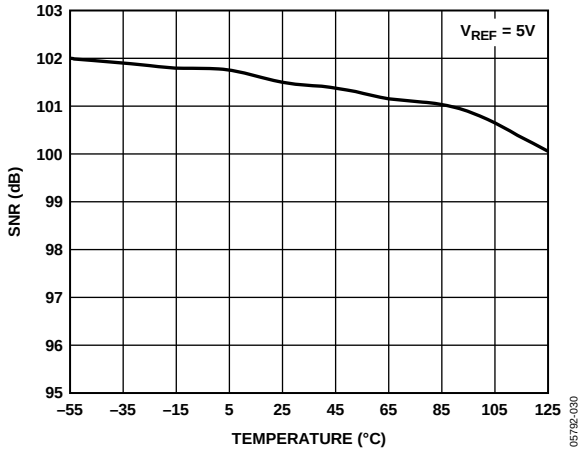


Figure 14. SNR vs. Temperature

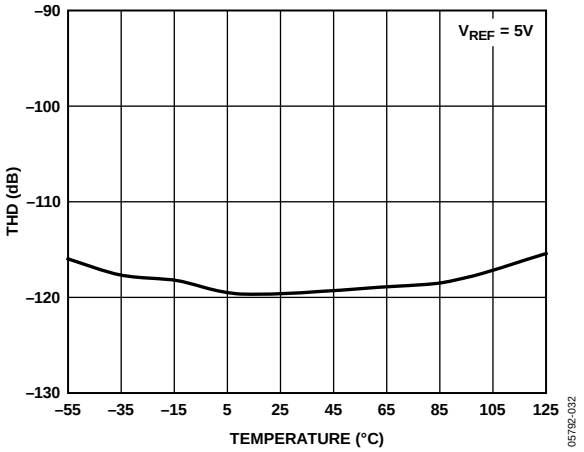


Figure 17. THD vs. Temperature

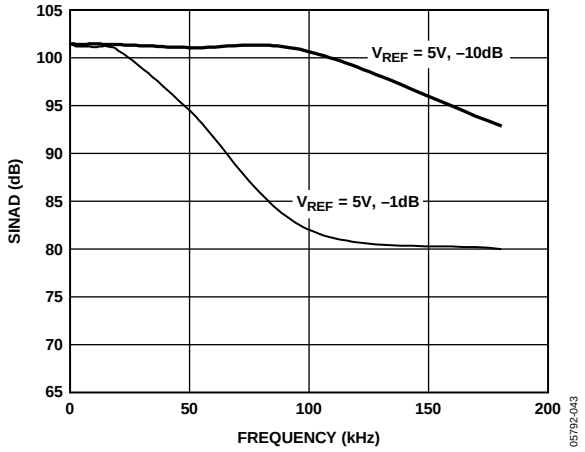


Figure 15. SINAD vs. Frequency

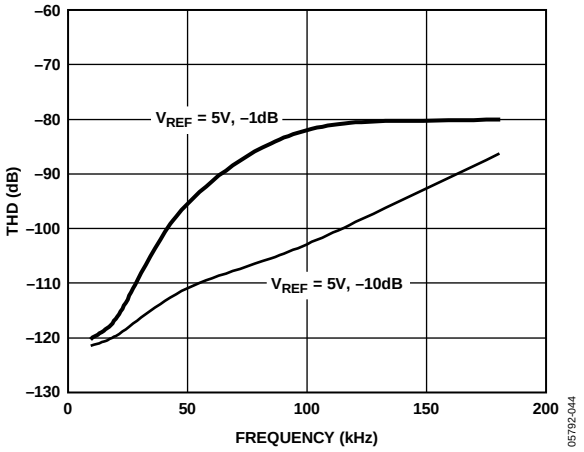


Figure 18. THD vs. Frequency

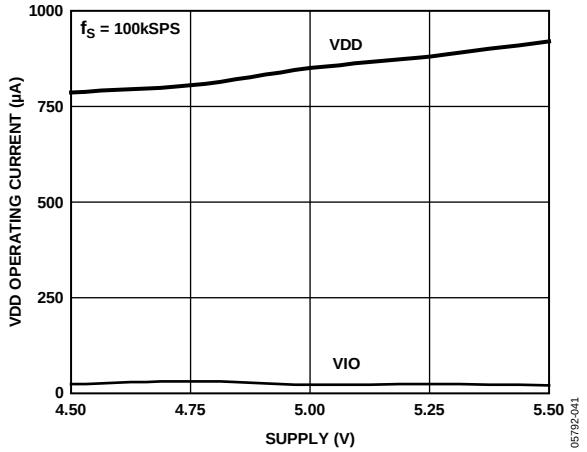


Figure 19. Operating Current vs. Supply

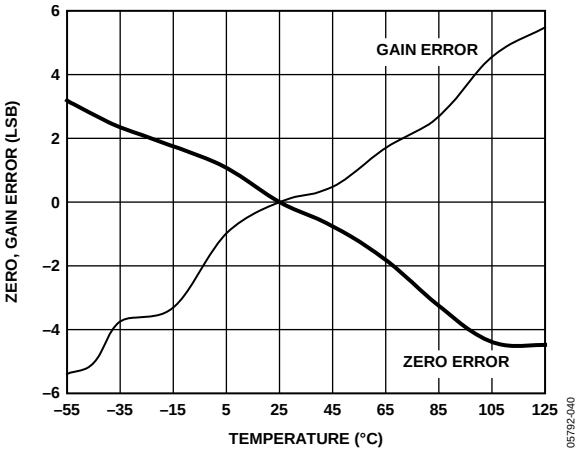


Figure 22. Zero and Gain Error vs. Temperature

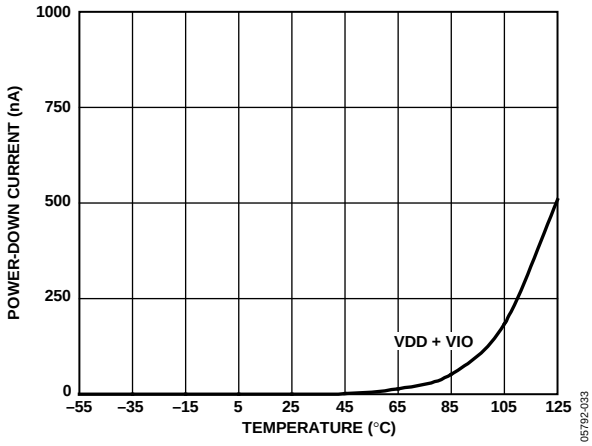


Figure 20. Power-Down Current vs. Temperature

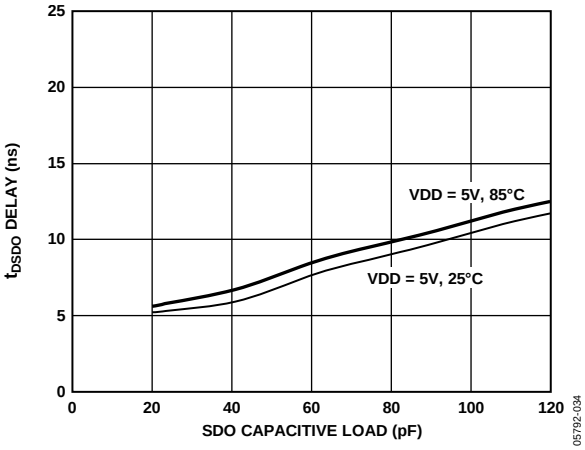


Figure 23. t_{DSDO} Delay vs. Capacitance Load and Supply

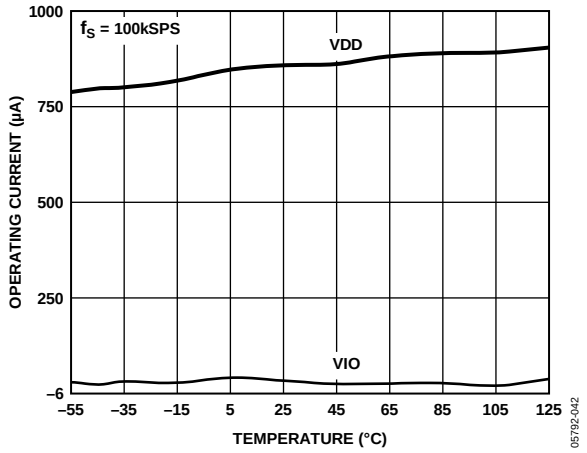


Figure 21. Operating Current vs. Temperature

THEORY OF OPERATION

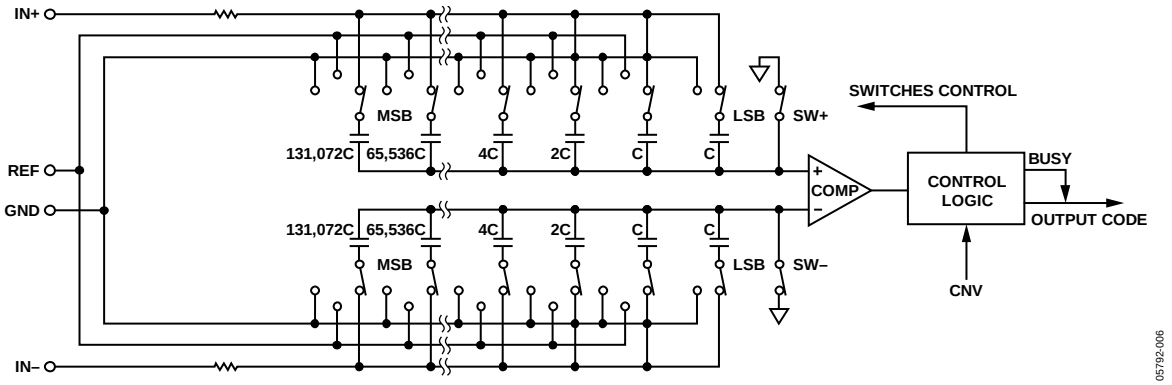


Figure 24. ADC Simplified Schematic

CIRCUIT INFORMATION

The AD7690 is a fast, low power, single-supply, precise, 18-bit ADC using a successive approximation architecture.

The AD7690 is capable of converting 400,000 samples per second (400 kSPS) and powers down between conversions. When operating at 1 kSPS, for example, it consumes 50 µW typically, ideal for battery-powered applications.

The AD7690 provides the user with an on-chip track-and-hold and does not exhibit pipeline delay or latency, making it ideal for multiple multiplexed channel applications.

The AD7690 is specified from 4.75 V to 5.25 V and can be interfaced to any 1.8 V to 5 V digital logic family. It is housed in a 10-lead MSOP or a tiny 10-lead LFCSP that allows space savings and flexible configurations.

It is pin-for-pin compatible with the 18-bit AD7691 and AD7982 and the 16-bit AD7687, AD7688, and AD7693.

CONVERTER OPERATION

The AD7690 is a successive approximation ADC based on a charge redistribution DAC. Figure 24 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 18 binary-weighted capacitors, which are connected to the two comparator inputs.

During the acquisition phase, terminals of the array tied to the comparator's input are connected to GND via SW+ and SW−. All independent switches are connected to the analog inputs. Thus, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs. When the acquisition phase is complete and the CNV input goes high, a conversion phase is initiated. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. Therefore, the differential voltage between the IN+ and IN− inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and REF, the comparator input varies by binary-weighted voltage steps ($V_{REF}/2$, $V_{REF}/4$ ... $V_{REF}/262,144$). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the part returns to the acquisition phase, and the control logic generates the ADC output code and a busy signal indicator.

Because the AD7690 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

Transfer Functions

The ideal transfer characteristic for the AD7690 is shown in Figure 25 and Table 7.

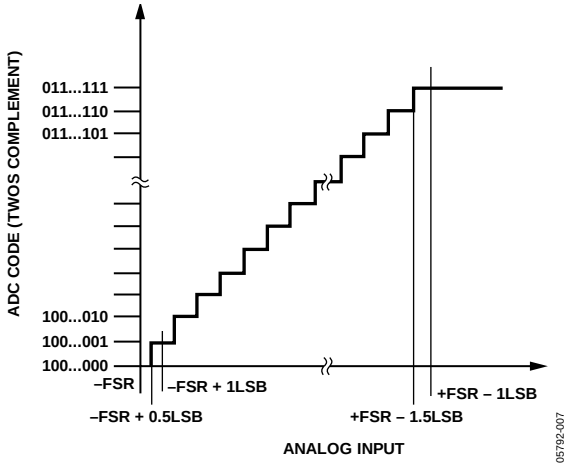


Figure 25. ADC Ideal Transfer Function

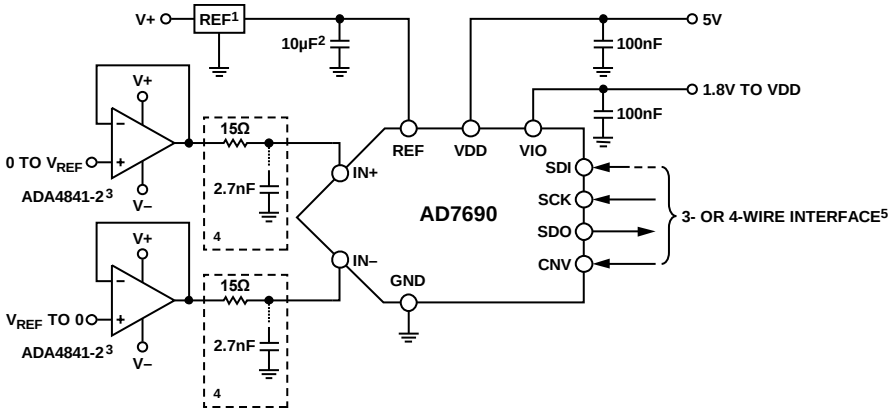
Table 7. Output Codes and Ideal Input Voltages

Description	Analog Input V_{REF} = 5 V	Digital Output Code (Hex)
FSR – 1 LSB	+4.999962 V	0x1FFFF[1]
Midscale + 1 LSB	+38.15 µV	0x00001
Midscale	0 V	0x00000
Midscale – 1 LSB	–38.15 µV	0x3FFFF
–FSR + 1 LSB	–4.999962 V	0x20001
–FSR	–5 V	0x20000[2]

[1] This is also the code for an overranged analog input (V_{IN+} – V_{IN-} above V_{REF} – V_{GND}).
[2] This is also the code for an underranged analog input (V_{IN+} – V_{IN-} below V_{GND}).

TYPICAL CONNECTION DIAGRAM

Figure 26 shows an example of the recommended connection diagram for the AD7690 when multiple supplies are available.



[1] SEE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION.
[2] C_{REF} IS USUALLY A 10µF CERAMIC CAPACITOR (X5R).
[3] SEE TABLE 8 FOR ADDITIONAL RECOMMENDED AMPLIFIERS.
[4] OPTIONAL FILTER. SEE ANALOG INPUT SECTION.
[5] SEE THE DIGITAL INTERFACE SECTION FOR MOST CONVENIENT INTERFACE MODE.

Figure 26. Typical Application Diagram with Multiple Supplies

ANALOG INPUTS

Figure 27 shows an equivalent circuit of the input structure of the AD7690.

The two diodes, D1 and D2, provide ESD protection for the analog inputs, IN+ and IN−. Care must be taken to ensure that the analog input signal does not exceed the supply rails by more than 0.3 V because this causes the diodes to become forward biased and start conducting current. These diodes can handle a forward-biased current of 130 mA maximum. For instance, these conditions could eventually occur when the input buffer's (U1) supplies are different from VDD. In such a case (for example, an input buffer with a short circuit), the current limitation can be used to protect the part.

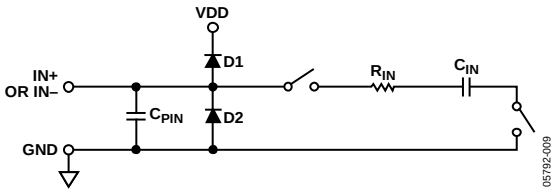


Figure 27. Equivalent Analog Input Circuit

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected.

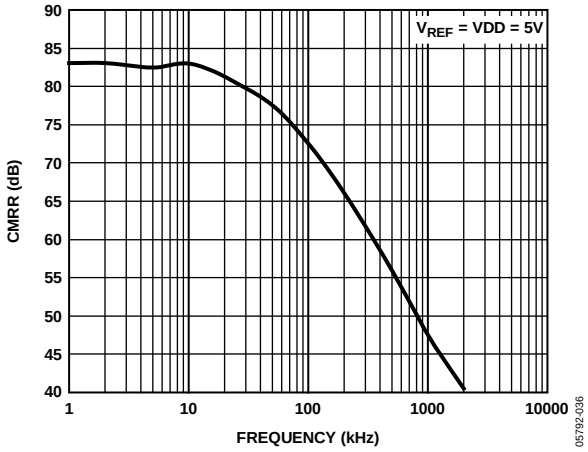


Figure 28. Analog Input CMRR vs. Frequency

During the acquisition phase, the impedance of the analog inputs (IN+ and IN−) can be modeled as a parallel combination of the capacitor, C_{PIN}, and the network formed by the series connection of R_{IN} and C_{IN}. C_{PIN} is primarily the pin capacitance. R_{IN} is typically 600 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C_{IN} is typically 30 pF and is mainly the ADC sampling capacitor.

During the conversion phase, where the switches are opened, the input impedance is limited to C_{PIN}. R_{IN} and C_{IN} make a 1-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

When the source impedance of the driving circuit is low, the AD7690 can be driven directly. Large source impedances significantly affect the ac performance, especially total harmonic distortion (THD). The dc performances are less sensitive to the input impedance. The maximum source impedance depends on the amount of THD that can be tolerated. The THD degrades as a function of the source impedance and the maximum input frequency.

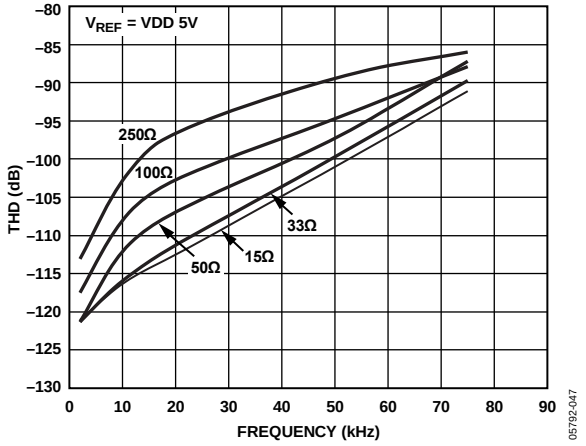


Figure 29. THD vs. Analog Input Frequency and Source Resistance

DRIVER AMPLIFIER CHOICE

Although the AD7690 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept as low as possible to preserve the SNR and transition noise performance of the AD7690. The noise from the driver is filtered by the AD7690 analog input circuit's 1-pole, low-pass filter made by R_{IN} and C_{IN} or by the external filter, if one is used. Because the typical noise of the AD7690 is 28 μV rms, the SNR degradation due to the amplifier is

$$SNR_{LOSS} = 20 \log \left(\frac{28}{\sqrt{28^2 + \frac{\pi}{2} f_{-3\,dB} (Ne_{N+})^2 + \frac{\pi}{2} f_{-3\,dB} (Ne_{N-})^2}} \right)$$

  where:
  $f_{-3\,dB}$ is the input bandwidth in megahertz of the AD7690 (9 MHz) or the cutoff frequency of the input filter, if one is used.
  N is the noise gain of the amplifier (for example, 1 in buffer configuration).
  e_{N+} and e_{N-} are the equivalent input noise voltage densities of the op amps connected to IN+ and IN−, in nV/√Hz.

  This approximation can be used when the resistances around the amplifiers are small. If larger resistances are used, their noise contributions should also be root summed squared.

- For ac applications, the driver should have a THD performance commensurate with the AD7690.

- For multichannel multiplexed applications, the driver amplifier and the AD7690 analog input circuit must settle for a full-scale step onto the capacitor array at an 18-bit level (0.0004%, 4 ppm). In the amplifier's data sheet, settling at 0.1% to 0.01% is more commonly specified. This may differ significantly from the settling time at an 18-bit level and should be verified prior to driver selection.

Table 8. Recommended Driver Amplifiers

Amplifier	Typical Application
ADA4941-1	Very low noise, low power single to differential
ADA4841-x	Very low noise, small, and low power
AD8655	5 V single supply, low noise
AD8021	Very low noise and high frequency
AD8022	Low noise and high frequency
OP184	Low power, low noise, and low frequency
AD8605, AD8615	5 V single supply, low power

SINGLE-TO-DIFFERENTIAL DRIVER

For applications using a single-ended analog signal, either bipolar or unipolar, the ADA4941-1 single-ended-to-differential driver allows for a differential input into the part. The schematic is shown in Figure 30.

R1 and R2 set the attenuation ratio between the input range and the ADC range (V_{REF}). R1, R2, and C_F are chosen depending on the desired input resistance, signal bandwidth, antialiasing, and noise contribution. For example, for the ±10 V range with a 4 kΩ impedance, R2 = 1 kΩ and R1 = 4 kΩ.

R3 and R4 set the common mode on the IN− input, and R5 and R6 set the common mode on the IN+ input of the ADC. The common mode should be set close to $V_{REF}/2$; however, if single supply is desired, it can be set slightly above $V_{REF}/2$ to provide some headroom for the ADA4941-1 output stage. For example, for the ±10 V range with a single supply, R3 = 8.45 kΩ, R4 = 11.8 kΩ, R5 = 10.5 kΩ, and R6 = 9.76 kΩ.

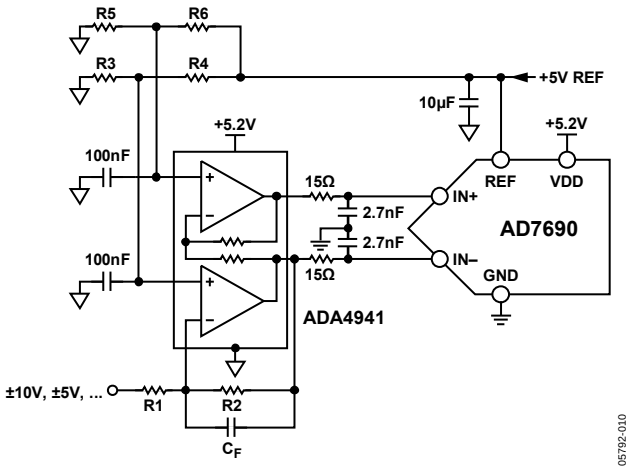


Figure 30. Single-Ended-to-Differential Driver Circuit

VOLTAGE REFERENCE INPUT

The AD7690 voltage reference input, REF, has a dynamic input impedance and should therefore be driven by a low impedance source with efficient decoupling between the REF and GND pins, as explained in the Layout section.

When REF is driven by a very low impedance source (for example, a reference buffer using the AD8031 or the AD8605), a 10 µF (X5R, 0805 size) ceramic chip capacitor is appropriate for optimum performance.

If an unbuffered reference voltage is used, the decoupling value depends on the reference used. For instance, a 22 µF (X5R, 1206 size) ceramic chip capacitor is appropriate for optimum performance using a low temperature drift ADR43x reference.

If desired, a reference-decoupling capacitor with a value as small as 2.2 µF can be used with a minimal impact on performance, especially DNL.

Regardless, there is no need for an additional lower value ceramic decoupling capacitor (for example, 100 nF) between the REF and GND pins.

POWER SUPPLY

The AD7690 uses two power supply pins: a core supply, VDD, and a digital input/output interface supply, VIO. VIO allows a direct interface with any logic between 1.8 V and V_{DD}. To reduce the number of supplies needed, the VIO and VDD pins can be tied together. The AD7690 is independent of power supply sequencing between VIO and VDD. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 31.

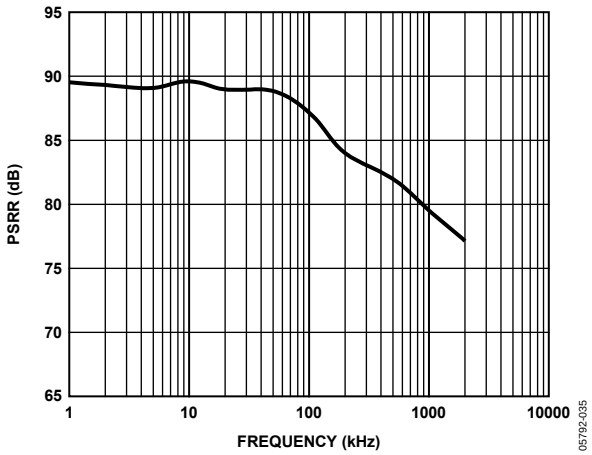


Figure 31. PSRR vs. Frequency

The AD7690 powers down automatically at the end of each conversion phase and, therefore, the power scales linearly with the sampling rate. This makes the part ideal for low sampling rates (even of a few hertz) and low battery-powered applications.

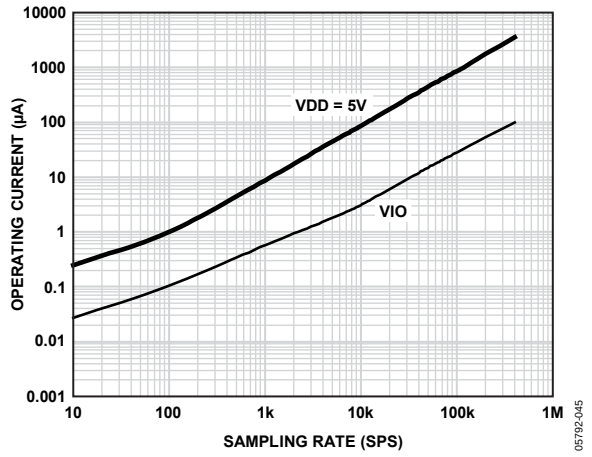
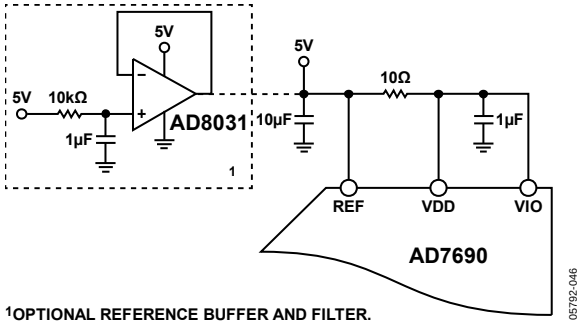


Figure 32. Operating Current vs. Sample Rate

SUPPLYING THE ADC FROM THE REFERENCE

For simplified applications, the AD7690, with its low operating current, can be supplied directly using the reference circuit shown in Figure 33. The reference line can be driven by

- The system power supply directly.
- A reference voltage with enough current output capability, such as the ADR43x.
- A reference buffer, such as the AD8031, which can also filter the system power supply, as shown in Figure 33.



[1]OPTIONAL REFERENCE BUFFER AND FILTER.

Figure 33. Example of Application Circuit

DIGITAL INTERFACE

Though the AD7690 has a reduced number of pins, it offers flexibility in its serial interface modes.

When in $\overline{CS}$ mode, the AD7690 is compatible with SPI, QSPI™, digital hosts, and DSPs, for example, Blackfin® ADSP-BF53x or ADSP-219x. In this mode, the AD7690 can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback timing (SDI). This is useful in low jitter sampling or simultaneous sampling applications.

When in chain mode, the AD7690 provides a daisy-chain feature using the SDI input for cascading multiple ADCs on a single data line similar to a shift register.

The mode in which the part operates depends on the SDI level when the CNV rising edge occurs. The $\overline{CS}$ mode is selected if SDI is high, and the chain mode is selected if SDI is low. The SDI hold time is such that when SDI and CNV are connected together, the chain mode is selected.

In either mode, the AD7690 offers the option of forcing a start bit in front of the data bits. This start bit can be used as a busy signal indicator to interrupt the digital host and trigger the data reading. Otherwise, without a busy indicator, the user must timeout the maximum conversion time prior to readback.

The busy indicator feature is enabled

- In $\overline{CS}$ mode if CNV or SDI is low when the ADC conversion ends (see Figure 37 and Figure 41).
- In chain mode if SCK is high during the CNV rising edge (see Figure 45).

$\overline{CS}$ MODE, 3-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when a single AD7690 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 34, and the corresponding timing is given in Figure 35.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. Once a conversion is initiated, it continues until completion irrespective of the state of CNV. This can be useful, for instance, to bring CNV low to select other SPI devices, such as analog multiplexers; however, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7690 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 18th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

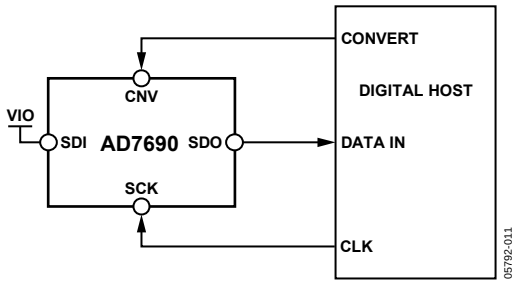


Figure 34. 3-Wire $\overline{CS}$ Mode Without Busy Indicator Connection Diagram (SDI High)

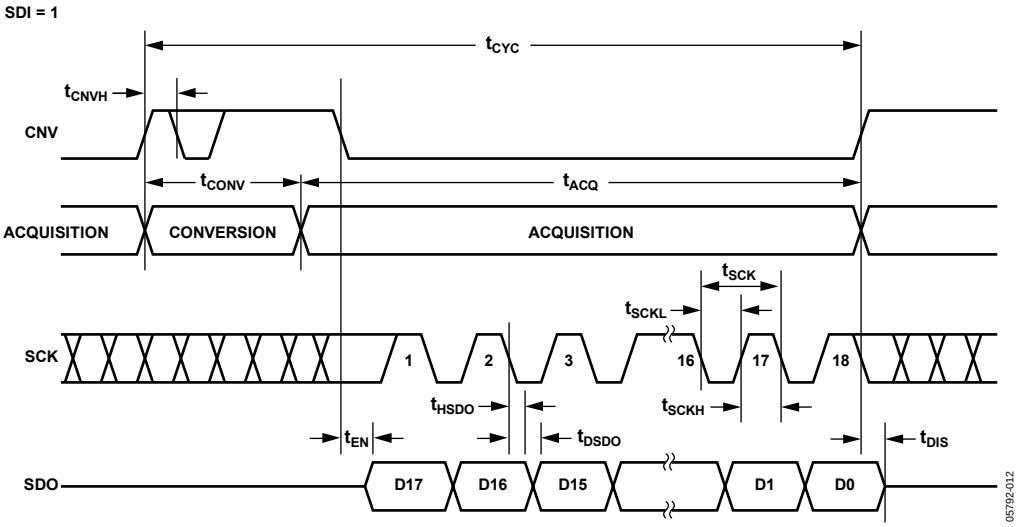


Figure 35. 3-Wire $\overline{CS}$ Mode Without Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 3-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7690 is connected to an SPI-compatible digital host having an interrupt input.

The connection diagram is shown in Figure 36, and the corresponding timing is given in Figure 37.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can be used to select other SPI devices, such as analog multiplexers, but CNV must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD7690 then enters the acquisition phase and powers down. The data bits are clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 19th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If multiple AD7690s are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation.

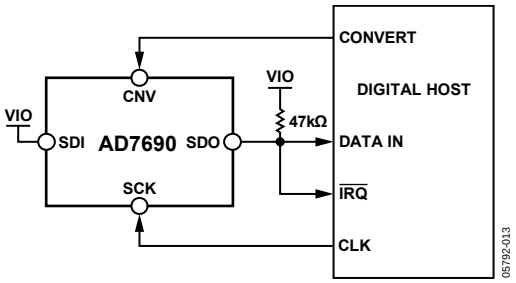


Figure 36. 3-Wire $\overline{CS}$ Mode with Busy Indicator Connection Diagram (SDI High)

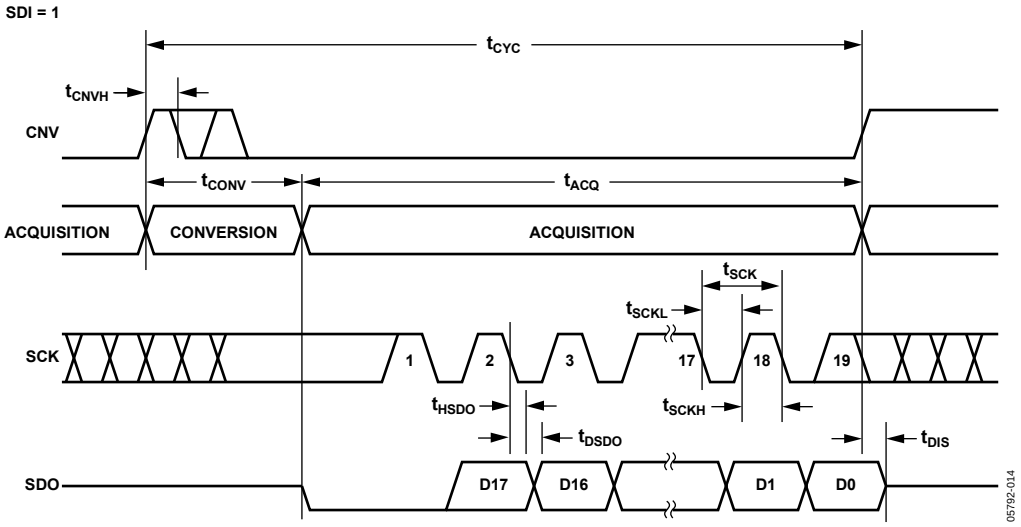


Figure 37. 3-Wire $\overline{CS}$ Mode with Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ MODE, 4-WIRE WITHOUT BUSY INDICATOR

This mode is usually used when multiple AD7690s are connected to an SPI-compatible digital host.

A connection diagram example using two AD7690s is shown in Figure 38, and the corresponding timing is given in Figure 39.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. (If SDI and CNV are low, SDO is driven low.) Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator. When the conversion is complete, the AD7690 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 18th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance and another AD7690 can be read.

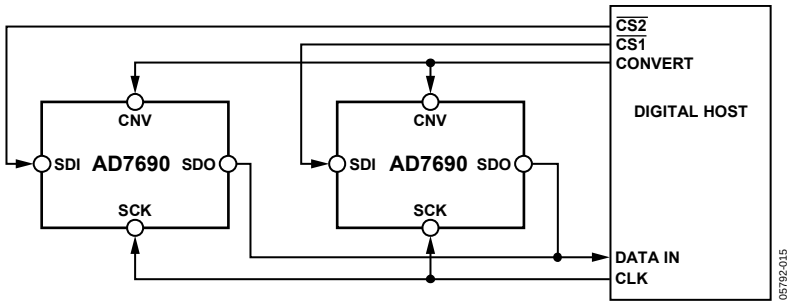


Figure 38. 4-Wire $\overline{CS}$ Mode Without Busy Indicator Connection Diagram

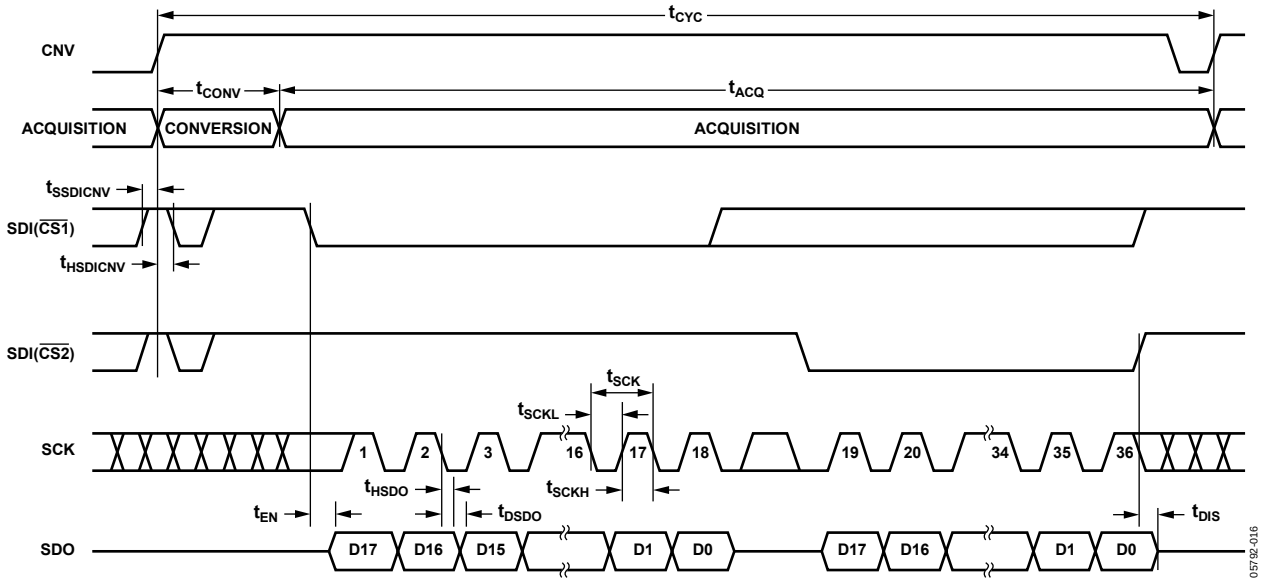


Figure 39. 4-Wire $\overline{CS}$ Mode Without Busy Indicator Serial Interface Timing

$\overline{CS}$ MODE, 4-WIRE WITH BUSY INDICATOR

This mode is usually used when a single AD7690 is connected to an SPI-compatible digital host, which has an interrupt input, and it is desired to keep CNV, which is used to sample the analog input, independent of the signal used to select the data reading. This independence is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 40, and the corresponding timing is given in Figure 41.

With SDI high, a rising edge on CNV initiates a conversion, selects the $\overline{CS}$ mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. (If SDI and CNV are low, SDO is driven low.) Prior to the minimum conversion time, SDI can be used to select other SPI devices, such as analog multiplexers, but SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator. When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD7690 then enters the acquisition phase and powers down. The data bits are clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 19th SCK falling edge or SDI going high (whichever occurs first), SDO returns to high impedance.

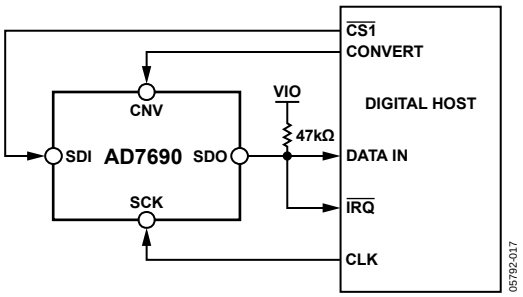


Figure 40. 4-Wire $\overline{CS}$ Mode with Busy Indicator Connection Diagram

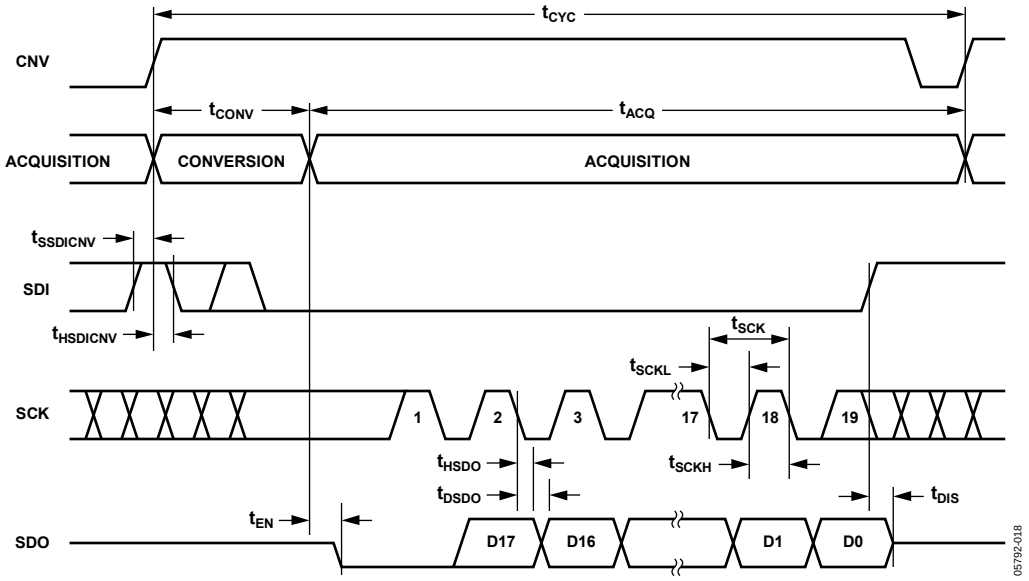


Figure 41. 4-Wire $\overline{CS}$ Mode with Busy Indicator Serial Interface Timing

CHAIN MODE WITHOUT BUSY INDICATOR

This mode can be used to daisy-chain multiple AD7690s on a 3-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD7690s is shown in Figure 42, and the corresponding timing is given in Figure 43.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects the chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO and the AD7690 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 18 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7690s in the chain, provided the digital host has an acceptable hold time. The maximum conversion rate may be reduced due to the total readback time.

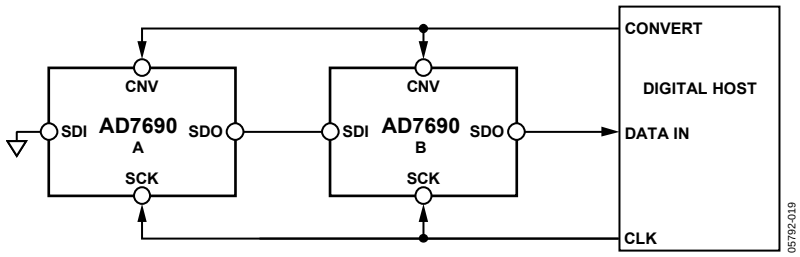


Figure 42. Chain Mode Without Busy Indicator Connection Diagram

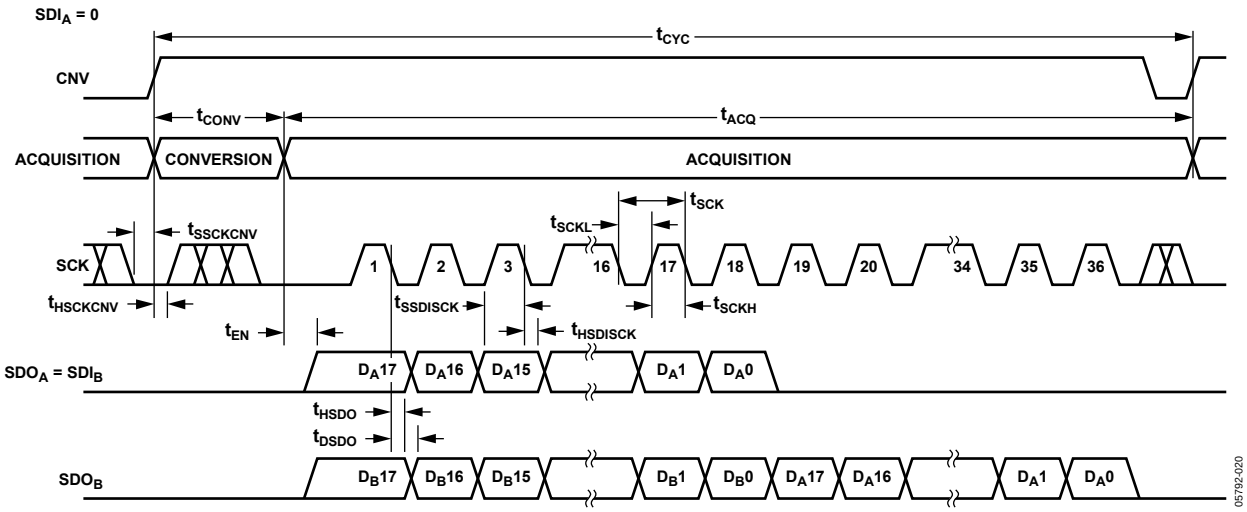


Figure 43. Chain Mode Without Busy Indicator Serial Interface Timing

CHAIN MODE WITH BUSY INDICATOR

This mode can also be used to daisy-chain multiple AD7690s on a 3-wire serial interface while providing a busy indicator. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using three AD7690s is shown in Figure 44, and the corresponding timing is given in Figure 45.

When SDI and CNV are low, SDO is driven low. With SCK high, a rising edge on CNV initiates a conversion, selects the chain mode, and enables the busy indicator feature. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When all ADCs in the chain have completed their conversions, the SDO pin of the ADC closest to the digital host (see the AD7690 ADC labeled C in Figure 44) is driven high. This transition on SDO can be used as a busy indicator to trigger the data readback controlled by the digital host. The AD7690 then enters the acquisition phase and powers down. The data bits stored in the internal shift register are clocked out, MSB first, by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK falling edge. Each ADC in the chain outputs its data MSB first, and 18 × N + 1 clocks are required to read back the N ADCs. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate and consequently more AD7690s in the chain, provided the digital host has an acceptable hold time.

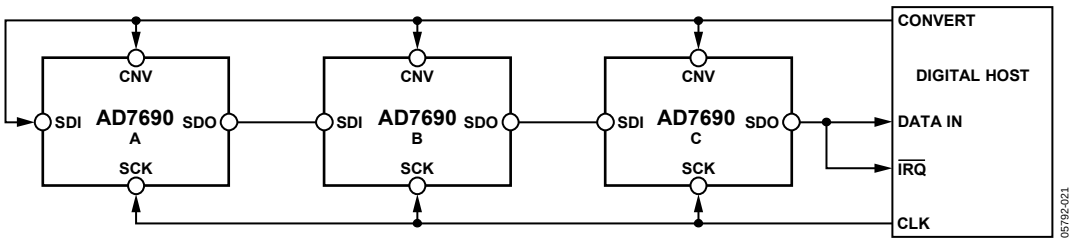


Figure 44. Chain Mode with Busy Indicator Connection Diagram

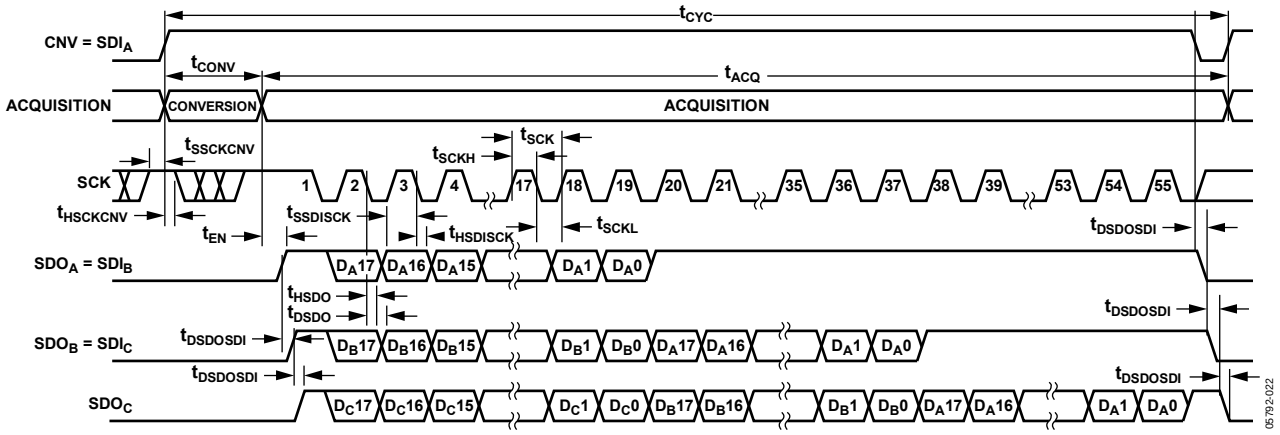


Figure 45. Chain Mode with Busy Indicator Serial Interface Timing

APPLICATION HINTS

LAYOUT

The printed circuit board that houses the AD7690 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD7690, with its analog signals on the left side and its digital signals on the right side, eases this task.

Avoid running digital lines under the device because these couple noise onto the die unless a ground plane under the AD7690 is used as a shield. Fast switching signals, such as CNV or clocks, should not run near analog signal paths. Crossover of digital and analog signals should be avoided.

At least one ground plane should be used. It can be common or split between the digital and analog sections. In the latter case, the planes should be joined underneath the AD7690s.

The AD7690 voltage reference input REF has a dynamic input impedance and should be decoupled with minimal parasitic inductances. This is done by placing the reference decoupling ceramic capacitor close to, ideally right up against, the REF and GND pins and connecting them with wide, low impedance traces.

Finally, the AD7690 VDD and VIO power supplies should be decoupled with ceramic capacitors, typically 100 nF, placed close to the AD7690 and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of a layout following these rules is shown in Figure 46 and Figure 47.

EVALUATING THE AD7690 PERFORMANCE

Other recommended layouts for the AD7690 are outlined in the documentation of the evaluation board (EVAL-AD7690SDZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CB1Z.

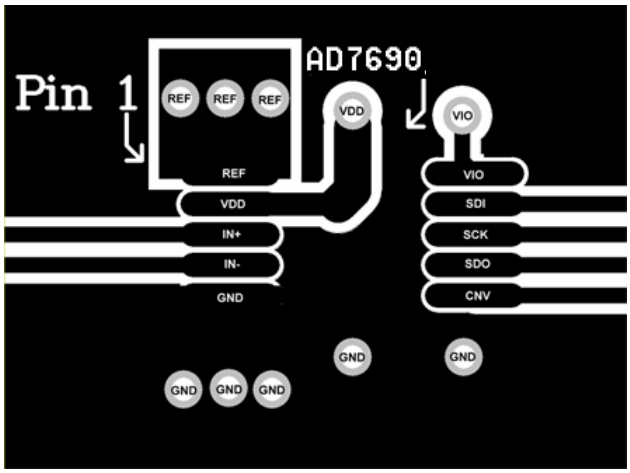


Figure 46. Example Layout of the AD7690 (Top Layer)

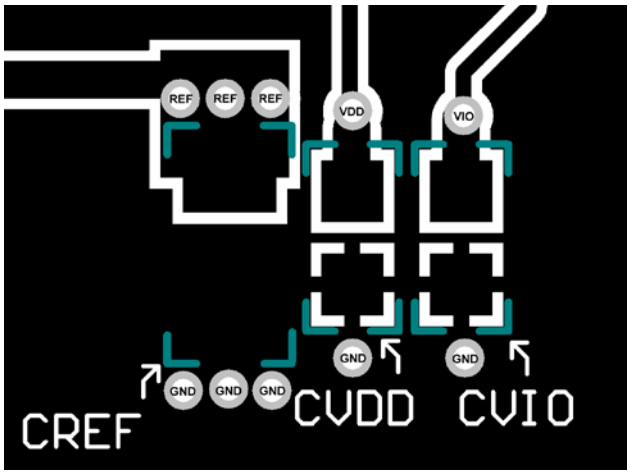


Figure 47. Example Layout of the AD7690 (Bottom Layer)

OUTLINE DIMENSIONS

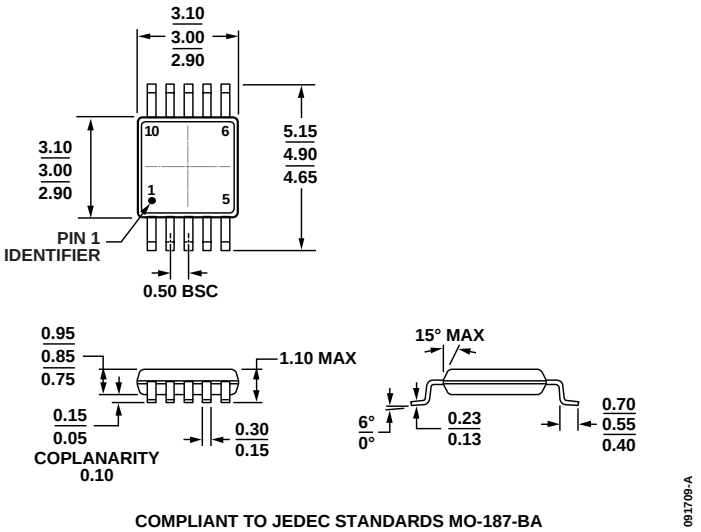


Figure 48.10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

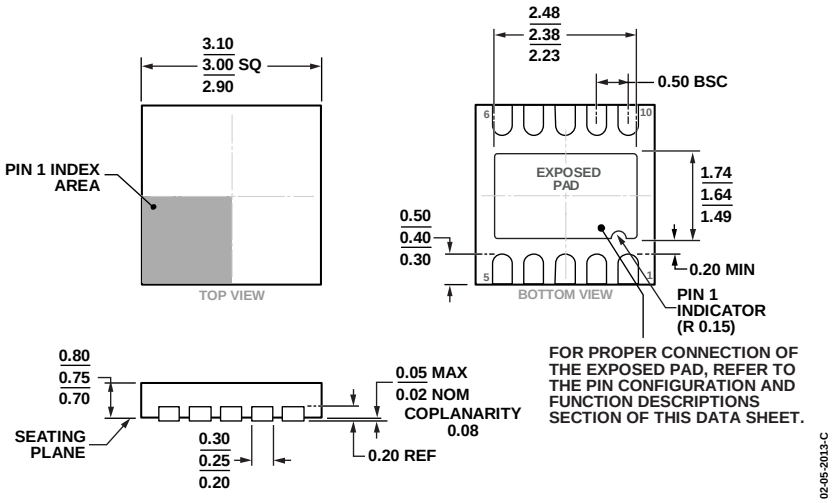


Figure 49. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Notes	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
AD7690BCPZRL		−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	C4C	Reel, 5,000
AD7690BCPZRL7		−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	C4C	Reel, 1,000
AD7690BRMZ		−40°C to +85°C	10-Lead MSOP	RM-10	C4C	Tube, 50
AD7690BRMZ-RL7		−40°C to +85°C	10-Lead MSOP	RM-10	C4C	Reel, 1,000
EVAL-AD7690SDZ			Evaluation Board			
EVAL-SDP-CB1Z			Controller Board			

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD7690SDZ board can be used as a standalone evaluation board or in conjunction with the EVAL-SDP-CB1Z for evaluation/demonstration purposes.
[3] The EVAL-SDP-CB1Z allows a PC to control and communicate with all Analog Devices evaluation boards ending in the SD designator.