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1/05—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; −40°C < T_A < +125°C; typical at +25°C; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
STATIC PERFORMANCE								
Resolution	14			14			Bits	
Relative Accuracy[1]			±16			±4	LSB	
Differential Nonlinearity[1]			±1			±1	LSB	Guaranteed monotonic by design
Zero-Code Error		0.5	10		0.5	10	mV	All 0s loaded to DAC register
Offset Error		±0.63	±10		±0.63	±10	mV	
Full-Scale Error		±0.5			±0.5		mV	All 1s loaded to DAC register
Gain Error		±0.004	±0.037		±0.004	±0.037	% of FSR	
Zero-Code Error Drift		5.0			5.0		µV/°C	
Gain Temperature Coefficient		2.0			2.0		ppm of FSR/°C	
OUTPUT CHARACTERISTICS[2]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Output Voltage Settling Time		6	10		6	10	µs	Code ¼ scale to ¾ scale, to ±1 LSB
Slew Rate		0.5			0.5		V/µs	
Capacitive Load Stability		470			470		pF	$R_L = \infty$
		1000			1000		pF	RL = 2 kΩ
Output Noise Spectral Density		120			120		nV/√Hz	DAC code = midscale, 1 kHz
Noise		2			2		µV	DAC code = midscale, 0.1 Hz to 10 Hz bandwidth
Digital-to-Analog Glitch Impulse		5			5		nV-s	1 LSB change around major carry
Digital Feedthrough		0.2			0.2		nV-s	
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		15			15		mA	V_{DD} = 3 V/5 V
LOGIC INPUTS								
Input Current[3]			±2			±2	µA	
V_{INL}, Input Low Voltage			0.8			0.8	V	V_{DD} = 4.5 V to 5.5 V
			0.6			0.6	V	V_{DD} = 2.7 V to 3.6 V
V_{INH}, Input High Voltage	1.8			1.8			V	V_{DD} = 4.5 V to 5.5 V
	1.4			1.4			V	V_{DD} = 2.7 V to 3.6 V
Pin Capacitance		3			3		pF	
POWER REQUIREMENTS								
V_{DD}	2.7		5.5	2.7		5.5	V	All digital inputs at 0 V or V_{DD}
I_{DD} (Normal Mode)								DAC active and excluding load current
V_{DD} = 4.5 V to 5.5 V		75	100		75	100	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		60	90		60	90	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
I_{DD} (All Power-Down Modes)								
V_{DD} = 4.5 V to 5.5 V		0.5			0.5		µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		0.2			0.2		µA	$V_{IH} = V_{DD}$ and V_{IL} = GND
POWER EFFICIENCY								
I_{OUT}/I_{DD}		96			96		%	I_{LOAD} = 2 mA and V_{DD} = ±5 V, full-scale loaded

[1] Linearity calculated using a reduced code range (Code 256 to Code 16,128).
[2] Guaranteed by design and characterization, not production tested.
[3] Total current flowing into all pins.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. See Figure 2.

Table 3.

Parameter	Limit[1]	Unit	Test Conditions/Comments
t_1[2]	33	ns min	SCLK cycle time
t_2	5	ns min	SCLK high time
t_3	5	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	4.5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	20	ns min	Minimum $\overline{SYNC}$ high time
t_9	13	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge ignored

[1] All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
[2] Maximum SCLK frequency is 30 MHz.

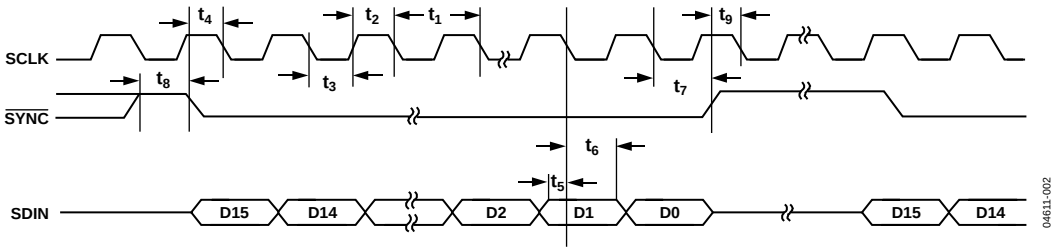

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +160°C
Maximum Junction Temperature	150°C
SC70 Package	
θ_{JA} Thermal Impedance	433.34°C/W
θ_{JC} Thermal Impedance	149.47°C/W
LFCSP Package	
θ_{JA} Thermal Impedance	95°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	20 sec to 40 sec
ESD	2.0 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

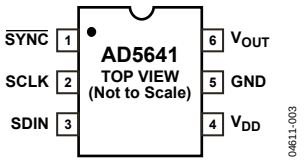

Figure 3. 6-Lead SC70 Pin Configuration

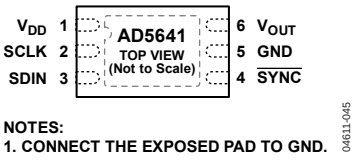

Figure 4. 6-Lead LFCSP Pin Configuration

Table 5. Pin Function Descriptions

SC70 Pin No.	LFCSP Pin No.	Mnemonic	Description
1	4	$\overline{\text{SYNC}}$	Level-Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the clocks that follow. The DAC is updated following the 16th clock cycle unless $\overline{\text{SYNC}}$ is taken high before this edge, in which case the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the DAC.
2	2	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
3	3	SDIN	Serial Data Input. This device has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
4	1	V_{DD}	Power Supply Input. The AD5641 can be operated from 2.7 V to 5.5 V. V_{DD} should be decoupled to GND.
5	5	GND	Ground Reference Point for All Circuitry on the AD5641.
6	6	V_{OUT}	Analog Output Voltage from the DAC. The output amplifier has rail-to-rail operation.
		EP	Exposed Pad. Connect to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

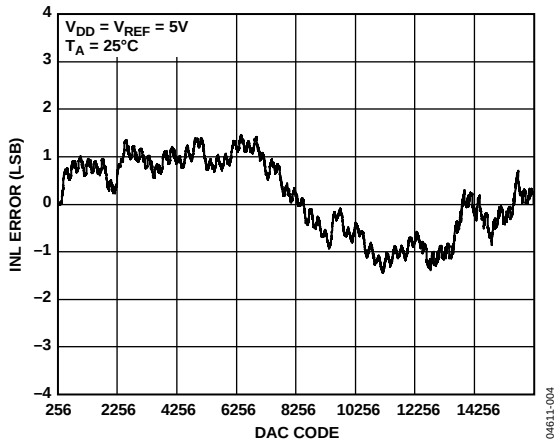

Figure 5. Typical INL

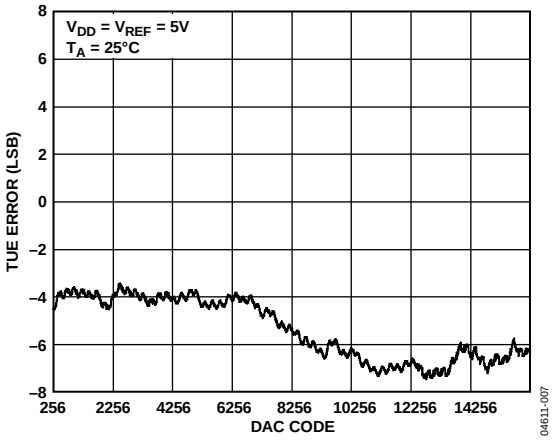

Figure 8. Typical Total Unadjusted Error (TUE)

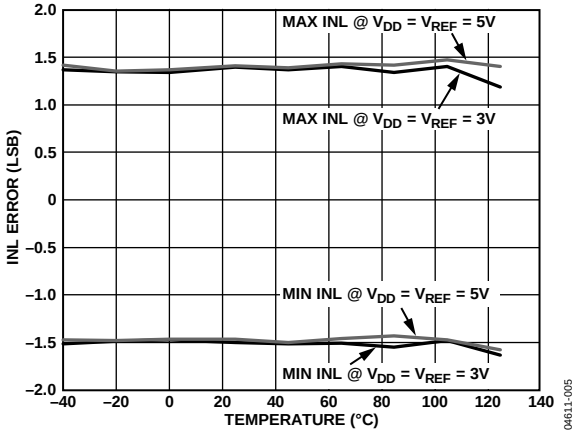

Figure 6. INL Error vs. Temperature (3 V/5 V Supply)

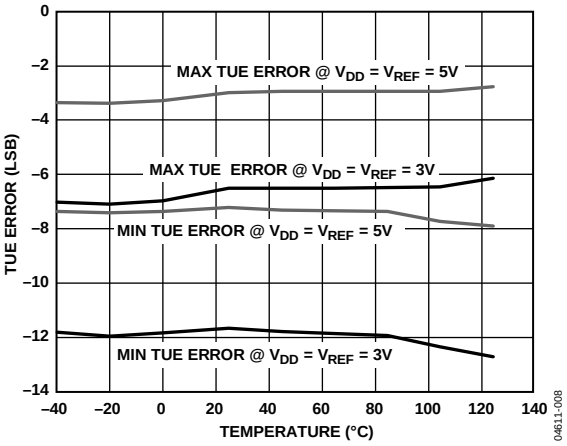

Figure 9. Total Unadjusted Error (TUE) vs. Temperature (3 V/5 V Supply)

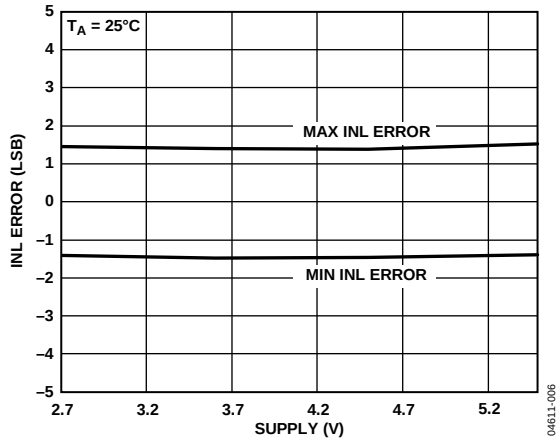

Figure 7. INL Error vs. Supply at 25°C

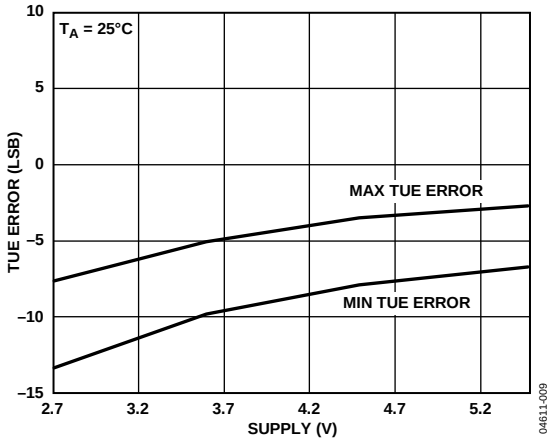

Figure 10. Total Unadjusted Error (TUE) vs. Supply at 25°C

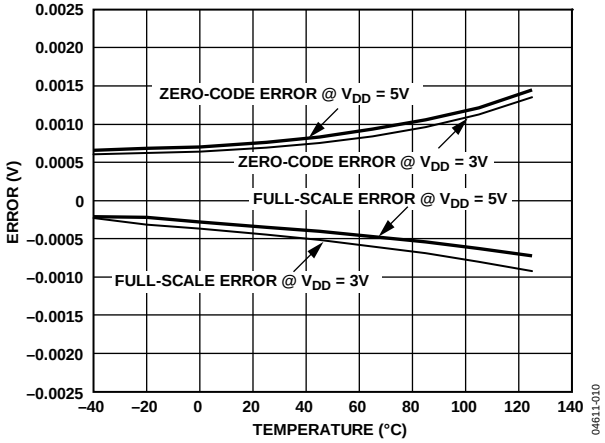

Figure 11. Zero-Code/Full-Scale Error vs. Temperature (3 V/5 V)

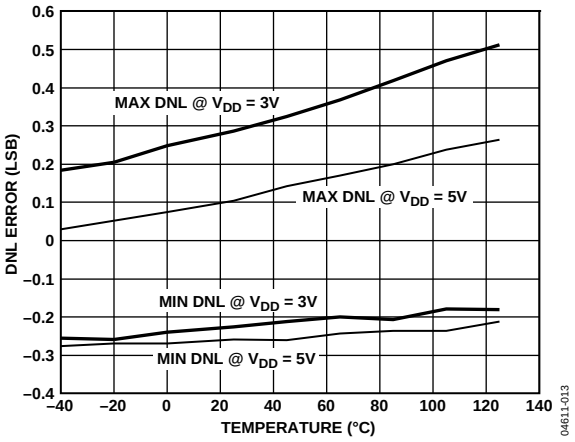

Figure 14. DNL Error vs. Temperature (3 V/5 V)

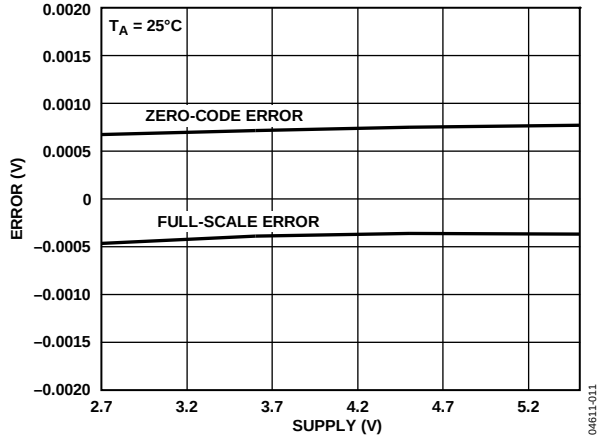

Figure 12. Zero-Code/Full-Scale Error vs. Supply at 25°C

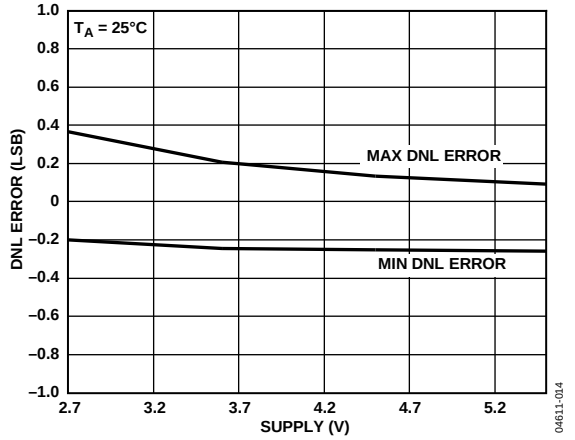

Figure 15. DNL Error vs. Supply at 25°C

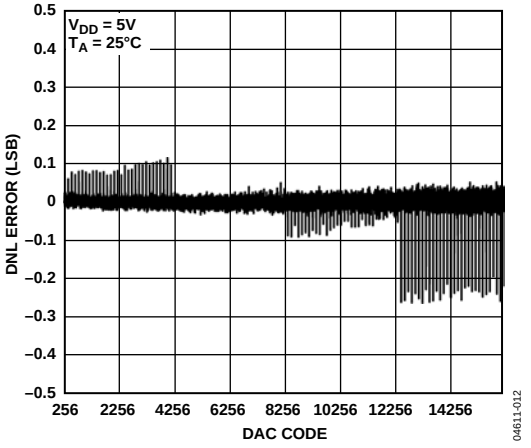

Figure 13. Typical DNL

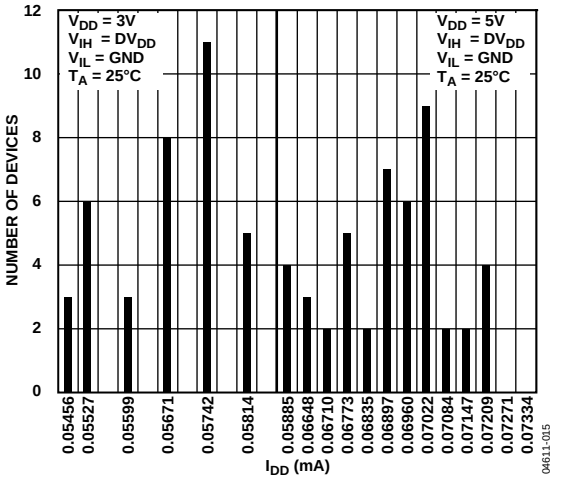

Figure 16. I_{DD} Histogram (3 V/5 V)

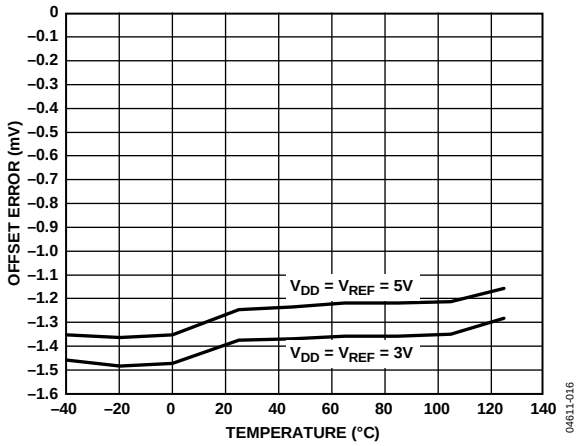

Figure 17. Offset Error vs. Temperature (3 V/5 V Supply)

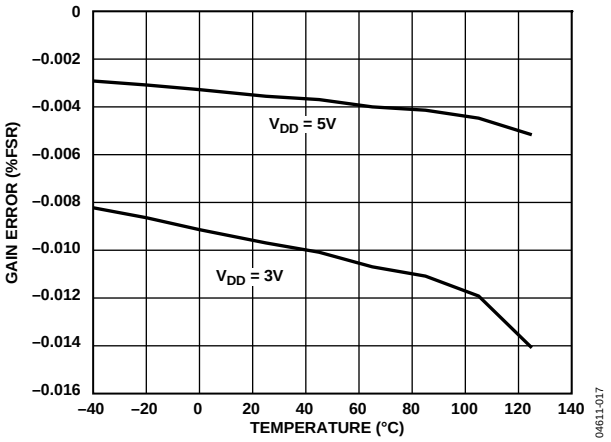

Figure 18. Gain Error vs. Temperature (3 V/5 V)

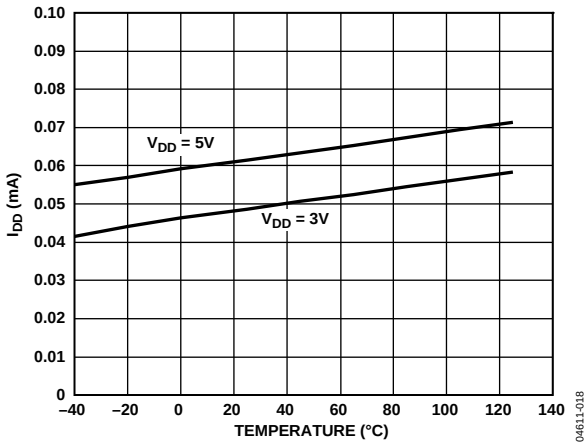

Figure 19. Supply Current vs. Temperature (3 V/5 V Supply)

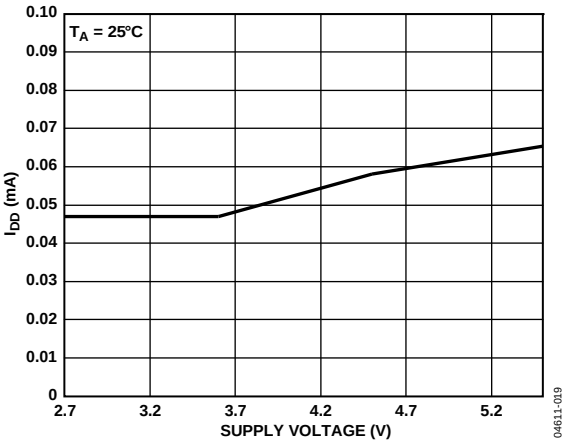

Figure 20. Supply Current vs. Supply Voltage at 25°C

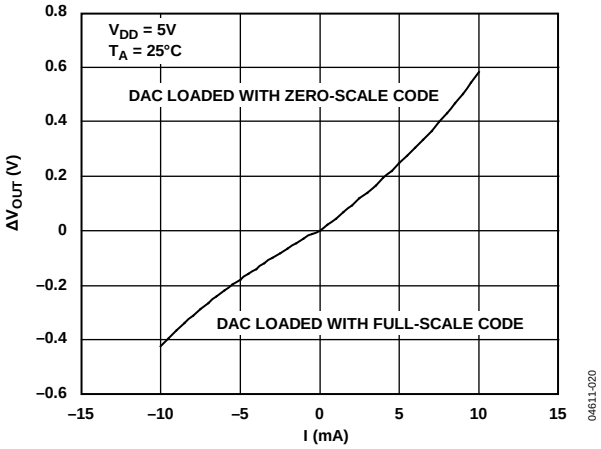

Figure 21. Sink and Source Capability

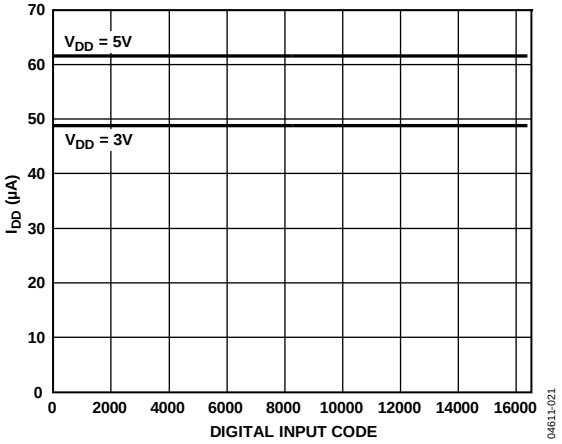

Figure 22. Supply Current vs. Digital Input Code

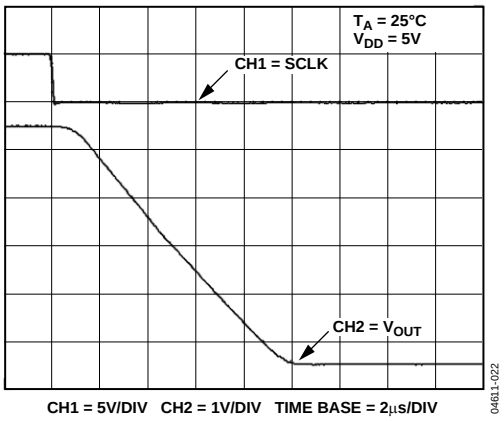

Figure 23. Full-Scale Settling Time

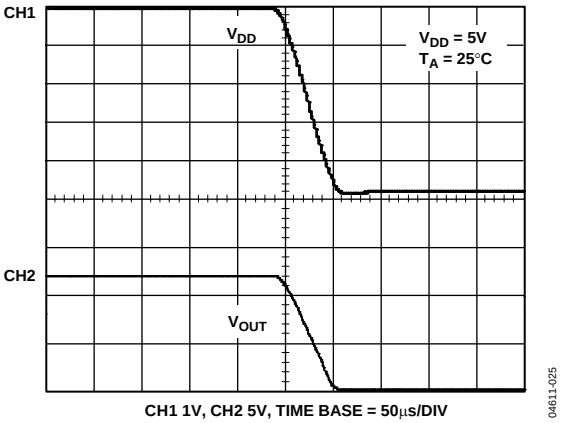

Figure 26. V_{DD} vs. V_{OUT}

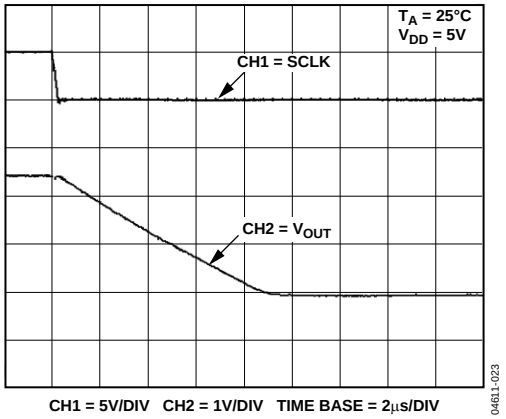

Figure 24. Midscale Settling Time

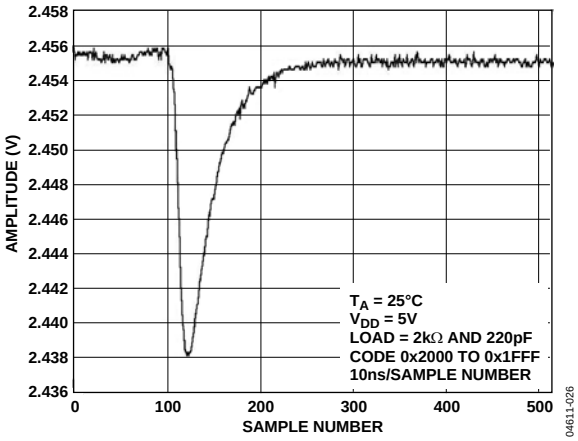

Figure 27. Digital-to-Analog Glitch Energy

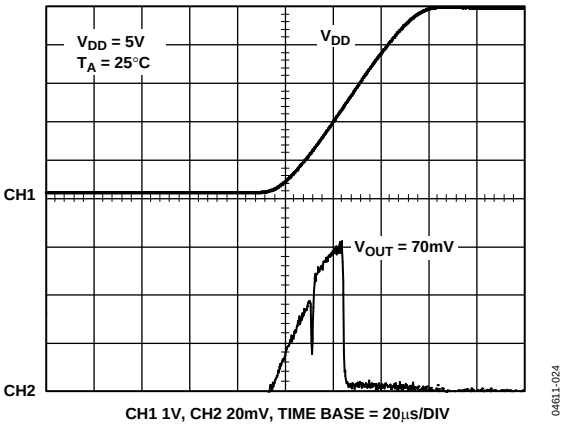

Figure 25. Power-On Reset to 0 V

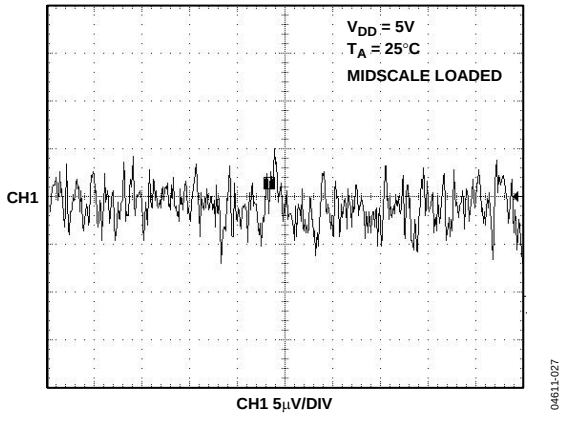

Figure 28. 1/f Noise, 0.1 Hz to 10 Hz Bandwidth

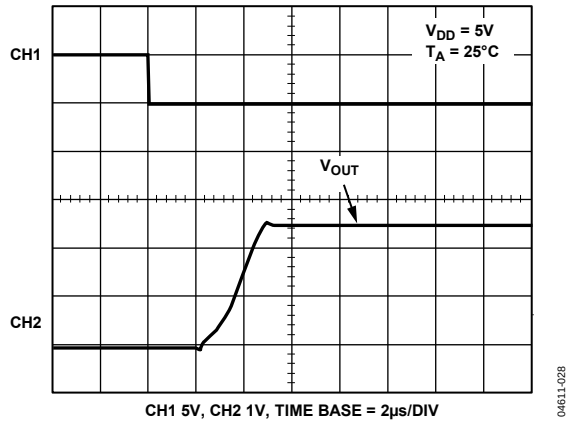

Figure 29. Exiting Power-Down Mode

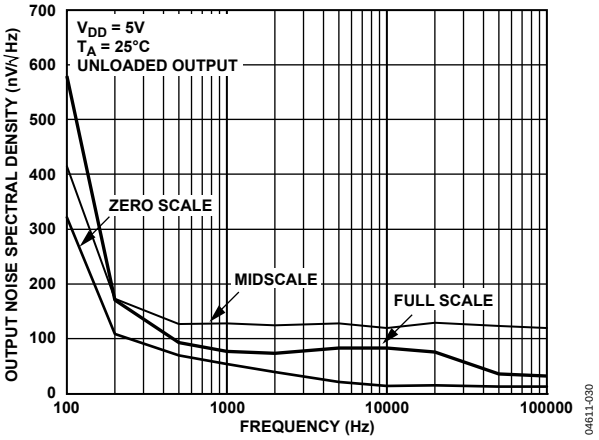

Figure 31. Noise Spectral Density

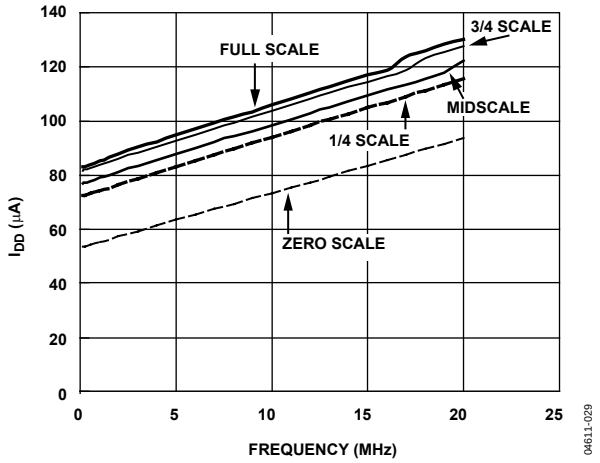

Figure 30. I_{DD} vs. SCLK vs. Code

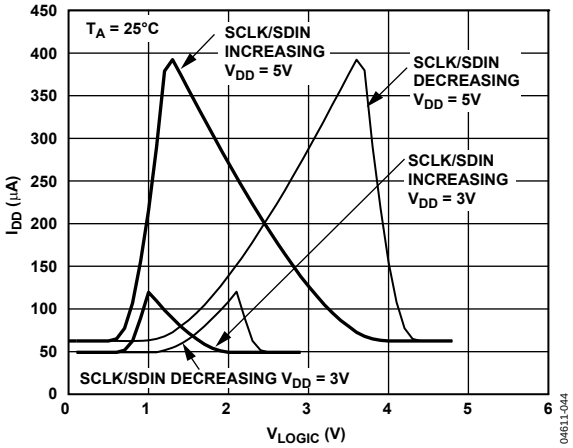

Figure 32. SCLK/SDIN vs. Logic Voltage

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. See Figure 5 for a plot of typical INL vs. code.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. See Figure 13 for a plot of typical DNL vs. code.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5641 because the output of the DAC cannot go below 0 V. Zero-code error is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mV. See Figure 11 for a plot of zero-code error vs. temperature.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output should be V_{DD} − 1 LSB. Full-scale error is expressed in mV. See Figure 11 for a plot of full-scale error vs. temperature.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal, expressed as a percent of the full-scale range.

Total Unadjusted Error (TUE)
Total unadjusted error is a measure of the output error taking the various errors into account. See Figure 8 for a plot of typical TUE vs. code.

Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x2000 to 0x1FFF). See Figure 27.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and is measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

THEORY OF OPERATION

DIGITAL-TO-ANALOG SECTION

The AD5641 DAC is fabricated on a CMOS process. The architecture consists of a string DAC followed by an output buffer amplifier. Figure 33 is a block diagram of the DAC architecture.

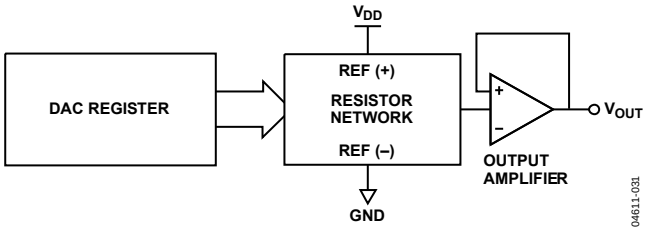

Figure 33. DAC Architecture

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{DD} \times \left(\frac{D}{16{,}384} \right)$$

where *D* is the decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 16,384.

RESISTOR STRING

The resistor string structure is shown in Figure 34. It is simply a string of resistors, each of value R. The code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

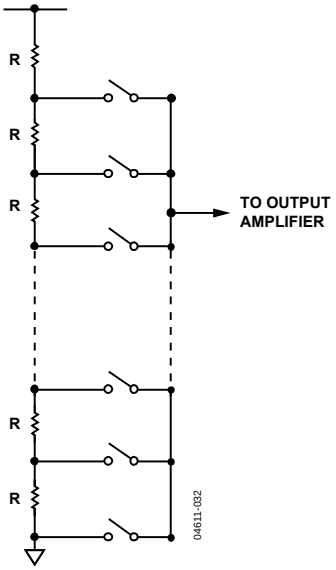

Figure 34. Resistor String Structure

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 21. The slew rate is 0.5 V/μs, with a midscale settling time of 8 μs with the output loaded.

SERIAL INTERFACE

The AD5641 has a 3-wire serial interface ($\overline{\text{SYNC}}$, SCLK, and SDIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{\text{SYNC}}$ line low. Data from the SDIN line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making the AD5641 compatible with high speed DSPs. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (a change in DAC register contents and/or a change in the mode of operation). At this stage, the $\overline{\text{SYNC}}$ line can be kept low or brought high. In either case, it must be brought high for a minimum of 20 ns before the next write sequence, so that a falling edge of $\overline{\text{SYNC}}$ can initiate the next write sequence.

Because the $\overline{\text{SYNC}}$ buffer draws more current when V_{IN} = 1.8 V than it does when V_{IN} = 0.8 V, $\overline{\text{SYNC}}$ should be idled low between write sequences for even lower power operation of the part, as previously mentioned. However, it must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide (see Figure 35). The first two bits are control bits, which determine the operating mode of the part (normal mode or any one of three power-down modes). For a complete description of the various modes, see the Power-Down Modes section. The next 14 bits are the data bits, which are transferred to the DAC register on the 16th falling edge of SCLK.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 36).

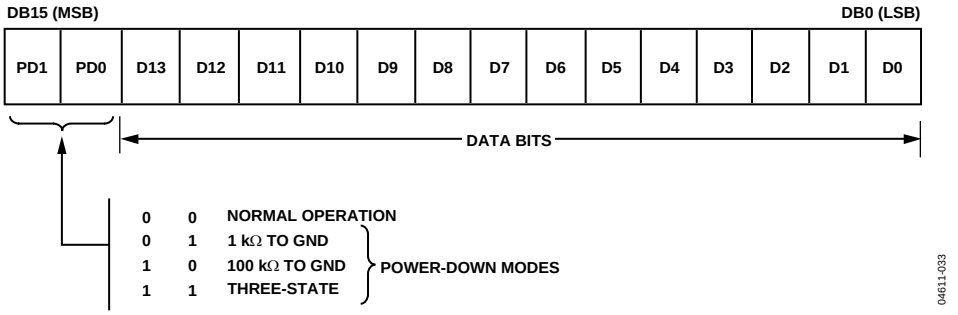

Figure 35. Input Register Contents

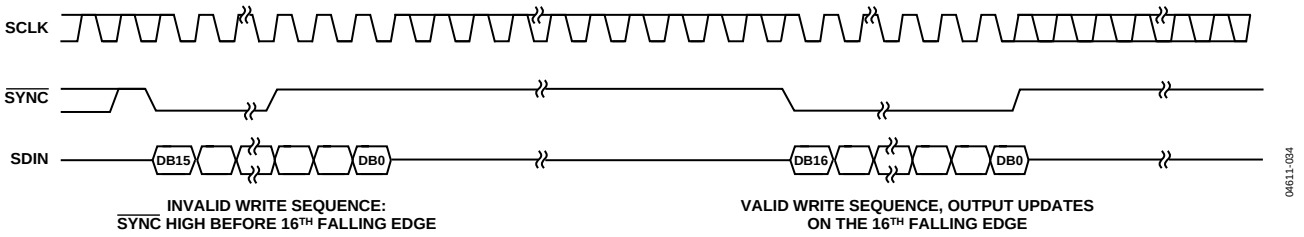

Figure 36. $\overline{SYNC}$ Interrupt Facility

POWER-ON RESET

The AD5641 contains a power-on reset circuit that controls the output voltage during power-up. The DAC register is filled with 0s and the output voltage is 0 V. It remains there until a valid write sequence is made to the DAC. This is useful in applications in which it is important to know the state of the DAC output while it is in the process of powering up.

POWER-DOWN MODES

The AD5641 has four separate modes of operation. These modes are software programmable by setting two bits (DB15 and DB14) in the control register. Table 6 shows how the state of the bits corresponds to the operating mode of the device.

Table 6. Operating Modes for the AD5641

DB15	DB14	Operating Mode
0	0	Normal operation
		Power-down mode:
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

When both bits are set to 0, the part has normal power consumption of 100 μA maximum at 5 V. However, for the three power-down modes, the supply current falls to typically 0.2 μA at 3 V.

Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options: the output is connected internally to GND through either a 1 kΩ resistor or a 100 kΩ resistor, or the output is left open-circuited (three-stated). Figure 37 shows the output stage.

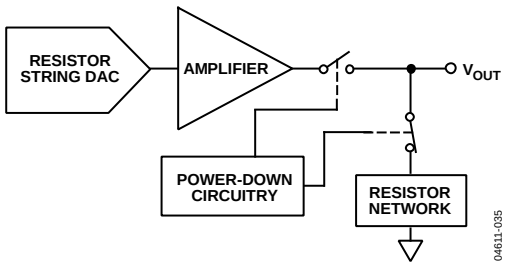

Figure 37. Output Stage During Power-Down

The bias generator, output amplifier, resistor string, and other associated linear circuitry are all shut down when power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 13 μs for V_{DD} = 5 V and 16 μs for V_{DD} = 3 V. See Figure 29 for a plot.

MICROPROCESSOR INTERFACING

AD5641 to ADSP-2101 Interface

Figure 38 shows a serial interface between the AD5641 and the ADSP-2101. The ADSP-2101 should be set up to operate in SPORT transmit alternate framing mode. The ADSP-2101 SPORT is programmed through the SPORT control register and should be configured as follows: internal clock operation, active low framing, and 16-bit word length. Transmission is initiated by writing a word to the Tx register after the SPORT is enabled.

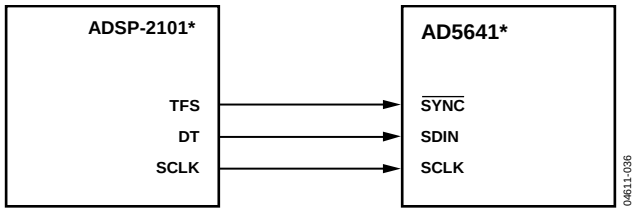

Figure 38. AD5641 to ADSP-2101 Interface

AD5641 to 68HC11/68L11 Interface

Figure 39 shows a serial interface between the AD5641 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5641, while the MOSI output drives the serial data line of the DAC. The SYNC signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: the 68HC11/68L11 should be configured so that the CPOL bit is 0 and the CPHA bit is 1. When data is being transmitted to the DAC, the SYNC line is taken low (PC7). When the 68HC11/68L11 are configured as previously described, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5641, PC7 is left low after the first eight bits are transferred and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

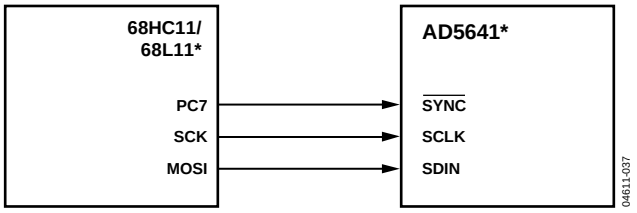

Figure 39. AD5641 to 68HC11/68L11 Interface

AD5641 to Blackfin® ADSP-BF53x Interface

Figure 40 shows a serial interface between the AD5641 and the Blackfin ADSP-BF53x microprocessor. The ADSP-BF53x processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5641, the setup for the interface is as follows: DT0PRI drives the SDIN pin of the AD5641, while TSCLK0 drives the SCLK of the part. The SYNC is driven from TFS0.

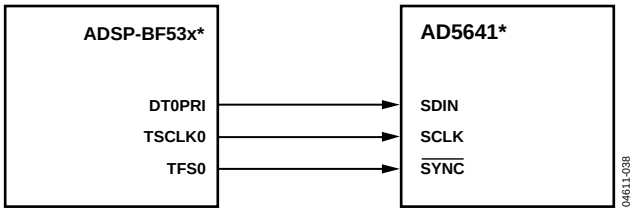

Figure 40. AD5641 to Blackfin ADSP-BF53x Interface

AD5641 to 80C51/80L51 Interface

Figure 41 shows a serial interface between the AD5641 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/80L51 drives SCLK of the AD5641, while RxD drives the serial data line of the part. The SYNC signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5641, P3.3 is taken low.

The 80C51/80L51 transmits data only in 8-bit bytes; therefore, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data LSB first. The AD5641 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine should take this into account.

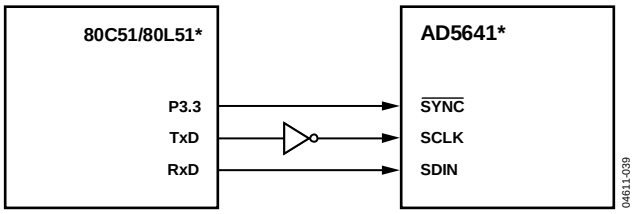

Figure 41. AD5641 to 80C51/80L51 Interface

AD5641 to MICROWIRE Interface

Figure 42 shows an interface between the AD5641 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5641 on the rising edge of SK.

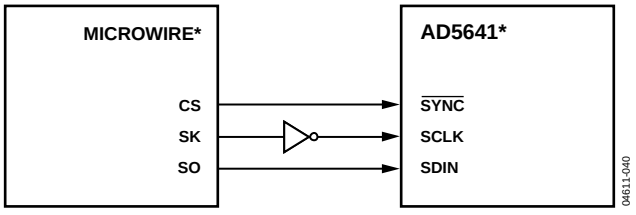

Figure 42. AD5641 to MICROWIRE Interface

APPLICATIONS

CHOOSING A REFERENCE AS POWER SUPPLY FOR THE AD5641

The AD5641 comes in tiny LFCSP and SC70 packages with less than 100 µA supply current. Because of this, the choice of reference depends on the application requirement. For space-saving applications, the ADR02 is available in an SC70 package and has excellent drift at 9 ppm/°C (3 ppm/°C in the R-8 package). It also provides very good noise performance at 3.4 µV p-p in the 0.1 Hz to 10 Hz range.

Because the supply current required by the AD5641 is extremely low, the parts are ideal for low supply applications. The ADR395 voltage reference is recommended in this case. It requires less than 100 µA of quiescent current and can, therefore, drive multiple DACs in one system, if required. It also provides very good noise performance at 8 µV p-p in the 0.1 Hz to 10 Hz range.

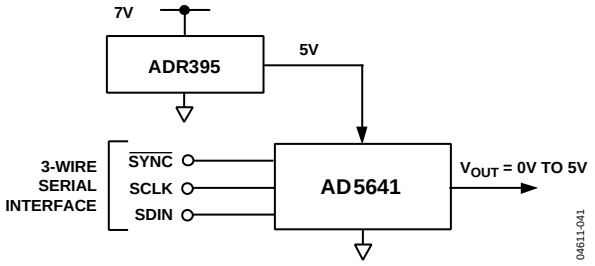

Figure 43. ADR395 as Power Supply to AD5641

Table 7 lists some recommended precision references for use as supplies to the AD5641.

Table 7. Precision References for Use with AD5641

Part No.	Initial Accuracy (mV max)	Temperature Drift (ppm/°C max)	0.1 Hz to 10 Hz Noise (µV p-p typ)
ADR435	±2	3 (R-8)	8
ADR425	±2	3 (R-8)	3.4
ADR02	±3	3 (R-8)	10
ADR02	±3	3 (SC70)	10
ADR395	±5	9 (TSOT-23)	8

BIPOLAR OPERATION USING THE AD5641

The AD5641 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 44. The circuit in Figure 44 gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

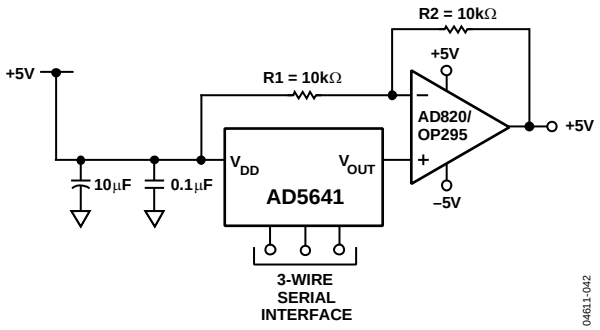

Figure 44. Bipolar Operation with the AD5641

The output voltage for any input code can be calculated as

$$V_{OUT} = \left[V_{DD} \times \left(\frac{D}{16{,}384} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 – 16384).

With V_{DD} = 5 V, R1 = R2 = 10 kΩ,

$$V_{OUT} = \left(\frac{10 \times D}{16{,}384} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V with 0x0000 corresponding to a –5 V output, and 0x3FFF corresponding to a +5 V output.

USING THE AD5641 WITH A GALVANICALLY ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur in the area where the DAC is functioning. *i*Coupler® provides isolation in excess of 2.5 kV. The AD5641 use a 3-wire serial logic interface, so the ADuM1300 three-channel digital isolator provides the required isolation (see Figure 45). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5641.

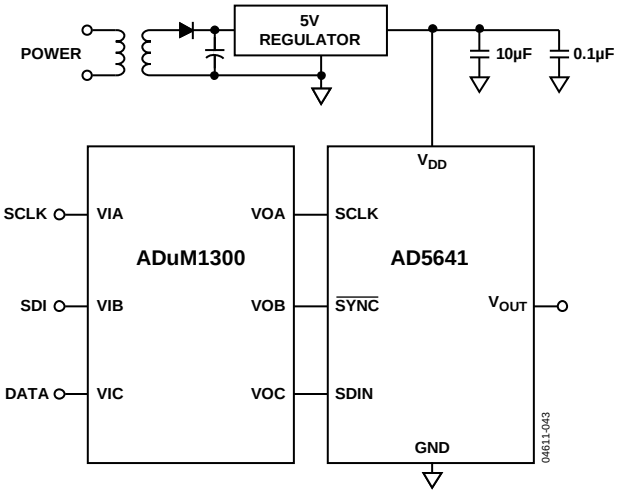

Figure 45. AD5641 with a Galvanically Isolated Interface

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5641 should have separate analog and digital sections, each having its own area of the board. If the AD5641 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5641.

The power supply to the AD5641 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be physically as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), such as in common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects on the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

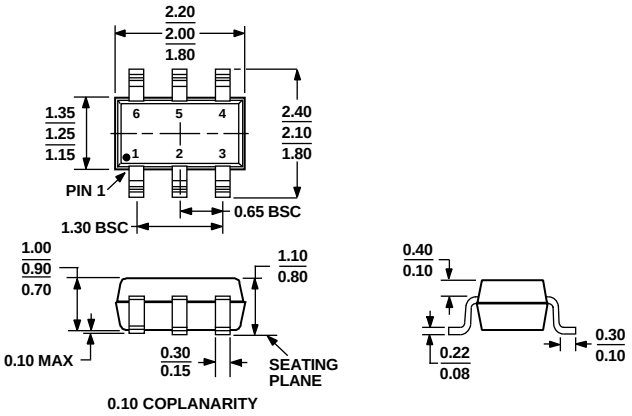

Figure 46. 6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)
Dimensions shown in millimeters

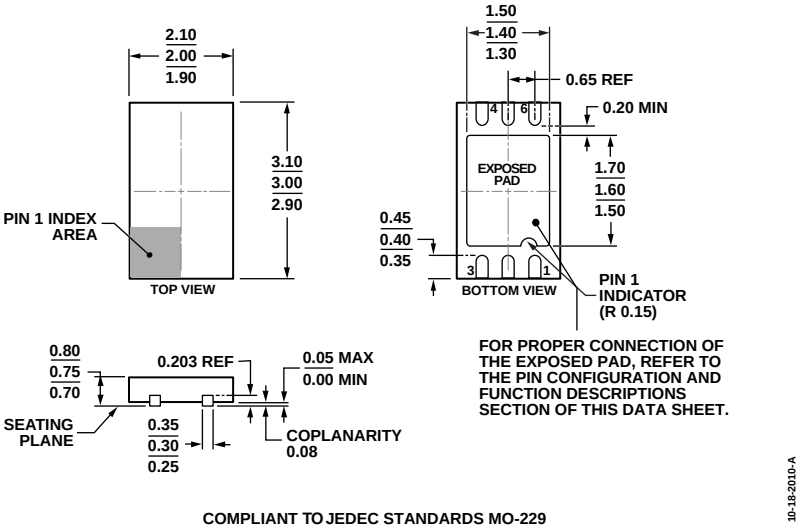

Figure 47. 6-Lead Lead Frame Chip Scale Package [LFCSP_WD]
2.00 × 3.00 mm Body, Very Very Thin, Dual Lead
(CP-6-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Description	Package Description	Package Option	Branding
AD5641AKSZ-REEL7	−40°C to +125°C	±16 LSB INL	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3Q
AD5641AKSZ-500RL7	−40°C to +125°C	±16 LSB INL	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3Q
AD5641ACPZ-REEL7	−40°C to +125°C	±16 LSB INL	6-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-6-5	8A
AD5641BKSZ-REEL7	−40°C to +125°C	±4 LSB INL	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3P
AD5641BKSZ-500RL7	−40°C to +125°C	±4 LSB INL	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	D3P

[1] Z = RoHS Compliant Part.

NOTES