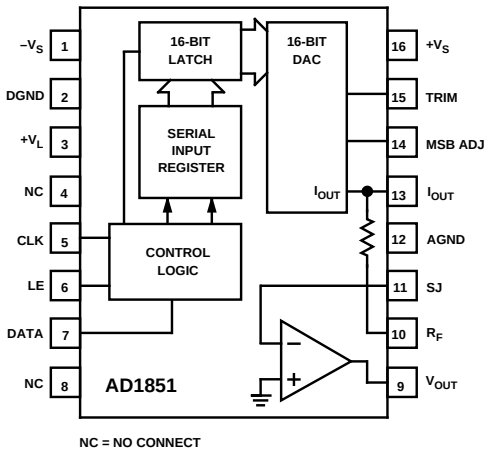
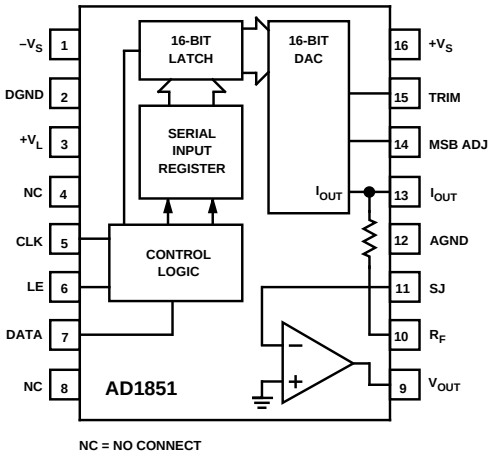
AD1851/AD1861–SPECIFICATIONS (T_A @ +25°C and ±5 V supplies, unless otherwise noted)

	Min	Typ	Max	Units
DIGITAL INPUTS				
V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = V_L$			**1.0**	µA
I_{IL}, $V_{IL} = 0.4$			**–10**	µA
ACCURACY				
Gain Error		±1		%
Midscale Output Voltage		±10		mV
DRIFT (0°C to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (To ±0.0015% of FSR)				
Voltage Output				
6 V Step		1.5		µs
1 LSB Step		1.0		µs
Slew Rate		9		V/µs
Current Output				
1 mA Step 10 Ω to 100 Ω Load		350		ns
1 kΩ Load		350		ns
OUTPUT				
Voltage Output Configuration				
Bipolar Range	**±2.88**	±3.0	**±3.12**	V
Output Current	±8			mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage				
$+V_L$ and $+V_S$	4.75		5.25	V
$–V_S$	–5.25		–4.75	V
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	–25		+70	°C
Storage	–60		+100	°C
WARM-UP TIME	1			min

Specifications subject to change without notice.



AD1851 Functional Block Diagram



AD1861 Functional Block Diagram

AD1851

	Min	Typ	Max	Units
RESOLUTION			16	Bits
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz				
AD1851N-J, R-J		0.003	**0.004**	%
AD1851N, R		0.004	**0.008**	%
–20 dB, 990.5 Hz				
AD1851N-J, R-J		0.009	**0.016**	%
AD1851N, R		0.009	**0.040**	%
–60 dB, 990.5 Hz				
AD1851N-J, R-J		0.9	**1.6**	%
AD1851N, R		0.9	**4.0**	%
D-RANGE* (With A-Weight Filter)				
–60 dB, 990.5 Hz AD1851N, R	**88**			dB
AD1851N-J, R-J	**96**			dB
SIGNAL-TO-NOISE RATIO	**107**	110		dB
MAXIMUM CLOCK INPUT FREQUENCY	**12.5**			MHz
ACCURACY				
Differential Linearity Error		±0.001		% of FSR
MONOTONICITY		14		Bits
POWER SUPPLY				
Current				
+I		10.0	**13.0**	mA
–I		–10.0	**–15.0**	mA
Power Dissipation		100		mW

AD1861

	Min	Typ	Max	Units
RESOLUTION			**18**	Bits
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz				
AD1861N-J, R-J		0.003	**0.004**	%
AD1861N, R		0.004	**0.008**	%
–20 dB, 990.5 Hz				
AD1861N-J, R-J		0.009	**0.016**	%
AD1861N, R		0.009	**0.040**	%
–60 dB, 990.5 Hz				
AD1861N-J, R-J		0.9	**1.6**	%
AD1861N, R		0.9	**4.0**	%
D-RANGE* (With A-Weight Filter)				
–60 dB, 990.5 Hz AD1861N, R	**88**			dB
AD1861N-J, R-J	**96**			dB
SIGNAL-TO-NOISE RATIO	**107**	110		dB
MAXIMUM CLOCK INPUT FREQUENCY	**13.5**			MHz
ACCURACY				
Differential Linearity Error		±0.001		% of FSR
MONOTONICITY		15		Bits
POWER SUPPLY				
Current				
+I		10.0	**13.0**	mA
–I		–10.0	**–15.0**	mA
Power Dissipation		100		mW

*Tested in accordance with EIAJ Test Standard CP-307.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND ..... 0 V to 6.50 V
V_S to AGND ..... 0 V to 6.50 V
$-V_S$ to AGND ..... –6.50 V to 0 V
Digital Inputs to DGND ..... –0.3 V to V_L
AGND to DGND ..... ±0.3 V
Short Circuit ..... Indefinite Short to Ground
Soldering ..... +300°C, 10 sec
Storage Temperature ..... –60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Resolution	THD + N	Package Option*
AD1851N	16 Bits	0.008%	N-16
AD1851N-J	16 Bits	0.004%	N-16
AD1851R	16 Bits	0.008%	R-16
AD1851R-J	16 Bits	0.004%	R-16
AD1861N	18 Bits	0.008%	N-16
AD1861N-J	18 Bits	0.004%	N-16
AD1861R	18 Bits	0.008%	R-16
AD1861R-J	18 Bits	0.004%	R-16

*N = Plastic DIP Package; R = Small Outline (SOIC) Package.

PIN DESCRIPTIONS

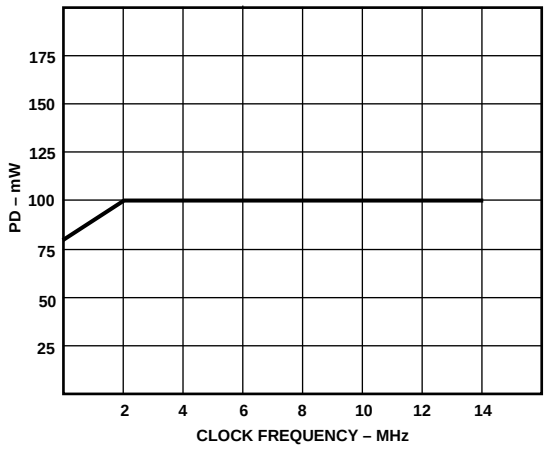
1	$-V_S$	Analog Negative Power Supply
2	DGND	Logic Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	NC	No Internal Connection*
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

*Pin 8 has no internal connection; $-V_L$ from AD1856 or AD1860 socket can be safely applied.

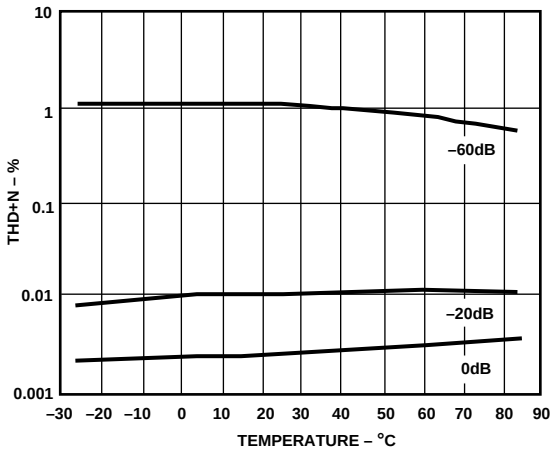
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

Typical Performance



Power Dissipation vs. Clock Frequency



THD vs. Temperature

TOTAL HARMONIC DISTORTION
Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the first 19 harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small signal amplitudes (–20 dB and –60 dB).

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. This specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

SETTLING TIME
Settling time is the time required for the output of the DAC to reach and remain within a specified error band about its final value, measured from the digital input transition. It is a primary measure of dynamic performance.

MIDSCALE ERROR
Midscale error, or bipolar zero error, is the deviation of the actual analog output from the ideal output (0 V) when the 2s complement input code representing half scale is loaded in the input register.

D-RANGE DISTORTION
D-range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of –60 dB below full scale is reproduced. D-range is tested with a 1 kHz input sine wave. This is measured with a standard A-weight filter as specified by EIAJ Standard CP-307.

SIGNAL-TO-NOISE RATIO
The signal-to-noise ratio (SNR) is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. This is measured with a standard A-weight filter as specified by EIAJ Standard CP-307.

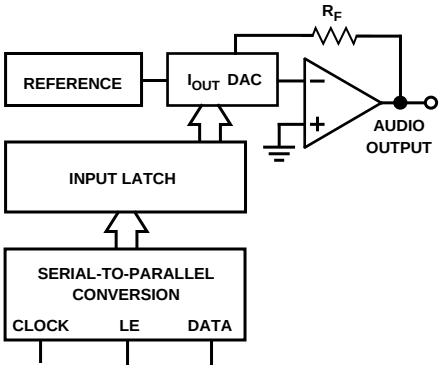


Figure 1. AD1851/AD1861 Functional Block Diagram

FUNCTIONAL DESCRIPTION
The AD1851/AD1861 is a complete monolithic PCM audio DAC. No additional external components are required for operation. As shown in Figure 1 above, each chip contains a voltage reference, an output amplifier, a DAC, an input latch and a parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This combination of elements produces a reference voltage that is unaffected by changes in temperature and age. The DAC output voltage, which is derived from the reference voltage, is also unaffected by these environmental changes.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew rate and optimum settling time. When combined with the on-chip feedback resistor, the output op amp converts the output current of the AD1851/AD1861 to a voltage output.

The DAC uses a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser-trimming of these resistors further reduces linearity error, resulting in low output distortion.

The input register and serial-to-parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. This contributes to the overall low power dissipation of the AD1851/AD1861.

Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1851/AD1861 has two ground pins, designated Analog and Digital ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1851/AD1861 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 2, the analog and digital grounds should be connected together at one point in the system.

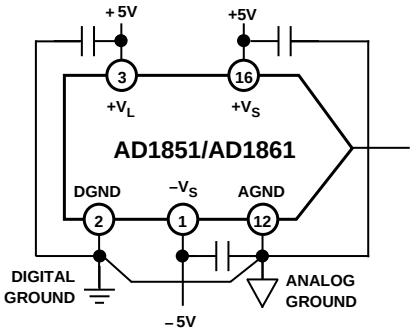


Figure 2. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1851/AD1861 has three power supply input pins. The $\pm V_S$ supplies provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate at ±5 V.

The $+V_L$ supply operates the digital portions of the chip including the input shift register and the input latching circuitry. The $+V_L$ supply is designed to operate at +5 V.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as to the common points. The logic supply, $+V_L$, should be decoupled to digital common, while the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of three separate power supplies will reduce feedthrough from the digital portion of the system to the linear portion of the system, thus contributing to improved performance.

However, three separate voltage supplies are not necessary for good circuit performance. For example, Figure 3 illustrates a system where only a single positive and a single negative supply are available.

In this example, the positive logic and positive analog supplies must both be connected to +5 V, while the negative analog supply will be connected to –5 V. Performance would benefit from a measure of isolation between the supplies introduced by using simple low pass filters in the individual power supply leads.

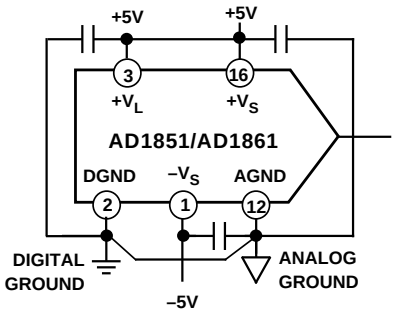


Figure 3. Alternate Recommended Schematic

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using the AD1851/AD1861.

OPTIONAL MSB ADJUSTMENT

Use of an optional adjustment circuit allows residual differential linearity error around midscale to be eliminated. This error is especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases, thereby increasing THD.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 4 may be used to improve performance. The adjustment should be made with a small signal input (–20 dB or –60 dB).

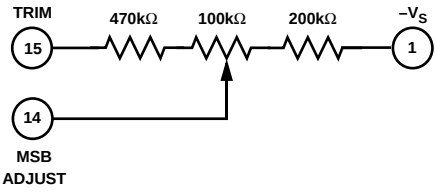


Figure 4. Optional THD Adjust Circuit

AD1851 DIGITAL CIRCUIT CONSIDERATIONS

AD1851 Input Data

Data is transmitted to the AD1851 in a bit stream composed of 16-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable (LE) signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 16th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 5 illustrates the general signal requirements for data transfer to the AD1851.

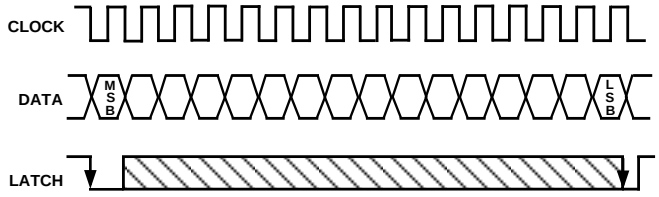


Figure 5. Signal Requirements for AD1851

Figure 6 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1851 are both TTL and 5 V CMOS compatible. The input requirements illustrated in Figures 5 and 6 are compatible with data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1851 input clock can run at a 12.5 MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× or 16× oversampling reconstructions.

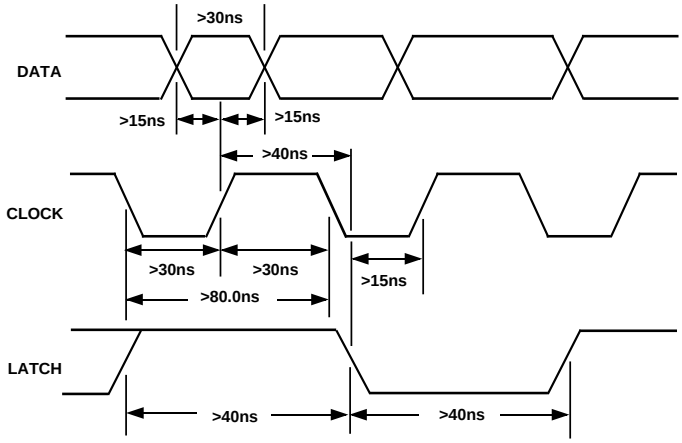


Figure 6. Timing Relationships of AD1851 Input Signals

AD1861 DIGITAL CIRCUIT CONSIDERATIONS

AD1861 Input Data

Data is transmitted to the AD1861 in a bit stream composed of 18-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable (LE) signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 18th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 7 illustrates the general signal requirements for data transfer to the AD1861.

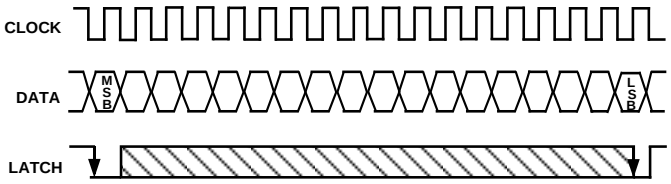


Figure 7. Signal Requirements for AD1861

Figure 8 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1861 are both TTL and 5 V CMOS compatible. The input requirements illustrated in Figures 7 and 8 are compatible with data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1861 input clock can run at a 13.5 MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× or 16× oversampling reconstructions.

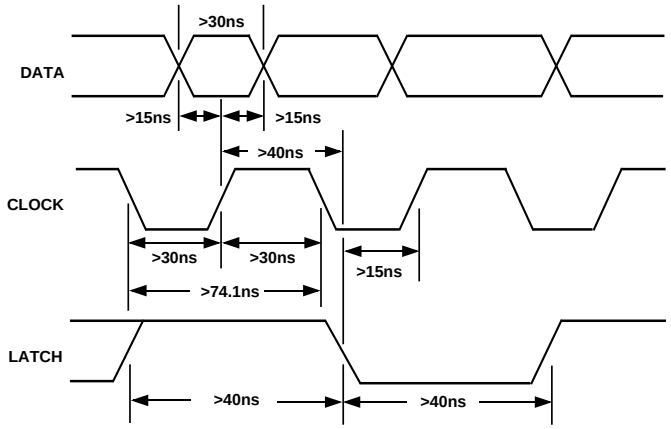


Figure 8. Timing Relationships of AD1861 Input Signals

APPLICATIONS

Figures 9 through 12 show connection diagrams for the AD1851 and AD1861 and the Yamaha YM3434 and the NPC SM5813AP/APT digital filter chips.

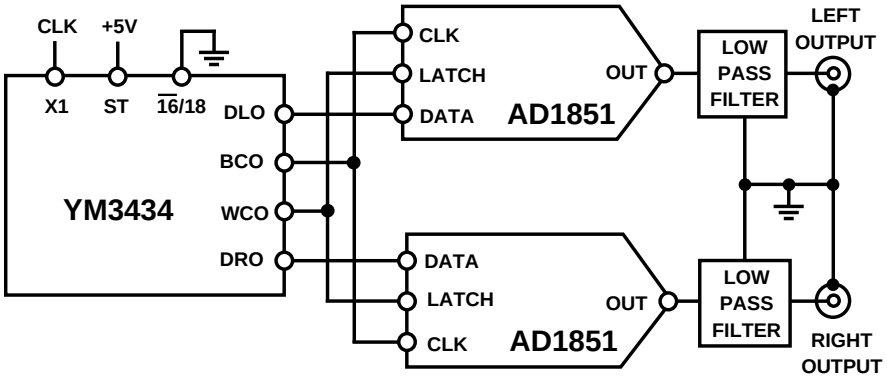


Figure 9. AD1851 with Yamaha YM3434 Digital Filter

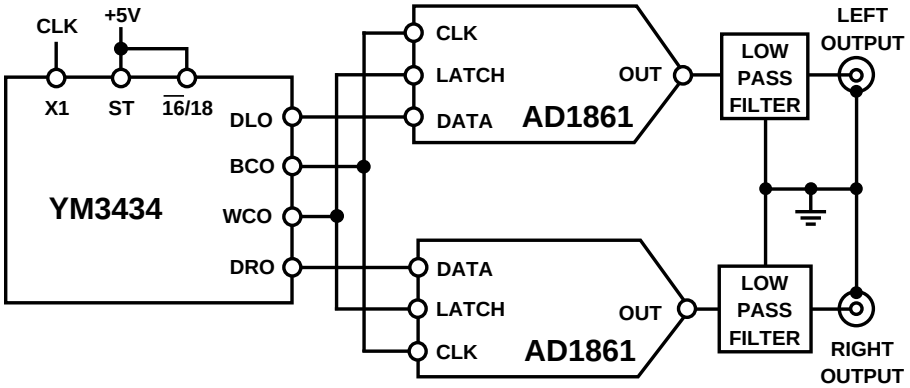


Figure 10. AD1861 with Yamaha YM3434 Digital Filter

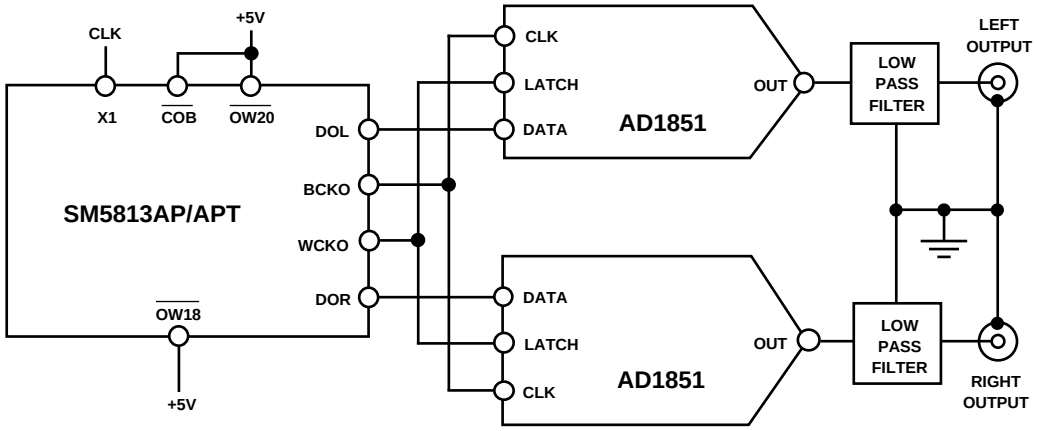


Figure 11. AD1851 with NPC SM5813AP/APT Digital Filter

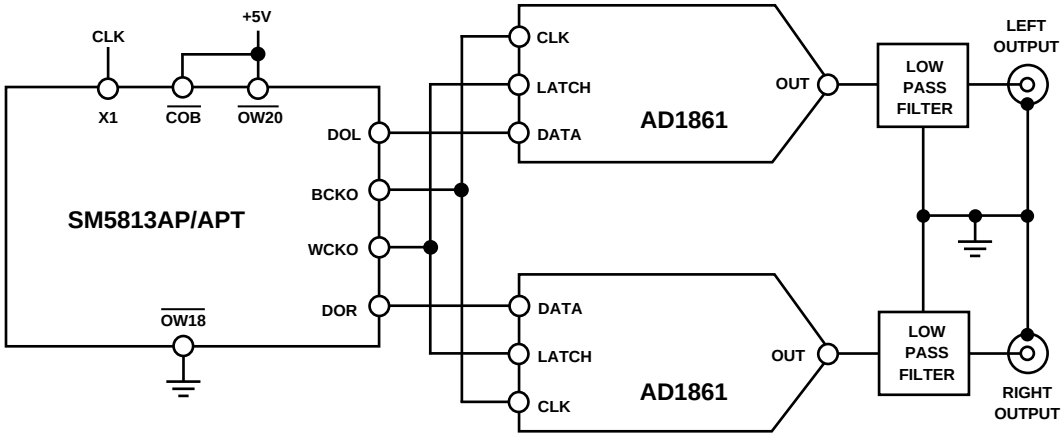
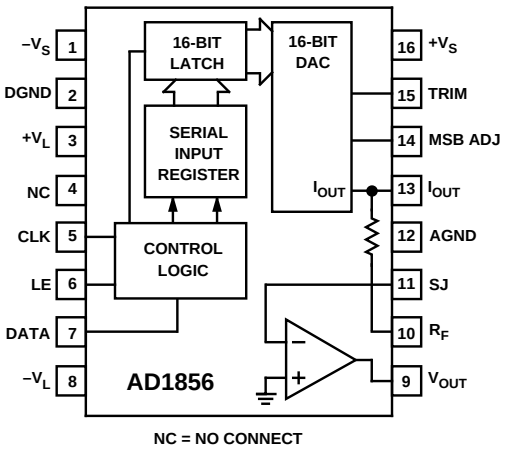
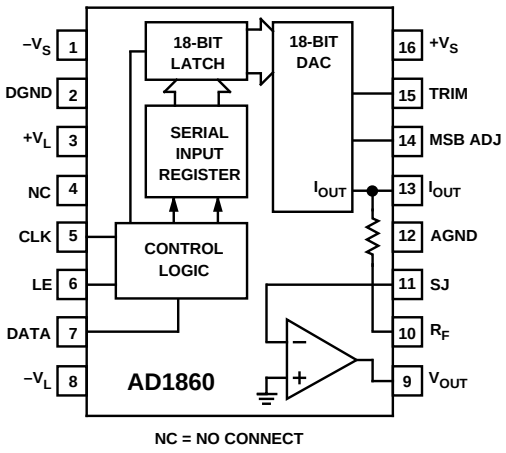


Figure 12. AD1861 with NPC SM5813AP/APT Digital Filter

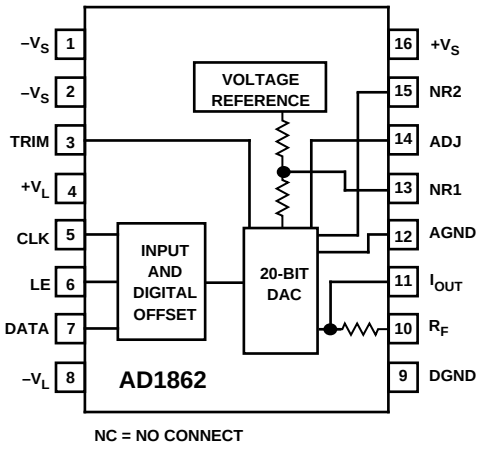
OTHER DIGITAL AUDIO COMPONENTS AVAILABLE FROM ANALOG DEVICES



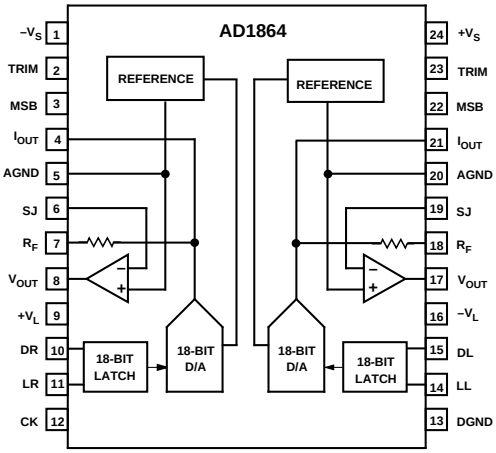
AD1856 16-BIT AUDIO DAC
Complete, No External Components Required
0.0025% THD
Low Cost
16-Pin DIP or SOIC Package
Standard Pinout



AD1860 18-BIT AUDIO DAC
Complete, No External Components Required
0.0025% THD+N
108 dB Signal-to-Noise Ratio
16-Pin DIP or SOIC Package
Standard Pinout



AD1862 20-BIT AUDIO DAC
119 dB Signal-to-Noise Ratio
0.0016% THD+N
102 dB D-Range Performance
±1 dB Gain Linearity
16-Pin DIP

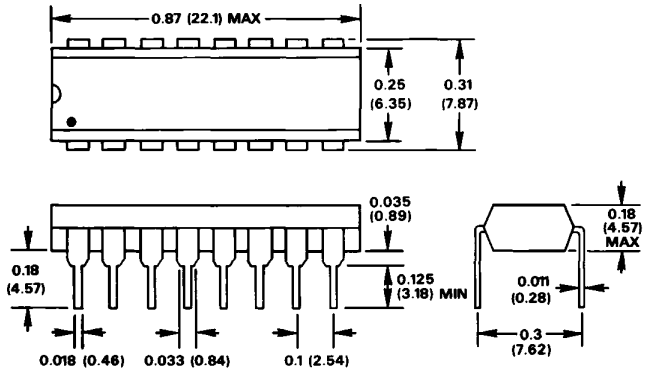


AD1864 DUAL 18-BIT AUDIO DAC
Complete, No External Components
0.0025% THD+N
108 dB Signal-to-Noise Ratio
Cophased Outputs
24-Pin Package

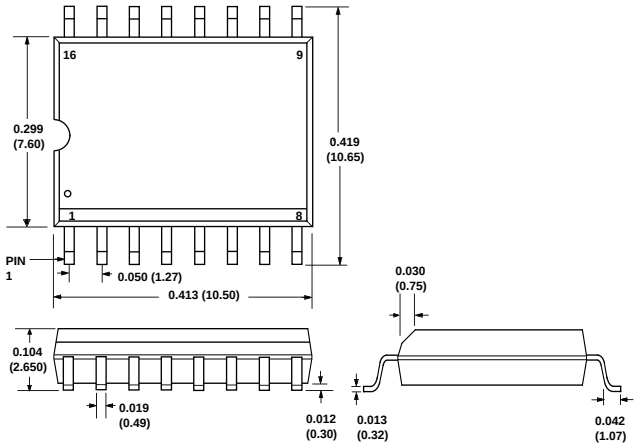
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

N (Plastic DIP) Package



R (SOIC Surface Mount) Package



C1458–7–10/90

PRINTED IN U.S.A.