ORDER NUMBERS:

ORDER NUMBERS	LEAD-FREE ROHS COMPLIANT PACKAGE	NUMBER OF SD/MMC PORTS	TEMPERATURE RANGE
USB82640AM	48QFN	1	-40ºC to 85ºC
USB82640AMR	48QFN Tape and Reel	1	-40ºC to 85ºC
USB82660AM	64QFN	2	-40ºC to 105ºC
USB82660AMR	64QFN Tape and Reel	2	-40ºC to 105ºC

TrueAuto™

TrueAuto is SMSC's automotive quality process. It has proven its ability to deliver leading-edge quality and services for IC device products to fulfill the needs of the most demanding automotive customers. TrueAuto is a proven total automotive-grade quality approach. TrueAuto IC device robustness begins with SMSC's design for reliability techniques within the silicon IC itself: automotive-grade robustness and testability are designed into the IC. Once available in silicon, the IC is fully-characterized and qualified over a multitude of operating parameters to prove quality under the harshest conditions. In this, SMSC's TrueAuto approach significantly exceeds the usual automotive reliability standards and customer-specific requirements and goes far beyond the stress tests prescribed by the AEC-Q100 specifications. During the fabrication of TrueAuto products, extensive technologies and processes, such as enhanced monitors are used in order to continuously drive improvements in accordance with SMSC's zero Defects per Million (DPM) goals.

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Conventions

Within this manual, the following abbreviations and symbols are used to improve readability.

Example	Description
BIT	Name of a single bit within a field
FIELD.BIT	Name of a single bit (BIT) in FIELD
x…y	Range from x to y, inclusive
BITS[m:n]	Groups of bits from m to n, inclusive
PIN	Pin Name
zzzzb	Binary number (value zzzz)
0xzzz	Hexadecimal number (value zzz)
zzh	Hexadecimal number (value zz)
rsvd	Reserved memory location. Must write 0, read value indeterminate
`code`	Instruction code, or API function or parameter
Section Name	Section or Document name
$\overline{\text{VAL}}$	Over-bar indicates active low pin or register bit
x	Don’t care
<Parameter>	<> indicate a Parameter is optional or is only used under some conditions
{,Parameter}	Braces indicate Parameter(s) that repeat one or more times
[Parameter]	Brackets indicate a nested Parameter. This Parameter is not real and actually decodes into one or more real parameters.

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Chapter 1 Overview

1.1 Introduction

The USB82640 offers a USB 2.0 compliant, versatile, cost-effective and energy-efficient Hi-Speed hub controller with 2 downstream USB ports and an SD/MS flash media card interface. The dedicated flash media reader is internally attached to a 3rd downstream port of the hub as a USB Compound device. The USB82660 includes a second SD/SDIO port for accessing two memory cards simultaneously. These combo solutions support today's popular multi-format flash media card formats. The flash media interface can support sustained transfer rates exceeding 35 MB/s if the media and host support those rates.

The USB82640/60 will attach to an upstream port as a Full-Speed hub or as a Full-/Hi-Speed hub. The hub supports Low-Speed, Full-Speed, and Hi-Speed (if operating as a Hi-Speed hub) downstream devices on all of the enabled downstream ports.

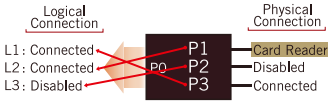
All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D- pins and all required pull-down and pull-up resistors. The over-current sense inputs for the downstream facing ports have internal pull-up resistors.

TrueAuto Quality: The USB82640/60 is specifically tailored for use in automotive applications requiring automotive grade robustness starting with the comprehension of proprietary design for reliability techniques within the silicon IC itself as well as for the package design.

- Automotive qualified technologies and processes are used to fabricate the products with enhanced monitors to continuously drive improvements in accordance with SMSC's zero-dpm methodology.
- Product qualification is focused on customer expectations and exceeds many of the automotive reliability standards including AEC-Q100.
- SMSC automotive services are provided during the life of the product from a dedicated organization of operations, quality, and product support personnel specialized in meeting the requirements of the automotive customer.

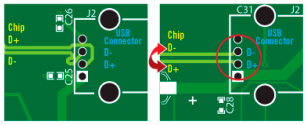
The USB82640/60 includes programmable features such as:

PortMap which provides flexible port mapping and disable sequences. The downstream ports of a USB82640/60 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB82640/60 automatically reorders the remaining ports to match the USB host controller's port numbering scheme.

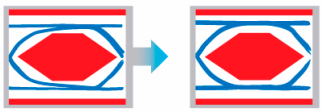


USB Port Virtualization

PortSwap which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors avoiding uneven trace length or crossing of the USB differential signals on the PCB.



PHYBoost which enables four programmable levels of USB signal drive strength in downstream port transceivers. PHYBoost attempts to restore USB signal integrity. The diagram on the right shows an example of Hi-Speed USB eye diagrams before (PHYBoost at 0%) and after (PHYBoost at 12%) signal integrity restoration in a compromised system environment.


Before Boost

After Boost

1.2 Device Features

1.2.1 Hardware Features

- Single chip hub and flash media controller combo
- USB82640 supports the temperature range of -40°C to +85°C
- USB82660 supports the temperature range of -40°C to +105°C
- Transaction Translator (TT) in the hub supports operation of FS and LS peripherals
- Full power management with individual or ganged power control of each downstream port
- Optional support for external firmware access via SPI interface
- Code execution via SPI ROM which must meet
  - 30 MHz or 60 MHz operation support
  - Single bit or dual bit mode support
  - Mode 0 or mode 3 SPI support

Compliance with the following flash media card specifications:

- Secure Digital 2.0/MultiMediaCard 4.2
  - SD 2.0, SD-HS, SD-HC
  - TransFlash™ and reduced form factor media
  - 1/4/8 bit MMC 4.2
- Memory Stick 1.43
- Memory Stick Pro Format 1.02
- Memory Stick Pro-HG Duo Format 1.01
  - Memory Stick, MS Duo™, MS-HS, MS Pro-HG, MS Pro
- MS Duo 1.10
- GPIO configuration and polarity for special function use. The number of actual GPIO's depends on the implementation configuration used.
  - USB82640: Up to 9 GPIOs (One GPIO internal card power FET with up to 200 mA drive)
  - USB82660: Up to 20 GPIOs (Two GPIO internal card power FETs with up to 200 mA drive)
  - Card Power FETs: "Fold-back" short circuit current protected
- 8051, 8-bit microprocessor
  - 60 MHz - single cycle execution
  - 64 kB ROM; 9 kB RAM
- Supports internal regulator for 1.8 V core operation
- Supports external regulator for 1.8 V core operation

1.2.2 Software Features

- Hub and flash media reader/writer configuration from a single source:
  External I^2C ROM or external SPI ROM
- If using an external EEPROM, the OEM can utilize:
  - Customizable vendor ID, product ID, and device ID
  - 12-hex digits maximum for the serial number string
  - 29-character manufacturer ID and product strings for flash media reader/writer

1.2.3 Configurable Hub Features

A default configuration is available in the USB82640/60 following a reset. The USB82640/60 may also be configured by an external I^2C EEPROM or via external SPI ROM flash.

The USB82640/60 supports several OEM selectable features:

- Compound device support on a port-by-port basis
  - a port is permanently hardwired to a downstream USB peripheral device
- Select over-current sensing and port power control on an individual or ganged (all ports together) basis to match the OEM's choice of circuit board component selection
- Port power control and over-current detection/delay features
- Configure the delay time for filtering the over-current sense inputs
- Configure the delay time for turning on downstream port power
- Bus- or self-powered selection
- Hub port disable or non-removable configurations
- Flexible port mapping and disable sequencing supports multiple platform designs
- Programmable USB differential-pair pin location eases PCB layout by aligning USB signal lines directly to connectors
- Programmable USB signal drive strength recovers USB signal integrity using 4 levels of signal drive strength
- Indicate the maximum current that the 2-port hub consumes from the USB upstream port
- Indicate the maximum current required for the hub controller

Chapter 2 Pin Configurations

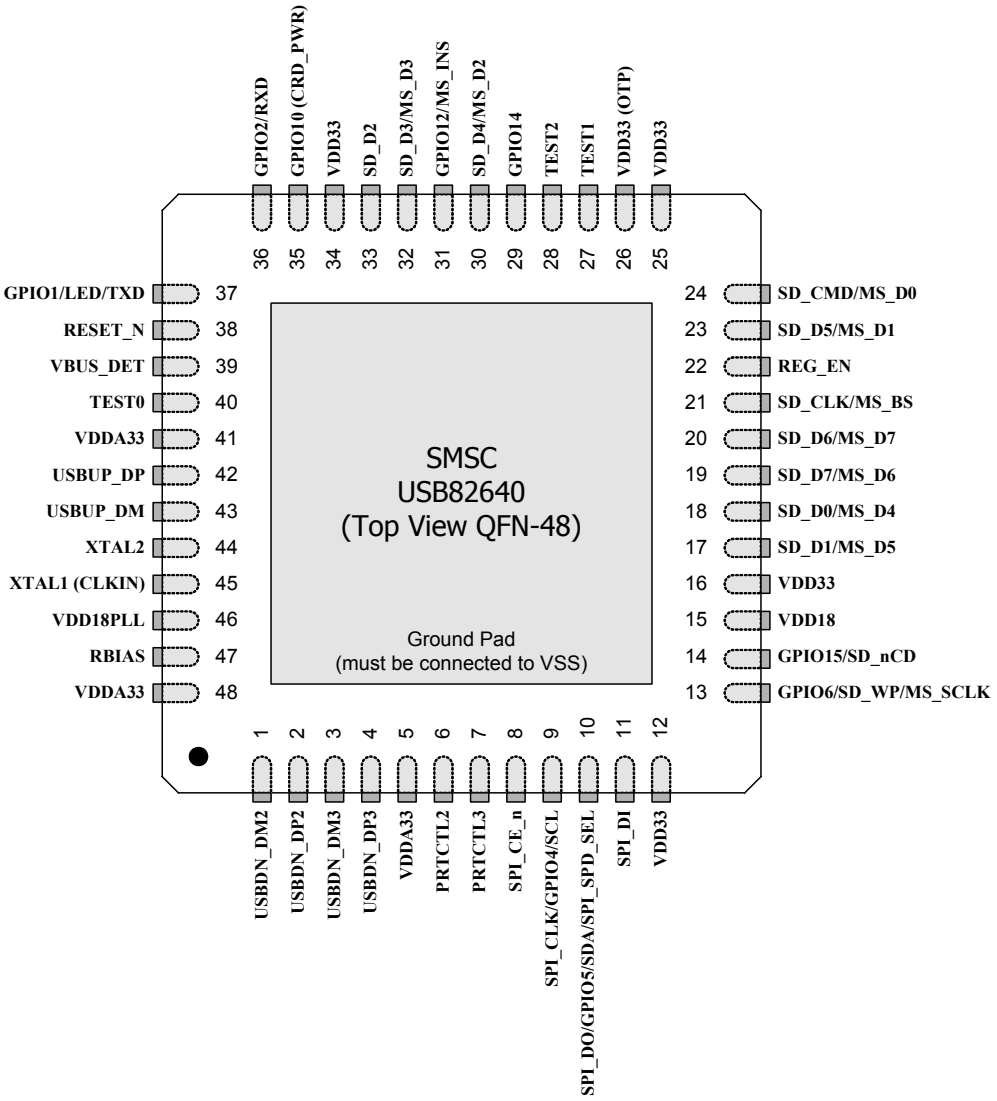


Figure 2.1 USB82640 48-Pin QFN

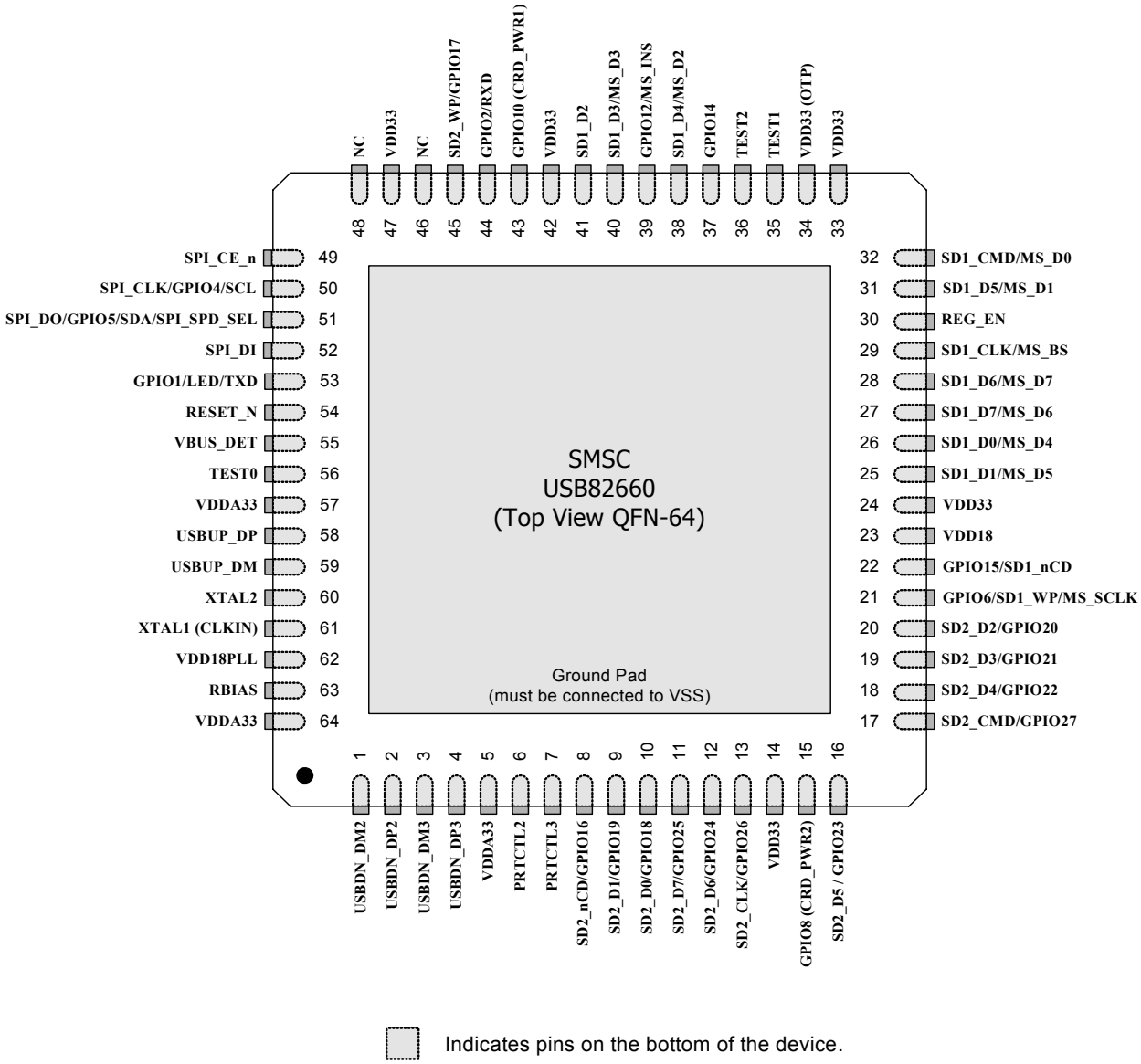


Figure 2.2 USB82660 64-Pin QFN

Chapter 3 Pin Tables

3.1 48-Pin Table

Table 3.1 USB82640 48-Pin Table

SECURE DIGITAL/MEMORY STICK INTERFACE (13 PINS)			
SD_D7/ MS_D6	SD_D6/ MS_D7	SD_D5/ MS_D1	SD_D4/ MS_D2
SD_D3/ MS_D3	SD_D2	SD_D1/ MS_D5	SD_D0/ MS_D4
SD_CLK/ MS_BS	SD_CMD/ MS_D0	GPIO15/ SD_nCD	GPIO12/ MS_INS
GPIO6/ SD_WP/ MS_SCLK	-	-	-
USB 2.0 INTERFACE (10 PINS)			
USBUP_DP	USBUP_DM	XTAL1 (CLKIN)	XTAL2
RBIAS	(3) VDDA33	VDD18PLL	REG_EN
2-PORT USB INTERFACE (7 PINS)			
USBDN_DP2	USBDN_DM2	PRTCTL2	PRTCTL3
USBDN_DP3	USBDN_DM3	VBUS_DET	-
SPI INTERFACE (4 PINS)			
SPI_CE_n	SPI_CLK/ GPIO4/ SCL	SPI_DO/ GPIO5/ SDA/ SPI_SPD_SEL	SPI_DI
MISC (8 PINS)			
RESET_N	TEST0	TEST1	TEST2
GPIO1/ LED/ TXD	GPIO2/ RXD	GPIO10 (CRD_PWR)	GPIO14
POWER (6 PINS)			
(4) VDD33	VDD33	VDD18	-
TOTAL 48			

3.2 64-Pin Table

Table 3.2 USB82660 64-Pin Table

SECURE DIGITAL/MEMORY STICK INTERFACE (13 PINS)			
SD1_D7/ MS_D6	SD1_D6/ MS_D7	SD1_D5/ MS_D1	SD1_D4/ MS_D2
SD1_D3/ MS_D3	SD1_D2	SD1_D1/ MS_D5	SD1_D0/ MS_D4
SD1_CLK/ MS_BS	SD1_CMD/ MS_D0	GPIO15/ SD1_nCD	GPIO12/ MS_INS
GPIO6/ SD1_WP/ MS_SCLK	-	-	-
SECOND SECURE DIGITAL INTERFACE (12 PINS)			
SD2_D7/ GPIO25	SD2_D6/ GPIO24	SD2_D5/ GPIO23	SD2_D4/ GPIO22
SD2_D3/ GPIO21	SD2_D2/ GPIO20	SD2_D1/ GPIO19	SD2_D0/ GPIO18
SD2_nCD/ GPIO16	SD2_CLK/ GPIO26	SD2_CMD/ GPIO27	SD2_WP/ GPIO17
USB 2.0 INTERFACE (10 PINS)			
USBUP_DP	USBUP_DM	XTAL1 (CLKIN)	XTAL2
RBIAS	(3) VDDA33	VDD18PLL	REG_EN
2-PORT USB INTERFACE (7 PINS)			
USBDN_DP2	USBDN_DM2	PRTCTL2	PRTCTL3
USBDN_DP3	USBDN_DM3	VBUS_DET	-
SPI INTERFACE (4 PINS)			
SPI_CE_n	SPI_CLK/ GPIO4/ SCL	SPI_DO/ GPIO5/ SDA/ SPI_SPD_SEL	SPI_DI
MISC (11 PINS)			
RESET_N	TEST0	TEST1	TEST2

Table 3.2 USB82660 64-Pin Table (continued)

GPIO1/ LED/ TXD	GPIO2/ RXD	GPIO8 (CRD_PWR2)	GPIO10 (CRD_PWR1)
GPIO14	(2) NC	-	-
POWER (7 PINS)			
(5) VDD33	VDD33	VDD18	-
TOTAL 64			

Chapter 4 Block Diagrams

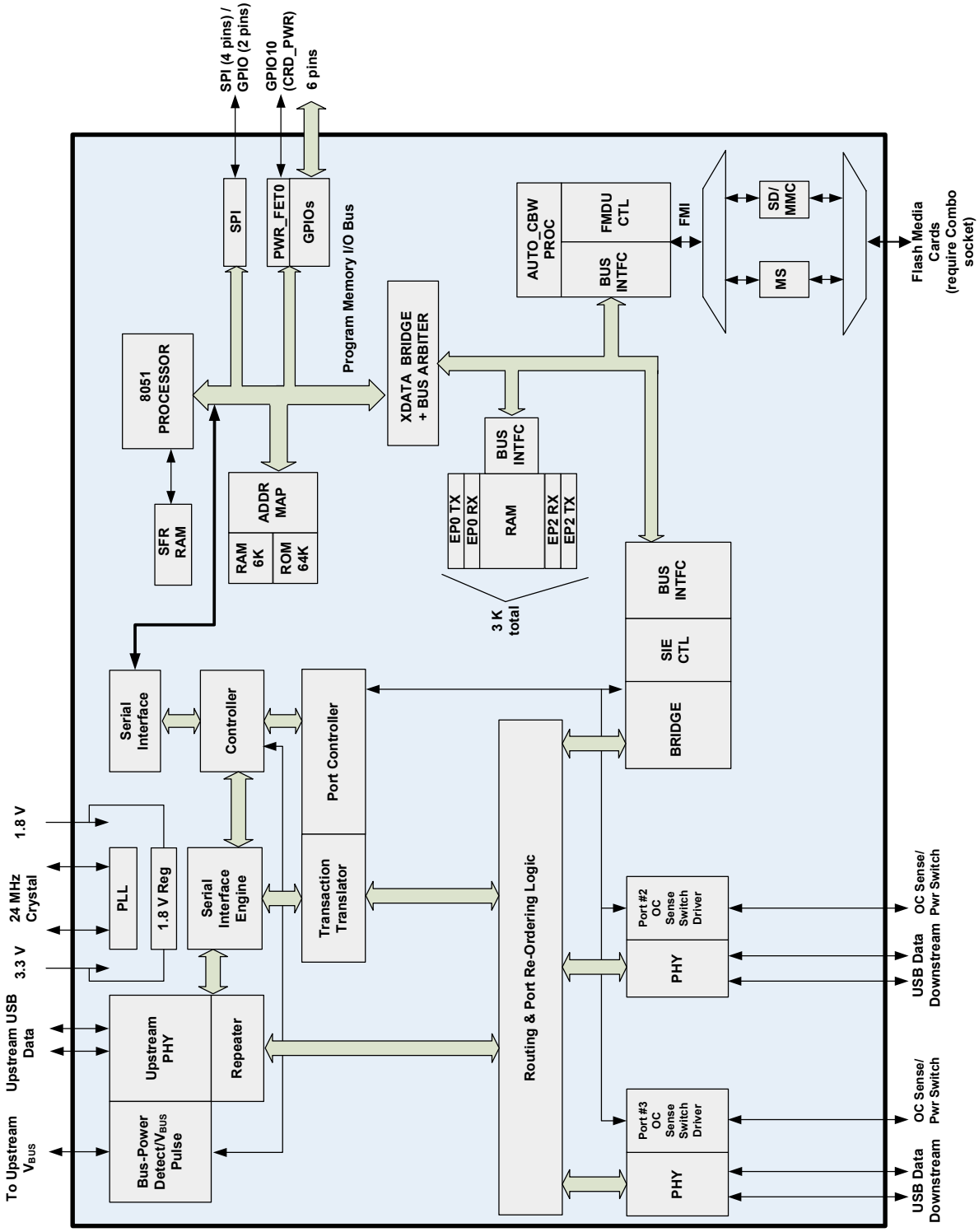


Figure 4.1 USB82640 Block Diagram

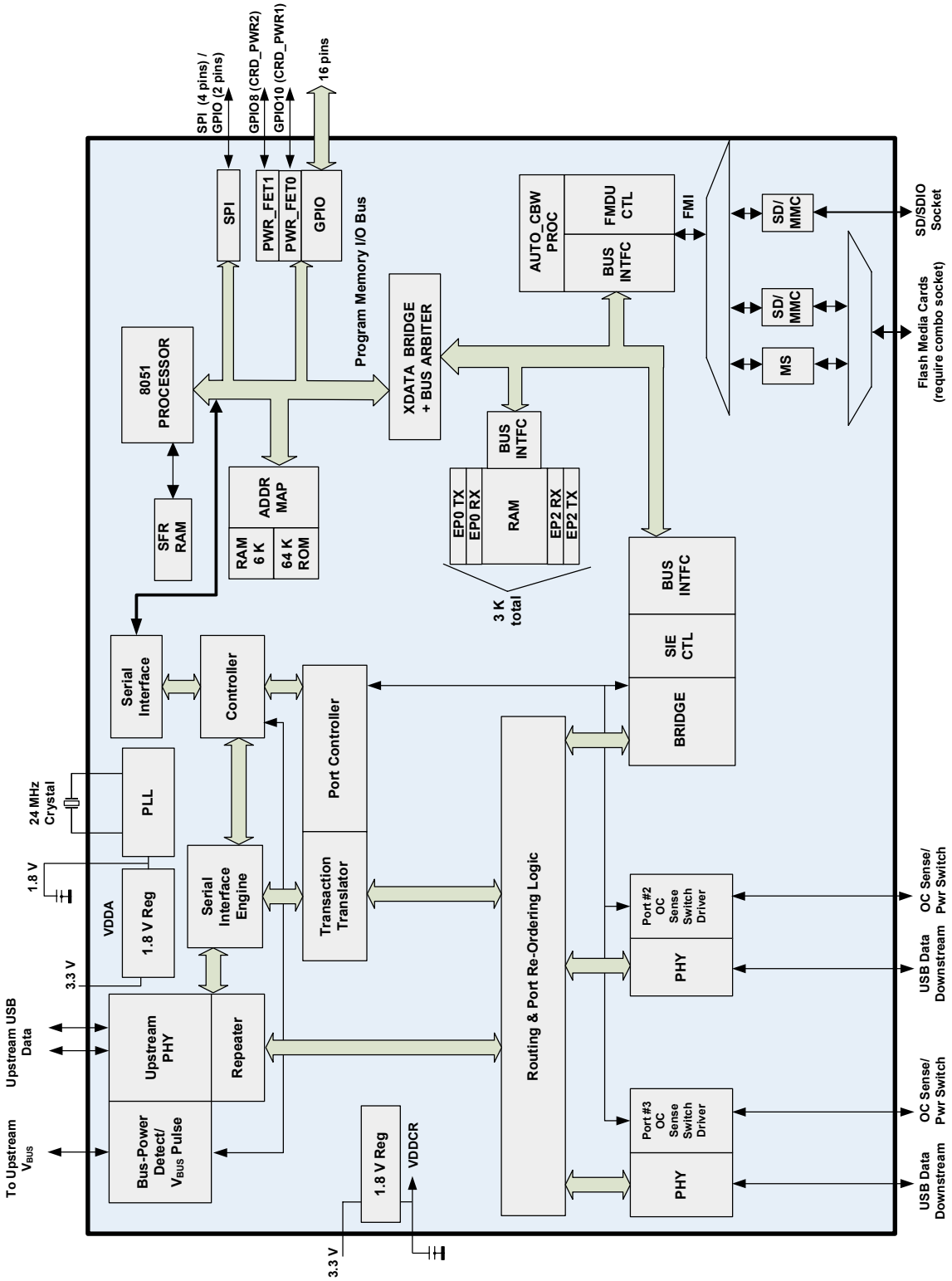


Figure 4.2 USB82660 Block Diagram

Chapter 5 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The pin descriptions below are applied when using the internal default firmware and can be referenced in Chapter 7, "Configuration Options," on page 33. The acronyms used in this chapter can be referenced in Chapter 2, "Acronyms," on page 10.

The "(#)" parentheses surrounding the number in the symbol name is only applicable to USB82660 pins to indicate which set of the function is named. For example, this is true in the case of having two sets of SD cards and a second card power pin.

An *N* at the end of a signal name indicates that the active (asserted) state occurs when the signal is at a low voltage level. When the *N* is not present, the signal is asserted when it is at a high voltage level. The terms assertion and negation are used exclusively in order to avoid confusion when working with a mixture of active low and active high signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

5.1 USB82640/60 Pin Descriptions

Table 5.1 USB82640/60 Pin Descriptions

SYMBOL	48-PIN QFN	64-PIN QFN	BUFFER TYPE	DESCRIPTION
SECURE DIGITAL INTERFACE				
SD(1)_D[7:0]	19 20 23 30 32 33 17 18	27 28 31 38 40 41 25 26	I/O12PU	Secure Digital Data 7-0 These are the bi-directional data signals **SD_D0** - **SD_D7** and have weak pull-up resistors.
SD(1)_CLK	21	29	O12	Secure Digital Clock This is an output clock signal to SD/MMC device.
SD(1)_CMD	24	32	I/O12PU	Secure Digital Command This is a bi-directional signal that connects to the CMD signal of the SD/MMC device. The bi-directional signal has a weak internal pull-up resistor.
GPIO15/	14	22	I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
SD(1)_nCD			I/O12PU	Secure Digital Card Detect GPIO This is a GPIO designated by the default firmware as the Secure Digital card detection pin and has a default internal pull-up.

Table 5.1 USB82640/60 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	64-PIN QFN	BUFFER TYPE	DESCRIPTION
GPIO6/	13	21	I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
SD(1)_WP				Secure Digital Write Protected GPIO This is a GPIO designated by the default firmware as the Secure Digital card mechanical write protect pin.
SECOND SECURE DIGITAL INTERFACE (ONLY APPLIES TO USB82660)				
SD2_D[7:0]	-	11 12 16 18 19 20 9 10	I/O12PU	Second Secure Digital Data 7-0 These are the bi-directional data signals **SD2_D0 - SD2_D7** and have weak pull-up resistors.
GPIO[27:18]			I/O12	These general purpose pins may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
SD2_CLK/	-	13	O12	Second Secure Digital Clock GPIO This is an output clock signal to the SD2/MMC device.
GPIO26			I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
SD2_CMD/	-	17	I/O12PU	Second Secure Digital Command GPIO This is a bi-directional signal that connects to the CMD signal of the SD2/MMC device. The bi-directional signal has a weak internal pull-up resistor.
GPIO27			I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
SD2_nCD/	-	8	I/O12	Second Secure Digital Card Detect GPIO This is a GPIO designated by the default firmware as the second Secure Digital card detection pin and has a default internal pull-up.
GPIO16				This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
SD2_WP/	-	45	I/O12	Second Secure Digital Write Protected GPIO This is a GPIO designated by the default firmware as the second Secure Digital card mechanical write protect pin.
GPIO17				This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.

Table 5.1 USB82640/60 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	64-PIN QFN	BUFFER TYPE	DESCRIPTION
MEMORY STICK INTERFACE				
MS_BS	21	29	O12	Memory Stick Bus State This pin is connected to the bus state pin of the MS device. It is used to control the bus states 0, 1, 2, and 3 (BS0, BS1, and BS3) of the MS device.
GPIO12/	31	39	IPU	This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
MS_INS			I/O12	Memory Stick Card Insertion GPIO This is a GPIO designated by the default firmware as the Memory Stick card detection pin.
MS_SCLK	13	21	O12	Memory Stick System Clock This pin is an output clock signal to the MS device.
MS_D[7:0]	20 19 17 18 32 30 23 24	28 27 25 26 40 38 31 32	I/O12PD	MS System Data In/Out These pins are the bi-directional data signals for the MS device. In serial mode, the most significant bit (MSB) of each byte is transmitted first by either MSC or MS device on **MS_D0**. **MS_D0**, **MS_D2**, and **MS_D3** have weak pull-down resistors. **MS_D1** has a pull down resistor if in parallel mode, otherwise it is disabled. In 4- or 8-bit parallel modes, there is a weak pull-down resistor on all **MS_D7** - **MS_D0** signals.
USB INTERFACE				
USBUP_DM USBUP_DP	43 42	59 58	I/O-U	USB Bus Data These pins connect to the upstream USB bus data signals (host port or upstream hub). USBUP_DM and USBUP_DP can be swapped using the PortSwap feature.
USBDN_DM [3:2] USBDN_DP [3:2]	3 1 4 2	3 1 4 2	I/O-U	USB Bus Data These pins connect to the downstream USB bus data signals and can be swapped using the PortSwap feature.
PRTCTL[3:2]	7 6	7 6	I/OD12PU	USB Power Enable As an output, these pins enables power downstream USB peripheral devices. See Section 5.3, "Port Power Control" for diagram and usage instructions. As an input, when the power is enabled, these pins monitor the over-current condition. When an over-current condition is detected, these pins turn the power off.

Table 5.1 USB82640/60 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	64-PIN QFN	BUFFER TYPE	DESCRIPTION
VBUS_DET	39	55	I	Detect Upstream VBUS Power The SMSC hub monitors **VBUS_DET** to determine when to assert the internal D+ pull-up resistor (signaling a connect event). When designing a detachable hub, connect this pin to the VBUS power pin of the USB port that is upstream of the hub. For self-powered applications with a permanently attached host, this pin should be pulled up, typically to VDD33. VBUS is a 3.3 volt input. A resistor divider must be used when connecting to 5 volts of USB power.
RBIAS	47	63	I-R	USB Transceiver Bias A 12.0 kΩ, ±1.0% resistor is attached from VSS to this pin in order to set the transceiver's internal bias currents.
XTAL1 (CLKIN)	45	61	ICLKx	24 MHz Crystal Input/External Clock Input This pin can be connected to one terminal of the crystal or it can be connected to an external 24 MHz clock when a crystal is not used.
XTAL2	44	60	OCLKx	24 MHz Crystal Output This is the other terminal of the crystal, or a no connect pin, when an external clock source is used to drive **XTAL1** (CLKIN).
VDD18PLL	46	62	-	1.8 V PLL Power Bypass This pin is the 1.8 V power bypass for the PLL. This pin requires an external bypass capacitor of 1.0 µF. If **REG_EN** is low, this pin serves as a power supply (1.8 V) for the device.
VDDA33	5 41 48	5 57 64	-	3.3 V Analog Power ▪ 48QFN - Pin 48 requires an external bypass capacitor of 4.7 µF. ▪ 64QFN - Pin 64 requires an external bypass capacitor of 4.7 µF.
SPI INTERFACE				
SPI_CE_n	8	49	O12	SPI Chip Enable This is the active low chip enable output. If the SPI interface is enabled, drive this pin high in power down states.

Table 5.1 USB82640/60 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	64-PIN QFN	BUFFER TYPE	DESCRIPTION
SPI_CLK/	9	50	I/O12	SPI Clock This is the SPI clock out to the serial ROM. See Section 5.4, "ROM BOOT Sequence" for diagram and usage instructions. During reset, this pin is driven low.
GPIO4/				This general purpose pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
SCL				When configured, this is the I^2C EEPROM clock pin.
SPI_DO/	10	51	I/O12	SPI Data Out This is the data out for the SPI port. See Section 5.4, "ROM BOOT Sequence" for diagram and usage instructions.
GPIO5/				This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
SDA/				This pin is the data pin when the device is connected to the optional I^2C EEPROM.
SPI_SPD_SEL				This pin is used to pick the speed of the SPI interface. During **RESET_N** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When **RESET_N** is negated, the value on the pin will be internally latched, and the pin will revert to **SPI_DO** functionality, the internal pull-down will be disabled. 0 : 30 MHz 1 : 60 MHz If the latched value is 1, then the pin is tri-stated when the chip is in the suspend state. If the latched value is 0, then the pin is driven low during a suspend state.
SPI_DI	11	52	I/O12PD	SPI Data In This is the data in to the controller from the ROM. This pin has a weak internal pull-down applied at all times to prevent floating.
MISC				
GPIO1/	37	53	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
LED/				GPIO1 can be used as an LED output.
TXD				This signal can be used as input to the TxD of UART in the device. Custom firmware is required to activate this alternate function.

Table 5.1 USB82640/60 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	64-PIN QFN	BUFFER TYPE	DESCRIPTION
GPIO2/	36	44	I/O12	This pin may be used either as input, edge sensitive interrupt input, or output. Custom firmware is required to activate this alternate function.
RXD				This signal can be used as input to the RXD of UART in the device. Custom firmware is required to activate this alternate function.
GPIO8 (CRD_PWR2)	-	15	I/O200	Card power drive: 3.3 V (200 mA) This pin specifically powers the second Secure Digital interface (slots). If card power is not being used to power the second SD interface, this pin may be used as a GPIO. Bits 0, 1, 2, and 3 control FET 0 of Register 14Ch. Please reference Section 7.3.4.10, "14Ch-14Dh: LUN 1 Power Configuration," on page 56 for more information.
GPIO10 (CRD_PWR(1))	35	43	I/O200	Card power drive: 3.3 V (200 mA) This pin powers the multiplexed flash media interface (slot) for MS and SD/MMC. If card power is not being used to power the multiplexed interface, this pin may be used as a GPIO. Bits 0, 1, 2, and 3 control FET 2 of Register A5h. Please reference Section 7.3.2.11, "A4h-A5h: LUN 0 Power Configuration," on page 41 for more information.
GPIO14	29	37	I/O12	This general purpose pin may be used either as input, edge sensitive interrupt input, or output.
REG_EN	22	30	IPU	Regulator Enable This pin is internally pulled up to enable the internal 1.8 V regulators. In order to disable the regulators, this pin will need to be externally connected to ground. When the internal regulator is enabled, the 1.8 V power pins must be left unconnected, except for the required bypass capacitors.
RESET_N	38	54	IS	RESET input This active low signal is used by the system to reset the chip. The active low pulse should be at least 1 µs wide.
TEST[2:0]	28 27 40	36 35 56	IPD	TEST Input Tie these test pins to ground for normal operation.
DIGITAL/POWER/GROUND				
VDD18	15	23	-	1.8 V Digital Core Power Bypass This pin requires an external bypass capacitor of 1.0 µF. If **REG_EN** is low, this pin serves as a power supply (1.8 V) for the device.

Table 5.1 USB82640/60 Pin Descriptions (continued)

SYMBOL	48-PIN QFN	64-PIN QFN	BUFFER TYPE	DESCRIPTION
VDD33	12 16 25 34	14 24 33 42 47	-	3.3 V Power and Regulator Input ■ 48QFN - Pin 16 requires an external bypass capacitor of 4.7 µF minimum. ■ 64QFN - Pin 24 requires an external bypass capacitor of 4.7 µF minimum.
VDD33	26	34	-	3.3 V Power
VSS	ePad	ePad	-	Ground Pad The ground pad is the only VSS for the device and must be tied to ground with multiple vias.
NC	-	46 48	-	No Connects No trace or signal should be routed/attached to these pins.

5.2 Buffer Type Descriptions

Table 5.2 USB82640/60 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IPU	Input with weak internal pull-up
IS	Input with Schmitt trigger
I/O12	Input/output buffer with 12 mA sink and 12 mA source
I/O200	Input/output buffer 12 mA with FET disabled, 100/200 mA source only when the FET is enabled
I/O12PD	Input/output buffer with 12 mA sink and 12 mA source, with an internal weak pull-down resistor
I/O12PU	Open drain, 12 mA sink with pull-up. Input with Schmitt trigger
I/OD12PU	Input/open drain output buffer with a 12 mA sink
O12	Output buffer with a 12 mA sink and a 12 mA source
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Analog input/output defined in *USB 2.0 Specification* [1]
I-R	RBIAS

5.3 Port Power Control

Port Power Control Using USB Power Switch

The USB82640/60 has a single port power control and over-current sense signal for each downstream port. When disabling port power, the driver will actively drive a 0. To avoid unnecessary power dissipation, the internal pull-up resistor will be disabled at that time. When port power is enabled, the output driver is disabled, and the pull-up resistor is enabled creating an open drain output.

If there is an over-current situation, the USB Power Switch will assert the open drain OCS signal. The Schmitt trigger input will detect this event as a low. The open drain output does not interfere. The over-current sense filter handles the transient conditions, such as low voltage, while the device is powering up.

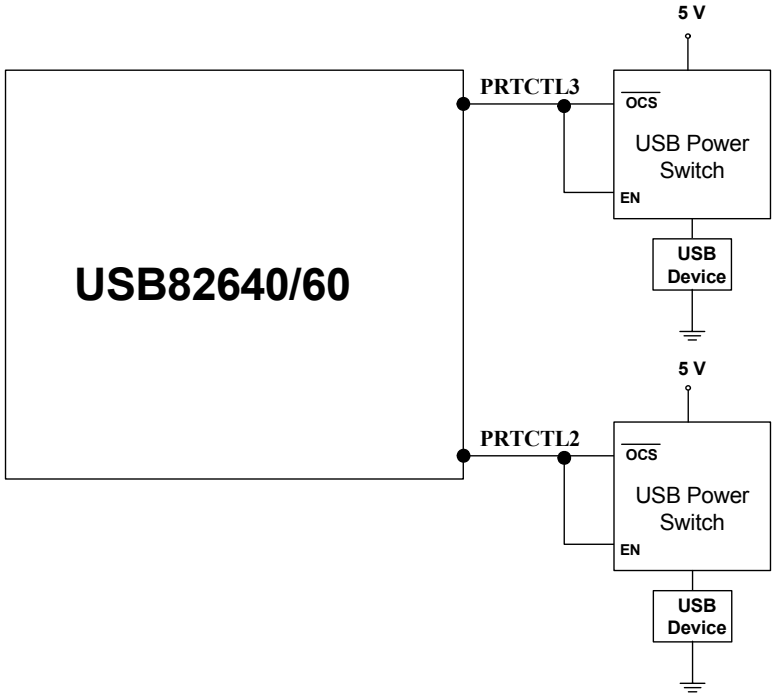


Figure 5.1 Port Power Control with USB Power Switch

Port Power Control Using a Poly Fuse

When using the USB82640/60 with a poly fuse, an external diode must be used (see Figure 5.2). When disabling port power, the USB82640/60 driver will drive a 0. This procedure will have no effect since the external diode will isolate the pin from the load. When port power is enabled, the USB82640/60 output driver is disabled, and the pull-up resistor is enabled which creates an open drain output. This means that the pull-up resistor is providing 3.3 volts to the anode of the diode. If there is an over-current situation, the poly fuse will open. This will cause the cathode of the diode to go to zero volts. The anode of the diode will be at 0.7 volts, and the Schmitt trigger input will register this as a low resulting in an over-current detection. The open drain output does not interfere.

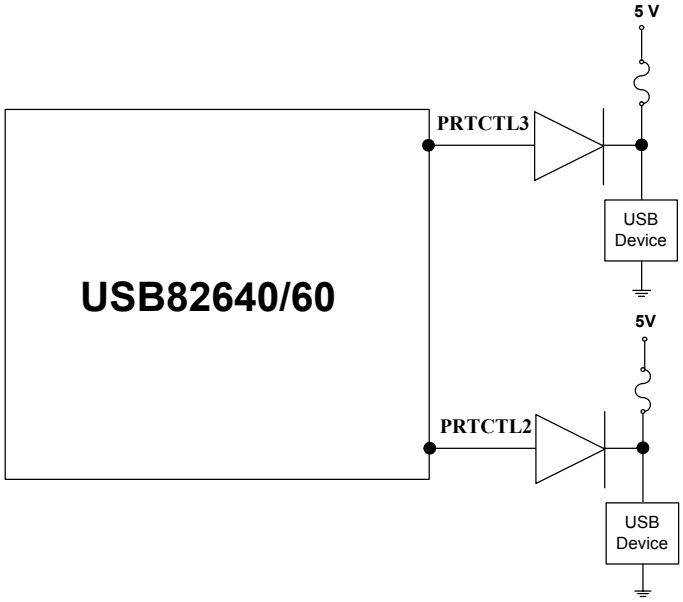


Figure 5.2 Port Power Control with Single Poly Fuse and Multiple Loads

When using a single poly fuse to power all devices, note that for the ganged situation, all power control pins must be tied together.

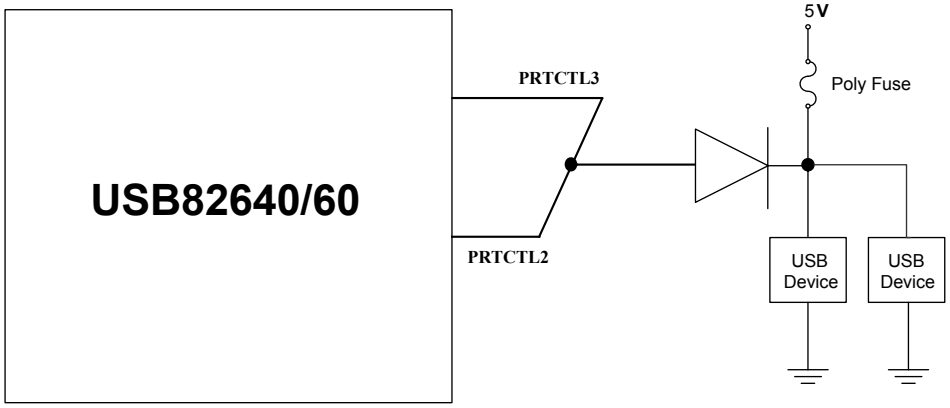


Figure 5.3 Port Power with Ganged Control with Poly Fuse

5.4 ROM BOOT Sequence

After power-on reset, the internal firmware checks for an external SPI flash device that contains a valid signature of `2DFU` (device firmware upgrade) beginning at address 0xFFFA. If a valid signature is found, then the external ROM is enabled and code execution begins at address 0x0000 in the external SPI device. Otherwise, code execution continues from the internal ROM.

If there is no SPI ROM detected, the internal firmware then checks for the presence of an I^2C ROM. The firmware looks for the signature `ATA2` at the offset of FCh-FFh and `ecf1` at the offset of 17Ch-17Fh in the I^2C ROM. The firmware reads in the I^2C ROM to configure the hardware and software internally. Refer to Section 7.3.2, "EEPROM Data Descriptor," on page 34 for the details of the configuration options.

The SPI ROM required for the USB82640/60 is a recommended minimum of 1 Mbit and support either 30 MHz or 60 MHz. The frequency used is set using the SPI_SPD_SEL. For 30 MHz operation, this pin must be pulled to ground through a 100 kΩ resistor. For 60 MHz operation, this pin must pulled up through a 100 kΩ resistor. SPI_SPD_SEL: This pin is used to choose the speed of the SPI interface. During **RESET_N** assertion, this pin will be tri-stated with the weak pull-down resistor enabled. When **RESET_N** is negated, the value on the pin will be internally latched, and the pin will revert to SPI_DO functionality, the internal pull-down will be disabled.

The firmware can determine the speed of operation on the SPI port by checking the SPI_SPEED in the SPI_CTL register (0x2400 - RESET = 0x02). Both 1- and 2-bit SPI operation is supported. For optimum throughput, a 2-bit SPI ROM is recommended. Both mode 0 and mode 3 SPI ROMS are also supported.

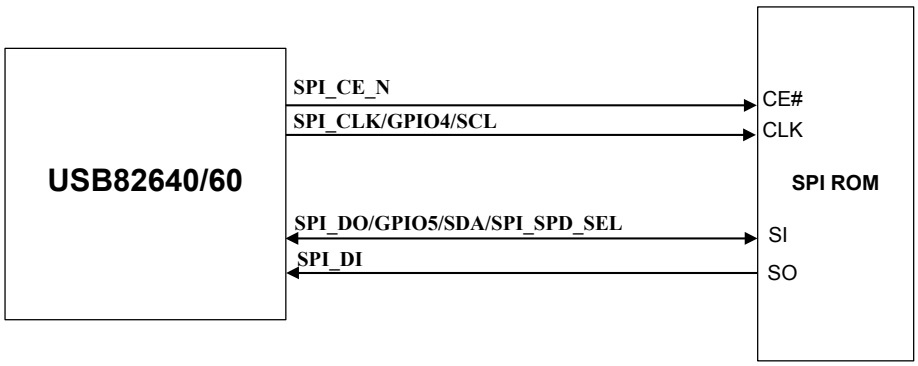


Figure 5.4 SPI ROM Connection

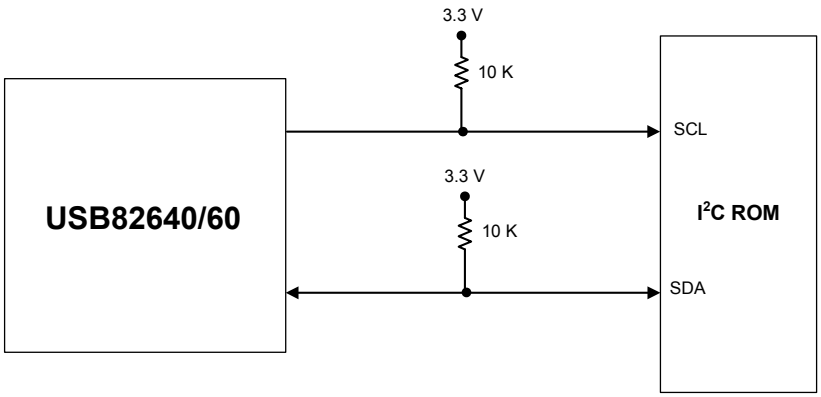


Figure 5.5 I^2C Connection

Chapter 6 Pin Reset States

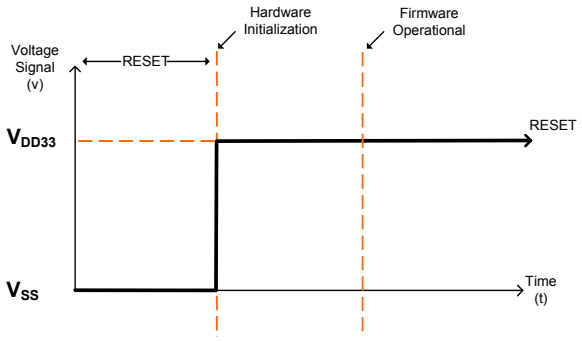


Figure 6.1 Pin Reset States

Table 6.1 Legend for Pin Reset States

SYMBOL	DESCRIPTION
0	Output driven low
1	Output driven high
IP	Input enabled
PU	Hardware enables pull-up
PD	Hardware enables pull-down
none	Hardware disables pad
--	Hardware disables function
Z	Hardware disables pad. Both output driver and input buffers are disabled.

6.1 Pin Reset States

Table 6.2 USB82640 Reset States

PIN	PIN NAME	RESET STATE		
		FUNCTION	INPUT/ OUTPUT	PU/ PD
1	USBDN_DM2	USBDN_DM2	IP	PD
2	USBDN_DP2	USBDN_DP2	IP	PD
3	USBDN_DM3	USBDN_DM3	IP	PD
4	USBDN_DP3	USBDN_DP3	IP	PD
6	PRTCTL2	PRTCTL	0	--
7	PRTCTL3	PRTCTL	0	--
8	SPI_CE_n	SPI_CE_n	1	--
9	SPI_CLK/GPIO4/SCL	GPIO	0	--
10	SPI_DO/GPIO5/SDA/SPI_SPD_SEL	GPIO	0	--
11	SPI_DI	SPI_DI	IP	PD
13	GPIO6/SD_WP/MS_SCLK	GPIO	0	--
14	GPIO15/SD_nCD	GPIO	IP	PU
17	SD_D1/MS_D5	none	Z	--
18	SD_D0/MS_D4	none	Z	--
19	SD_D7/MS_D6	none	Z	--
20	SD_D6/MS_D7	none	Z	--
21	SD_CLK/MS_BS	none	Z	--
22	REG_EN	none	IP	PU
23	SD_D5/MS_D1	none	Z	--
24	SD_CMD/MS_D0	none	Z	--
27	TEST1	none	Z	--
28	TEST2	none	Z	--
29	GPIO14	GPIO	IP	PU
30	SD_D4/MS_D2	none	Z	--

Table 6.2 USB82640 Reset States (continued)

PIN	PIN NAME	RESET STATE		
		FUNCTION	INPUT/ OUTPUT	PU/ PD
31	GPIO12/MS_INS	GPIO	IP	PU
32	SD_D3/MS_D3	none	Z	--
33	SD_D2	none	Z	--
35	GPIO10 (CRD_PWR)	GPIO	Z	--
36	GPIO2/RXD	GPIO	0	--
37	GPIO1/LED/TXD	GPIO	0	--
38	RESET_N	RESET_N	IP	--
39	VBUS_DET	VBUS_DET	IP	--
40	TEST0	TEST	IP	PD
42	USBUP_DP	USBUP_DP	Z	--
43	USBUP_DM	USBUP_DM	Z	--

Table 6.3 USB82660 Reset States

PIN	PIN NAME	RESET STATE		
		FUNCTION	INPUT/ OUTPUT	PU/ PD
1	USBDN_DM2	USBDN_DM2	IP	PD
2	USBDN_DP2	USBDN_DP2	IP	PD
3	USBDN_DM3	USBDN_DM3	IP	PD
4	USBDN_DP3	USBDN_DP3	IP	PD
6	PRTCTL2	PRTCTL	0	--
7	PRTCTL3	PRTCTL	0	--
8	SD2_nCD/GPIO16	GPIO	IP	PU
9	SD2_D1/GPIO19	SD2_D1	Z	--
10	SD2_D0/GPIO18	SD2_D0	Z	--
11	SD2_D7/GPIO25	SD2_D7	Z	--

Table 6.3 USB82660 Reset States (continued)

PIN	PIN NAME	RESET STATE		
		FUNCTION	INPUT/ OUTPUT	PU/ PD
12	SD2_D6/GPIO24	SD2_D6	Z	--
13	SD2_CLK/GPIO26	SD2_CLK	Z	--
15	GPIO8 (CRD_PWR2)	GPIO	Z	--
16	SD2_D5/GPIO23	SD2_D5	Z	--
17	SD2_CMD/GPIO27	SD2_CMD	Z	--
18	SD2_D4/GPIO22	SD2_D4	Z	--
19	SD2_D3/GPIO21	SD2_D3	Z	--
20	SD2_D2/GPIO20	SD2_D2	Z	--
21	GPIO6/SD1_WP/MS_SCLK	GPIO	0	--
22	GPIO15/SD1_nCD	GPIO	IP	PU
25	SD1_D1/MS_D5	none	Z	--
26	SD1_D0/MS_D4	none	Z	--
27	SD1_D7/MS_D6	none	Z	--
28	SD1_D6/MS_D7	none	Z	--
29	SD1_CLK/MS_BS	none	Z	--
30	REG_EN	none	IP	PU
31	SD1_D5/MS_D1	none	Z	--
32	SD1_CMD/MS_D0	none	Z	--
35	TEST1	none	Z	--
36	TEST2	none	Z	--
37	GPIO14	GPIO	IP	PU
38	SD1_D4/MS_D2	none	Z	--
39	GPIO12/MS_INS	GPIO	IP	PU
40	SD1_D3/MS_D3	none	Z	--
41	SD1_D2	none	Z	--

Table 6.3 USB82660 Reset States (continued)

PIN	PIN NAME	RESET STATE		
		FUNCTION	INPUT/ OUTPUT	PU/ PD
43	GPIO10 (CRD_PWR1)	GPIO	Z	--
44	GPIO2/RXD	GPIO	0	--
45	SD2_WP/GPIO17	GPIO	0	--
49	SPI_CE_n	SPI_CE_n	1	--
50	SPI_CLK/GPIO4/SCL	GPIO	0	--
51	SPI_DO/GPIO5/SDA/SPI_SPD_SEL	GPIO	0	--
52	SPI_DI	SPI_DI	IP	PD
53	GPIO1/LED/TXD	GPIO	0	--
54	RESET_N	RESET_N	IP	--
55	VBUS_DET	VBUS_DET	IP	--
56	TEST0	TEST	IP	PD
58	USBUP_DP	USBUP_DP	Z	--
59	USBUP_DM	USBUP_DM	Z	--

Chapter 7 Configuration Options

7.1 Hub

SMSC's USB 2.0 hub is fully compliant to the *Universal Serial Bus 2.0 Specification* [1]. See Chapter 11 (Hub Specification) for general details regarding hub operation and functionality.

The hub provides 1 Transaction Translator (TT) that is shared by both downstream ports defined as a single-TT configuration. The TT contains 4 non-periodic buffers.

7.1.1 Hub Configuration Options

The SMSC hub supports a large number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are two principal ways to configure the hub:

- internal default settings
- use settings stored on an external EEPROM or SPI Flash device

7.1.1.1 Power Switching Polarity

The hub will only support active high power controllers.

7.1.2 VBus Detect

According to Section 7.2.1 of the *USB 2.0 Specification*, a downstream port can never provide power to its D+ or D- pull-up resistors unless the upstream port's VBUS is in the asserted (powered) state. The **VBUS_DET** pin on the hub monitors the state of the upstream VBUS signal and will not pull-up the D+ resistor if VBUS is not active. If VBUS goes from an active to an inactive state (not powered), the hub will remove power from the D+ pull-up resistor within 10 seconds.

7.2 Card Reader

The SMSC USB82640/60 is fully compliant with the following flash media card reader specifications:

- Secure Digital 2.0/MultiMediaCard Specification 4.2
  - SDSC and SDHC
  - TransFlash and reduced form factor media
  - 1/4/8 bit MMC
- Memory Stick Specification 1.43
- Memory Stick Pro Format Specification 1.02
- Memory Stick Pro-HG Duo Format Specification 1.01
  - Memory Stick, MS Duo, HS-MS, MS Pro-HG, MS Pro

7.3 System Configurations

7.3.1 EEPROM/SPI Interface

The USB82640/60 can be configured via a 2-wire (I^2C) EEPROM (512x8) or an external SPI flash device containing the firmware for the USB82640/60. If an external configuration device does not exist

the internal default values will be used. If one of the external devices is used for configuration, the values can be updated through the USB interface. The hub then attaches to the upstream USB host.

The USBDM tool set is available in the Hub Card reader combo software release package:

https://www2.smsc.com/mkt/CW_SFT_Pub.nsf/Agreements/OBJ+Hub+Card+Reader

Select the OBJ Hub Card Reader Software Download Agreement, review the license, and select the *I agree* checkbox, followed by *Confirm*.

Note 7.1 Refer to the *USB 2.0 Specification* for other language codes.

7.3.2 EEPROM Data Descriptor

Table 7.1 Internal Flash Media Controller Configurations

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
00h-19h	USB_SER_NUM	USB Serial Number	000008264001 (Unicode)
1Ah-1Bh	USB_VID	USB Vendor ID	0424
1Ch-1Dh	USB_PID	USB Product ID	4040
1Eh-21h	USB_LANG_ID	USB Language Identifier	0409 (Note 7.1)
22h-5Dh	USB_MFR_STR	USB Manufacturer String	Generic (Unicode)
5Eh-99h	USB_PRD_STR	USB Product String	Ultra Fast Media Reader (Unicode)
9Ah	USB_BM_ATT	USB BmAttribute	80h
9Bh	USB_MAX_PWR	USB Max Power	30h (96 mA)
9Ch	ATT_LB	Attribute Lo byte	40h (Reverse SD_WP only)
9Dh	ATT_HLB	Attribute Hi Lo byte	80h (Reverse SD2_WP only)
9Eh	ATT_LHB	Attribute Lo Hi byte	00h
9Fh	ATT_HB	Attribute Hi byte	00h
A0h-A3h	rsvd		
A4h	LUN_PWR_LB	LUN Power Lo byte	00h
A5h	LUN_PWR_HB	LUN Power Hi byte	0Ah
A6h-A7h	rsvd		
A8h	LED_BLK_INT	LED Blink Interval	02h
A9h	LED_BLK_DUR	LED Blink After Access	28h
AAh-B0h	rsvd		
B1h-B7h	DEV1_ID_STR	Device 1 Identifier String	MS

Table 7.1 Internal Flash Media Controller Configurations (continued)

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
B8h-BEh	rsvd		
BFh-C5h	DEV3_ID_STR	Device 3 Identifier String	SD/MMC
C6h-CDh	INQ_VEN_STR	Inquiry Vendor String	Generic
CEh-D2h	INQ_PRD_STR	48QFN Inquiry Product String	82640
CEh-D2h	INQ_PRD_STR	64QFN Inquiry Product String	82660
D3h	DYN_NUM_LUN	Dynamic Number of LUNs	01h
D4h-D7h	LUN_DEV_MAP	LUN to Device Mapping	FFh, 00h, 00h, 00h
D8h-DAh	MS_BUS_TIMING	MS Bus Timing Control	00h, 06h, 0Dh (Note 7.2)
DBh-DDh	SD_MMC_BUS_TIMING	SD1/MMC Bus Timing Control	59h, 56h, 97h (Note 7.2)
Please refer to Table 7.2, “Hub Controller Configurations,” on page 37 for a continuation of the register values DEh-17Fh. **Internal Flash Media Controller Extended Configurations:** The registers below are enabled by setting bit 7 of bmAttribute.			
100h-106h	CLUN0_ID_STR	LUN 0 Identifier String	COMBO
107h-10Dh	CLUN1_ID_STR	LUN 1 Identifier String	COMBO
10Eh-114h	CLUN2_ID_STR	LUN 2 Identifier String	COMBO
115h-11Bh	CLUN3_ID_STR	LUN 3 Identifier String	COMBO
11Ch-122h	CLUN4_ID_STR	LUN 4 Identifier String	COMBO
123h-129h	rsvd	Reserved for USB82640	
123h-129h	DEV4_ID_STR	64QFN Device 4 Identifier String	SD2/MMC2
12Ah-145h	rsvd		
146h	DYN_NUM_ EXT_LUN	48QFN Dynamic Number of Extended LUNs	00h
146h	DYN_NUM_ EXT_LUN	64QFN Dynamic Number of Extended LUNs	01h
147h-14Bh	LUN_DEV_MAP	48QFN LUN to Device Mapping	FFh, FFh, FFh, FFh, FFh
147h-14Bh	LUN_DEV_MAP	64QFN LUN to Device Mapping	01h, FFh, FFh, FFh, FFh
14Ch-14Dh	rsvd	Reserved for USB82640	

Table 7.1 Internal Flash Media Controller Configurations (continued)

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
14Ch	SD2_PWR_LB	64QFN LUN Power Lo byte	08h
14Dh	SD2_PWR_HB	64QFN LUN Power Hi byte	00h
14Eh-17Bh	rsvd		
17Ch-17Fh	NVSTORE_SIG2	Non-Volatile Storage Signature	ecf1

Note 7.2 This register value must not be changed from the default value.

Table 7.2 Hub Controller Configurations

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
DEh	VID_LSB	Vendor ID Least Significant Byte	24h
DFh	VID_MSB	Vendor ID Most Significant Byte	04h
E0h	PID_LSB	48QFN Product ID Least Significant Byte	40h
E0h	PID_LSB	64QFN Product ID Least Significant Byte	60h
E1h	PID_MSB	Product ID Most Significant Byte	26h
E2h	DID_LSB	Device ID Least Significant Byte	A1h
E3h	DID_MSB	Device ID Most Significant Byte	08h
E4h	CFG_DAT_BYT1	Configuration Data Byte 1	8Bh
E5h	CFG_DAT_BYT2	Configuration Data Byte 2	28h
E6h	CFG_DAT_BYT3	Configuration Data Byte 3	00h
E7h	NR_DEVICE	Non-Removable Devices	02h
E8h	PORT_DIS_SP	Port Disable (Self)	00h
E9h	PORT_DIS_BP	Port Disable (Bus)	00h
EAh	MAX_PWR_SP	Max Power (Self)	01h
EBh	MAX_PWR_BP	Max Power (Bus)	32h
ECh	HC_MAX_C_SP	Hub Controller Max Current (Self)	01h
EDh	HC_MAX_C_BP	Hub Controller Max Current (Bus)	32h
EEh	PWR_ON_TIME	Power-on Time	32h
EFh	BOOST_UP	Boost_Up	00h
F0h	BOOST_3:2	Boost_3:2	00h
F1h	PRT_SWP	PortSwap	00h
F2h	PRTM12	PortMap 12	00h
F3h	PRTM3	PortMap 3	00h

Table 7.3 Other Internal Configurations

ADDRESS	REGISTER NAME	DESCRIPTION	INTERNAL DEFAULT VALUE
F4h	MS_SD_1_CLK_LIM	MS/SD Clock Limit for Flash Media Controller	00h
F5h	rsvd		
F6h	MEDIA_SETTINGS	SD1/2 Timeout Configuration	00h
F7h	SD_2_CLK_LIM	64QFN SD2 Clock Limit for Flash Media Controller	00h
F8h-FAh	SD_2_MMC_TIMING	64QFN SD2 Bus Timing Control	5Ch, 59h, 9Ah
FBh	rsvd		
FCh-FFh	NVSTORE_SIG	Non-Volatile Storage Signature	ATA2

7.3.2.1 00h-19h: USB Serial Number Option

BYTE	NAME	DESCRIPTION
25:0	USB_SER_NUM	Maximum string length is 12 hex digits. Must be unique to each device.

7.3.2.2 1Ah-1Bh: USB Vendor Identifier Option

BYTE	NAME	DESCRIPTION
1:0	USB_VID	This ID is unique for every vendor. The vendor ID is assigned by the USB Implementer's Forum.

7.3.2.3 1Ch-1Dh: USB Product Identifier Option

BYTE	NAME	DESCRIPTION
1:0	USB_PID	This ID is unique for every product. The product ID is assigned by the vendor.

7.3.2.4 1Eh-21h: USB Language Identifier Option

BYTE	NAME	DESCRIPTION
3:0	USB_LANG_ID	English language code = 0409

7.3.2.5 22h-5Dh: USB Manufacturer String Length

BYTE	NAME	DESCRIPTION
59:0	USB_MFR_STR	Maximum string length is 29 characters.

7.3.2.6 5Eh-99h: USB Product String Length

BYTE	NAME	DESCRIPTION
59:0	USB_PRD_STR	This string will be used during the USB enumeration process in Windows®. Maximum string length is 29 characters.

7.3.2.7 9Ah: USB BmAttribute (1 byte)

BIT	NAME	DESCRIPTION
7:0	USB_BM_ATT	Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated. When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. 80 = Bus-powered operation C0 = Self-powered operation A0 = Bus-powered operation with remote wake-up E0 = Self-powered operation with remote wake-up

7.3.2.8 9Bh: USB MaxPower (1 byte)

BYTE	NAME	DESCRIPTION
7:0	USB_MAX_PWR	USB Max Power per USB specification. Do NOT set this value greater than 100 mA.

7.3.2.9 9Ch-9Fh: Attribute Byte Descriptions

BYTE	BYTE NAME	BIT NUMBER	DESCRIPTION
1	ATT_LB	3:0	Always read as 0
		4	Inquire Manufacturer and Product ID Strings 1 : use the Inquiry Manufacturer and Product ID Strings. 0 : (default) use the USB Descriptor Manufacturer and Product ID Strings.
		5	Always read as 0
		6	Reverse SD Card Write Protect Sense 1 : (default) SD cards will be write protected when **SW_nWP** is high, and writable when SW_nWP is low. 0 : SD cards will be write protected when **SW_nWP** is low, and writable when **SW_nWP** is high.
		7	rsvd
2	ATT_HLB	3:0	Always read as 0
		4	Activity LED True Polarity 1 : Activity LED to Low True 0 : (default) Activity LED polarity to High True
		5	Common Media Insert/Media Activity LED 1 : the activity LED will function as a common media inserted/media access LED. 0 : (default) the activity LED will remain in its idle state until media is accessed.
		6	Always read as 0
		7	Reverse SD2 Card Write Protect Sense 1 : (default) SD cards in LUN 1 will be write protected when **SW_nWP** is high, and writable when **SW_nWP** is low. 0 : SD cards in LUN 1 will be write protected when **SW_nWP** is low, and writable when **SW_nWP** is high.
3	ATT_LHB	0	Attach on Card Insert/Detach on Card Removal 1 : attach on Insert is enabled. 0 : (default) attach on Insert is disabled.
		1	Always read as 0
		2	Use LUN Power Configuration 1 : custom LUN Power Configuration stored in the NVSTORE is used. 0 : (default) default LUN Power Configuration is used.
		7:3	Always read as 0
4	ATT_HB	7:0	Always read as 0

7.3.2.10 A0h-A3h: Reserved

BYTE	NAME	DESCRIPTION
3:0	rsvd	

7.3.2.11 A4h-A5h: LUN 0 Power Configuration

The USB82640 has one internal FET which can be utilized for card power. The USB82660 has two internal FETs which can be utilized for card power. Please reference Section 7.3.4.10, "14Ch-14Dh: LUN 1 Power Configuration," on page 56 for information on the other internal FET. The settings are stored in NVSTORE and provide the following features:

1. A card can be powered by an external FET or by an internal FET.
2. The power limit is set to 100 mA or 200 mA (Default) for the internal FET.

Each media uses two bytes to store its LUN power configuration. Bit 3 selects between internal or external. For internal FETs Bits 0 through 2 are used for the power limit. Only 2 of the possible 8 values are currently specified.

Table 7.4 FET Configuration

FET	TYPE	BITS	BIT TYPE	DESCRIPTION
0	FET Lo Byte	3:0	Low Nibble	Unused
1		7:4	High Nibble	
2	**FET Hi Byte**	**3:0**	**Low Nibble**	**0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit 1010b Internal FET with 200 mA power limit**
3		7:4	High Nibble	Unused

7.3.2.12 A6h-A7h: Reserved

BYTE	NAME	DESCRIPTION
1:0	rsvd	

7.3.2.13 A8h: LED Blink Interval (1 byte)

BIT	NAME	DESCRIPTION
7:0	LED_BLK_INT	The blink rate is programmable in 50 ms intervals. The high bit (7) indicates an idle state: 0 : off 1 : on The remaining bits (6:0) are used to determine the blink interval up to a max of 128 x 50 ms.

7.3.2.14 A9h: Blink Duration

BIT	NAME	DESCRIPTION
7:0	LED_BLK_DUR	LED Blink After Access This byte is used to designate the number of seconds that the GPIO 1 LED will continue to blink after a drive access. Setting this byte to 05 will cause the GPIO 1 LED to blink for 5 seconds after a drive access.

7.3.3 Device ID Strings

7.3.3.1 AAh-B0h: Reserved

BYTE	NAME	DESCRIPTION
6:0	rsvd	

7.3.3.2 B1h-B7h: Device 1 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV1_ID_STR	These bytes are used to specify the LUN descriptor returned by the device. These bytes are used in combination with the LUN to device mapping bytes in applications that reorder and rename the LUNs. If this device is configured to be part of a COMBO LUN then this string is ignored for the appropriate **CLUNx_ID_STR**.

7.3.3.3 B8h-BEh: Reserved

BYTE	NAME	DESCRIPTION
6:0	rsvd	

7.3.3.4 BFh-C5h: Device 3 Identifier String

BYTE	NAME	DESCRIPTION
6:0	DEV3_ID_STR	These bytes are used to specify the LUN descriptor returned by the device. These bytes are used in combination with the LUN to device mapping bytes in applications that reorder and rename the LUNs. If this device is configured to be part of a COMBO LUN then this string is ignored for the appropriate **CLUNx_ID_STR**.

7.3.3.5 C6h-CDh: Inquiry Vendor String

BYTE	NAME	DESCRIPTION
7:0	INQ_VEN_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

7.3.3.6 CEh-D2h: Inquiry Product String

BYTE	NAME	DESCRIPTION
4:0	INQ_PRD_STR	If bit 4 of the 1st attribute byte is set, the device will use these strings in response to a USB inquiry command, instead of the USB descriptor manufacturer and product ID strings.

7.3.3.7 D3h: Dynamic Number of LUNs

BIT	NAME	DESCRIPTION
7:0	DYN_NUM_LUN	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and only a single icon is displayed for one or more interfaces. If this field is set to FF, the program assumes that you are using the default value and icons will be configured per the default configuration.

7.3.3.8 D4h-D7h: LUN to Device Mapping

BYTE	NAME	DESCRIPTION
3:0	LUN_DEV_MAP	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and only a single icon is displayed for one or more interfaces. If this field is set to FF, the program assumes that you are using the default values and LUNs will be configured per the default configuration.

7.3.3.9 D8h-DAh: MS Bus Timing Control

BIT	BYTE NAME	DESCRIPTION
2:0	MS_BUS_TIMING	The values for these bytes are set internally and must not be altered.

7.3.3.10 DBh-DDh: SD/MMC Bus Timing Control

BYTE	BYTE NAME	DESCRIPTION
2:0	SD_1_MMC_BUS_TIMING	The values for these bytes are set internally and must not be altered.

7.3.3.11 DEh: Vendor ID (LSB)

BIT	BYTE NAME	DESCRIPTION
7:0	VID_LSB	Least Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementer's Forum).

7.3.3.12 DFh: Vendor ID (MSB)

BIT	BYTE NAME	DESCRIPTION
7:0	VID_MSB	Most Significant Byte of the Vendor ID. This is a 16-bit value that uniquely identifies the vendor of the user device (assigned by USB Implementer's Forum).

7.3.3.13 E0h: Product ID (LSB)

BIT	BIT NAME	DESCRIPTION
7:0	PID_LSB	Least Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product.

7.3.3.14 E1h: Product ID (MSB)

BIT	BIT NAME	DESCRIPTION
7:0	PID_MSB	Most Significant Byte of the Product ID. This is a 16-bit value that the vendor can assign that uniquely identifies this particular product.

7.3.3.15 E2h: Device ID (LSB)

BIT	BIT NAME	DESCRIPTION
7:0	DID_LSB	Least Significant Byte of the Device ID. This is a 16-bit device release number in BCD (binary coded decimal) format.

7.3.3.16 E3h: Device ID (MSB)

BIT	BIT NAME	DESCRIPTION
7:0	DID_MSB	Most Significant Byte of the Device ID. This is a 16-bit device release number in BCD format.

7.3.3.17 E4h: Configuration Data Byte 1 (CFG_DAT_BYT1)

BIT	NAME	DESCRIPTION
7	SELF_BUS_PWR	Self- or Bus-Power: Selects between self- and bus-powered operation. The hub is either self-powered (draws less than 2 mA of upstream bus power) or bus-powered (limited to a 100 mA maximum of upstream power prior to being configured by the host controller). When configured as a bus-powered device, the SMSC hub consumes less than 100 mA of current prior to being configured. After configuration, the bus-powered SMSC hub (along with all associated hub circuitry, any embedded devices if part of a compound device, and 100 mA per externally available downstream port) must consume no more than 500 mA of upstream VBUS current. The current consumption is system dependent, and the OEM must ensure that the USB 2.0 specifications are not violated. When configured as a self-powered device, <1 mA of upstream VBUS current is consumed and all ports are available, with each port being capable of sourcing 500 mA of current. 0 : bus-powered operation 1 : self-powered operation
6	rsvd	
5	HS_DISABLE	Hi-Speed Disable: Disables the capability to attach as either a Hi-/Full-Speed device, and forces attachment as Full-Speed only (i.e. no Hi-Speed support). 0 : hi-/full-speed 1 : full-speed only (hi-speed disabled)
4	rsvd	
3	EOP_DISABLE	EOP Disable: Disables EOP generation of EOF1 when in Full-Speed mode. During FS operation only, this permits the hub to send EOP if no downstream traffic is detected at EOF1. See Section 11.3.1 of the *USB 2.0 Specification* [1] for additional details. 0 : an EOP is generated at the EOF1 point if no traffic is detected. 1 : EOP generation at EOF1 is disabled (normal USB operation). Generation of an EOP at the EOF1 point may prevent a host controller (operating in FS mode) from placing the USB bus in suspend.
2:1	CURRENT_SNS	Over-Current Sense: Selects current sensing on a port-by-port basis, all ports ganged, or none (only for bus-powered hubs). The ability to support current sensing on a per port or ganged basis is dependent upon the hardware implementation. 00 : fanged sensing (all ports together) 01 : Individual (port-by-port) 1x : over-current sensing is not supported (must only be used with bus-powered configurations)
0	PORT_PWR	Port Power Switching: Enables power switching on all ports simultaneously (ganged), or port power is individually switched on and off on a port-by-port basis (individual). The ability to support power enabling on a port or ganged basis is dependent upon the hardware implementation. 0 : ganged switching (all ports together) 1 : individual port-by-port switching

7.3.3.18 E5h: Configuration Data Byte 2 (CFG_DAT_BYT2)

BIT	NAME	DESCRIPTION
7:6	rsvd	
5:4	OC_TIMER	OverCurrent Timer: Over-current timer delay. 00 : 50 ns 01 : 100 ns 10 : 200 ns 11 : 400 ns
3	COMPOUND	Compound Device: Allows OEM to indicate that the hub is part of a compound device per the *USB 2.0 Specification* [1]. The applicable port(s) must also be defined as having a “non-removable device”. When configured via strapping options, declaring a port as non-removable automatically causes the hub controller to report that it is part of a compound device. 0 : no 1 : yes, the hub is part of a compound device
2:0	rsvd	

7.3.3.19 E6h: Configuration Data Byte 3 (CFG_DAT_BYT3)

BIT	NAME	DESCRIPTION
7:4	rsvd	
3	PRTMAP_EN	Port Mapping Enable: Selects the method used by the hub to assign port numbers and disable ports. 0 : Standard Mode. Strap options or the following registers are used to define which ports are enabled, and the ports are mapped as port ‘n’ on the hub is reported as port ‘n’ to the host, unless one of the ports is disabled, then the higher numbered ports are remapped in order to report contiguous port numbers to the host. Register 300Ah: Port disable for self-powered operation (Reset = 0x00). Register 300Bh: Port disable for bus-powered operation (Reset = 0x00). 1 : PortMap mode. The mode enables remapping via the registers defined below. Register 30FBh: PortMap 12 (Reset = 0x00) Register 30FCh: PortMap 3 (Reset = 0x00)
2:0	rsvd	

7.3.3.20 E7h: Non-Removable Device

BIT	BYTE NAME	DESCRIPTION
7:0	NR_DEVICE	Indicates which port(s) include non-removable devices. 0 : port is removable 1 : port is non-removable Informs the host if one of the active ports has a permanent device that is undetachable from the hub. The device must provide its own descriptor data. When using the internal default option, the **NON_REM[1:0]** pins will designate the appropriate ports as being non-removable. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = Controls physical port 3 Bit 2 = Controls physical port 2 Bit 1 = Controls physical port 1 Bit 0 = rsvd **Note:** Bit 1 must be set to a 1 by the firmware for proper identification of the card reader as a non-removable device.

7.3.3.21 E8h: Port Disable for Self-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	PORT_DIS_SP	Disables 1 or more ports. 0 : port is available 1 : Port is disabled During self-powered operation this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a host controller. The ports can be disabled in any order since the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = Controls physical port 3 Bit 2 = Controls physical port 2 Bit 1 = Controls physical port 1 Bit 0 = rsvd **Note:** Bit 1 must be set to 0 in order for the card reader to enumerate.

7.3.3.22 E9h: Port Disable for Bus-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	PORT_DIS_BP	Disables 1 or more ports. 0 : port is available 1 : port is disabled During self-powered operation, this register selects the ports which will be permanently disabled. The ports are unavailable to be enabled or enumerated by a host controller. The ports can be disabled in any order, the internal logic will automatically report the correct number of enabled ports to the USB host and will reorder the active ports in order to ensure proper function. When using the internal default option, the **PRT_DIS[1:0]** pins will disable the appropriate ports. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = Controls physical port 3 Bit 2 = Controls physical port 2 Bit 1 = Controls physical port 1 Bit 0 = rsvd **Note:** Bit 1 must be set to 0 in order for the card reader to enumerate.

7.3.3.23 EAh: Max Power for Self-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	MAX_PWR_SP	Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. **Note:** The *USB 2.0 Specification* [1] does not permit this value to exceed 100 mA.

7.3.3.24 EBh: Max Power for Bus-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	MAX_PWR_BP	Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value also includes the power consumption of a permanently attached peripheral if the hub is configured as a compound device, and the embedded peripheral reports 0 mA in its descriptors. **Note:** The *USB 2.0 Specification* does not permit this value to exceed 100 mA.

7.3.3.25 ECh: Hub Controller Max Current For Self-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	HC_MAX_C_SP	Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a self-powered hub. This value includes the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value does NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. **Note:** The *USB 2.0 Specification* does not permit this value to exceed 100 mA. A value of 50 (decimal) indicates 100 mA, which is the default value.

7.3.3.26 EDh: Hub Controller Max Current For Bus-Powered Operation

BIT	BYTE NAME	DESCRIPTION
7:0	HC_MAX_C_BP	Value in 2 mA increments that the hub consumes from an upstream port (VBUS) when operating as a bus-powered hub. This value will include the hub silicon along with the combined power consumption (from VBUS) of all associated circuitry on the board. This value will NOT include the power consumption of a permanently attached peripheral if the hub is configured as a compound device. A value of 50 (decimal) would indicate 100 mA, which is the default value.

7.3.3.27 EEh: Power-On Time

BIT	BYTE NAME	DESCRIPTION
7:0	POWER_ON_TIME	The length of time that it takes (in 2 ms intervals) from the time the host initiated power-on sequence begins on a port until power is adequate on that port. If the host requests the power-on time, the system software uses this value to determine how long to wait before accessing a powered-on port.

7.3.3.28 EFh: Boost_Up

BIT	BIT NAME	DESCRIPTION
7:2	rsvd	
1:0	BOOST_IOUT	USB electrical signaling drive strength boost bit for the upstream port A. 00 : normal electrical drive strength = no boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost) **Note:** “Boost” could result in non-USB Compliant parameters. The value should be set to 00 unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.

7.3.3.29 F0h: Boost_3:2

BIT	BIT NAME	DESCRIPTION
7:6	rsvd	
5:4	BOOST_IOUT_3	Upstream USB electrical signaling drive strength boost bit for downstream port 3. 00 : normal electrical drive strength = no boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost)
3:2	BOOST_IOUT_2	Upstream USB electrical signaling drive strength boost bit for downstream port 2. 00 : normal electrical drive strength = No boost 01 : elevated electrical drive strength = low (approximately 4% boost) 10 : elevated electrical drive strength = medium (approximately 8% boost) 11 : elevated electrical drive strength = high (approximately 12% boost) **Note:** "Boost" could result in non-USB Compliant parameters. The value should be set to 00 unless specific implementation issues require additional signal boosting to correct for degraded USB signaling levels.
1:0	Reserved	Always read as 0

7.3.3.30 F1h: PortSwap

BIT	BYTE NAME	DESCRIPTION
7:0	PRT_SWP	Swaps the upstream and downstream USB DP and DM pins for ease of board routing to devices and connectors. 0 : USB D+ functionality is associated with the DP pin and D- functionality is associated with the DM pin. 1 : USB D+ functionality is associated with the DM pin and D- functionality is associated with the DP pin. Bit 7 = rsvd Bit 6 = rsvd Bit 5 = rsvd Bit 4 = rsvd Bit 3 = Controls physical port 3 Bit 2 = Controls physical port 2 Bit 1 = rsvd Bit 0 = Controls physical port 0

7.3.3.31 F2h: PortMap 12

<table>
<tr><th>BIT</th><th>BYTE NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7:0</td><td>PRTM12</td><td>PortMap register for ports 1 and 2

When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reported having.

The host's port number is referred to as “logical port number” and the physical port on the hub is the “physical port number”. When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).

Note: Contiguous logical port numbers must be used, starting from number 1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.

Table 7.5 PortMap Register for Ports 1 & 2
<table>
<tr><td>Bit [7:4]</td><td>0000</td><td>Physical port 2 is disabled</td></tr>
<tr><td></td><td>0001</td><td>Physical port 2 is mapped to Logical port 1</td></tr>
<tr><td></td><td>0010</td><td>Physical port 2 is mapped to Logical port 2</td></tr>
<tr><td></td><td>0011</td><td>Physical port 2 is mapped to Logical port 3</td></tr>
<tr><td></td><td>0100 to 1111</td><td>Illegal; Do not use</td></tr>
<tr><td>Bit [3:0]</td><td>0000</td><td>Physical port 1 is disabled</td></tr>
<tr><td></td><td>0001</td><td>Physical port 1 is mapped to Logical port 1</td></tr>
<tr><td></td><td>0010</td><td>Physical port 1 is mapped to Logical port 2</td></tr>
<tr><td></td><td>0011</td><td>Physical port 1 is mapped to Logical port 3</td></tr>
<tr><td></td><td>0100 to 1111</td><td>Illegal; Do not use</td></tr>
</table>
</td></tr>
</table>

7.3.3.32 F3h: PortMap 3

<table>
<tr><th>BIT</th><th>BYTE NAME</th><th>DESCRIPTION</th></tr>
<tr><td>7:0</td><td>PRTM3</td><td>PortMap register for port 3

When a hub is enumerated by a USB host controller, the hub is only permitted to report how many ports it has; the hub is not permitted to select a numerical range or assignment. The host controller will number the downstream ports of the hub starting with the number 1, up to the number of ports that the hub reported having.

The host's port number is referred to as “logical port number” and the physical port on the hub is the “physical port number”. When remapping mode is enabled (see PRTMAP_EN in Register 08h: Configuration Data Byte 3) the hub's downstream port numbers can be remapped to different logical port numbers (assigned by the host).

Note: Contiguous logical port numbers must be used, starting from number 1 up to the maximum number of enabled ports; this ensures that the hub's ports are numbered in accordance with the way a host will communicate with the ports.</td></tr>
</table>

Table 7.6 PortMap Register for Port 3

Bit [7:4]	0000	Reserved
	0001	Reserved
	0010	Reserved
	0011	Reserved
	0100 to 1111	Illegal; Do not use
Bit [3:0]	0000	Physical port 3 is disabled
	0001	Physical port 3 is mapped to Logical port 1
	0010	Physical port 3 is mapped to Logical port 2
	0011	Physical port 3 is mapped to Logical port 3
	0100 to 1111	Illegal; Do not use

7.3.3.33 F4h: MS/SD Clock Limit for the Flash Media Controller

BYTE NAME	TYPE	BITS	DESCRIPTION
MS_SD_CLK_LIM	Upper Nibble Bits	7:4	0: MS - 60 MHz -- Default, no limit 1: MS - 40 MHz 2: MS - 20 MHz 3: MS - 15 MHz
	Lower Nibble Bits	3:0	0: SD/MMC - 48 MHz 1: SD/MMC - 24 MHz 2: SD/MMC - 20 MHz 3: SD/MMC - 15 MHz

7.3.3.34 F5h: Reserved

BIT	BYTE NAME	DESCRIPTION
7:0	rsvd	

7.3.3.35 F6h: SD1/2 Timeout Options

BIT	NAME	DESCRIPTION
7:0	MEDIA_SETTINGS	The SD1 and SD2 Timeout Options: Bit 0 : rsvd Bit 1 : rsvd Bits 2-4 : SD1 timeout Bits 5-7 : SD2 timeout A value of 001b equates to a timeout of 0.81 seconds, where 010b indicates an additional 0.81 seconds for a total of 1.62, and so on. The maximum value is 000b (default), which indicates a total timeout of 6.5 seconds.

7.3.3.36 F7h: SD2 Clock Limit for Flash Media Controller (64QFN Only)

BIT	BYTE NAME	DESCRIPTION
7:0	SD_2_CLK_LIM	The values for these bytes are set internally and must not be altered.

7.3.3.37 F8h-FAh: SD2 Bus Timing Control (64QFN Only)

BYTE	BYTE NAME	DESCRIPTION
2:0	SD_2_MMC_ TIMING	The values for these bytes are set internally and must not be altered.

7.3.3.38 FBh: Reserved

BIT	BYTE NAME	DESCRIPTION
7:0	rsvd	

7.3.3.39 FCh-FFh: Non-Volatile Storage Signature

BYTE	NAME	DESCRIPTION
3:0	NVSTORE_SIG	This signature is used to verify the validity of the data in the first 256 bytes of the configuration area. The signature must be set to `ATA2`.

7.3.4 Internal Flash Media Controller Extended Configurations

Enable Registers 100h - 17Fh by setting bit 7 of bmAttribute.

7.3.4.1 100h-106h: Combo LUN 0 Identifier String

BYTE	NAME	DESCRIPTION
6:0	CLUN0_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs then these strings will be used to identify the LUN rather than the device identifier strings.

7.3.4.2 107h-10Dh: Combo LUN 1 Identifier String

BYTE	NAME	DESCRIPTION
6:0	CLUN1_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs then these strings will be used to identify the LUN rather than the device identifier strings.

7.3.4.3 10Eh-114h: Combo LUN 2 Identifier String

BYTE	NAME	DESCRIPTION
6:0	CLUN2_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs then these strings will be used to identify the LUN rather than the device identifier strings.

7.3.4.4 115h-11Bh: Combo LUN 3 Identifier String

BYTE	NAME	DESCRIPTION
6:0	CLUN3_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs then these strings will be used to identify the LUN rather than the device identifier strings.

7.3.4.5 11Ch-122h: Combo LUN 4 Identifier String

BYTE	NAME	DESCRIPTION
6:0	CLUN4_ID_STR	If the LUN to device mapping bytes have configured this LUN to be a combo LUNs then these strings will be used to identify the LUN rather than the device identifier strings.

7.3.4.6 123h-129h: Device 4 Identifier String (Only Applies to 64QFN)

BYTE	NAME	DESCRIPTION
6:0	DEV4_ID_STR	These bytes are used to specify the LUN descriptor returned by the device. These bytes are used in combination with the LUN to device mapping bytes in applications where the OEM wishes to reorder and rename the LUNs. If this device is configured to be part of a COMBO LUN then this string is ignored for the appropriate **CLUN_ID_STR**. **Note:** Not applicable to USB82640.

7.3.4.7 12Ah-145h: Reserved

BYTE	NAME	DESCRIPTION
27:0	rsvd	

7.3.4.8 146h: Dynamic Number of Extended LUNs

BIT	NAME	DESCRIPTION
7:0	DYN_NUM_ EXT_LUN	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to FF, the program assumes that you are using the default value and icons will be configured per the default configuration.

7.3.4.9 147h-14Bh: LUN to Device Mapping

BYTE	NAME	DESCRIPTION
4:0	LUN_DEV_MAP	These bytes are used to specify the number of LUNs the device exposes to the host. These bytes are also used for icon sharing by assigning more than one LUN to a single icon. This is used in applications where the device utilizes a combo socket and the OEM wishes to have only a single icon displayed for one or more interfaces. If this field is set to FF, the program assumes that you are using the default value and icons will be configured per the default configuration.

7.3.4.10 14Ch-14Dh: LUN 1 Power Configuration

USB82660 has two internal FETs which can be utilized for card power. Please reference Section 7.3.2.11, "A4h-A5h: LUN 0 Power Configuration," on page 41 for information about the other FET. The settings are stored in NVSTORE and provide the following features:

1. A card can be powered by an external FET or by an internal FET.
2. The power limit is set to 100 mA or 200 mA (Default) for the internal FET.

Each media uses two bytes to store its LUN power configuration. Bit 3 selects between internal or external. For internal FETs Bits 0 through 2 are used for the power limit. Only 2 of the possible 8 values are currently specified

Table 7.7 FET Configuration

FET	TYPE	BITS	BIT TYPE	DESCRIPTION
0	**FET Lo Byte**	**3:0**	**Low Nibble**	**0000b Disabled 0001b External FET enabled 1000b Internal FET with 100 mA power limit 1010b Internal FET with 200 mA power limit**
1		7:4	High Nibble	Unused
2	FET Hi Byte	3:0	Low Nibble	Unused
3		7:4	High Nibble	Unused

7.3.4.11 14Eh-17Bh: Reserved

BYTE	NAME	DESCRIPTION
45:0	rsvd	

7.3.4.12 17Ch -17Fh: Non-Volatile Storage Signature for Extended Configuration

BYTE	NAME	DESCRIPTION
3:0	NVSTORE_SIG2	This signature is used to verify the validity of the data in the upper 256 bytes if a 512-byte EEPROM is used. Otherwise this bank is a read-only configuration area. The signature must be set to `ecf1`.

7.3.5 I²C EEPROM

The I²C EEPROM interface implements a subset of the *I²C Master Specification* (refer to the Philips Semiconductor Standard I²C-Bus Specification for details on I²C bus protocols). The device's I²C EEPROM interface is designed to attach to a single "dedicated" I²C EEPROM, and it conforms to the *Standard-mode I²C Specification* (100 kbit/s transfer rate and 7-bit addressing) for protocol and electrical compatibility.

Note: Extensions to the *I²C Specification* are not supported. The device acts as the master and generates the serial clock SCL, controls the bus access (determines which device acts as the transmitter and which device acts as the receiver), and generates the START and STOP conditions.

7.3.5.1 Implementation Characteristics

The device will only access an EEPROM using the sequential read protocol.

7.3.5.2 Pull-Up Resistor

The circuit board designer is required to place external pull-up resistors (10 kΩ recommended) on the **SPI_DO/GPIO5/SDA/SPI_SPD_SEL** and **SPI_CLK/GPIO4/SCL** lines (per *SMBus 1.0 Specification* [3] and EEPROM manufacturer guidelines) to VDD33 in order to assure proper operation.

7.3.5.3 I^2C EEPROM Slave Address

Slave address is 1010000. 10-bit addressing is not supported.

7.3.6 In-Circuit EEPROM Programming

The EEPROM can be programmed via automatic test equipment (ATE) by pulling **RESET_N** low which tri-states the device's EEPROM interface and allows an external source to program the EEPROM.

7.4 Default Configuration Option

The SMSC device can be configured via its internal default configuration. Please see Section 7.3.2, "EEPROM Data Descriptor" for specific details on how to enable default configuration. Please refer to Table 7.1 for the internal default values that are loaded when this option is selected.

7.5 Reset

There are two different resets that the device experiences. One is a hardware reset (either from the internal POR (power-on reset) circuit or via the **RESET_N** pin) and the second is a USB bus reset.

7.5.1 Internal POR Hardware Reset

All reset timing parameters are guaranteed by design.

7.5.2 External Hardware RESET_N

A valid hardware reset is defined as assertion of **RESET_N** for a minimum of 1 µs after all power supplies are within operating range. While reset is asserted, the device (and its associated external circuitry) consumes less than IRST µA of current from the upstream USB power source.

Assertion of **RESET_N** (external pin) causes the following:

1. All downstream ports are disabled, and **PRTCTL** power to downstream devices is removed.
2. The PHYs are disabled, and the differential pairs will be in a high-impedance state.
3. All transactions immediately terminate; no states are saved.
4. All internal registers return to the default state (in most cases, 00h).
5. The external crystal oscillator is halted.
6. The PLL is halted.

7.5.2.1 RESET_N for EEPROM Configuration

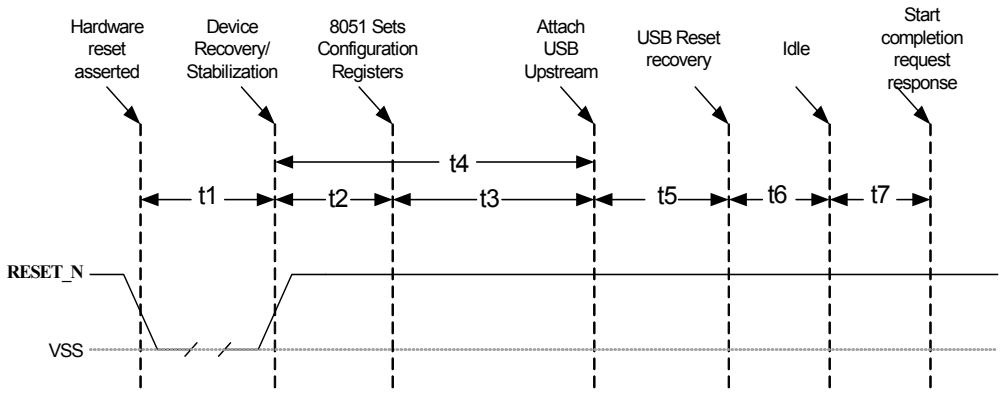


Figure 7.1 RESET_N Timing for EEPROM Mode

Table 7.8 RESET_N Timing for EEPROM Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	**RESET_N** asserted	1	-	-	µsec
t2	Device recovery/stabilization	-	-	500	µsec
t3	8051 programs device configuration	-	20	50	msec
t4	USB attach (see Note 7.3)	-	-	100	msec
t5	Host acknowledges attach and signals USB reset	100	-	-	msec
t6	USB idle	-	Undefined	-	msec
t7	Completion time for requests (with or without data stage)	-	-	5	msec

Note 7.3 All power supplies must have reached the operating levels mandated in Chapter 8, DC Parameters, prior to (or coincident with) the assertion of **RESET_N**.

7.5.3 USB Bus Reset

In response to the upstream port signaling a reset to the device, the device does the following:

Note: The device does not propagate the upstream USB reset to downstream devices.

1. Sets default address to 0.
2. Sets configuration to: Unconfigured.
3. Negates **PRTCTL[3:2]** to all downstream ports.
4. Clears all TT buffers.
5. Moves device from suspended to active (if suspended).
6. Complies with Section 11.10 of the *USB 2.0 Specification* [1] for behavior after completion of the reset sequence.

The host then configures the device and the device's downstream port devices in accordance with the *USB 2.0 Specification*.

Chapter 8 DC Parameters

8.1 Maximum Guaranteed Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
Storage Temperature	T_{STOR}	-55	150	°C	
3.3 V supply voltage	V_{DD33}, V_{DDA33}	-0.5	4.0	V	-
Voltage on GPIO8 and GPIO10	-	-0.5	V_{DD33} + 0.3	V	When internal power FET operation of these pins are enabled, these pins may be simultaneously shorted to ground or any voltage up to 3.63 V indefinitely, without damage to the device as long as V_{DD33} and V_{DDA33} are less than 3.63 V and T_A is less than 70 ^oC.
Voltage on any signal pin	-	-0.5	V_{DD33} + 0.3	V	-
Voltage on XTAL1	-	-0.5	3.6	V	-

Stresses above the specified parameters may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at any condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies the absolute maximum ratings must not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, a clamp circuit should be used.

8.2 Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	COMMENTS
48-pin package Operating Temperature	T_A	-40	85	°C	Ambient temperature in still air. (See Note 8.1)
64-pin package Operating Temperature	T_A	-40	105	°C	Ambient temperature in still air. (See Note 8.1)
3.3 V supply voltage	V_{DD33}, V_{DDA33}	3.0	3.6	V	A 3.3 V regulator with an output tolerance of ±1% must be used if the output of the internal power FET's must support a 5% tolerance.
3.3 V supply rise time	t_{RT}	0	400	ms	(Figure 8.1, "Supply Rise Time Models")
1.8 V supply rise time	t_{RT}	0	400	ms	(Figure 8.1, "Supply Rise Time Models")
Voltage on any signal pin	-	-0.3	V_{DD33}	V	-
Voltage on XTAL1	-	-0.3	2.0	V	-

Note 8.1 The T_J (junction temperature) must not exceed 125°C.

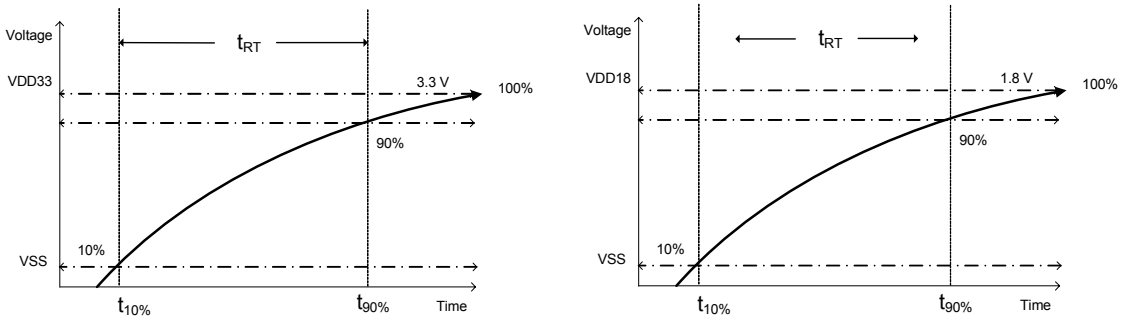


Figure 8.1 Supply Rise Time Models

Note 8.2 The 3.3 V supply should be at least at 75% of its operating condition before the 1.8 V supply is allowed to ramp up.

8.3 Package Thermal Specifications

Table 8.1 48-pin QFN Package Thermal Parameters

PARAMETER	SYMBOL	VALUE	UNIT	COMMENTS
Thermal Resistance	Θ_{JA}	28	°C/W	Measured from the die to the ambient air
Junction-to-Top-of-Package	Ψ_{JT}	0.2	°C/W	-

Table 8.2 64-pin QFN Package Thermal Parameters

PARAMETER	SYMBOL	VALUE	UNIT	COMMENTS
Thermal Resistance	Θ_{JA}	25	°C/W	Measured from the die to the ambient air
Junction-to-Top-of-Package	Ψ_{JT}	0.2	°C/W	-

Note 8.3 Thermal parameters are estimated for devices with the exposed pad soldered to thermal vias in a multi-layer 2S2P PCB per JESD51.

8.4 DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I, IPU, IPD Type Input Buffer						
Low Input Level	V_{ILI}	-	-	0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0	-	-	V	
Pull Down	PD	-	72	-	µA	
Pull Up	PU	-	58	-	µA	
IS Type Input Buffer						
Low Input Level	V_{ILI}	-	-	0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0	-	-	V	
ICLK Input Buffer						
Low Input Level	V_{ILCK}	-	-	0.5	V	
High Input Level	V_{IHCK}	1.4	-	-	V	
Input Leakage	I_{IL}	-10	-	+10	µA	V_{IN} = 0 to V_{DD33}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage						
(All I and IS buffers)						
Low Input Leakage	I_{IL}	-10	-	+10	µA	V_{IN} = 0 V
High Input Leakage	I_{IH}	-10	-	+10	µA	V_{IN} = V_{DD33}
O12 Type Buffer						
Low Output Level	V_{OL}	-	-	0.4	V	I_{OL} = 6 mA @ V_{DD33} = 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4	-	-	V	I_{OH} = -6 mA @ V_{DD33} = 3.3 V
Output Leakage	I_{OL}	-10	-	+10	µA	V_{IN} = 0 to V_{DD33} (Note 8.4)
I/O12, I/O12PU & I/O12PD Type Buffer						
Low Output Level	V_{OL}	-	-	0.4	V	I_{OL} = 6 mA @ V_{DD33} = 3.3 V
High Output Level	V_{OH}	V_{DD33} - 0.4	-	-	V	I_{OH} = -6 mA @ V_{DD33} = 3.3 V
Output Leakage	I_{OL}	-10	-	+10	µA	V_{IN} = 0 to V_{DD33} (Note 8.4)
Pull Down	PD	-	72	-	µA	
Pull Up	PU	-	58	-	µA	
IO-U						(Note 8.5)
I-R						(Note 8.6)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Integrated Power FET Set to 200 mA						
Output Current (Note 8.7)	I_{OUT}	-	200	-	mA	$Vdrop_{FET} \approx 0.46$ V
Short Circuit Current Limit	I_{SC}	-	181	-	mA	$Vout_{FET} = 0$ V
On Resistance (Note 8.7)	R_{DSON}	-	-	2.1	Ω	$I_{FET} = 70$ mA
Output Voltage Rise Time	t_{DSON}	-	800	-	µs	$C_{LOAD} = 10$ µF
48QFN						
Supply Current Unconfigured Hi-Speed Host Full Speed Host	 $I_{CCINTHS}$ $I_{CCINITFS}$	 - -	 - -	 75 70	 mA mA	Note 8.8
Supply Current Active HS Host (Note 8.9)	I_{CC}	-	-	330	mA	
Supply Current Suspend	I_{CSBY}	-	-	2500	µA	
Supply Current Reset	I_{RST}	-	-	2500	µA	
64QFN						
Supply Current Unconfigured Hi-Speed Host Full Speed Host	 $I_{CCINTHS}$ $I_{CCINITFS}$	 - -	 TBD TBD	 TBD TBD	 mA mA	Note 8.8
Supply Current Active HS Host	I_{CC}	-	TBD	TBD	mA	
Supply Current Suspend	I_{CSBY}	-	TBD	TBD	µA	
Supply Current Reset	I_{RST}	-	TBD	TBD	µA	

Note 8.4 Output leakage is measured with the current pins in high impedance.

Note 8.5 See the USB 2.0 Specification, Chapter 7, for USB DC electrical characteristics.

Note 8.6 RBIAS is a 3.3 V tolerant analog pin.

Note 8.7 Output current range is controlled by program software. The software disables the FET during short circuit condition.

Note 8.8 Supply currents do not include power FET currents.

Note 8.9 HS Host, 2 ports active, MS Card active.

8.5 Capacitance

T_A = 25 °C; fc = 1 MHz; V_{DD33} = 3.3 V, V_{DD18} = 1.8 V

Table 8.3 Pin Capacitance

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
XTAL Pin Input Capacitance	C_{XTAL}	-	-	4	pF	All pins (except USB pins and pins under test) are tied to AC ground.
Input Capacitance	C_{IN}	-	-	10	pF	

Chapter 9 AC Specifications

9.1 Oscillator/Crystal

Parallel Resonant, Fundamental Mode, 24 MHz ± 350 ppm.

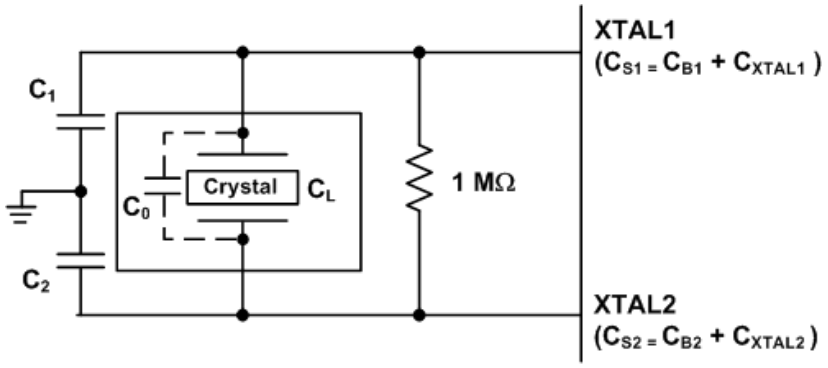


Figure 9.1 Typical Crystal Circuit

Table 9.1 Crystal Circuit Legend

SYMBOL	DESCRIPTION	IN ACCORDANCE WITH
C_0	Crystal shunt capacitance	Crystal manufacturer's specification (see Note 9.1)
C_L	Crystal load capacitance	
C_B	Total board or trace capacitance	OEM board design
C_S	Stray capacitance	SMSC IC and OEM board design
C_{XTAL}	XTAL pin input capacitance	SMSC IC
C_1	Load capacitors installed on OEM board	Calculated values based on Figure 9.2, "Capacitance Formulas" (see Note 9.2)
C_2		

$$C_1 = 2 \times (C_L - C_0) - C_{S1}$$

$$C_2 = 2 \times (C_L - C_0) - C_{S2}$$

Figure 9.2 Capacitance Formulas

Note 9.1 C_0 is usually included (subtracted by the crystal manufacturer) in the specification for C_L and should be set to 0 for use in the calculation of the capacitance formulas in Figure 9.2, "Capacitance Formulas". However, the OEM PCB itself may present a parasitic capacitance between **XTAL1** and **XTAL2**. For an accurate calculation of C_1 and C_2, take the parasitic capacitance between traces **XTAL1** and **XTAL2** into account.

Note 9.2 Each of these capacitance values is typically approximately 18 pF.

9.2 Ceramic Resonator

24 MHz ± 350 ppm

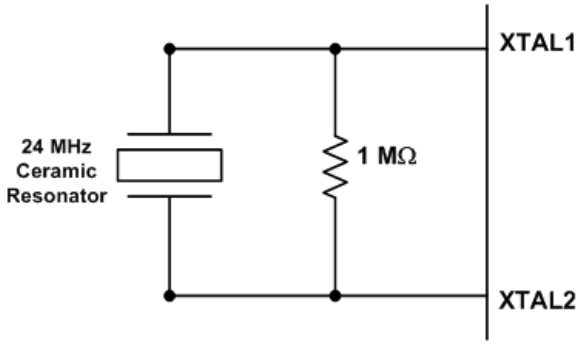


Figure 9.3 Ceramic Resonator Usage with SMSC IC

9.3 External Clock

50% Duty cycle ± 10%, 24 MHz ± 350 ppm, Jitter < 100 ps rms

The external clock is recommended to conform to the signaling level designated in the *JESD76-2 Specification* [5] on 1.8 V CMOS Logic. XTAL2 should be treated as a no connect.

9.3.1 I²C EEPROM

Frequency is fixed at 58.6 kHz ± 20%.

9.3.2 USB 2.0

The SMSC device conforms to all voltage, power, and timing characteristics and specifications as set forth in the *USB 2.0 Specification* [1]. Refer to the *USB 2.0 Specification* for more information.

Chapter 10 GPIO Usage

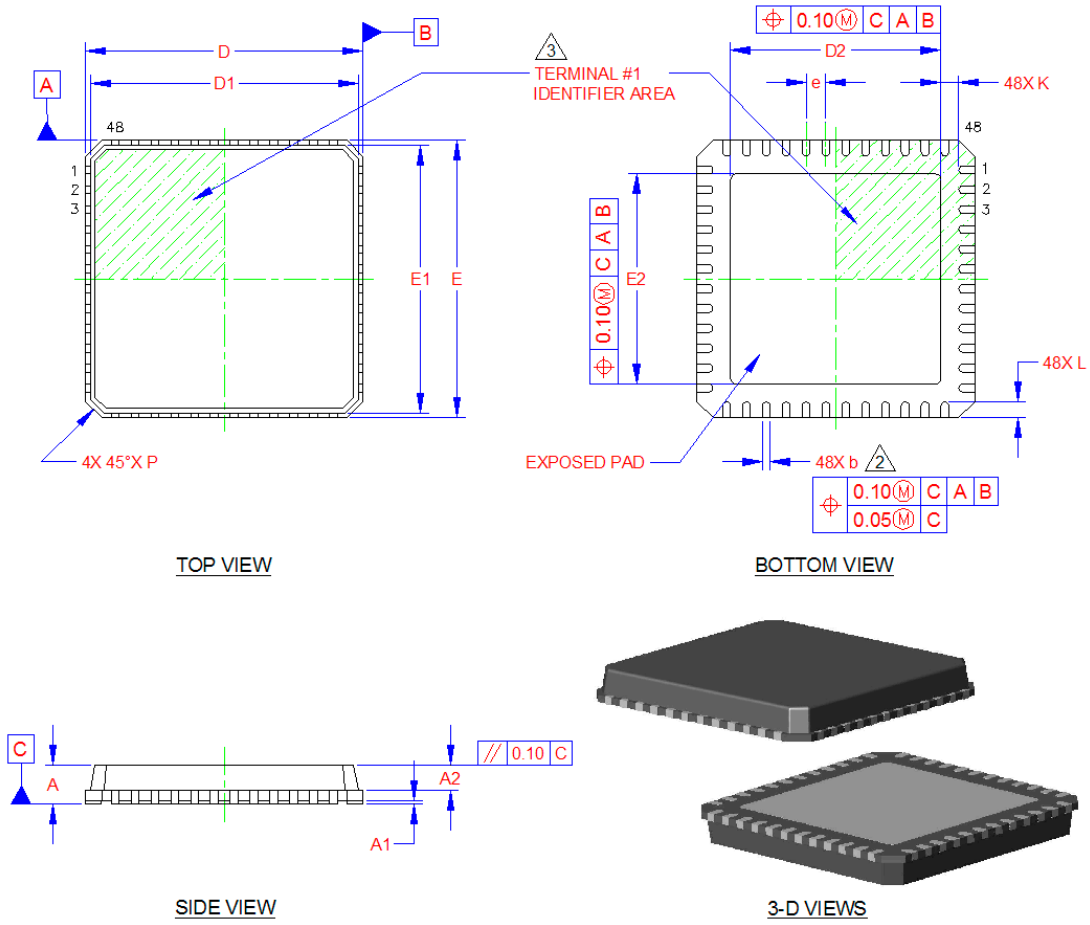
Table 10.1 USB82640 GPIO Usage

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED/TxD	LED indicator/Serial port transmit line
GPIO2	H	RxD	Serial port receive line
GPIO4	H	SCK	Serial EEPROM clock
GPIO5	H	SDA	Serial EEPROM data
GPIO6	L	SD_WP	SD card write protect assertion
GPIO10	L	CRD_PWR_CTRL	Card power control
GPIO12	L	MS_nCD	Memory Stick card detect
GPIO14	L	GPIO	User defined
GPIO15	L	SD_nCD	Secure Digital card detect

Table 10.2 USB82660 GPIO Usage

NAME	ACTIVE LEVEL	SYMBOL	DESCRIPTION AND NOTE
GPIO1	H	LED/TxD	LED indicator/Serial port transmit line
GPIO2	H	RxD	Serial port receive line
GPIO4	H	SCK	Serial EEPROM clock
GPIO5	H	SDA	Serial EEPROM data
GPIO6	L	SD1_WP	SD card write protect
GPIO8	L	CRD_PWR_CTRL	Card power control
GPIO10	L	CRD_PWR_CTRL	Card power control
GPIO12	L	MS_nCD	Memory Stick card detect
GPIO14	L	GPIO	User defined
GPIO15	L	SD1_nCD	Secure Digital card detect
GPIO16	L	SD2_nCD	SD2 card detect
GPIO17	L	SD2_WP	SD2 card write protect
GPIO[25:18]	H	SD2_D[7:0]	SD2 data
GPIO26	H	SD2_CLK	Output clock signal to the SD/MMC2 device
GPIO27	H	SD2_CMD	SD/MMC2 CMD signal

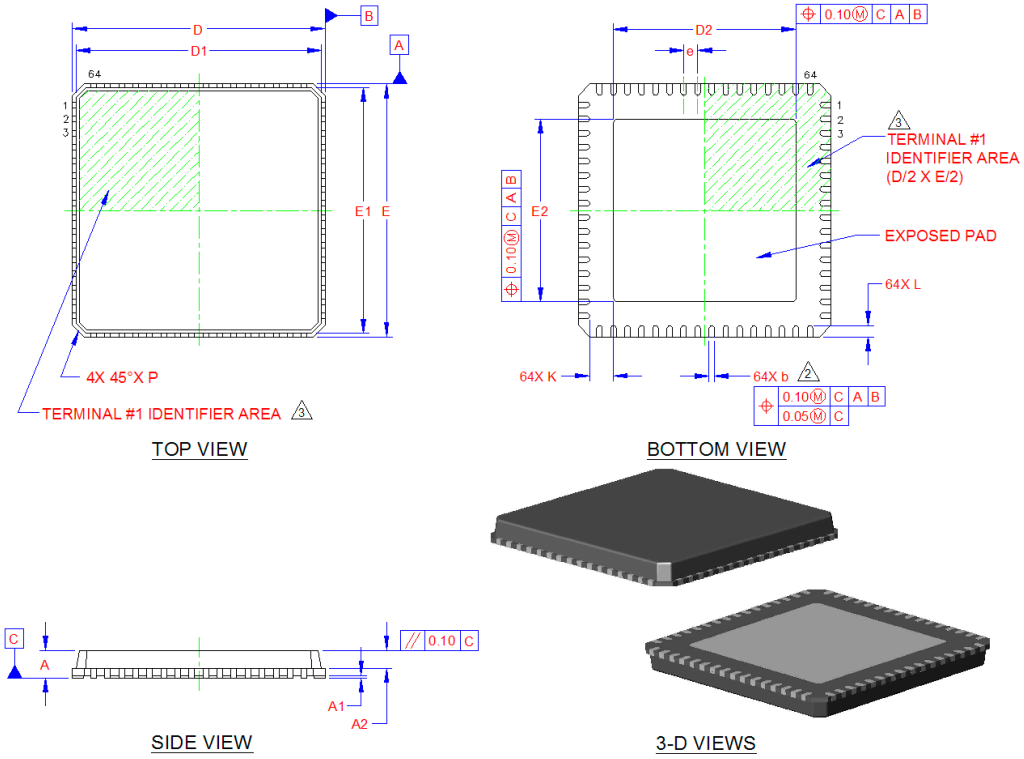
Chapter 11 Package Outlines



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.01	0.05	-	STANDOFF
A2	0.60	0.65	0.70	-	MOLD CAP THICKNESS
D/E	6.90	7.00	7.10	-	X/Y BODY SIZE
D1/E1	6.65	6.75	6.85	-	X/Y MOLD CAP SIZE
D2/E2	5.20	5.30	5.40	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.23	0.30	2	TERMINAL WIDTH
K	-	0.45	-	-	CENTER PAD TO PIN CLEARANCE
P	0.24	0.42	0.60	-	PACKAGE CORNER CHAMFER
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 11.1 USB82640 48-Pin QFN



COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.01	0.05	-	STANDOFF
A2	0.60	0.65	0.70	-	MOLD CAP THICKNESS
D/E	8.90	9.00	9.10	-	X/Y BODY SIZE
D1/E1	8.65	8.75	8.85	-	X/Y MOLD CAP SIZE
D2/E2	6.40	6.50	6.60	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.23	0.30	2	TERMINAL WIDTH
K	-	0.85	-	-	CENTER PAD TO PIN CLEARANCE
P	0.24	0.42	0.60	-	PACKAGE CORNER CHAMFER
e	0.50 BSC			-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 11.2 USB82660 64-Pin QFN

Appendix A (Acronyms)

ACRONYM	DESCRIPTION
ACK	Handshake packet (positive acknowledgement)
EOF	End of (micro) Frame
EOP	End of Packet
FMC	Flash Media Controller
FS	Full-Speed Device
HS	Hi-Speed Device
I²C™	Inter-Integrated Circuit[a]
LS	Low-Speed Device
LUN	Logical Unit Number
MMC	MultiMediaCard

ACRONYM	DESCRIPTION
MSC	Memory Stick Controller
OCS	Over-current Sense
PHY	Physical Layer
PLL	Phase-Locked Loop
RXD	Received eXchange Data
SDC	Secure Digital Controller
TXD	Transmit eXchange data
UART	Universal Asynchronous Receiver-Transmitter
UCHAR	Unsigned Character
UINT	Unsigned Integer

a. I²C is a trademark of Philips Corporation.

Appendix B (References)

[1] Universal Serial Bus Specification, Version 2.0, April 27, 2000 (12/7/2000 and 5/28/2002 Errata)
USB Implementers Forum, Inc. http://www.usb.org

[2] I^2C-Bus Specification Version 1.1
NXP (formerly a division of Philips). http://www.nxp.com

[3] System Management Bus Specification, version 1.0
SMBus. http://smbus.org/specs/

[4] MicroChip 24AA02/24LC02B (Revision C)
Microchip Technology Inc. http://www.microchip.com/

[5] JEDEC Specifications: JESD76-2 (June 2001) and J-STD-020D.1 (March 2008)
JEDEC Global Standards for the Microelectronics Industry.http://www.jedec.org/standards-documents

Revision History

Table 11.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.2 (06-20-11)	Section 7.3.3.35	Updated register description to indicate new function.
	Table 7.1	Cleaned up Table 7.1 for clarity.
Rev. 1.1 (10-12-10)	Page 2	Ordering information completed.
Rev. 1.1 (07-07-10)	Section 5.1, "USB82640/60 Pin Descriptions"	GPIO8 and GPIO10 pin description: Some values adapted.
	Section 7.3.2, "EEPROM Data Descriptor"	Table 7.1: Value corrected for LUN Power Hi Byte.
	Section 7.3.2.11, "A4h-A5h: LUN 0 Power Configuration"	Default values adapted.
	Section 7.3.4.10, "14Ch-14Dh: LUN 1 Power Configuration"	Default values adapted.
	Section Chapter 8, "DC Parameters"	XTAL2 and hysteresis removed. Typical values added, Min values removed. TBD replaced by correct values in section referring to 48QFN.
	Section 8.1, "Maximum Guaranteed Ratings" and Section 8.2, "Operating Conditions"	Row that shows Voltage on USB+ and USB- pins removed as the USB pins are covered in row 'Voltage on any signal pin'.

Further Information

For more information on SMSC automotive products, including integrated circuits, software, and MOST® development tools and modules, visit our web site: http://www.smsc-ais.com. Direct contact information is available at: http://www.smsc-ais.com/offices.

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