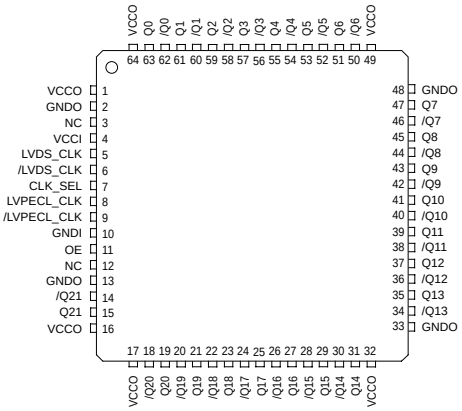
PACKAGE/ORDERING INFORMATION



64-Pin TQFP (H64-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89826LHI	H64-1	Industrial	SY89826LHI	Sn-Pb
SY89826LHITR[2]	H64-1	Industrial	SY89826LHI	Sn-Pb
SY89826LHY[3]	H64-1	Industrial	SY89826LHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89826LHYTR[2, 3]	H64-1	Industrial	SY89826LHY with Pb-Free bar-line indicator	Pb-Free Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTIONS

Pin Number	Pin Name	I/O	Type	Internal Pull-up/ Pull-down	Pin Function
5, 6	LVDS_CLK /LVDS_CLK	Input	LVDS w/100Ω internal terminator	3.3kΩ pull-up (Figure 2)	Differential LVDS clock input. Selected when CLKSEL = LOW (Can be left floating if CLKSEL = HIGH). This input pair includes internal termination, and is intended to interface directly to LVDS. Leave floating if not used.
8, 9	LVPECL_CLK /LVPECL_CLK	Input	LVPECL	75kΩ pull-down (Figure 1)	Differential LVPECL clock input. Selected when CLKSEL = HIGH (Can be left floating if CLKSEL = LOW). Requires external termination. Leave floating if not used.
7	CLK_SEL	Input	LVTTL/ CMOS	11kΩ to VCCI	Selects LVDS_CLK when LOW and LVPECL_CLK when HIGH. Default condition is HIGH if left floating.
11	OE	Input	LVTTL/		Output enable/disable function. When LOW, Q outputs go LOW, /Q outputs go HIGH. Asynchronous input that is synchronized internally to prevent output glitches or runt pulses.
63, 61, 59, 57, 55, 53, 51, 47, 45, 43, 41, 39, 37, 35, 31, 29, 27, 25, 23, 21, 19, 15	Q0 – Q21	Output	LVDS		Differential LVDS clock outputs when OE = HIGH and static LOW when OE = LOW. Unused output pairs must be terminated with 100Ω across the differential pair to maintain low skew and jitter.
62, 60, 58, 56, 54, 52, 50, 46, 44, 42, 40, 38, 36, 34, 30, 28, 26, 24, 22, 20, 18, 14	/Q0 – /Q21	Output	LVDS		Differential clock outputs (complement) when OE = HIGH and static HIGH when OE = LOW. Unused output pairs must be terminated with 100Ω across the differential pair to maintain low skew and jitter.
4	VCCI	Power			Core VCC connect to 3.3V supply. Not connected to VCCO internally. Connect to VCCO on PCB. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to VCC pins as possible.
1, 16, 17, 32, 49, 64	VCCO	Power			Output buffer VCC connects to 3.3V supply. Not connected to VCCI internally. Connect to VCCI on PCB. Bypass with 0.1µF in parallel with 0.01µF low ESR capacitors as close to VCC pins as possible.
10	GNDI	Power			Core ground not connected to GNDO internally. Connect to GNDO on PCB.
2, 13, 33, 48	GNDO	Power			Output buffer ground not connected to GNDI internally. Connect to GNDI on PCB.
3, 12	NC				No connect pins to be left open.

Downloaded from Arrow.com.

Absolute Maximum Ratings(Note 1)

Power Supply Voltage (V_{CCI}, V_{CCO}) ..... –0.5 to +4.0V
Input Voltage (V_{IN}) ..... –0.5 to V_{CCI}
Output Current (I_{OUT}) ..... ±10mA
Lead Temperature (T_{LEAD}, Soldering, 20sec.) ..... 260°C
Storage Temperature (T_S) ..... –65 to +150°C
ESD Rating, **Note 3** ..... >1kV

Operating Ratings(Note 2)

Supply Voltage (V_{CC} to GND) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance
TQFP (θ_{JA})
Exposed pad soldered to GND
Still-Air(multi-layer PCB) ..... 23°C/W
–200lfpm (multi-layer PCB) ..... 18°C/W
–500lfpm (multi-layer PCB) ..... 15°C/W
Exposed pad NOT soldered to GND (not recommened)
Still-Air(multi-layer PCB) ..... 44°C/W
–200lfpm (multi-layer PCB) ..... 36°C/W
–500lfpm (multi-layer PCB) ..... 30°C/W
TQFP (θ_{JC}) ..... 4.4°C/W

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Devices are ESD sensitive. Handling precautions recommended.

DC ELECTRICAL CHARACTERISTICS

Power Supply: T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCI}, V_{CCO}	V_{CC} Core, V_{CC} Output	**Note 4**	3.0	3.3	3.6	V
I_{CCI}	I_{CC} Core	Max. V_{CC}		46	70	mA
I_{CCO}	I_{CC} Output	No Load, Max. V_{CC}		175	260	mA

Note 4. V_{CCI} and V_{CCO} must be connected together on the PCB such that they remain at the same potential. V_{CCI} and V_{CCO} are not internally connected on the die.

LVDS Input: V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range		0		2.4	V
V_{ID}	Differential Input Swing		100			mV
I_{IL}	Input LOW Current		–1.25			mA
R_{IN}	LVDS Differential Input Resistance (LVDS_CLK to /LVDS_CLK)		80	100	120	Ω

Downloaded from Arrow.com.

DC ELECTRICAL CHARACTERISTICS

LVPECL Input: V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage (Single-Ended)		V_{CC} –1.165		V_{CC} –0.880	V
V_{IL}	Input LOW Voltage		V_{CC} –1.945		V_{CC} –1.625	V
V_{PP}	Minimum Input Swing (LVPECL_CLK)	**Note 6**	300			mV
V_{CMR}	Common Mode Range (LVPECL_CLK)	**Note 7**	GNDI +1.8		V_{CCI} –0.4	V
I_{IH}	Input HIGH Current				150	µA
I_{IL}	Input LOW Current		0.5			µA

Note 6. The V_{PP} (min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.

Note 7. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI}. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP} (min.). V_{CMR} range varies 1:1 with V_{CCI}. V_{CMR} (min) is fixed at GNDI +1.8V.

CMOS/LVTTL Inputs: V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current	$V_{IN} = V_{CC}$			150	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V	–600			µA

LVDS Output: V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage	**Note 8, 9**	250	350	400	mV
V_{OH}	Output HIGH Voltage	**Note 8**			1.474	V
V_{OL}	Output LOW Voltage	**Note 8**	0.925			V
V_{OCM}	Output Common Mode Voltage	**Note 9**	1.125		1.375	V
ΔV_{OCM}	Change in Common Mode Voltage		–50		50	mV

Note 8. Measured as per Figure 3, 100Ω across Q and /Q outputs.

Note 9. Measured as per Figure 4.

Downloaded from Arrow.com.

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 3.3V ±10%, T_A = –40°C to +85°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Toggle Frequency	**Note 2**	1.0			GHz
t_{PHL} t_{PLH}	Differential Propagation Delay, **Note 3**	LVPECL Input: 150mV LVPECL Input: 800mV	0.750 0.6	1.0 0.850	1.250 1.10	ns ns
		LVDS Input: 100mV LVDS Input: 400mV	0.950 0.800	1.2 1.0	1.450 1.30	ns ns
$t_{SWITCHOVER}$	Clock Input Switchover	CLK_SEL-to-Valid Output		1.4	1.7	ns
$t_{S(OE)}$	Output Enable Set-Up Time	**Note 4**	1.0			ns
$t_{H(OE)}$	Output Enable Hold Time	**Note 4**	0.5			ns
t_{skew}	Within Device Skew	**Note 5** 0°C to +85°C –40°C		25	50 75	ps ps
	Part-to-Part Skew	**Note 6**			400	ps
t_{JITTER}	Cycle-to-Cycle Total Jitter	**Note 7** **Note 8**		<1	1 2	ps_{RMS} ps_{PP}
t_r, t_f	Output Rise/Fall Times (20% to 80%)		200	290	400	ps

Note 1. 100Ω termination between Q and /Q outputs. Airflow ≥300lfpm, or exposed pad soldered to ground plane. Typicals are at nominal supply, T_A = 25°C.

Note 2. f_{MAX} is defined as the maximum toggle frequency, measured with a 750mV LVPECL input or 350mV LVDS input. Output swing is ≥ 200mV.

Note 3. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.

Note 4. Set-up and hold time applies to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold time does not apply. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW to HIGH transition enables normal operation of the next input clock.

Note 5. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device with identical input transition, operating at the same voltage and temperature.

Note 6. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature. Part-to-part skew is the total skew difference; pin-to-pin skew + part-to-part skew.

Note 7. Cycle-to-cycle jitter definition: The variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{JITTER\_CC} = T_n - T_{n+1}$ where T is the time between rising edges of the output signal.

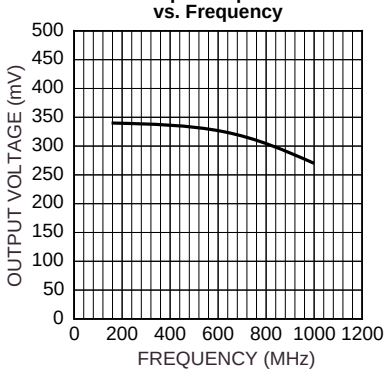
Note 8. Total jitter definition: with an ideal clock input, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Downloaded from Arrow.com.

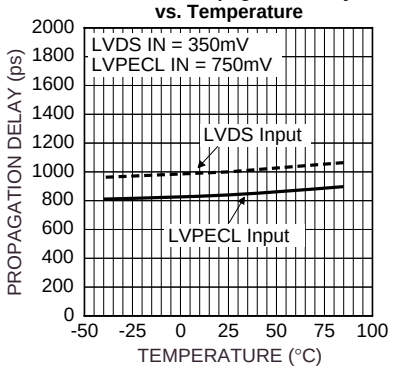
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{EE} = GND, T_A = 25°C, unless otherwise stated

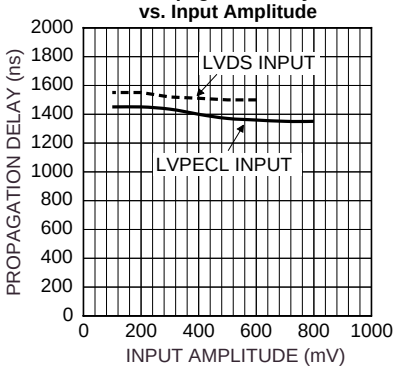
Output Amplitude vs. Frequency



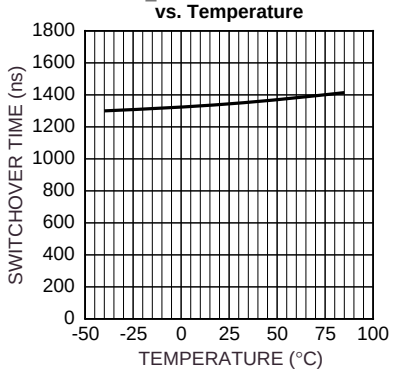
Nominal Propagation Delay vs. Temperature



Propagation Delay vs. Input Amplitude



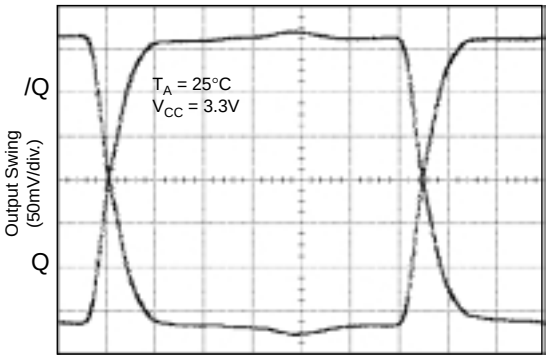
CLK_SEL Switchover Time vs. Temperature



Downloaded from Arrow.com.

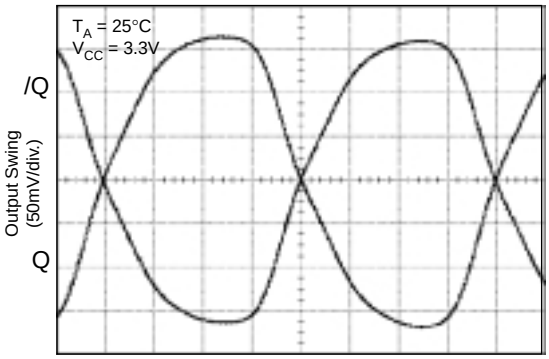
FUNCTIONAL CHARACTERISTICS

155MHz Output



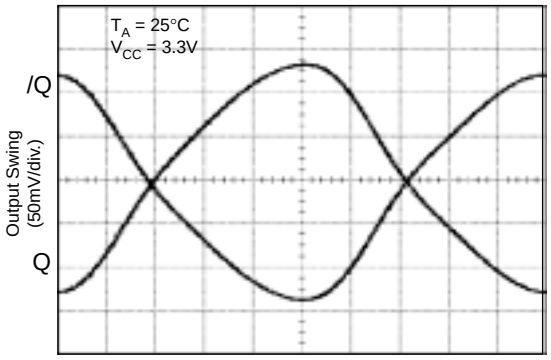
TIME (500ps/div.)

622MHz Output



TIME (200ps/div.)

1GHz Output



TIME (100ps/div.)

Downloaded from Arrow.com.

LVPECL/LVDS INPUTS

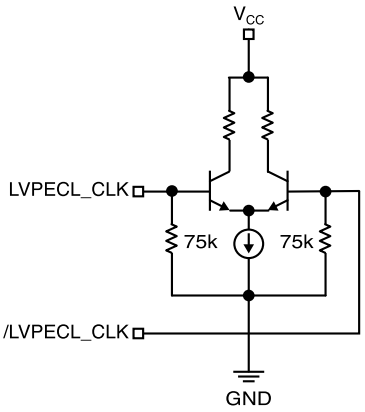


Figure 1. Simplified LVPECL Input Stage

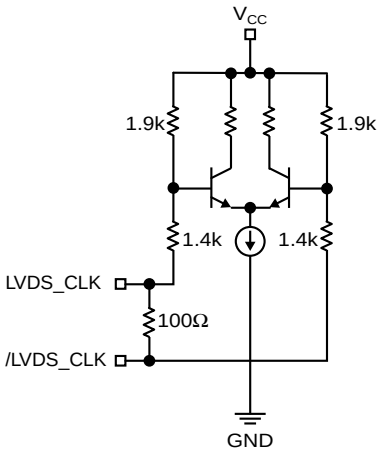


Figure 2. Simplified LVDS Input Stage

LVDS OUTPUTS

LVDS specifies a small swing of 350mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is also kept tight, to keep EMI low.

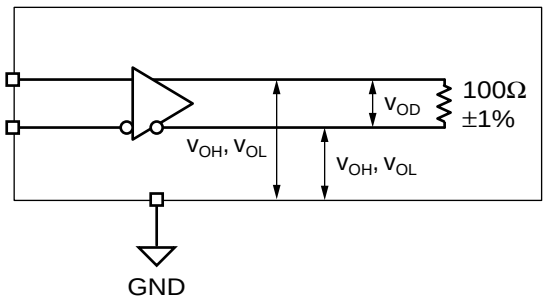


Figure 3. LVDS Differential Measurement

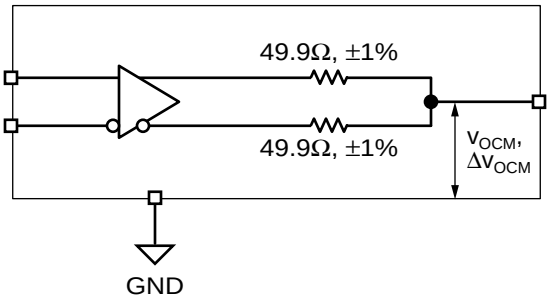


Figure 4. LVDS Common Mode Measurement

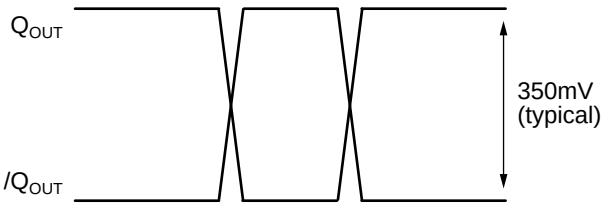


Figure 5. Output Driver Signal Levels (Single-Ended)

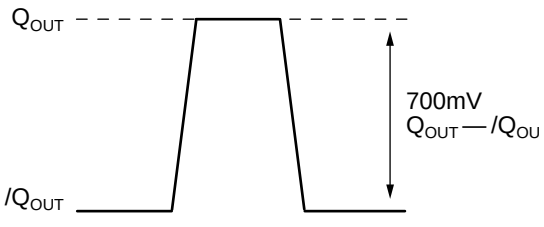


Figure 6. Output Driver Signal Levels (Differential)

Downloaded from Arrow.com.

DETAILED DESCRIPTION

The SY89826L is a precision 1:22 fanout buffer. It accepts either an LVPECL or LVDS input, selectable by an input mux, and outputs 22 LVDS output pairs. The device features a synchronous output enable. The SY89826L provides extremely low skew across its outputs.

LVPECL_CLK

The SY89826L allows one input with standard LVPECL voltage swing. This input may be adjusted per the data sheet characteristics regarding the CMR and minimum input swing. As the SY89826L contains no appropriate internal termination, upstream devices need to be properly terminated to provide the proper LVPECL input swing. If not being used (CLK_SEL is LOW), this input pair may be left floating, as it is internally terminated to ground via a 75kΩ pull-down resistor.

LVDS_CLK

The SY89826L allows one input with standard LVDS voltage swing. The SY89826L provides an appropriate internal 100Ω termination resistor. Hence, upstream LVDS devices do not require external termination to drive the SY89826L. If not being used (CLK_SEL is HIGH), this input pair may be left floating.

CLK_SEL Input

The CLK_SEL TTL Input is used to select either LVDS_CLK (CLK_SEL is LOW) or LVPECL_CLK (CLK_SEL is LOW),.

OE

The SY89826L's output enable function is designed to disable the outputs only when the outputs are LOW. This avoids the possibility of generating runt pulses. The OE input is an asynchronous input, but operates as a synchronous enable. For synchronous operation, please adhere to the specific setup and hold times. When disabled, the Q outputs are LOW and the /Q outputs are HIGH.

LVDS Outputs

The SY89826L's LVDS outputs swing typically 350mV around a 1.25V common mode voltage above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input is kept tight to keep EMI low.

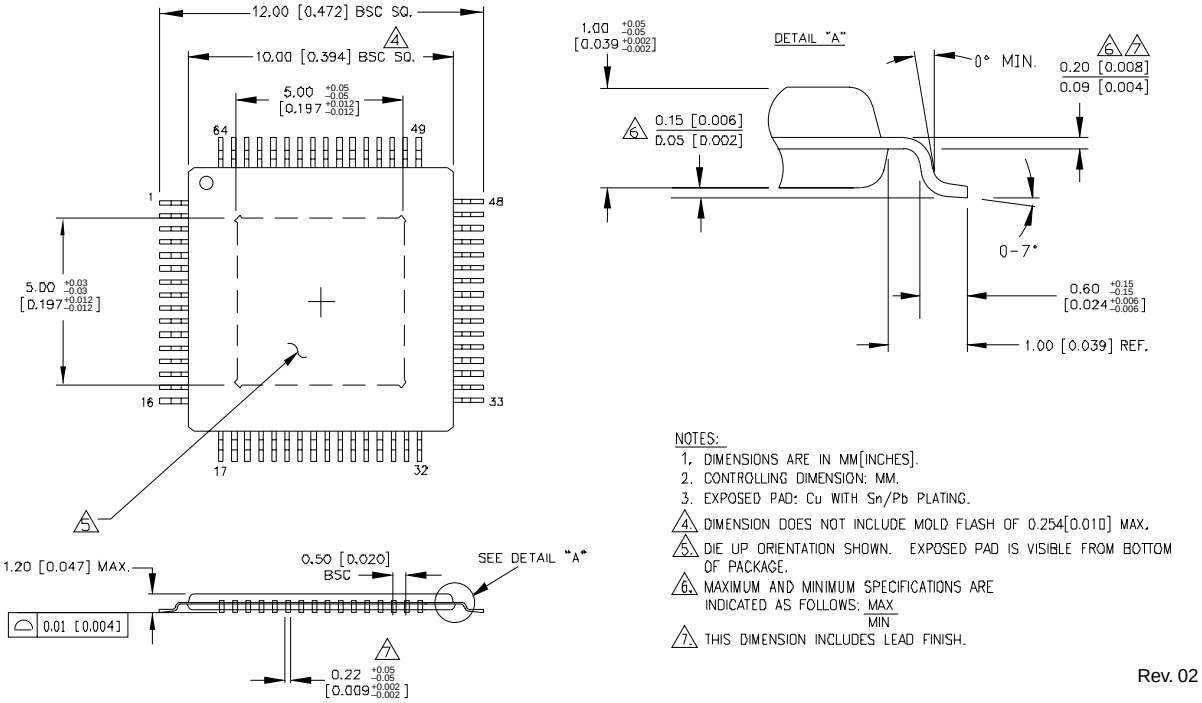
Each of the SY89826L's LVDS outputs should be terminated with a 100Ω termination resistor including any unused output pairs. This ensures the best jitter and skew performance of the device.

RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY55855V	Dual CML/PECL/LVPECL-to-LVDS Translator	www.micrel.com/product-info/products/sy55855v.shtml
SY89825U	2.5/3.3V 1:22 High-performance, Low-voltage PECL Bus Clock Driver & Translator w/ Internal Termination	www.micrel.com/product-info/products/sy89825u.shtml
SY89828L	3.3V 1GHz Dual 1:10 Precision LVDS Fanout Buffer with 2:1 Input Mux	www.micrel.com/product-info/products/sy89828l.shtml
SY89829U	2.5/3.3V High-performance, Dual 1:10 LVPECL Clock Driver w/ Internal Termination & Redundant Switchover	www.micrel.com/product-info/products/sy89829u.shtml
M-0317	HBW Solutions	www.micrel.com/product-info/as/solutions.shtml
Exposed Pad	Amkor Exposed Pad Application Note	www.amkor.com/products/notes_papers/epad.pdf

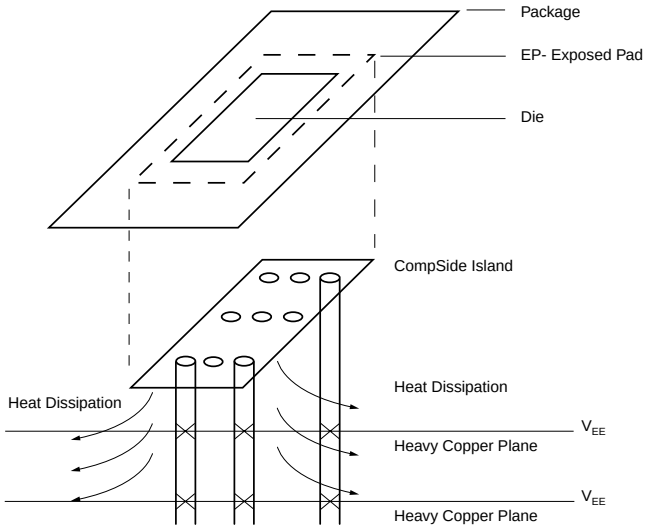
Downloaded from Arrow.com.

64-PIN EPAD-TQFP (DIE UP) (H64-1)



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
4. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
5. DIE UP ORIENTATION SHOWN. EXPOSED PAD IS VISIBLE FROM BOTTOM OF PACKAGE.
6. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX / MIN
7. THIS DIMENSION INCLUDES LEAD FINISH.

Rev. 02



PCB Thermal Consideration for 64-Pin EPAD-TQFP Package

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is at Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2005 Micrel, Incorporated.

Downloaded from Arrow.com.