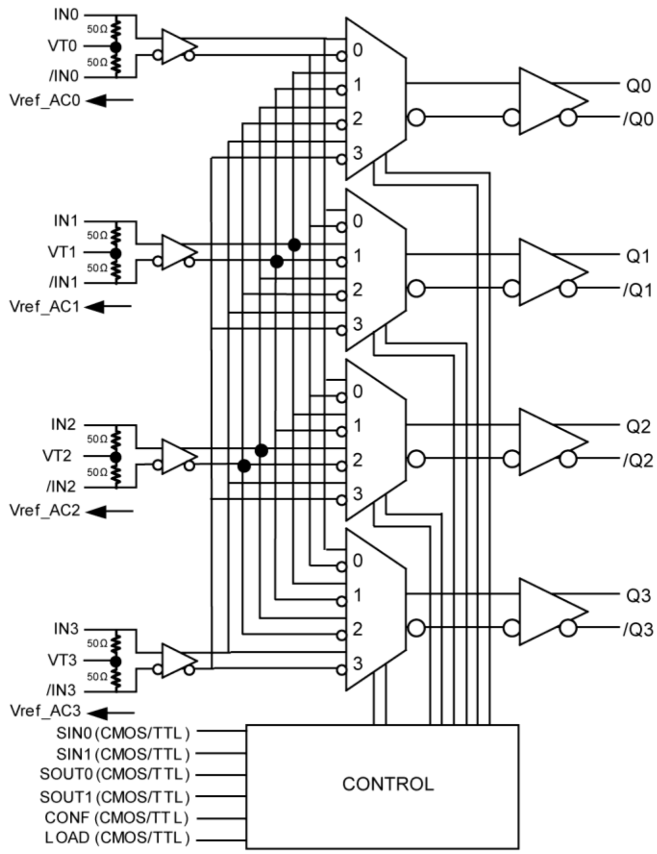
Functional Block Diagram



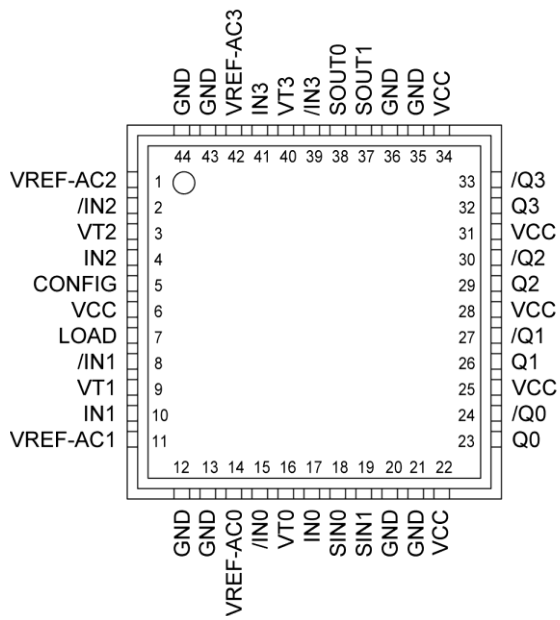
Ordering Information[1]

Part Number	Package Type	Temperature Range	Package Marking	Lead Finish
SY89540UMY	QFN-44	Industrial	SY89540U with Pb-Free bar-line indicator	Pb-Free Matte-Sn
SY89540UMYTR[2]	QFN-44	Industrial	SY89540U with Pb-Free bar-line indicator	Pb-Free Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electrical only.
2. Tape and Reel ordering option.

Pin Configuration



44-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
17, 15, 10, 8 4, 2 41, 39	IN0, /IN0, IN1, /IN1, IN2, /IN2, IN3, /IN3	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Please refer to the "Input Interface Applications" section for more details.
16, 9, 3, 40	VT0, VT1, VT2, VT3	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section for more details.
14, 11, 1, 42	VREF_AC0, VREF_AC1, VREF_AC2, VREF_AC3	Reference Voltage: This output biases to V_{CC}–1.2V. It is used when AC-coupling the inputs (IN, /IN). Connect VREF_AC to the VT pin. Bypass each VREF-AC pin with a 0.01μF low ESR capacitor. See "Input Interface Applications" section for more details.
18, 19	SIN0, SIN1	These single-ended TTL/CMOS-compatible inputs address the data inputs. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
38, 37	SOUT0, SOUT1	These single-ended TTL/CMOS-compatible inputs address the data outputs. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open.
5, 7	CONF, LOAD	These single-ended TTL/CMOS-compatible inputs control the transfer of the addresses to the internal multiplexers. See "Address Tables" and "Timing Diagram" sections for more details. Note that these inputs are internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state if left open. *Configuration Sequence* 1. Load: Loads configuration into buffer, while Configuration Buffer holds existing switch configuration. 2. Configuration: Loads new configuration into the Configuration Buffer and updates switch configuration. *Buffer Mode* The SY89540U defaults to buffer mode (IN to Q) if the load and configuration control signals are not exercised.
23, 24, 26, 27, 29, 30, 32, 33	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3,	Differential Outputs: These LVDS output pairs are the outputs of the device. Please refer to the truth table below for details. Unused output pairs may be left open. Each output is designed to drive 350mV into 100Ω across the pair.
6, 22, 25, 28, 31, 34	VCC	Positive power supply. Bypass with 0.1μF//0.01μF low ESR capacitors and place as close to each V_{CC} pin.
12, 13, 20, 21,35, 36, 43, 44	GND, Exposed pad	Ground. GND and EPad must both be connected to the same ground.

Functional Description

Buffer Mode

SY89540 can be used as a 1:4 fanout buffer. This is the default mode with LOAD and CONFIG being HIGH when the device is first powered up. The SIN0 and SIN1 inputs select the input signal that will be buffered. Regardless of the output switch selection, the input signal will be buffered to all four outputs.

Crosspoint Mode

SY89540 can be programmed to take differential input signals from any input and buffer the signals to one or more outputs. Prior to configuring SIN and SOUT, LOAD and CONFIG must be LOW. To program the desired I/O combination, follow the following sequence:

1) Select the desired input with the SIN0 and SIN1 inputs and the output with the SOUT0 and SOUT1.
2) Pulse the LOAD with a positive pulse to load SIN and SOUT.
3) Pulse the CONFIG pin with a positive pulse to latched the I/O configuration.
4) This method can be used to create independent paths between inputs and outputs. Below is the truth table to create a 4:4 buffer where IN0 -> Q3, IN1 -> Q2, IN2 -> Q1, and IN3 -> Q0:

The SY89540 can be switched from crosspoint mode to a 1:4 fanout buffer simply by providing a LOW-to-HIGH pulse to the LOAD and CONFIG pins. The input configuration (SIN0:1) will select the desired input signal while the output switch will buffer the selected input signal. To get the same desired input to all four outputs (1:4), LOAD and CONFIG must be repeated four times to cover all outputs (i.e., SOUT0:1 must go through all four output combinations, repeated by LOAD and CONFIG).

Input	SIN1	SIN0	SOUT1	SOUT0	Load	Config.	Output
					↑ (pulse)	0	Q3
IN0	0	0	1	1	0	↑ (pulse)	
					↑ (pulse)	0	Q2
IN1	0	1	1	0	0	↑ (pulse)	
					↑ (pulse)	0	Q1
IN2	1	0	0	1	0	↑ (pulse)	
					↑ (pulse)	0	Q0
IN3	1	1	0	0	0	↑ (pulse)	

Table 1. 4:4 Buffer Truth Table

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ....–0.5V to +4.0V
Input Voltage (V_{IN}) ....–0.5V to V_{CC}
CML Output Voltage (V_{OUT}) .... V_{CC}–1.0V to V_{CC}+5.0V
Termination Current[3]
  Source or sink current on V_T .... ±100mA
Input Current
  Source or sink current on IN, /IN............. ±50mA
V_{REF-AC} Current
  Source or sink current on V_{REF-AC} .... ±2mA
Lead Temperature (soldering, 20sec.) ....260°C
Storage Temperature (T_s)............... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}).................. +2.375V to +2.625V
Ambient Temperature (T_A) .... –40°C to +85°C
Package Thermal Resistance[4]
  QFN (θ_{JA})
Still-air ....23°C/W
  QFN (ψ_{JB})
Junction-to-board ....12°C/W

DC Electrical Characteristics[5]

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply	V_{CC} = 2.5V	2.375	2.5	2.625	V
I_{CC}	Power Supply Current	No load, max. V_{CC}.		200	280	mA
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		40	50	60	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)		1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)		0		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	See Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage |IN, /IN|	See Figure 1b.	0.2			V
IN-to-V_T	Maximum Input Voltage |IN-to-V_T|				1.28	V
V_{REF-AC}	Reference Voltage		V_{CC}–1.3	V_{CC}–1.2	V_{CC}–1.1	V

Notes:

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to limited drive capability use for input of the same package only.
4. Assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB. Ψ_{JB} uses a 4-layer θ_{JA} in still-air unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

LVDS Outputs DC Electrical Characteristics

V_{CC} = 2.5V ±5%, T_A = –40°C to +85°C, R_L = 100Ω across Q and /Q, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage (Q, /Q)				1.475	V
V_{OL}	Output LOW Voltage (Q, /Q)		0.925			V
V_{OUT}	Output Voltage Swing (Q, /Q)	See Figure 1a.	250	350		mV
V_{DIFF_OUT}	Differential Output Voltage Swing |Q – /Q|	See Figure 1b.	500	700		mV
V_{OCM}	Output Common Mode Voltage (Q, /Q)	See Figure 4b.	1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage (Q, /Q)	See Figure 4b.	–50		+50	mV

LVTTL/CMOS DC Electrical Characteristics

V_{CC} = 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current	V_{IL} = 0V	–300			µA

AC Electrical Characteristics[7]

V_{CC} = 2.5V ±5%, T_A = –40°C to +85°C, R_L = 100Ω across each output pair, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data	3.2	4		Gbps
		Clock, V_{OUT} ≥200mV		4		GHz
t_{PD}	Propagation Delay	IN-to-Q	280	380	480	Ω
		CONFIG-to-Q	350		800	
t_{PD} Tempco				160		fs/°C
t_S	Set-up Time SIN-to-LOAD SOUT-to-LOAD LOAD-to-CONFIG CONFIG-to-LOAD		 800 800 800 950			ps
t_h	Hold Time LOAD-to-SIN, LOAD-to-SOUT		800			ps
t_{PW}	Minimum LOAD and CONFIG Pulse Width		800			ps
t_{SKEW}	Output-to-Output Skew Part-to-Part Skew	Note 8 Note 9			30 150	ps ps
t_{JITTER}	RMS Phase Jitter	Output = 622MHz Integration Range 12kHz – 20MHz		95		fs
	Crosstalk-Induced Jitter	Note 10			0.7	ps_{RMS}
t_r, t_r	Rise/Fall Times	At full output swing (20% to 80%)	40	80	120	ps

Notes:

7. High frequency AC-parameters are guaranteed by design and characterization.
8. Output to output skew is measured between two different outputs under identical transitions. Input voltage swing is ≥100mV.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
10. Crosstalk induced jitter is defined as the added jitter that results from signals applied to two adjacent channels. It is measured at the output while applying two similar, differential clock frequencies that are asynchronous with respect to each other at the inputs.

Single-Ended and Differential Swing

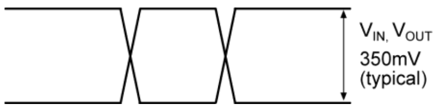


Figure 1a. Single-Ended Voltage Swing

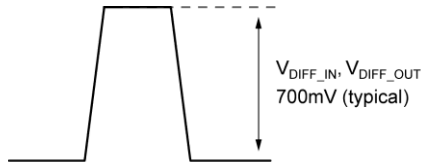
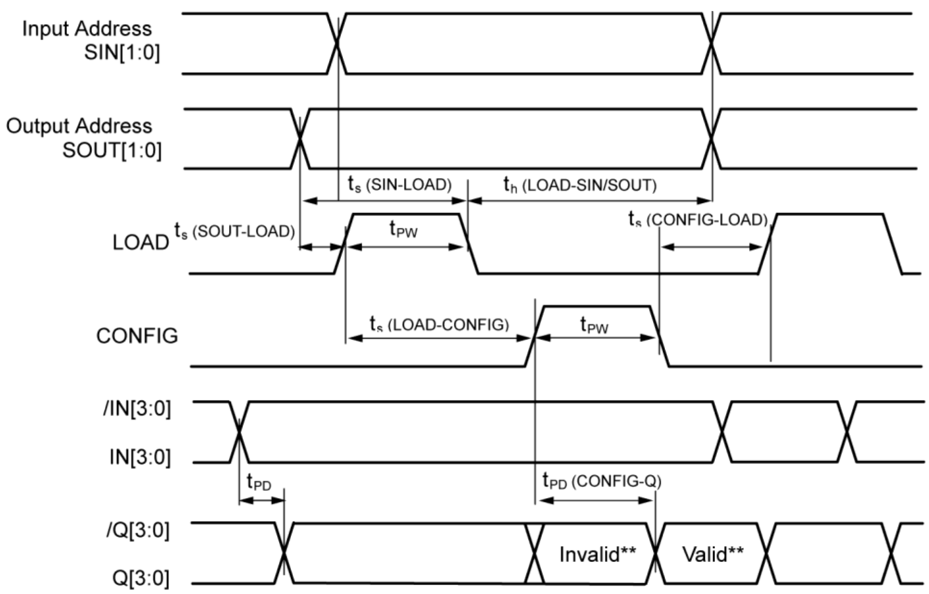


Figure 1b. Differential Voltage Swing

Timing Diagram



**Invalid and Valid refers to configuration being changed. All outputs with unchanged configuration remain valid.

Figure 2. Timing Diagram

Truth Tables

Input Select Address Table		
SIN1	**SIN0**	**Input**
0	0	IN0
0	1	IN1
1	0	IN2
1	1	IN3

Output Select Address Table		
SOUT1	**SOUT0**	**Output**
0	0	Q0
0	1	Q1
1	0	Q2
1	1	Q3

Typical Operating Characteristics

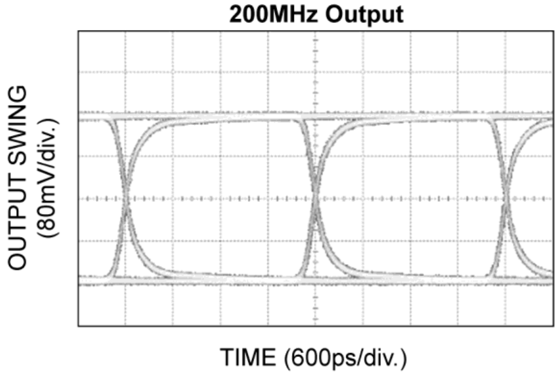
V_{CC} = 2.5, V_{IN} = 100mV, at 25°C.

Functional Characteristics

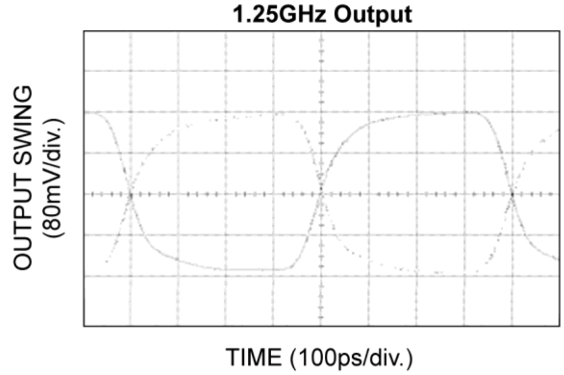
V_{CC} = 2.5, V_{IN} = 100mV, at 25°C.

Clock Pattern

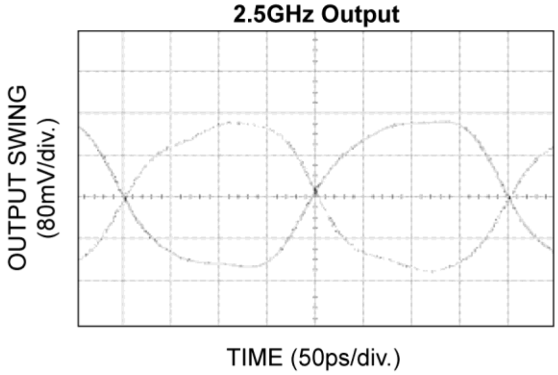
200MHz Output



1.25GHz Output

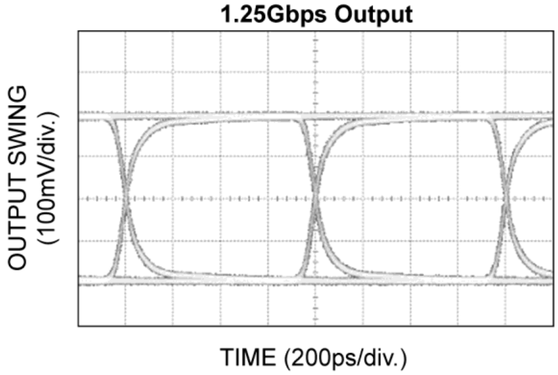


2.5GHz Output

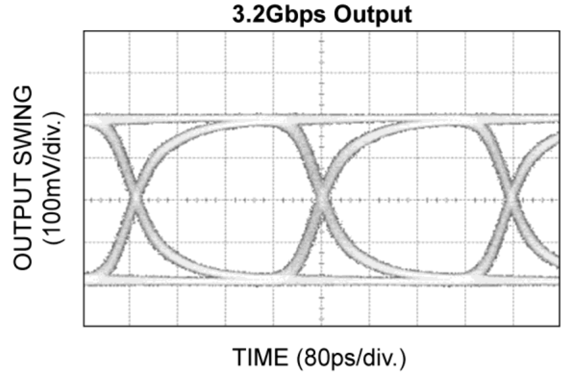


Data Pattern

1.25Gbps Output



3.2Gbps Output



Input and Output Stage Internal Termination

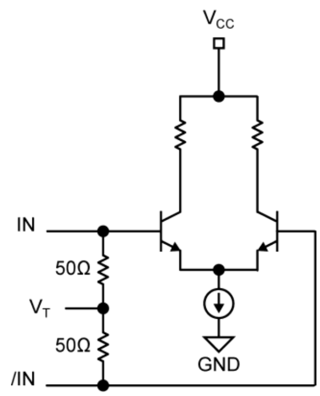


Figure 3. Simplified Differential Input Stage

Output Stage Internal Termination

On a nominal 1.25V common mode above ground, LVDS specifies a small swing of 350mV, typical. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum to keep EMI low.

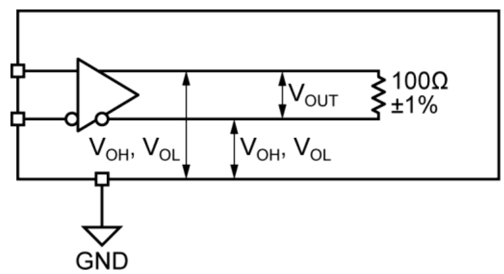


Figure 4a. LVDS Differential Measurement

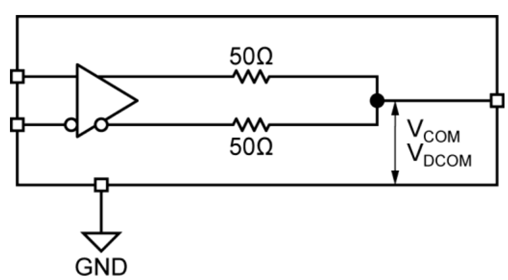


Figure 4b. LVDS Common Mode Measurement

Input Interface Applications

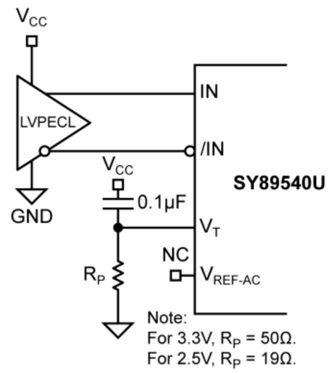


Figure 5a. LVPECL Interface (DC-Coupled)

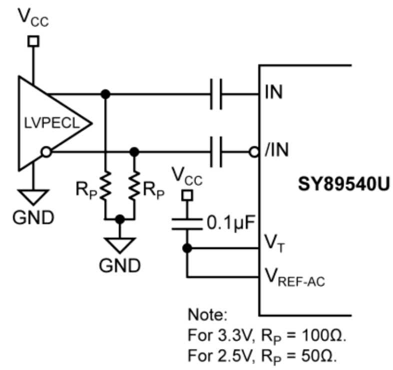


Figure 5b. LVPECL Interface (AC0Coupled)

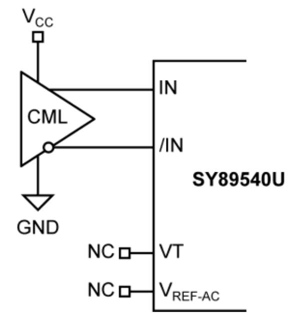


Figure 5c. CML Interface (DC-Coupled)

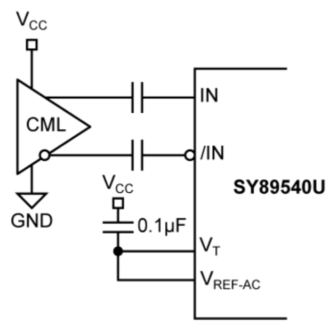


Figure 5d. CML Interface (AC-Coupled)

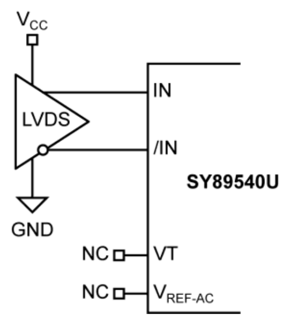
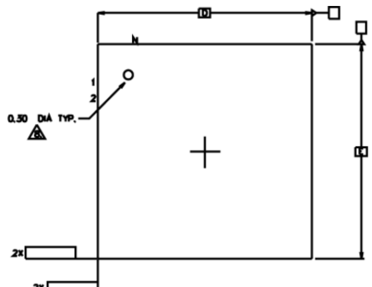


Figure 5e. LVDS Interface

Related Product and Support Documentation

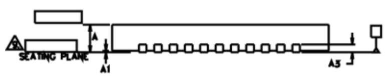
Part Number	Function	Datasheet Link
SY58540U	Ultra Precision 4x4 CML Crosspoint Switch w/Internal I/O Termination	http:///www.micrel.com/product-info/products/sy89540u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



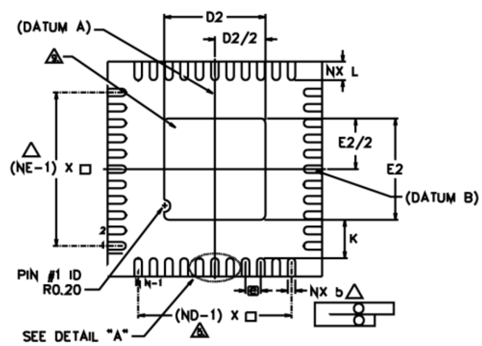
TOP VIEW

NOTES :
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220

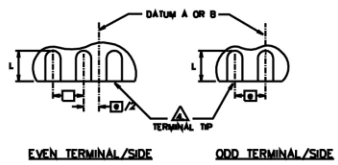


SIDE VIEW

SYMBOL	DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
e	0.50 BSC			
N	44			3
ND	11			5
NE	11			
L	0.55	0.60	0.65	
b	0.18	0.25	0.30	4
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
D	7.00 BSC			
E	7.00 BSC			
A	0.80	0.85	1.00	
A1	0.00	0.02	0.05	
K	0.20 MIN.			
θ	0	—	12	2



BOTTOM VIEW



DETAIL "A"

44-Pin QFN

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