1 Electrical characteristics

Table 1. Absolute maximum ratings (limiting value)

Symbol	Parameter	Rating	Unit
AV_{DD}	Analog supply voltage	-0.3 to +5.5	V
$V_{I/O}$	Digital supply voltage	-0.3 to +3.3	V
V_{LOG}	Input voltage logic lines (DATA, CLK, SEL_ID0, SEL_ID1)	-0.5 to $V_{I/O}$ + 0.5	V
$V_{ESD\ (HBM)}$	Human body model, JESD22-A114-B, All I/O	2	kV
T_{stg}	Storage temperature	-55 to +150	ºC
T_j	Maximum junction temperature	150	°C

Table 2. Recommended operating conditions

Symbol	Parameter	Rating			Unit
		min.	typ.	max.	
T_{AMB_OP}	Operating ambient temperature	-30	-	+85	ºC
AV_{DD}	Analog supply voltage	2.3	-	5	V
$V_{I/O}$	Digital supply voltage	1.65	-	1.95	V
VIH	Input voltage logic level High (DATA, CLK, SEL_ID0, SEL_ID1)	0.7*$V_{I/O}$	-	$V_{I/O}$+ 0.3	V
VIL	Input voltage logic level Low (DATA, CLK, SEL_ID0, SEL_ID1)	-0.3	-	0.3*$V_{I/O}$	V

Table 3. DC characteristics

Conditions: AV_{DD} 3.3V, VI/O from 1.65 to 1.95V, T_{amb} from -30 °C to +85 °C,L_{BOOST} = 15 µH unless otherwise specified							
Symbol	**Parameter**	**Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
I_{LBOOST}	Boost inductor supply current L=15µH, AV_{DD}=3.3V	Low Power mode or shutdown			0.28	1	µA
		I_{LBOOST_SS2}	Active mode, 1 output steady state 2V		130		
			Active mode, 3 outputs steady state 2V		310	700	
		I_{LBOOST_SS20}	Active mode, 1 output steady state 20V		150		
			Active mode, 3 outputs steady state 20V		380	800	
I_{AVDD}	AVDD supply current AVDD=3.3V	Low Power mode or shutdown			1.55	5	µA
		I_{AVDDT_SS2}	Active mode, 1 output steady state 2V		600		
			Active mode, 3 outputs steady state 2V		720	1200	
		I_{AVDD_SS20}	Active mode, 1 output steady state 20V		600		
			Active mode, 3 outputs steady state 20V		700	1200	
$I_{I/O}$	$V_{I/O}$ supply current	Low Power mode or shutdown			1.8	5	µA
		Active mode: (3 outputs active) No activity on CLK, VI/O=1.8V FCLK = 13MHz FCLK = 26MHz			 28 560 1100	 50 800 1500	µA
I_{IH}	Input current logic level high	Any mode, DATA, CLK, SEL_ID0, SEL_ID1 pins		-1		+1	µA
I_{IL}	Input current logic level low	Any mode, DATA, CLK, SEL_ID0, SEL_ID1 pins		-1		+1	µA
V_{IORST}	VIO low threshold					0.5	V

Table 4. High voltage DAC output characteristics

Conditions: AV_{DD} from 2.3 to 5V, VI/O from 1.65 to 1.95 V, T_{amb} from -30 °C to +85 °C, OUTA-C, unless otherwise specified						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
LOW POWER MODE						
Z_{out}	OUTA-OUTC output impedance		6			MΩ
ACTIVE MODE						
V_{OH}	OUTA-OUTC maximum output voltage	DAC = 7Fh, I_{LOAD} < 1 µA	23.17	23.88		V
V_{OL}	OUTA-OUTC minimum output voltage	DAC = 0Ah, I_{LOAD} < 1 µA		1.88	1.94	V
Resolution	Voltage resolution / OUTA- OUTC	7 bits DAC, 01h to 7Fh range		188		mV
INL	Integral Non Linearity	DAC A – DAC C from 0Ah to 7Fh	-3		+3	LSB
DNL	Differential non Linearity	DAC A – DAC C from 0Ah to 7Fh	-0.5		+0.5	LSB
Error	DACs error	DAC A – DAC C from 0Ah to 7Fh	-3		+3	% V_{out}
Isc	Over Current Protection	Any DAC output			50	mA

2 Functional block diagram

Figure 2. HVDAC functional block diagram

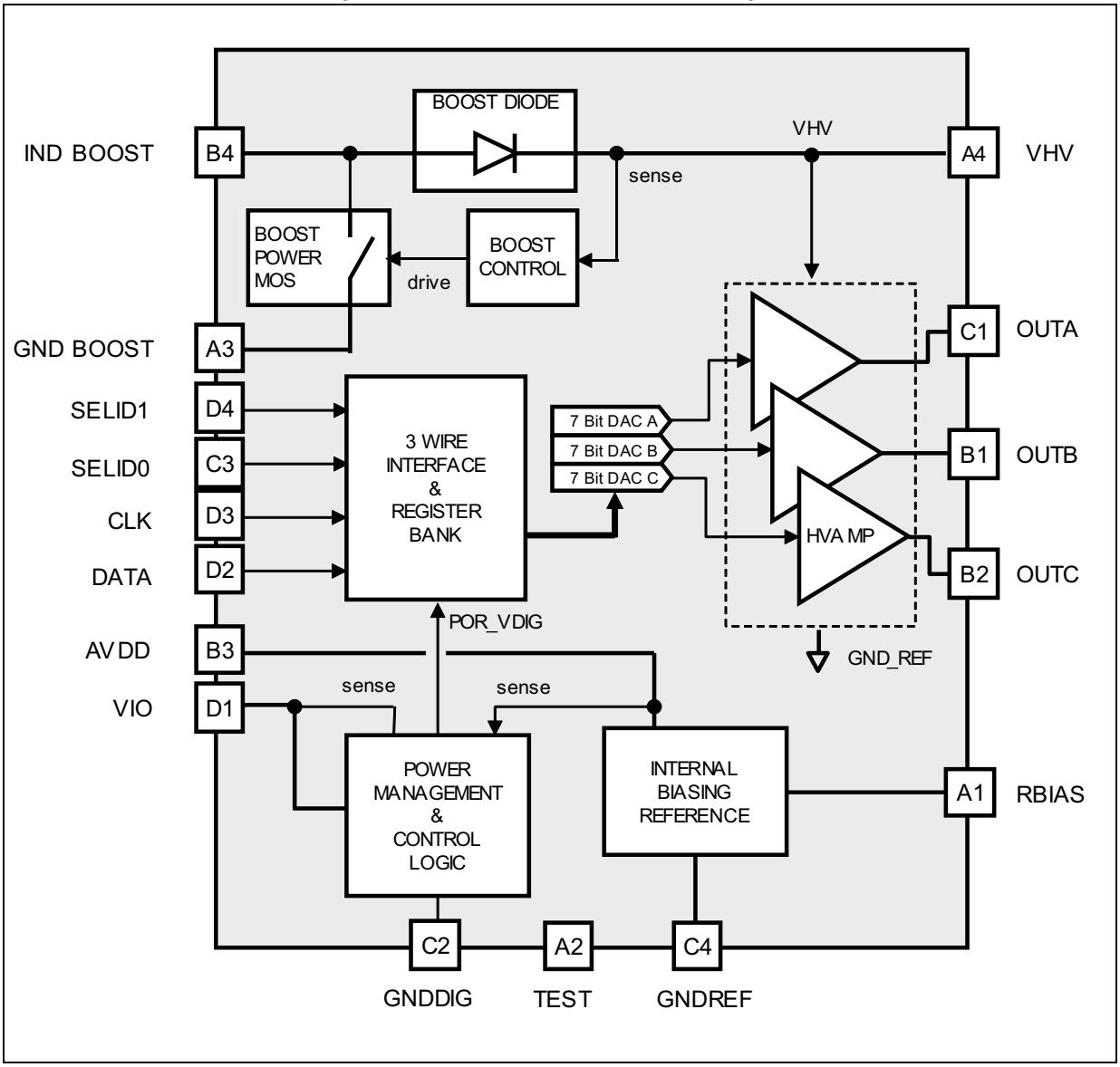


Table 5. Signals description

Pin number	Pin name	Description
A1	RBIAS	Biasing reference resistance
A2	TEST	Reserved for test, leave unconnected in application PCB
A3	GND_BOOST	Power Ground
A4	VHV	Boost High voltage output
B1	OUTB	High voltage output B
B2	OUTC	High voltage output C
B3	AVDD	Analog supply
B4	IND_BOOST	Boost inductance
C1	OUTA	High voltage output A
C2	GNDDIG	Digital Ground
C3	SELID0	RFFE interface / SELID0
C4	GND_REF	Reference Ground
D1	VIO	IO supply voltage
D2	DATA	RFFE interface / Serial Data
D3	CLK	RFFE interface / Serial Clock
D4	SELID1	RFFE interface / SELID1

3 Theory of operation

3.1 HVDAC output voltages

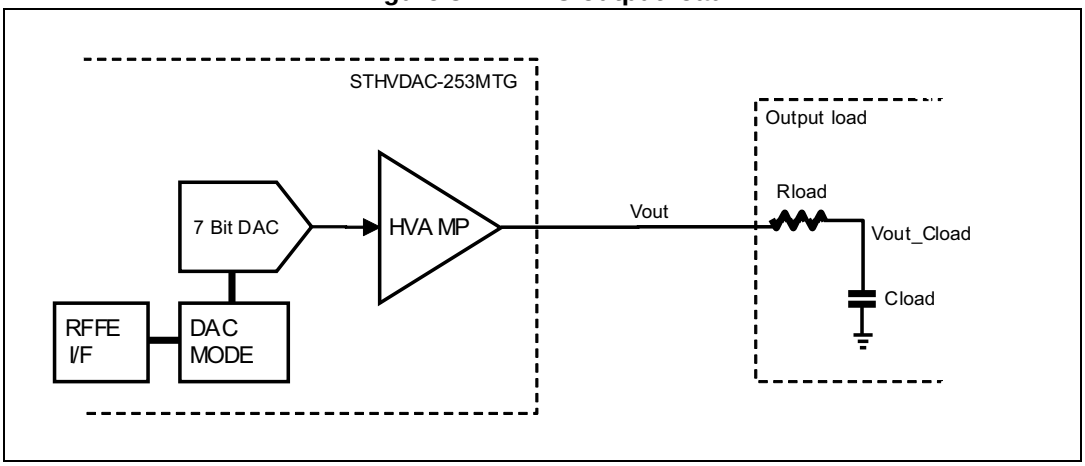
The HVDAC outputs are directly controlled by programming the 7 bits DAC (DAC A to DAC C) through the RFFE interface.

The DAC stages are driven from a reference voltage, generating an analog output voltage driving a high voltage amplifier supplied from the boost converter (see HVDAC block diagram *Figure 2*).

The HVDAC output voltages are scaled from 0 to 24 V, with 127 steps of 188 mV. If DAC value is set to 00h, then the corresponding output is setup to be in high impedance state (6 MΩ).

STHVDAC-253MTG has been specifically designed to drive BST tunable capacitors, equivalent to RC output loads as shown in *Figure 3*.

Figure 3. HVDAC output load



Each DAC output can be operated either in normal, turbo or glide mode. The DAC mode is set by controlling turbo mode bit of each DAC register (MSB of registers 2, 3, 4, 6, 7, 8), and Glide_enable bits (defined in registers#1 and 5).

3.1.1 DAC operation in normal mode -- glide_enable = 0b, turbo_mode = 0b

In normal mode, the DAC output directly switches from old to new output voltage after programming. The DAC output is controlled to ensure the output voltage (V_{out}, see *Figure 3*) reaches its final value within 10µs typical after valid RFFE command.

Typical timing diagram in Normal mode is shown on *Figure 4*.

3.1.2 DAC operation in turbo mode -- glide_enable = 0b, turbo_mode = 1b

A specific turbo mode is implemented in the STHVDAC-253MTG to ensure a fast system settling time.

In this mode, the DAC voltage outputs are optimized to minimize the settling time on the output capacitor load (V_{out}_Cload, see *Figure 3*). Once enabled, the output voltage on the output capacitor reaches its final value within 55µs typical.

In turbo mode, STHVDAC-253MTG has been optimized to support up to 4 different output RC loads, as defined in *Table 6*. The RC loads can be selected for each output independently, by controlling PTIC_selection bits in registers#9 to 11.

Typical timing diagram in turbo mode is shown on *Figure 4*.

3.1.3 DAC operation in glide mode - glide_enable = 1b, turbo_mode = x

Glide mode has been implemented to smooth DAC output voltage transition, and to minimize the impact of tunable capacitor changes on RF system performance (especially to meet 3GPP phase discontinuity requirements).

In this mode, the DAC output voltage transitions from old to new voltage value, in a period of time equal to the glide_delay defined as :

Glide_delay = glide_step_delay * 256 (programmable from 512 µs up to 16.84 ms)

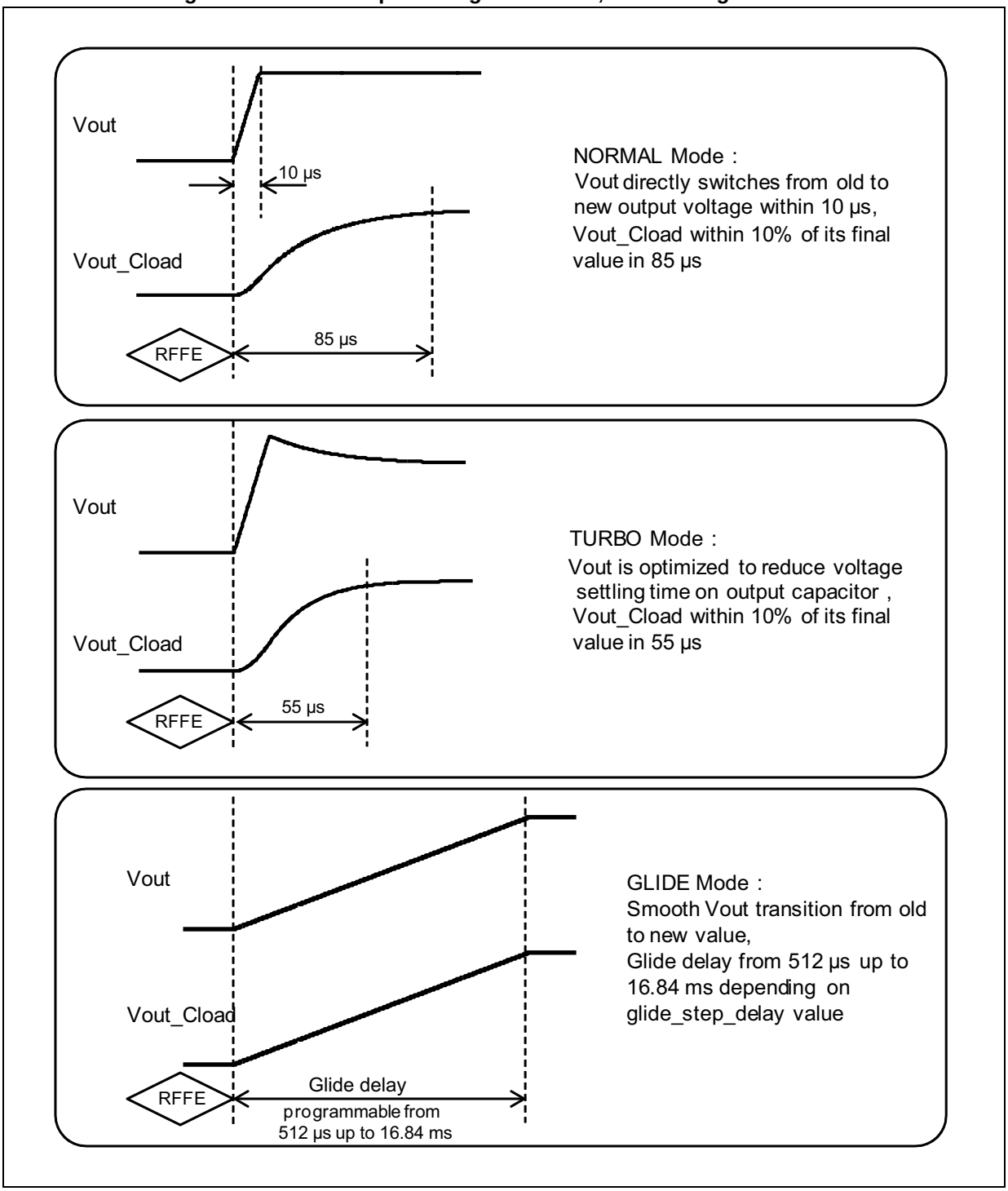
glide_step_delay defined in registers#1 and 5 as per *Table 11*.

Typical timing diagram in glide mode is shown on *Figure 4*.

Table 6. Supported output RC loads (turbo mode only)

PTIC_selection bits		Rload	Cload
0	0	12 kΩ	2.7 nF
0	1	17 kΩ	2.7 nF
1	0	22 kΩ	2.7 nF
1	1	27 kΩ	2.7 nF

Figure 4. HVDAC output voltage in normal, turbo and glide modes



4 Devices operating modes

The following operating modes are accessible through the serial interface:

4.1 Shutdown mode:

The HVDAC is switched OFF, and all the blocks in the control ASIC are switched OFF. Power consumption is almost zero in this mode, the DAC outputs are in high Z state.The shutdown mode is set by driving VIO to LOW level.

4.2 Active mode:

The device is directly set into this mode after startup, or by driving PWR_MODE bits to 00b in register #0 or 28#.

Active mode is further controlled through reg0 bit D5:

D5 = 0b (default) : Idle mode

the device is switched OFF except the RFFE interface. Power consumption is almost zero in this mode, the DAC outputs are in high Z state. (same as Low power mode)

D5 = 1b : Operating mode :

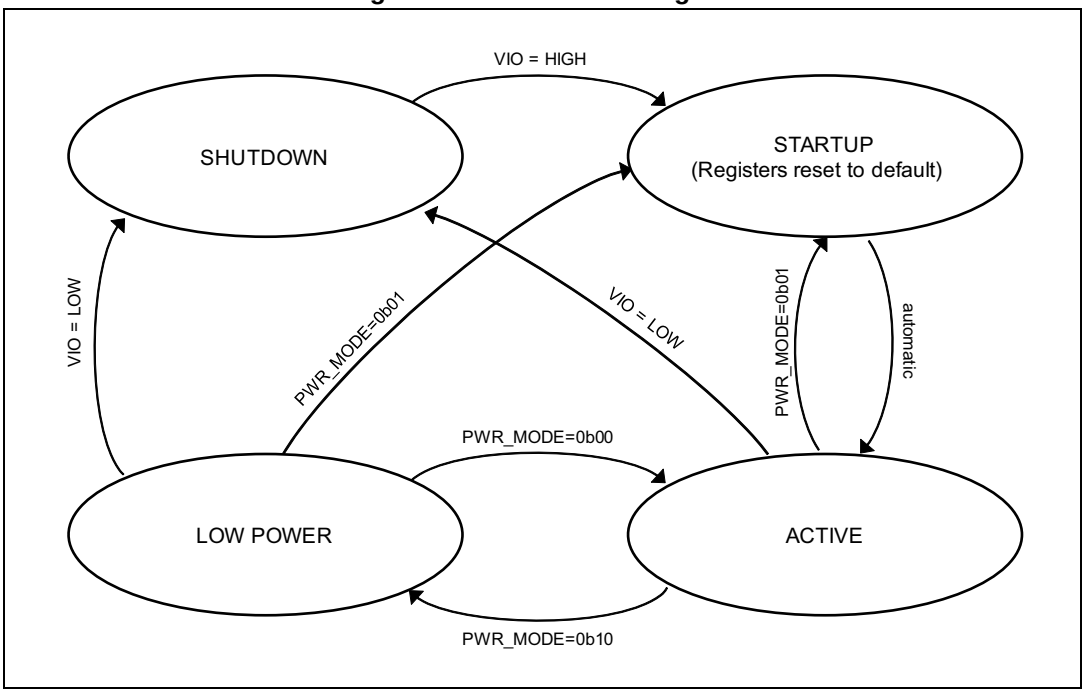
The HVDAC is switched ON and the DAC outputs are fully controlled through the RFFE serial interface. The DAC settings can be dynamically modified and the outputs will be adjusted according to the specified timing diagrams. Each DAC can be individually controlled and/or pulled down according to application requirements.

4.3 Low power mode:

The HVDAC is switched OFF except the RFFE interface. Power consumption is almost zero in this mode, the DAC outputs are in high Z state.

The device is set into this mode by driving PWR_MODE bits to 10b. All registers can be controlled and accessed in low power mode.

Figure 5. HVDAC state diagram



4.4 Device reset

Power-On Reset is implemented on the VI/O supply input, ensuring the HVDAC will be reset to default mode once VI/O supply line rises above a given threshold (typically 1V). This trigger will force all registers to their default value.

Device Reset is also implemented as defined in the MIPI RFFE specification. Setting PWR_MODE bits to 01b will force the device to reset all registers to their default value, and then automatically switch the device into low power mode.

A Soft Reset is implemented using register #26 MSB. Setting this bit will reset all registers to their default values, except PM_TRIG register (reg #28) and device USID (reg #31).

4.5 RFFE serial interface

The HVDAC is fully controlled through RFFE serial interface (DATA, VIO, CLOCK).

This interface is further described in the next sections of this document and is made compliant to the MIPI Alliance Specification for RF Front End control Interface version 1.10 - 26 July 2011 (see *Figure 12* and *Figure 13*).

Sequence Start Condition (SSC): One rising edge followed by falling edge on DATA while CLK remains at logic level low. This is used by the Master to identify the start of a Command frame.

Parity (P): Each frame shall end with a single parity bit. The parity bit shall be driven such that the total number of bits in the frame that are driven to logic level one, including the parity bit, is odd.

Bus park cycle (BP): The slave releasing DATA will drive the DATA to logic level zero during the first half of the CLK clock cycle. This is used by the master as the indication of the end of Frame.

4.6 RFFE serial interface extended mode

All the registers in the device can be addressed in extended mode, by sending appropriate command sequences as per MIPI RFFE specification (see *Figure 14*).

4.7 RFFE serial interface broadcast capability

Registers#28 to 31 can be addressed in broadcast mode, by sending appropriate command sequences as per MIPI RFFE specification.

4.8 RFFE interface - command and data frame structure

The STHVDAC-253MTG RFFE interface has been implemented to support the following command sequences :

- Register WRITE
- Register READ
- Extended register write

These supported command sequences are described in *Figure 6*.

Figure 6. Supported command sequences

	SSC			Command Frame								Data frame																			
Register WRITE	0	1	0	USID	0	1	0	REG Address[4,0]					P	DATA[7,0]								P	BP									
Register READ	0	1	0	USID	0	1	1	REG Address[4,0]					P	BP	DATA[7,0]							P	BP									
Extended Register WRITE	0	1	0	USID	0	0	0	0	0	0	0	0	P	Address[7,0]								P	Up to 4 bytes of data with parity								BP
								BC[3,0]																							
								1	1	1	1																				

USID : Unique Slave Identifier
SSC : Sequence Start Condition
P : Parity Bit
BP : Bus Park Cycle
BC : Byte Count

All frames are required to end with a single parity bit. The parity bit shall be driven such that the total number of bits in the frame that are driven to logic level 1, including the parity bit, is odd. In case the device detects a parity error, the frame is considered not valid and is ignored.

4.9 Power-up/down sequence

Table 7 and *Figure 8* are describing the HVDAC settling time requirements and recommended timing diagrams.

Switching from Shutdown to Active mode is triggered by setting VIO to HIGH level.

Switching from Low Power to Active mode will occur setting PWR_MODE bits to 00b (REGISTER#28 or REGISTER#0).

Switching from active to low power mode will occur setting PWR_MODE bits to 10b (REGISTER#28 or REGISTER#0).

Foallowing active mode command (from Low power), the HVDAC will be operational after t_{active} (typ. 100 µs). Once in active mode, a settling time of 10 µs typ (Tset) is required following each DAC command in active mode. During this settling time the HVDAC output voltages will vary from the initial to the updated DAC command.

4.10 Power supply sequencing

No specific power supply sequencing is required on the STHVDAC-253MTG.

The STHVDAC-253MTG is fully functional only once both VIO and AVDD are supplied.

4.11 Trigger mode

To meet precise timing requirements and avoid RFFE interface traffic congestion at critical timing, trigger mode has been implemented in the RFFE interface.

Three triggers (TRIG0, TRIG1 and TRIG2) are available and can be controlled through the RFFE interface.

By default, registers 2 to 4 (DAC A, DAC B and DAC C) are associated to TRIG0. Each DAC can be independently mapped to TRIG0, TRIG1 or TRIG2 by controlling trigger configuration bits in registers 9 and 10.

Trigger mode enabled (default mode):

By default, the different triggers are enabled and the device is running in triggered mode.

In this case, once in ACTIVE mode, the following sequence must be followed to control the HVDAC outputs:

- Send any valid write command sequence to Register#0 - Register#10. The new DAC register values will be temporarily stored in shadow registers.
- Send a register#28 write command sequence, setting trigger bits (D2 to D0) and keeping trigger mask bits (D5 to D3) low. The shadow registers will be loaded to destination registers and this will trigger the corresponding DAC outputs to their new values.

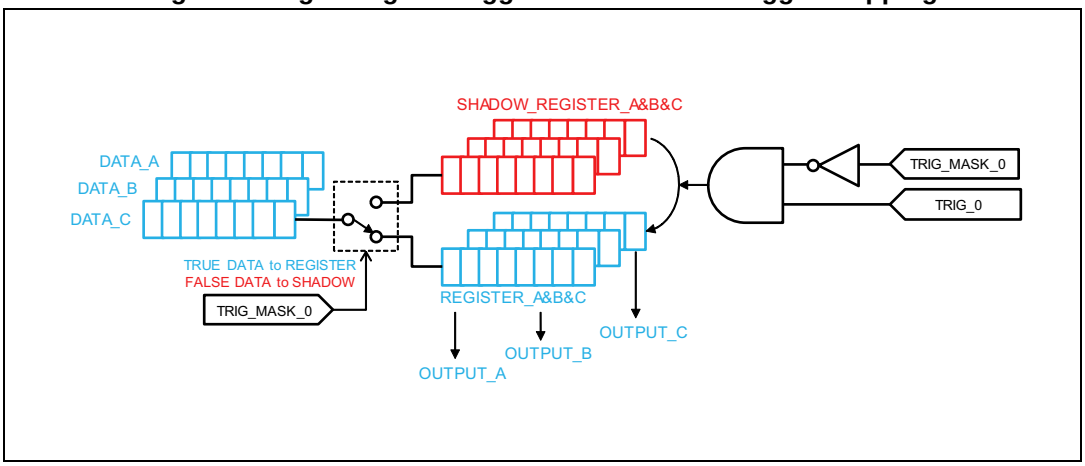
Trigger mode disabled:

The different triggers are disabled setting corresponding trigger mask bits in register#28 (D5 to D3).

In this case, any valid DAC register write command sequence is directly loaded to the destination register, directly triggering the corresponding DAC output to its new value.

The following logic diagram illustrates the trigger mode function. By default the trigger mode is enabled and the DATA are first sent to SHADOW registers, then transferred into DAC register once valid trigger is sent to register#28.

Figure 7. Logic diagram trigger mode / default trigger mapping



4.12 Settling time

The STHVDAC will set the bias voltage of the tunable capacitors within 10 µs typical after

- Bus Park (BP) of register #28 write sequence data frame if trigger mode is enabled.
- Parity Bit (P) of each data frame of register #1 to 8 extended write sequence if trigger mode is disabled.

Table 7. Timing

Conditions: AV_{DD} from 2.5 to 5 V, $V_{I/O}$ from 1.65 to 1.95 V, T_{amb} from -30 °C to +85 °C, OUTA-OUTC unless otherwise specified						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
T_{active}	Activation time	Internal voltages activation time from Low Power (or shutdown) to Active mode Chv=33 nF	-	100	250	µs
T_{set+}	Output positive setting time @ 95% of delta V	V_{out} 2 V to 20 V, equivalent load of 12 kΩ and 2.7 nF / Normal mode	-	10	25	µs
T_{set-}	Output negative setting time @ 95% of delta V	V_{out} 20 V to 2 V, equivalent load of 12 kΩ and 2.7 nF / Normal mode	-	10	25	µs

4.13 Recommended operation with trigger and extended commands

It is recommended to use trigger so that outputs will be activated by write to REG_28. By default the device is set in triggered mode.

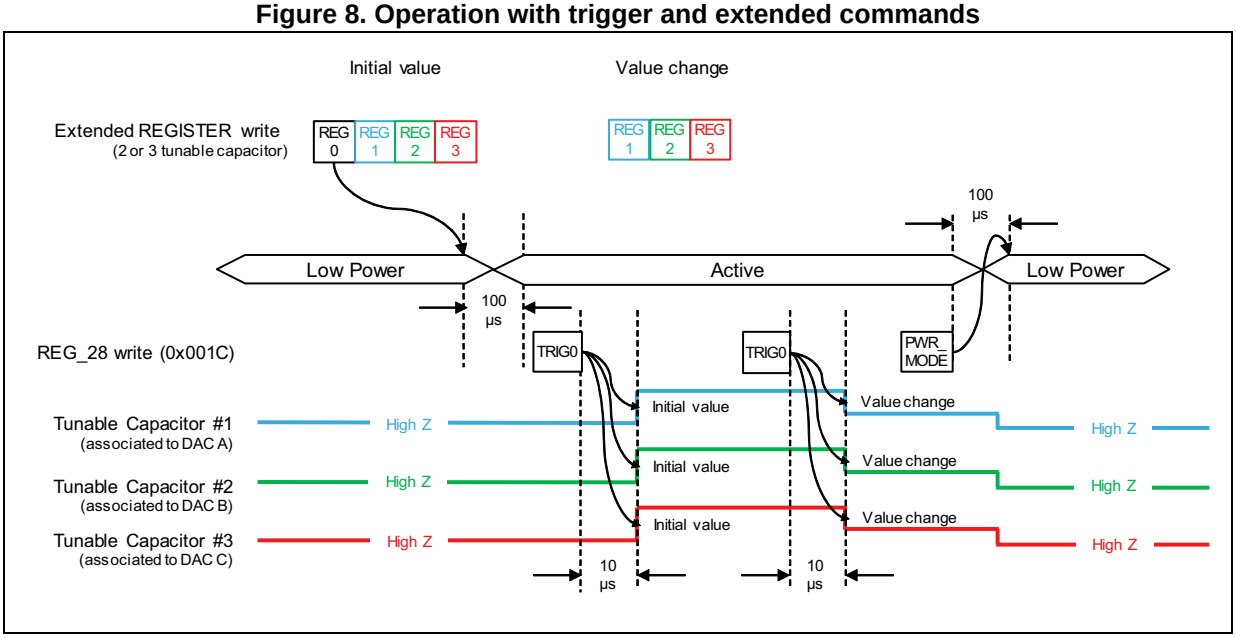
PWR_MODE bits from REG_28 have been duplicated in REG_0 to ensure the device can be setup from low power to active using one single extended mode RFFE command, as illustrated on *Figure 8*.

By default, DAC_A, B and C are mapped to TRIG0 and DAC_D, E and F to TRIG1. In this configuration, DAC values can be updated through RFFE extended commands, and DAC outputs for a given antenna synchronized through trigger control.

Each DAC output can be mapped to TRIG0, 1 or 2 through registers 9 to 11.

The timing diagram below represents recommended operation when default trigger mapping and extended write are in use.

Figure 8. Operation with trigger and extended commands



4.14 Registers table

The STHVDAC is embedding 12 x 8 bits registers. Registers content is described in *Figure 9*, and registers default values are provided in *Figure 10*.

Figure 9. Registers table

Reg #	Reg address hex	Reg address bin	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Access type	Default Triggers
0	*00h*	[00000]	x	x	Active	0	1	0	PWR_MODE		RW	no
1	*01h*	[00001]	glide_step_delay					Glide A EN	Glide B EN	Glide C EN	RW	no
2	*02h*	[00010]	TM_A	DAC A							RW	TRIG0
3	*03h*	[00011]	TM_B	DAC B							RW	TRIG0
4	*04h*	[00100]	TM_C	DAC C							RW	TRIG0
9	*09h*	[01001]	TRIG_CONFIG_A		PTIC_Select_A		TRIG_CONFIG_B		PTIC_Select_B		RW	no
10	*0Ah*	[01010]	TRIG_CONFIG_C		PTIC_Select_C						RW	no
26	*1Ah*	[11010]	SW reset	RFFE status							RW	no
28	*1Ch*	[11100]	PWR_MODE		Trig mask 2	Trig mask 1	Trig mask 0	TRIG2	TRIG1	TRIG0	RW	no
29	*1Dh*	[11101]	SELSID1	SELSID0	PRODUCT ID *[xx000100b]*						R	no
30	*1Eh*	[11110]	MANUFACTURER ID [7,0] *[00000100b]*								R	no
31	*1Fh*	[11111]	0	0	MANUF_ID[9,8] *[01b]*		USID *[0111b]*				RW	no

Figure 10. Registers default values

Reg #	Reg address hex	Reg address bin	D7	D6	D5	D4	D3	D2	D1	D0
0	00h	[00000]	0	0	0	0	1	0	0	0
1	01h	[00001]	0	0	0	0	0	0	0	0
2	02h	[00010]	0	0	0	0	0	0	0	0
3	03h	[00011]	0	0	0	0	0	0	0	0
4	04h	[00100]	0	0	0	0	0	0	0	0
9	09h	[01001]	0	0	0	0	0	0	0	0
10	0Ah	[01010]	0	0	0	0	0	1	0	0
26	1Ah	[11010]	0	0	0	0	0	0	0	0
28	1Ch	[11100]	0	0	0	0	0	0	0	0
29	1Dh	[11101]	SELSID1(*)	SELSID0(*)	0	0	0	1	0	0
30	1Eh	[11110]	0	0	0	0	0	1	0	0
31	1Fh	[11111]	0	0	0	1	0	1	1	1

Note: (*)Reg#29 - D7 and D6 (MSBs DEVICE ID) default values are directly tied to SELID1 and SELID0 pins, respectively. These bits are set to 1 if the corresponding pin is tied to $V_{I/O}$, and set to 0 if tied to GND. This will allow to have up to four HVDAC with different product ID connected to the same RFFE master.

4.15 RFFE interface - registers content description

Registers content and control are further described in tables#8 to 14 and *Figure 11*.

Table 8. STHVDAC mode selection

D7	D6	Reg #0 D5	Comments
PWR_MODE		Active	
0	0	0	Active mode - idle
0	0	1	Active mode - operating
0	1	x	Start up / registers reset to default
1	0	x	Low power
1	1	x	N/A

PWR_MODE bits located in D7-D6 of reg#28, and duplicated in D1-D0 of reg#0.

Table 9. STHVDAC trigger control register - reg#28

D5	D4	D3	D2	D1	D0	Comments
Trig mask 2	**Trig mask 1**	**Trig mask 0**	**Trig 2**	**Trig 1**	**Trig 0**	
0	0	0	0	0	0	Triggers 2, 1, 0 are unmasked / triggers 2, 1, 0 are disabled (default)
0	0	0	1	1	1	Triggers 2, 1, 0 are unmasked / triggers 2, 1, 0 are enabled
1	1	1	0	0	0	Triggers 2, 1, 0 are masked

Table 10. HVDAC unique slave identifier control - reg#31

D7	D6	D5	D4	D3	D2	D1	D0	Comments
spare		**MANUFACTURER_ID [9,8]**		**USID**				
0	0	0	1	0	1	1	1	Default value
0	0	0	1	x	x	x	x	USID can be modified by RFFE master, see detailed programming procedure in MIPI RFFE specification

Table 11. Glide step delay control - reg#1

Address	D7	D6	D5	D4	D3	Comments
	Glide step delay DAC A, B, C					Glide_step_delay value
[00001]	0	0	0	0	0	2 µs
	0	0	0	0	1	4 µs
	0	0	0	1	0	6 µs
	1	1	1	1	0	62 µs
	1	1	1	1	1	64 µs

Table 12. Glide enable bits - reg#1

Address	D2	D1	D0	Comments
	Glide A EN	Glide B EN	Glide C EN	
[00001]	0	0	0	Glide enable = 0:DAC mode set by DAC register MSB
	1	1	1	Glide enable = 1:DAC in glide mode

Table 13. DAC control registers - reg#2, 3, 4

Address	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Comments
[00010]	TM_A	DAC A							D7:Turbo mode control: 0:Turbo OFF 1:Turbo ON D7 is disregarded if glide mode is enabled D6-D0:DAC output
[00011]	TM_B	DAC B							
[00100]	TM_C	DAC C							

Table 14. RFFE status register - reg#26

Reg#	Address	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Access type	Triggered
26	[11010]	SW reset	RFFE status							RW	no

D7: Software reset:

- 0: Normal operation
- 1: Software reset - all configurable registers are reset to their default values (except USID and reg#28)

D6-D0: RFFE status and error reporting

Figure 11. Trigger configuration and PTIC selection registers - reg#9, 10 and 11

Reg #	Reg address hex	Reg address bin	D7 MSB	D6	D5	D4	D3	D2	D1	D0 LSB	Access type	Default Triggers
9	09h	[01001]	TRIG_CONFIG_A		PTIC_Select_A		TRIG_CONFIG_B		PTIC_Select_B		RW	no
10	0Ah	[01010]	TRIG_CONFIG_C		PTIC_Select_C						RW	no
11	0Bh	[01011]									RW	no

Each DAC output can be connected to RFFE TRIG#0, TRIG#1 or TRIG2

TRIG CONFIG x : 00b	DAC x triggered through TRIG#0	default for DAC A, B & C
TRIG CONFIG x : 01b	DAC x triggered through TRIG#1	
TRIG CONFIG x : 10b	DAC x triggered through TRIG#2	

In TURBO mode, Each DAC output is optimized to supply 4 different RC loads (corresponding to 4 different PTIC designs)

PTIC_Selection_bits = 00b	Rload = 12kΩ	Cload = 2.7nF	(24 capacitor stack STPTIC F1, G1, G2 series)
PTIC_Selection_bits = 01b	Rload = 17kΩ	Cload = 2.7nF	(36 capacitor stack STPTIC H1, L2 series)
PTIC_Selection_bits = 10b	Rload = 22kΩ	Cload = 2.7nF	(48 capacitor stack STPTIC L1, L2 series)
PTIC_Selection_bits = 11b	Rload = 27kΩ	Cload = 2.7nF	(Spare)

5 Serial interface specification

Table 15. Interface specifications

Conditions: AV_{DD} from 2.3 to 5 V, VIO from 1.65 to 1.95 V, T_{amb} from -30 °C to +85 °C, unless otherwise specified						
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
F_{CLK}	Clock Frequency			-	26	MHz
T_{CLK}	Clock Period		38.4	-		ns
T_{HIGH}	Clock High Time		11.25	-		ns
T_{LOW}	Clock Low Time		11.25	-		ns
TD_{setup}	DATA setup time	Relative to 30% of CLK falling edge	1	-		ns
TD_{hold}	DATA hold time	Relative to 70% of CLK falling edge	5	-		ns
C_{CLK}	CLK pin input capacitor			2.5	5	pF
C_{DATA}	DATA pin input			2.5	5	pF

Figure 12. Operation register WRITE command sequence

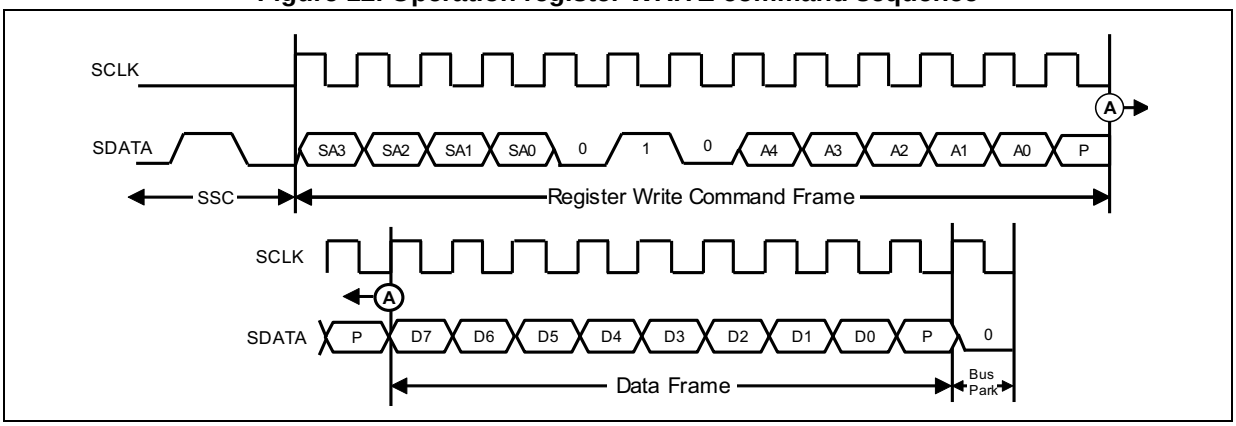


Figure 13. Operation register READ command sequence

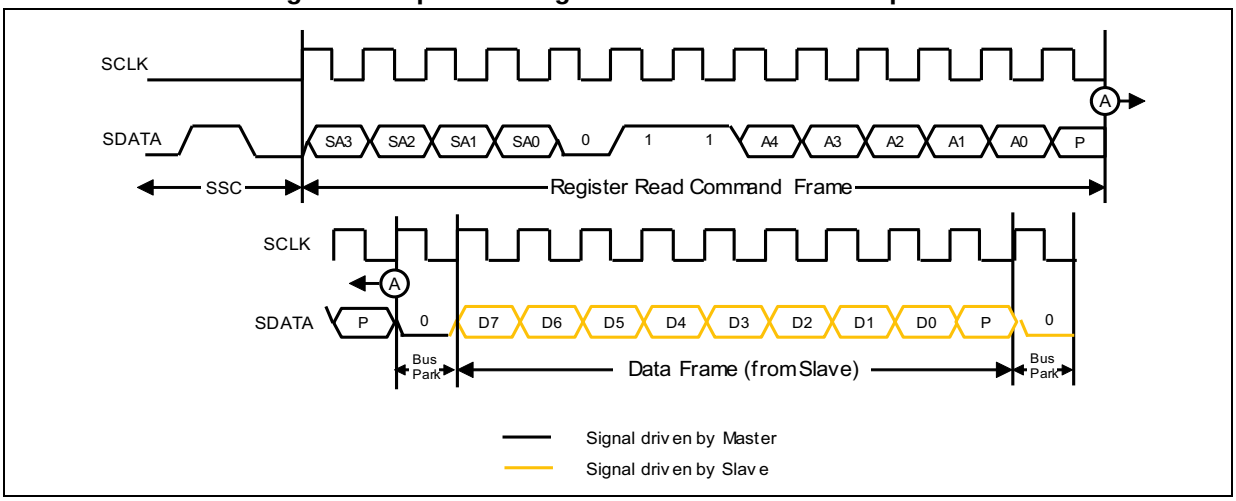
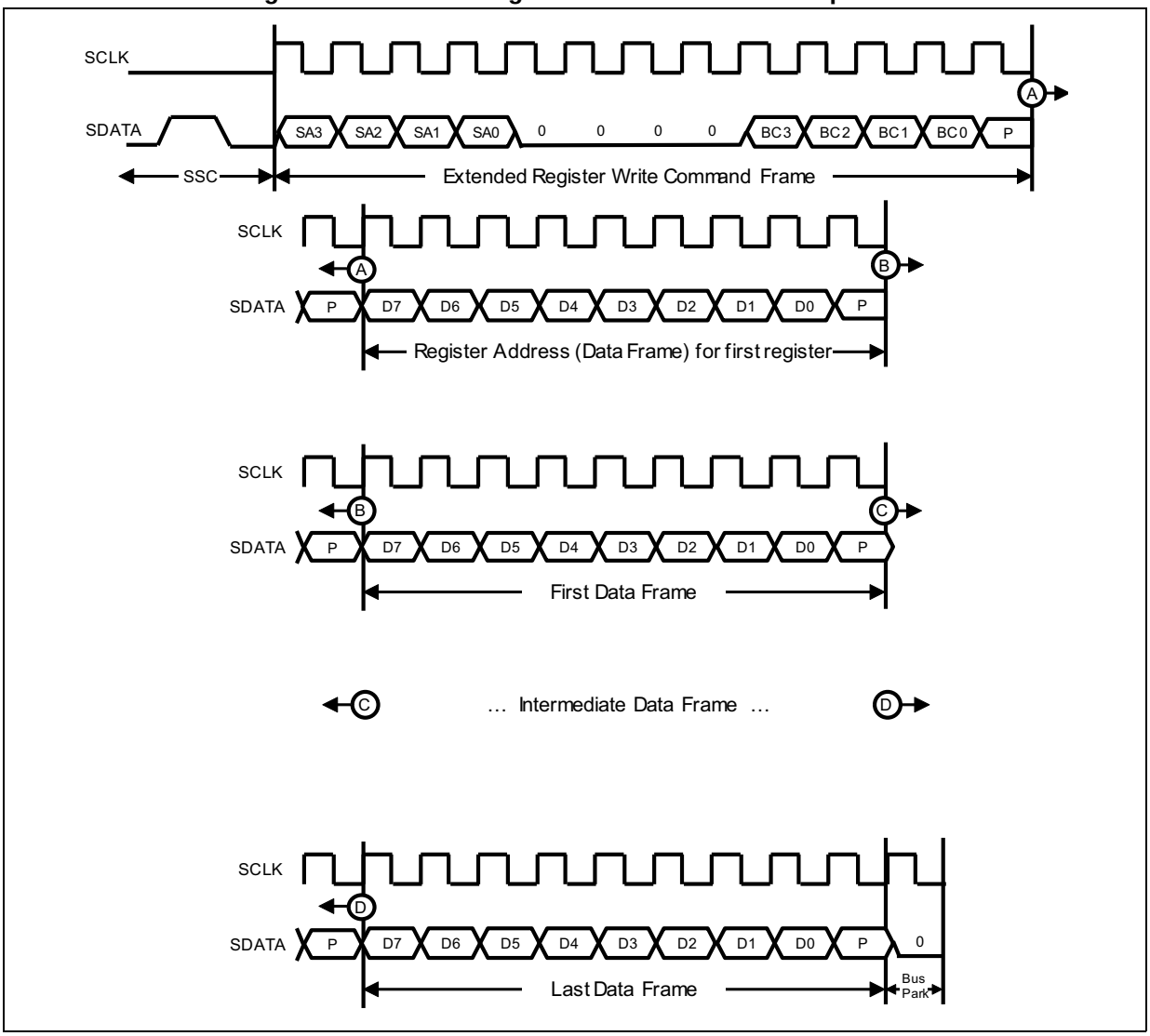


Figure 14. Extended register WRITE command sequence



6 Application schematic

Figure 15. Recommended application schematic

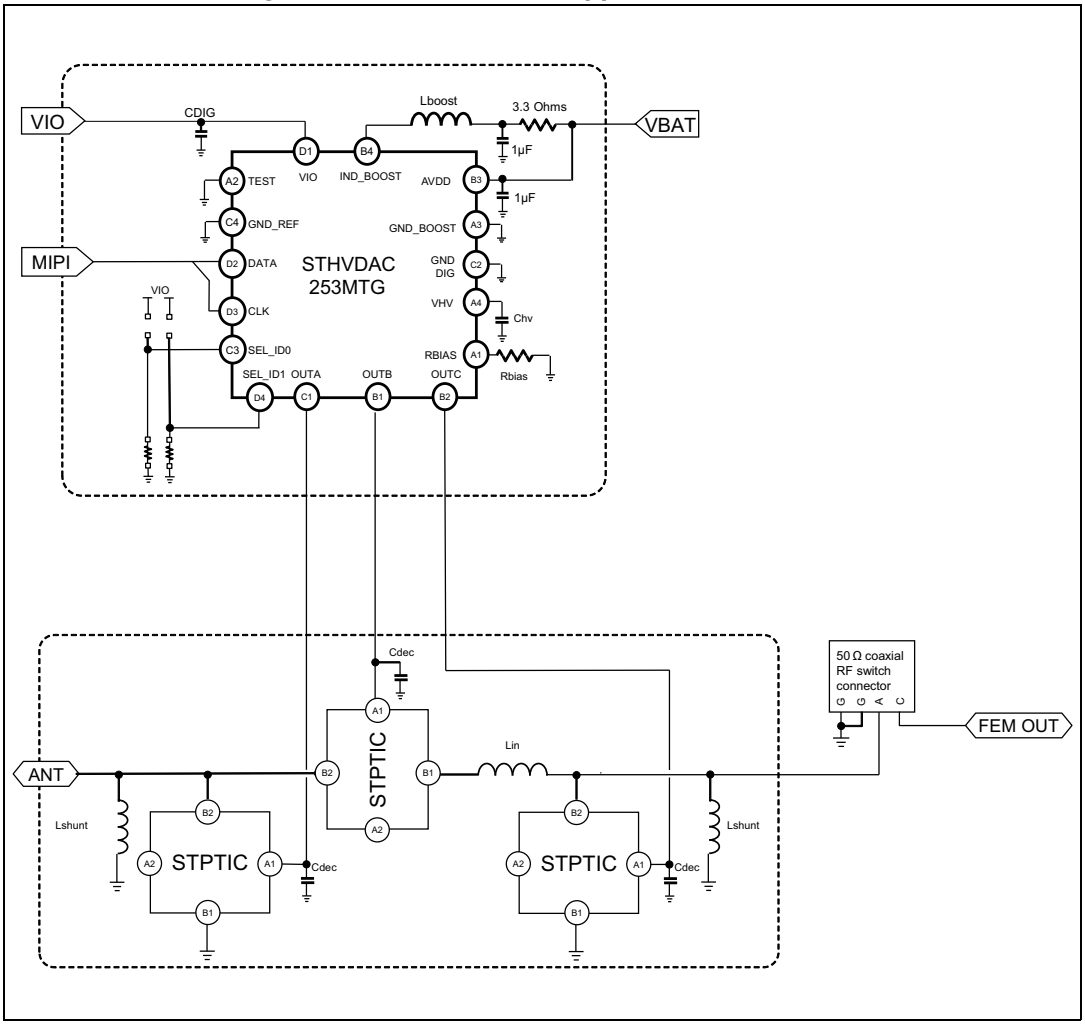


Figure 16. Evaluation board

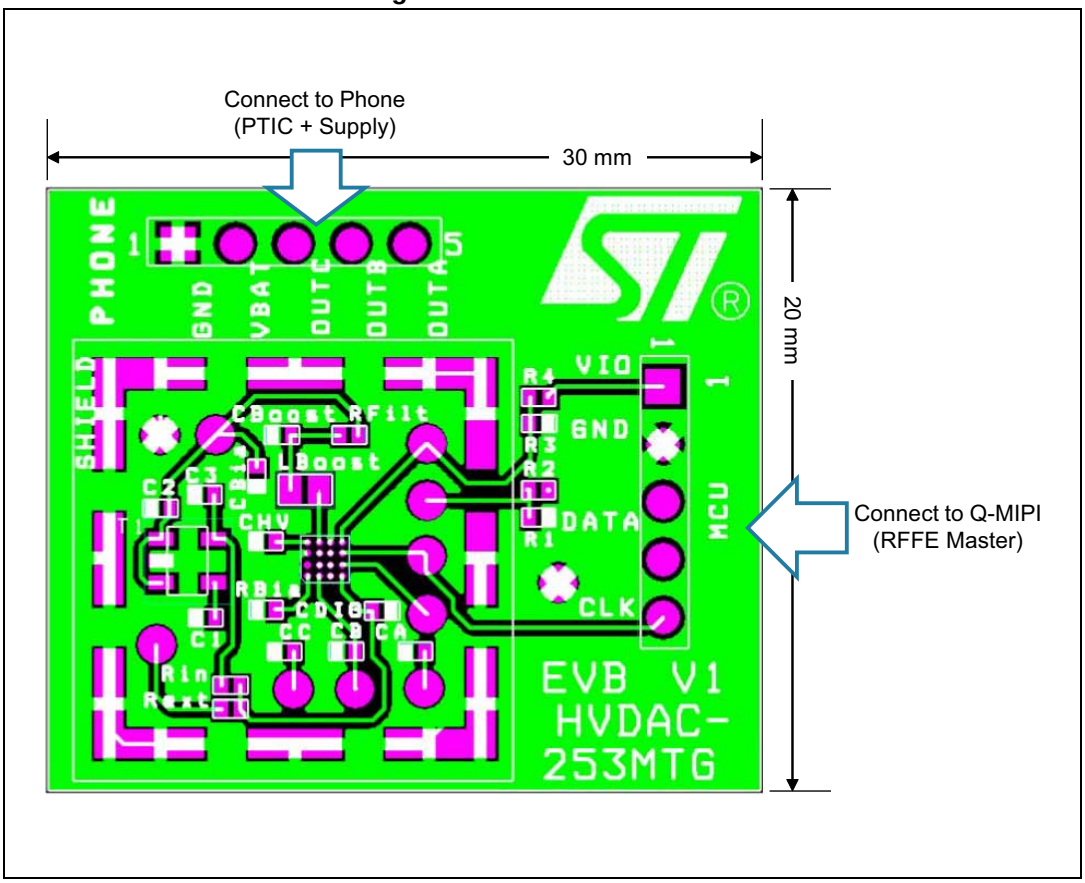


Table 16. Recommended external BOM

Components	Description	Nominal value	Package (inch)	Package (mm)	Recommended P/N
Cboost	Boost supply capacitor	1 µF	0201	0603	AVX: 02016D105MAT2A
Lboost	Boost inductance	15 µH	0603	1608	COILCRAFT: 0603LS-153XGL
Rbias	Reference bias resistor, 1%	110 kΩ	0201	0603	Multicomp: MC 0.0625W 0402 1%
Chv	Boost output capacitor, 50V	33 nF	0402	1005	Murata: GRM155R61H333KE19
Cdec	Decoupling capacitor, 50V	100 pF	0201	0603	TDK: C0603COG1H101J

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 Flip-chip package information

Figure 17. Flip-chip package outline

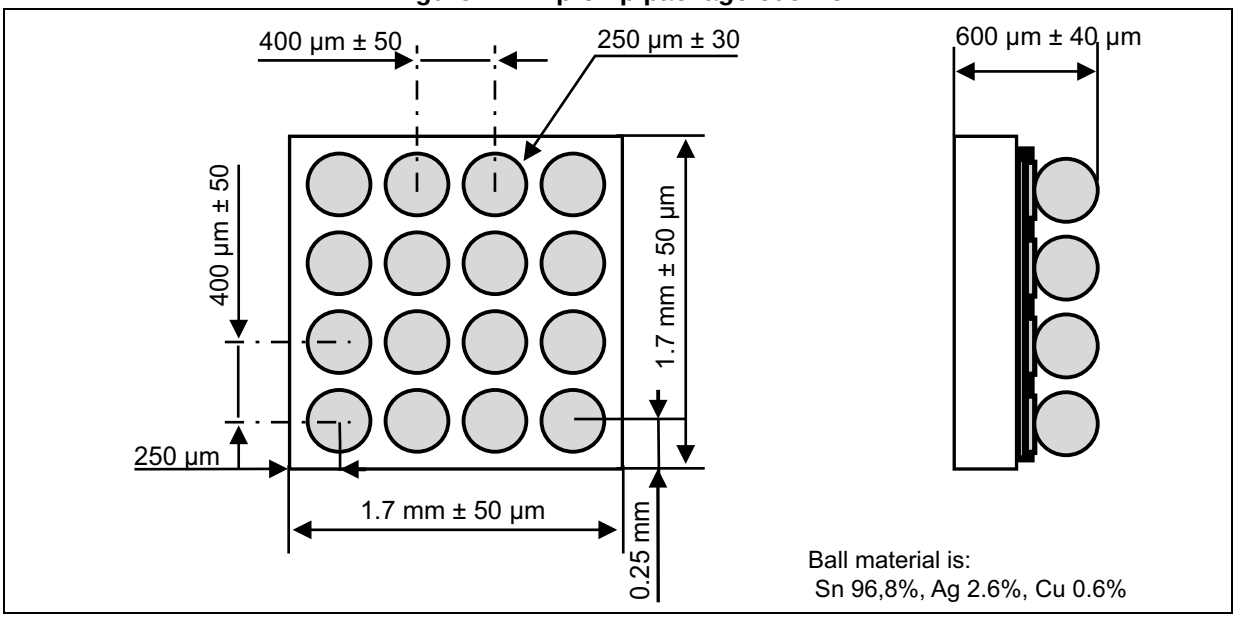


Figure 18. Footprint

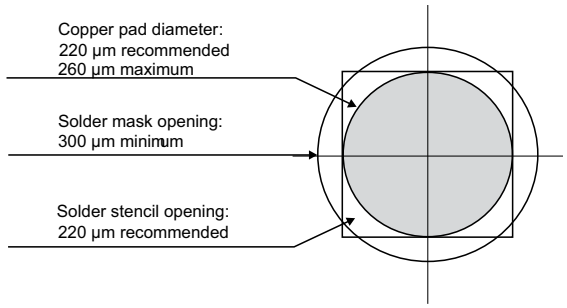


Figure 19. Marking

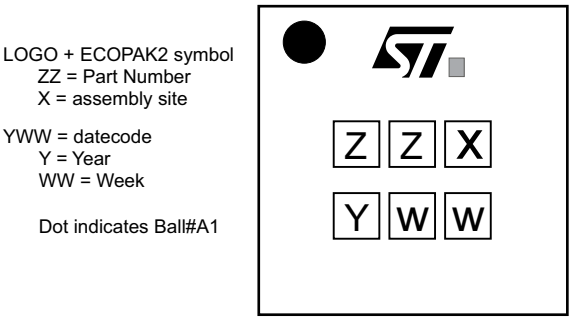
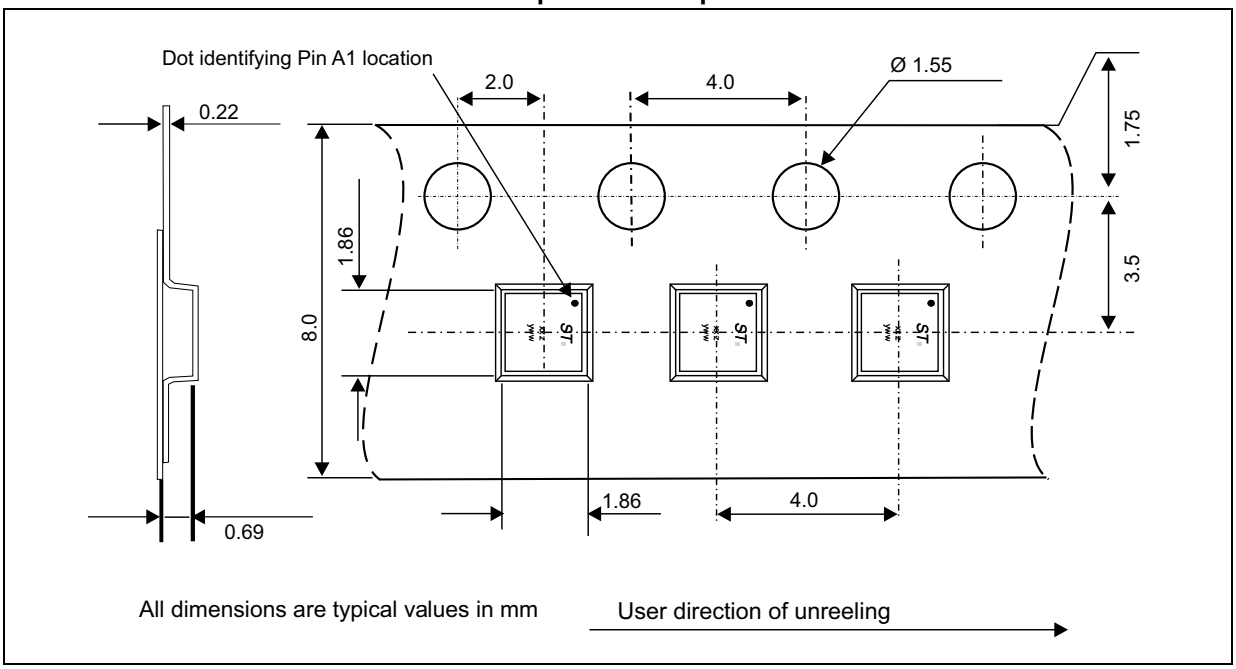


Table 17. Tape and reel specification



8 Ordering information

Table 18. Ordering information

Part Number	Marking	Base Qty.	Delivery mode
STHVDAC-253MTGF3	PU	5000	Tape & reel

Note: More information is available in the STMicroelectronics Application note: AN1235: "Flip Chip: Package description and recommendations for use"

9 Revision history

Table 19. Document revision history

Date	Revision	Changes
10-Jun-2015	1	Initial release.
24-Jun-2015	2	Updated description.
9-Jul-2015	3	Updated figure16.
17-Nov-2015	4	Updated *Figure 15*.
16-Nov-2017	5	Updated *Table 15*.