Figure 1: Schematic diagram				
1 2 3 4 5 6 7 8 9 10 11 12	V^{C} $R1$ $R1$ T $R1$ T $R1$ T $R1$ V^{C} $R3$ $R1$ T $R3$ $R1$ T $R3$ $R1$ T $R2$ T	$ \begin{array}{c} $	R2 C ↓ ↓ 28 27 26 25 24 4 V∞ 23	
[10] [11]	$ \begin{array}{c} $		19	
	D4	Po	De	^

Figure 1: Schematic diagram

	R1	R2	RS	С
Code 01	4.7 kΩ	4.7 kΩ	33 Ω	180 pF
Tolerance	±10 %	±10 %	±10 %	±20 %



1 Characteristics

Table 1: Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	P	Value	Unit		
		MIL STD 883E - method 3015-7	±25		
V _{pp}	V _{pp} Peak pulse voltage	IEC61000-4-2 contact discharge	±9	kV	
		IEC61000-4-2 air discharge	±16		
Vcc	Supply voltage		5.5	V	
Pr	Power rating per resistor		100	mW	
PP	Package power rating		1	Ω	
T _{stg}	Storage junction temperature range		-55 to +150		
Tj	Maximum operating junction temperature		125	°C	
Top	Operating temperature ran	-40 to +125			

Table 2: Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test condition	Min.	Тур.	Max.	Unit
I _R	Leakage current	$V_{CC} = 5.0 V$			10	μA
VBR	Breakdown voltage	I _R = 1 mA	6			V
VF	Forward voltage drop	I _F = 50 mA		0.9		V



1.1 Basic cell configurations

The ST1284-01A8 is built around the two basic cells described below which integrate the recommended IEEE1284 network and the ESD protection compatible with IEC 61000-4-2 level 4.





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2 Application information

The functional diagram here above presents a IEEE1284-A connector pinout and shows how to connect the ST1284-01A8 in order to correctly terminate and filter the 17 signal lines. The IEEE1284-A connector is the PC standard for the host connection.

Control and status lines (from 10 to 17) only require a pull-up resistor (R_p) and a filter capacitor (C).

The data lines (from 2 to 9) and the STROBE (pin 1) also require a termination series resistor (R_s) in addition to the pull-up resistor and a filter capacitor. The V_{CC} is connected to pin 20 and the ground to pin 22.

The ST1284-01A8 can be used with all 3 types of connectors defined in the IEEE1284 standard:

- IEEE1284-A is a 25 dB connector which is the PC standard for the host connection.
- IEEE1284-B is a 36 pin, 0.085 inch center line connector used on the peripheral device.
- IEEE1284-C is a new 36 pin, 0.050 inch center line connector which can be used for both host and peripherals.

3 Technical information

3.1 Frequency behavior of data and strobe signals



3.2 ESD protection

In addition to the termination requirements and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test, already in place in Europe, is described as per IEC 61000-4-2 standard. This test requires that a device tolerates ESD events and remains operational without user intervention.

The ST1284-01A8 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at:

 $V_{ouput} = V_{BR} + R_d \times I_{PP}$

This protection function is split in 2 stages. As shown in *Figure* 7, the ESD strikes are clamped by the first stage S_1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the voltage very low at the output.





To have a good approximation of the remaining voltages at both V_{in} and V_{out} stages, we give the typical dynamic resistance value R_{d} .

Taking into account these hypothesis $R_t > R_d$, $R_g > R_d$ and $R_{load} > R_d$, gives these formulas:

$$V_{input} = \frac{R_g \times V_{BR} + R_d \times V_{PP}}{R_g}$$

$$V_{output} = \frac{R_t \times V_{BR} + R_d \times V_{input}}{R_t}$$

The results of the calculation done for V_{PP} = 8 kV, R_g = 330 Ω (IEC 61000-4-2 standard), V_{BR} = 7 V (typ.) and R_d = 1 Ω (typ.) give:

- V_{input} = 31.2 V
- V_{output} = 7.95 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the input side. This parasitic effect is not present at the output side due to the low current involved after the resistance R.

The measurements in *Figure 9* clearly show the high efficiency of the ESD protection:

- no influence of the parasitic inductances on Vout stage
- Voutput clamping voltage very close to VBR (positive strike) and -VF (negative strike)



Technical information







4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

4.1 QSOP28 package information



Table 3: QSOP28 package mechanical data

	Dimensions						
Ref.	Millimeters			Inches			
	Min.	Тур.	Max.	Min.	Тур.	Max.	
А	1.55		1.75	0.061		0.069	
a1	0.10		0.25	0.004		0.010	
b	0.20		0.30	0.008		0.012	
b1	0.18		0.25	0.007		0.010	
D	9.80		9.98	0.386		0.393	
E	3.80		3.98	0.15		0.157	
е		0.64			0.025		
F	5.79		6.20	0.228		0.244	
L	0.40		0.90	0.016		0.035	
S		8° max.			8° max.		



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Table 4: Mechanical specifications

Lead plating	Tin-lead		
Lead plating thickness	7 μm min. 25 μm max.		
Lead material	Copper Alloy		
Lead coplanarity	0.102 mm (0.004")		
Body material	Molded epoxy		
Resin	Meets UL94V-0 standard		



5 Ordering information

Table 5: Ordering information					
Order code	Marking	Package	Weight	Base qty.	Delivery mode
ST1284-01A8	ST1294 01		0.147 a	48	Tube
ST1284-01A8RL	ST1284-01	QSOP28	0.147 g	2500	Tape and reel

6 Revision history

Date	Revision	Changes
Oct-2003	2B	Last release.
12-Mar-2010	3	Updated table in Figure 1 and Figure 10.
11-May-2012	4	Updated Table 3.
09-Jul-2014	5	Corrected typographical error in Table 2.
05-May-2017	6	Updated Table 1: "Absolute maximum ratings (Tamb = $25 \degree C$)". Minor text changes to improve readability.



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