## Product Description

SST49LF080A flash memory device is designed to interface with the LPC bus for PC and Internet Appliance application in compliance with Intel Low Pin Count (LPC) Interface Specification 1.0. Two interface modes are supported: LPC mode for in-system operations and Parallel Programming (PP) mode to interface with programming equipment.

SST49LF080A flash memory device is manufactured with proprietary, high-performance SuperFlash Technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST49LF080A device significantly improves performance and reliability, while lowering power consumption. The SST49LF080A device writes (Program or Erase) with a single 3.0-3.6V power supply. It uses less energy during Erase and Program than alternative flash memory technologies. The total energy consumed is a function of the applied voltage, current and time of application. For any give voltage range, the SuperFlash technology uses less current to program and has a shorter erase time; the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies. The SST49LF080A product provides a maximum Byte-Program time of 20 µsec. The entire memory can be erased and programmed byte-by-byte typically in 16 seconds when using status detection features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. The SuperFlash technology provides fixed Erase and Program time, independent of the number of Erase/Program cycles that have performed. Therefore the system software or hardware does not have to be calibrated or correlated to the cumulative number of Erase cycles as is necessary with alternative flash memory technologies, whose Erase and Program time increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST49LF080A device is offered in 32-lead TSOP and 32-lead PLCC packages. See Figures 2 and 3 for pin assignments and Table 1 for pin descriptions.

## Functional Block Diagram

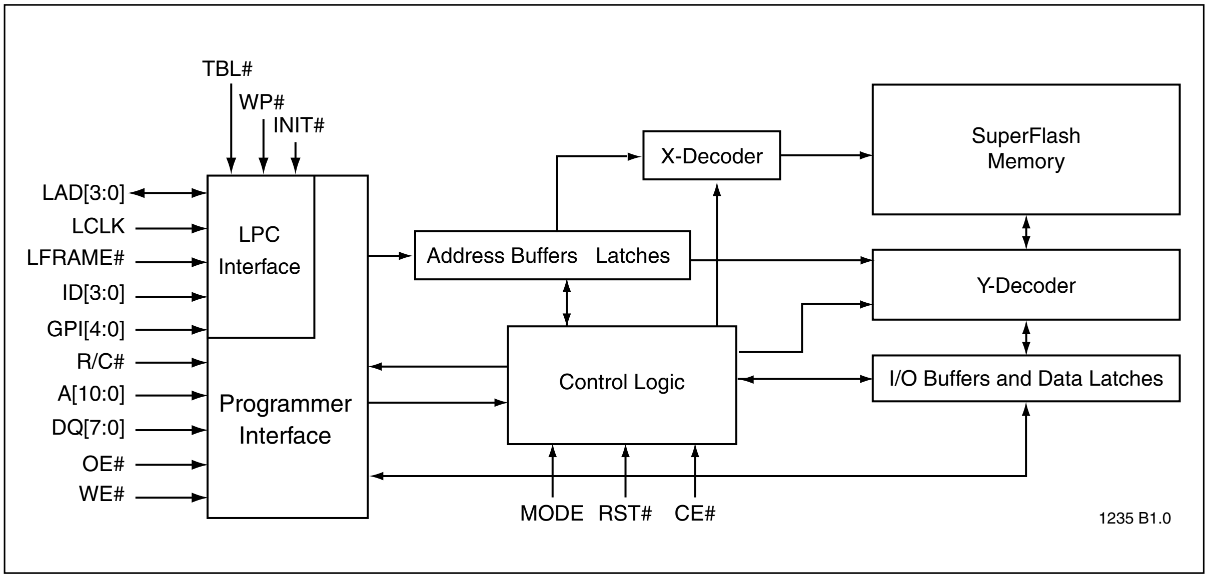


**Figure 1:** Functional Block Diagram

## Pin Assignments

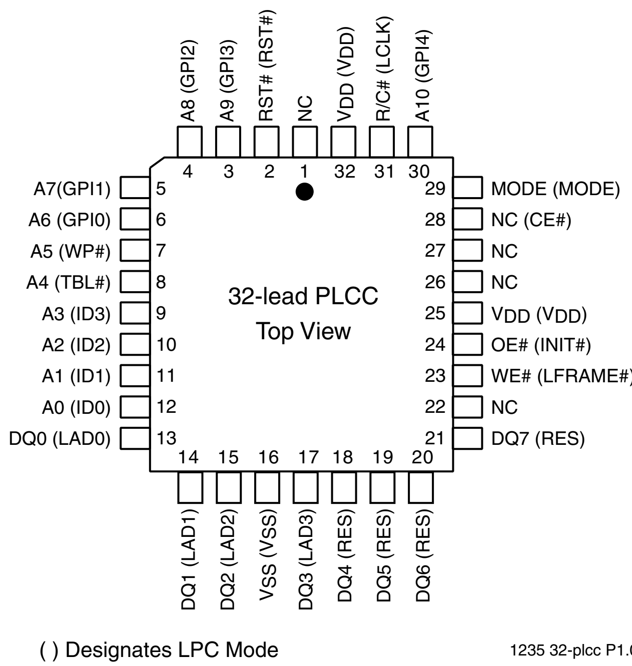


**Figure 2:** Pin Assignments for 32-lead PLCC

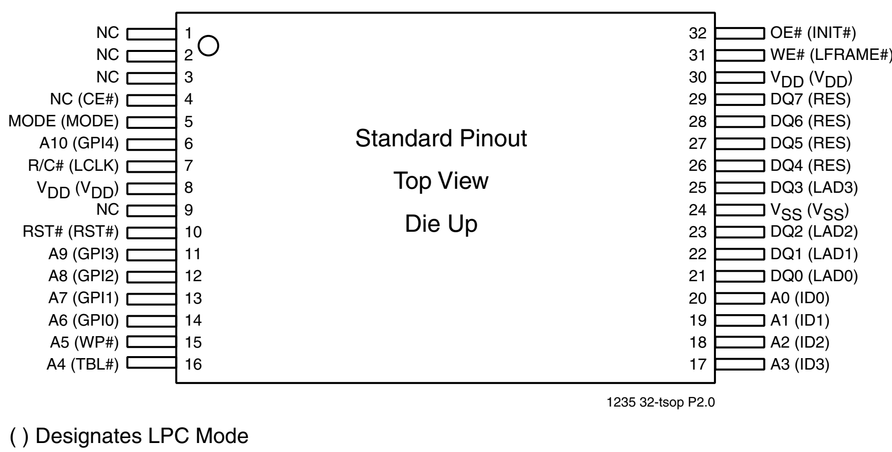


**Figure 3:** Pin Assignments for 32-lead TSOP (8mm x 14mm)

**Table 1:** Pin Description

| Symbol | Pin Name | Type[1] | Interface PP | Interface LPC | Functions |
|---|---|---|---|---|---|
| $A_{10}$-$A_0$ | Address | I | X | | Inputs for low-order addresses during Read and Write operations. Addresses are internally latched during a Write cycle. For the programming interface, these addresses are latched by R/C# and share the same pins as the high-order address inputs. |
| $DQ_7$-$DQ_0$ | Data | I/O | X | | To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high. |
| OE# | Output Enable | I | X | | To gate the data output buffers. |
| WE# | Write Enable | I | X | | To control the Write operations. |
| MODE | Interface Mode Select | I | X | X | This pin determines which interface is operational. When held high, programmer mode is enabled and when held low, LPC mode is enabled. This pin must be setup at power-up or before return from reset and not change during device operation. This pin must be held high ($V_{IH}$) for PP mode and low ($V_{IL}$) for LPC mode. |
| INIT# | Initialize | I | | X | This is the second reset pin for in-system use. This pin is internally combined with the RST# pin; If this pin or RST# pin is driven low, identical operation is exhibited. |
| ID[3:0] | Identification Inputs | I | | X | These four pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component.The boot device must have ID[3:0]=0000 for all subsequent devices should use sequential up-count strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ |
| GPI[4:0] | General Purpose Inputs | I | | X | These individual inputs can be used for additional board flexibility. The state of these pins can be read through LPC registers. These inputs should be at their desired state before the start of the PCI clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated. |
| TBL# | Top Block Lock | I | | X | When low, prevents programming to the boot block sectors at top of memory. When TBL# is high it disables hardware write protection for the top block sectors. This pin cannot be left unconnected. |
| LAD[3:0] | Address and Data | I/O | | X | To provide LPC control signals, as well as addresses and Command Inputs/Outputs data. |
| LCLK | Clock | I | | X | To provide a clock input to the control unit |
| LFRAME# | Frame | I | | X | To indicate start of a data transfer operation; also used to abort an LPC cycle in progress. |
| RST# | Reset | I | X | X | To reset the operation of the device |
| WP# | Write Protect | I | | X | When low, prevents programming to all but the highest addressable blocks. When WP# is high it disables hardware write protection for these blocks. This pin cannot be left unconnected. |
| R/C# | Row/Column Select | I | X | | Select for the Programming interface, this pin determines whether the address pins are pointing to the row addresses, or to the column addresses. |
| RES | Reserved | | | X | These pins must be left unconnected. |
| $V_{DD}$ | Power Supply | PWR | X | X | To provide power supply (3.0-3.6V) |
| $V_{SS}$ | Ground | PWR | X | X | Circuit ground (0V reference) |
| CE# | Chip Enable | I | | X | This signal must be asserted to select the device. When CE# is low, the device is enabled. When CE# is high, the device is placed in low power standby mode. |
| NC | No Connection | I | X | X | Unconnected pins. |

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1. I=Input, O=Output

## Device Memory Maps

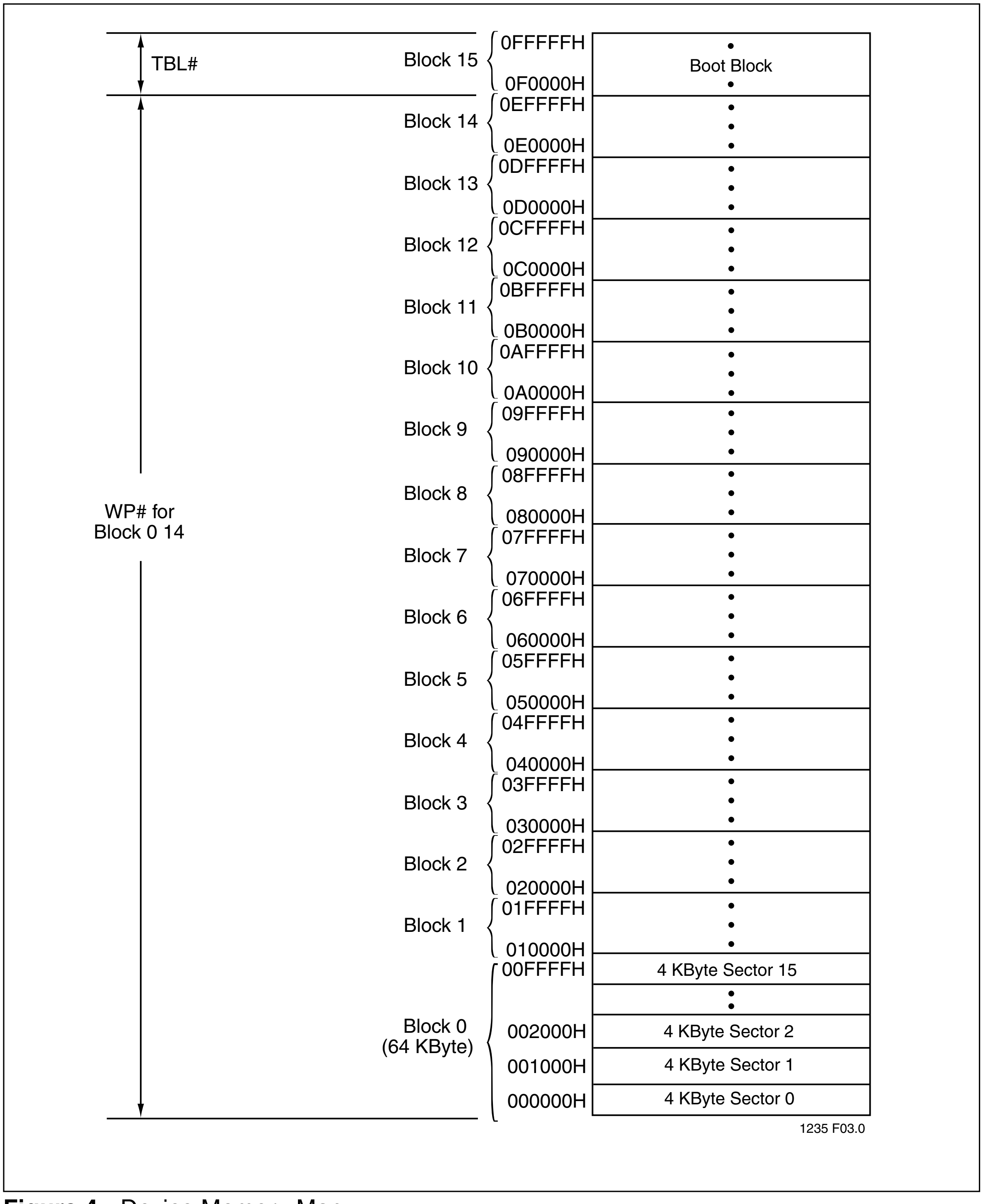


**Figure 4:** Device Memory Map

## Design Considerations

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between $V_{DD}$ and $V_{SS}$ less than 1 cm away from the $V_{DD}$ pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from $V_{DD}$ to $V_{SS}$ should be placed within 5 cm of the $V_{DD}$ pin. If you use a socket for programming purposes add an additional 1-10 µF next to each socket.

## Product Identification

The Product Identification mode identifies the device as the SST49LF080A and manufacturer as SST.

**Table 2:** Product Identification

| | Address | Data |
|---|---|---|
| Manufacturer's ID | 0000H | BFH |
| Device ID | | |
| SST49LF080A | 0001H | 5BH |

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## Mode Selection

The SST49LF080A flash memory devices can operate in two distinct interface modes: the LPC mode and the Parallel Programming (PP) mode. The mode pin is used to set the interface mode selection. If the mode pin is set to logic High, the device is in PP mode. If the mode pin is set Low, the device is in the LPC mode. The mode selection pin must be configured prior to device operation. The mode pin is internally pulled down if the pin is left unconnected. In LPC mode, the device is configured to its host using standard LPC interface protocol. Communication between Host and the SST49LF080A occurs via the 4-bit I/O communication signals, LAD [3:0] and LFRAME#. In PP mode, the device is programmed via an 11-bit address and an 8-bit data I/O parallel signals. The address inputs are multiplexed in row and column selected by control signal R/C# pin. The row addresses are mapped to the lower internal addresses ($A_{10-0}$), and the column addresses are mapped to the higher internal addresses ($A_{MS-11}$). See Figure 4, the Device Memory Map, for address assignments.

# LPC Mode

## Device Operation

The LPC mode uses a 5-signal communication interface, a 4-bit address/data bus, LAD[3:0], and a control line, LFRAME#, to control operations of the SST49LF080A. Cycle type operations such as Memory Read and Memory Write are defined in Intel Low Pin Count Interface Specification, Revision 1.0. JEDEC Standard SDP (Software Data Protection) Program and Erase commands sequences are incorporated into the standard LPC memory cycles. See Figures 7 through 12 for command sequences.

LPC signals are transmitted via the 4-bit Address/Data bus (LAD[3:0]), and follow a particular sequence, depending on whether they are Read or Write operations. LPC memory Read and Write cycle is defined in Tables 5 and 6.

Both LPC Read and Write operations start in a similar way as shown in Figures 5 and 6. The host (which is the term used here to describe the device driving the memory) asserts LFRAME# for two or more clocks and drives a start value on the LAD[3:0] bus.

At the beginning of an operation, the host may hold the LFRAME# active for several clock cycles, and even change the Start value. The LAD[3:0] bus is latched every rising edge of the clock. On the cycle in which LFRAME# goes inactive, the last latched value is taken as the Start value. CE# must be asserted one cycle before the start cycle to select the SST49LF080A for Read and Write operations.

Once the SST49LF080A identifies the operation as valid (a start value of all zeros), it next expects a nibble that indicates whether this is a memory Read or Write cycle. Once this is received, the device is now ready for the Address cycles. The LPC protocol supports a 32-bit address phase. The SST49LF080A encodes ID and register space access in the address field. See Table 3 for address bits definition.

For Write operation the Data cycle will follow the Address cycle, and for Read operation TAR and SYNC cycles occur between the Address and Data cycles. At the end of every operation, the control of the bus must be returned to the host by a 2-clock TAR cycle.

**Table 3:** Address bits definition

| $A_{31}$: $A_{25}$[1] | $A_{24}$:$A_{23}$ | $A_{22}$ | $A_{21}$: $A_{20}$ | $A_{19}$:$A_0$ |
|---|---|---|---|---|
| 1111 111b or 0000 000b | ID[3:2][2] | 1 = Memory Access<br>0 = Register access | ID[1:0][2] | Device Memory address |

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1. The top 32MByte address range FFFF FFFFH to FE00 0000H and the bottom 128 KByte memory access address 000F FFFFH to 000E 0000H are decoded.
2. See Table 7 for multiple device selection configuration

## CE#

The CE# pin, enables and disables the SST49LF080A, controlling read and write access of the device. To enable the SST49LF080A, the CE# pin must be driven low one clock cycle prior to LFRAME# being driven low. The device will enter standby mode when internal Write operations are completed and CE# is high.

## LFRAME#

The LFRAME# signifies the start of a (frame) bus cycle or the termination of an undesired cycle. Asserting LFRAME# for one or more clock cycle and driving a valid START value on LAD[3:0] will initiate device operation. The device will enter standby mode when internal operations are completed and LFRAME# is high.

## TBL#, WP#

The Top Boot Lock (TBL#) and Write Protect (WP#) pins are provided for hardware write protection of device memory. The TBL# pin is used to Write-Protect 16 boot sectors (64 KByte) at the highest memory address range for the SST49LF080A. The WP# pin write protects the remaining sectors in the flash memory.

An active low signal at the TBL# pin prevents Program and Erase operations of the top boot sectors. When TBL# pin is held high, the write protection of the top boot sectors is disabled. The WP# pin serves the same function for the remaining sectors of the device memory. The TBL# and WP# pins write protection functions operate independently of one another.

Both TBL# and WP# pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the TBL# or WP# pin during a Program or Erase operation could cause unpredictable results.

## INIT#, RST#

A $V_{IL}$ on INIT# or RST# pin initiates a device reset. INIT# and RST# pins have the same function internally. It is required to drive INIT# or RST# pins low during a system reset to ensure proper CPU initialization. During a Read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, LAD[3:0], in a high-impedance state. The reset signal must be held low for a minimal duration of time $T_{RSTP}$. A reset latency will occur if a reset procedure is performed during a Program or Erase operation. See Table 19, Reset Timing Parameters for more information. A device reset during an active Program or Erase will abort the operation and memory contents may become invalid due to data being altered or corrupted from an incomplete Erase or Program operation.

## System Memory Mapping

The LPC interface protocol has address length of 32-bit or 4 GByte. The SST49LF080A will respond to addresses in the range as specified in Table 4.

Refer to “Multiple Device Selection” section for more detail on strapping multiple SST49LF080A devices to increase memory densities in a system and “Registers” section on valid register addresses.

**Table 4:** Address Decoding Range

| ID Strapping | Device Access | Address Range | Memory Size |
|---|---|---|---|
| Device #0 - 3 | Memory Access | FFFF FFFFH : FFC0 0000H | 4 MByte |
| | Register Access | FFBF FFFFH : FF80 0000H | 4 MByte |
| Device #4 - 7 | Memory Access | FF7F FFFFH : FF40 0000H | 4 MByte |
| | Register Access | FF3F FFFFH : FF00 0000H | 4 MByte |
| Device #8 - 11 | Memory Access | FEFF FFFFH : FEC0 0000H | 4 MByte |
| | Register Access | FEBF FFFFH : FE80 0000H | 4 MByte |
| Device #12 - 15 | Memory Access | FE7F FFFFH : FE40 0000H | 4 MByte |
| | Register Access | FE3F FFFFH : FE00 0000H | 4 MByte |
| Device #0[1] | Memory Access | 000F FFFFH : 000E 0000H | 128 KByte |

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1. For device #0 (Boot Device), SST49LF080A decodes the physical addresses of the top 2 blocks (including Boot Block) both at
system memory ranges FFFF FFFFH to FFFE 0000H and 000F FFFFH to 000E 0000H.

**Table 5:** LPC Read Cycle

| Clock Cycle | Field Name | Field Contents LAD[3:0][1] | LAD[3:0] Direction | Comments |
|---|---|---|---|---|
| 1 | START | 0000 | IN | LFRAME# must be active (low) for the part to respond. Only the last start field (before LFRAME# transitions high) should be recognized. |
| 2 | CYCTYPE + DIR | 010X | IN | Indicates the type of cycle. Bits 3:2 must be "01b" for memory cycle. Bit 1 indicates the type of transfer "0" for Read. Bit 0 is reserved. |
| 3-10 | ADDRESS | YYYY | IN | Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble fist. See Table 3 for address bits definition and Table 4 for valid memory address range. |
| 11 | TAR0 | 1111 | IN then Float | In this clock cycle, the host has driven the bus to all 1s and then floats the bus. This is the first part of the bus "turnaround cycle." |
| 12 | TAR1 | 1111 (float) | Float then OUT | The SST49LF080A takes control of the bus during this cycle |
| 13 | SYNC | 0000 | OUT | The SST49LF080A outputs the value 0000b indicating that data will be available during the next clock cycle. |
| 14 | DATA | ZZZZ | OUT | This field is the least-significant nibble of the data byte. |
| 15 | DATA | ZZZZ | OUT | This field is the most-significant nibble of the data byte. |
| 16 | TAR0 | 1111 | OUT then Float | In this clock cycle, the SST49LF080A has driven the bus to all 1s and then floats the bus. This is the first part of the bus "turnaround cycle." |
| 17 | TAR1 | 1111 (float) | Float then IN | The host takes control of the bus during this cycle |

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1. Field contents are valid on the rising edge of the present clock cycle.

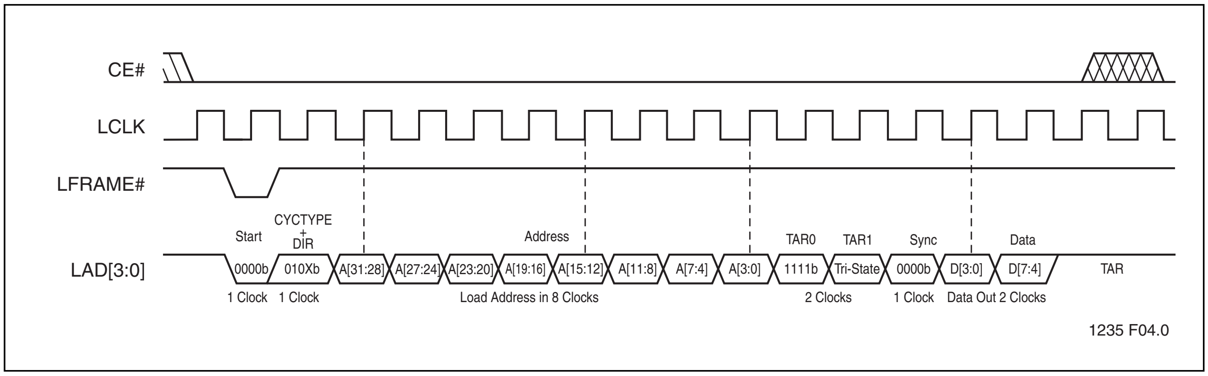


**Figure 5:** LPC Read Cycle Waveform

**Table 6:** LPC Write Cycle

| Clock Cycle | Field Name | Field Contents LAD[3:0][1] | LAD[3:0] Direction | Comments |
|---|---|---|---|---|
| 1 | START | 0000 | IN | LFRAME# must be active (low) for the part to respond. Only the last start field (before LFRAME# transitions high) should be recognized. |
| 2 | CYCTYPE + DIR | 011X | IN | Indicates the type of cycle. Bits 3:2 must be "01b" for memory cycle. Bit 1 indicates the type of transfer "1" for Write. Bit 0 is reserved. |
| 3-10 | ADDRESS | YYYY | IN | Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first. See Table 3 for address bits definition and Table 4 for valid memory address range. |
| 11 | DATA | ZZZZ | IN | This field is the least-significant nibble of the data byte. |
| 12 | DATA | ZZZZ | IN | This field is the most-significant nibble of the data byte. |
| 13 | TAR0 | 1111 | IN then Float | In this clock cycle, the host has driven the bus to all '1's and then floats the bus. This is the first part of the bus "turnaround cycle." |
| 14 | TAR1 | 1111 (float) | Float then OUT | The SST49LF080A takes control of the bus during this cycle. |
| 15 | SYNC | 0000 | OUT | The SST49LF080A outputs the values 0000, indicating that it has received data or a flash command. |
| 16 | TAR0 | 1111 | OUT then Float | In this clock cycle, the SST49LF080A has driven the bus to all '1's and then floats the bus. This is the first part of the bus "turnaround cycle." |
| 17 | TAR1 | 1111 (float) | Float then IN | Host resumes control of the bus during this cycle. |

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1. Field contents are valid on the rising edge of the present clock cycle.

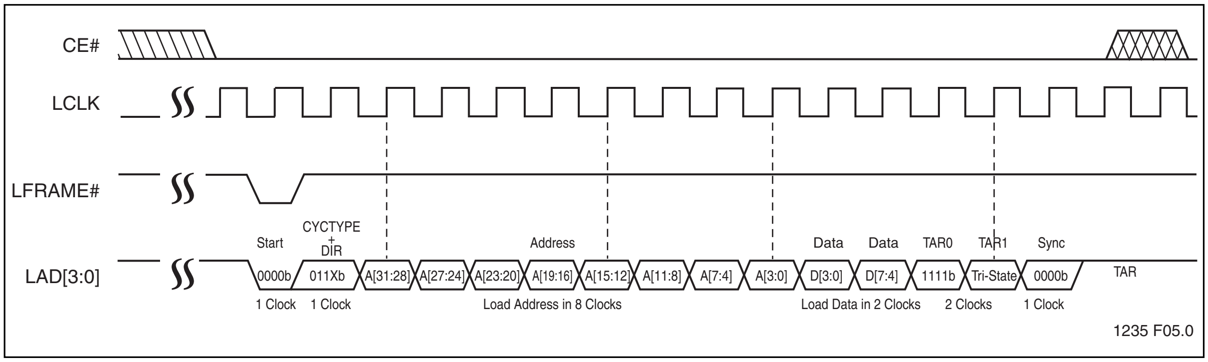


**Figure 6:** LPC Write Cycle Waveform

## Response To Invalid Fields

During LPC Read/Write operations, the SST49LF080A will not explicitly indicate that it has received invalid field sequences. The response to specific invalid fields or sequences is as follows:

**Address out of range:** The SST49LF080A will only respond to address ranges as specified in Table 4.

**ID mismatch**: ID information is included in every address cycle. The SST49LF080A will compare ID bits in the address field with the hardware ID strapping. If there is a mis-match, the device will ignore the cycle. See Multiple Device Selection section for details.

Once valid START, CYCTYPE + DIR, valid address range and ID bits are received, the SST49LF080A will always complete the bus cycle. However, if the device is busy performing a flash Erase or Program operation, no new internal Write command (memory write or register write) will be executed. As long as the states of LAD[3:0] and LAD[4] are known, the response of the SST49LF080A to signals received during the LPC cycle should be predictable.

## Abort Mechanism

If LFRAME# is driven low for one or more clock cycles after the start of an LPC cycle, the cycle will be terminated. The host may drive the LAD[3:0] with '1111b' (ABORT nibble) to return the interface to ready mode. The ABORT only affects the current bus cycle. For a multi-cycle command sequence, such as the Erase or Program SDP commands, ABORT doesn't interrupt the entire command sequence, but only the current bus cycle of the command sequence. The host can re-send the bus cycle and continue the SDP command sequence after the device is ready again.

## Write Operation Status Detection

The SST49LF080A device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling, D[7], and Toggle Bit, D[6]. The End-of-Write detection mode is incorporated into the LPC Read Cycle. The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either D[7] or D[6]. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

### Data# Polling

When the SST49LF080A device is in the internal Program operation, any attempt to read D[7] will produce the complement of the true data. Once the Program operation is completed, D[7] will produce true data. Note that even though D[7] may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read D[7] will produce a '0'. Once the internal Erase operation is completed, D[7] will produce a '1'. Proper status will not be given using Data# Polling if the address is in the invalid range.

### Toggle Bit

During the internal Program or Erase operation, any consecutive attempts to read D[6] will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop.

## Multiple Device Selection

Multiple LPC flash devices may be strapped to increase memory densities in a system. The four ID pins, ID[3:0], allow up to 16 devices to be attached to the same bus by using different ID strapping in a system. BIOS support, bus loading, or the attaching bridge may limit this number. The boot device must have an ID of 0 (determined by ID[3:0]); subsequent devices use incremental numbering. Equal density must be used with multiple devices.

When used as a boot device, ID[3:0] must be strapped as 0000; all subsequent devices should use a sequential up-count strapping (i.e. 0001, 0010, 0011, etc.). With the hardware strapping, ID information is included in every LPC address memory cycle. The ID bits in the address field are inverse of the hardware strapping. The address bits [$A_{24}$:$A_{23}$, $A_{21}$:$A_{20}$] are used to select the device with proper IDs. See Table 7 for IDs. The SST49LF080A will compare these bits with ID[3:0]'s strapping values. If there is a mismatch, the device will ignore the remainder of the cycle.

**Table 7:** Multiple Device Selection Configuration

| Device # | Hardware Strapping ID[3:0] | Address Bits Decoding | | | |
|---|---|---|---|---|---|
| | | $A_{24}$ | $A_{23}$ | $A_{21}$ | $A_{20}$ |
| 0 (Boot device) | 0000 | 1 | 1 | 1 | 1 |
| 1 | 0001 | 1 | 1 | 1 | 0 |
| 2 | 0010 | 1 | 1 | 0 | 1 |
| 3 | 0011 | 1 | 1 | 0 | 0 |
| 4 | 0100 | 1 | 0 | 1 | 1 |
| 5 | 0101 | 1 | 0 | 1 | 0 |
| 6 | 0110 | 1 | 0 | 0 | 1 |
| 7 | 0111 | 1 | 0 | 0 | 0 |
| 8 | 1000 | 0 | 1 | 1 | 1 |
| 9 | 1001 | 0 | 1 | 1 | 0 |
| 10 | 1010 | 0 | 1 | 0 | 1 |
| 11 | 1011 | 0 | 1 | 0 | 0 |
| 12 | 1100 | 0 | 0 | 1 | 1 |
| 13 | 1101 | 0 | 0 | 1 | 0 |
| 14 | 1110 | 0 | 0 | 0 | 1 |
| 15 | 1111 | 0 | 0 | 0 | 0 |

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## Registers

There are two registers available on the SST49LF080A, the General Purpose Inputs Registers (GPI_REG) and the JEDEC ID Registers. Since multiple LPC memory devices may be used to increase memory densities, these registers appear at its respective address location in the 4 GByte system memory map. Unused register locations will read as 00H. Any attempt to read registers during internal Write operation will respond as “Write operation status detection” (Data# Polling or Toggle Bit). Any attempt to write any registers during internal Write operation will be ignored. Table 9 lists GPI_REG and JEDEC ID address locations for SST49LF080A with its respective device strapping.

**Table 8:** General Purpose Inputs Register

| Bit | Function | Pin # | |
|---|---|---|---|
| | | 32-PLCC | 32-TSOP |
| 7:5 | Reserved | - | - |
| 4 | GPI[4]<br>Reads status of general purpose input pin | 30 | 6 |
| 3 | GPI[3]<br>Reads status of general purpose input pin | 3 | 11 |
| 2 | GPI[2]<br>Reads status of general purpose input pin | 4 | 12 |
| 1 | GPI[1]<br>Reads status of general purpose input pin | 5 | 13 |
| 0 | GPI[0]<br>Reads status of general purpose input pin | 6 | 14 |

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## General Purpose Inputs Register

The GPI_REG (General Purpose Inputs Register) passes the state of GPI[4:0] pins at power-up on the SST49LF080A. It is recommended that the GPI[4:0] pins be in the desired state before LFRAME# is brought low for the beginning of the next bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. See the General Purpose Inputs Register table for the GPI_REG bits and function, and Table 9 for memory address locations for its respective device strapping.

## JEDEC ID Registers

The JEDEC ID registers identify the device as SST49LF080A and manufacturer as SST in LPC mode. See Table 9 for memory address locations for its respective JEDEC ID location.

**Table 9:** Memory Map Register Addresses for SST49LF080A

| Device # | Hardware Strapping ID[3:0] | GPI_REG | JEDEC ID | |
|---|---|---|---|---|
| | | | Manufacturer | Device |
| 0 (Boot device) | 0000 | FFBC 0100H | FFBC 0000H | FFBC 0001H |
| 1 | 0001 | FFAC 0100H | FFAC 0000H | FFAC 0001H |
| 2 | 0010 | FF9C 0100H | FF9C 0000H | FF9C 0001H |
| 3 | 0011 | FF8C 0100H | FF8C 0000H | FF8C 0001H |
| 4 | 0100 | FF3C 0100H | FF3C 0000H | FF3C 0001H |
| 5 | 0101 | FF2C 0100H | FF2C 0000H | FF2C 0001H |
| 6 | 0110 | FF1C 0100H | FF1C 0000H | FF1C 0001H |
| 7 | 0111 | FF0C 0100H | FF0C 0000H | FF0C 0001H |
| 8 | 1000 | FEBC 0100H | FEBC 0000H | FEBC 0001H |
| 9 | 1001 | FEAC 0100H | FEAC 0000H | FEAC 0001H |
| 10 | 1010 | FE9C 0100H | FE9C 0000H | FE9C 0001H |
| 11 | 1011 | FE8C 0100H | FE8C 0000H | FE8C 0001H |
| 12 | 1100 | FE3C 0100H | FE3C 0000H | FE3C 0001H |
| 13 | 1101 | FE2C 0100H | FE2C 0000H | FE2C 0001H |
| 14 | 1110 | FE1C 0100H | FE1C 0000H | FE1C 0001H |
| 15 | 1111 | FE0C 0100H | FE0C 0000H | FE0C 0001H |

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# Parallel Programming Mode

## Device Operation

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#. During the software command sequence the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

## Reset

Driving the RST# low will initiate a hardware reset of the SST49LF080A. See Table 25 for Reset timing parameters and Figure 17 for Reset timing diagram.

## Read

The Read operation of the SST49LF080A device is controlled by OE#. OE# is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram, Figure 18, for further details.

## Byte-Program Operation

The SST49LF080A device is programmed on a byte-by-byte basis. Before programming, one must ensure that the sector in which the byte is programmed is fully erased. The Byte-Program operation is initiated by executing a four-byte command load sequence for Software Data Protection with address (BA) and data in the last byte sequence. During the Byte-Program operation, the row address ($A_{10}$-$A_0$) is latched on the falling edge of R/C# and the column address ($A_{21}$-$A_{11}$) is latched on the rising edge of R/C#. The data bus is latched on the rising edge of WE#. The Program operation, once initiated, will be completed, within 20 µs. See Figure 22 for Program operation timing diagram and Figure 34 for its flowchart. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

## Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 23 for Sector-Erase timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

## Block-Erase Operation

The Block-Erase Operation allows the system to erase the device in 64 KByte uniform block size for the SST49LF080A. The Block-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Block-Erase command (50H) and block address. The internal Block-Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 24 for Block-Erase timing waveforms. Any commands written during the Block-Erase operation will be ignored.

## Chip-Erase Operation

The SST49LF080A devices provide a Chip-Erase operation, which allows the user to erase the entire memory array to the “1s” state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six- byte Software Data Protection command sequence with Chip-Erase command (10H) with address 5555H in the last byte sequence. The internal Erase operation begins with the rising edge of the sixth WE#. During the internal Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 11 for the command sequence, Figure 25 for Chip-Erase timing diagram, and Figure 37 for the flowchart. Any commands written during the Chip-Erase operation will be ignored.

## Write Operation Status Detection

The SST49LF080A devices provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling D[7] and Toggle Bit D[6]. The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either D[7] or D[6]. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

### Data# Polling ($DQ_7$)

When the SST49LF080A device is in the internal Program operation, any attempt to read $DQ_7$ will produce the complement of the true data. Once the Program operation is completed, $DQ_7$ will produce true data. Note that even though $DQ_7$ may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs. During internal Erase operation, any attempt to read $DQ_7$ will produce a ‘0’. Once the internal Erase operation is completed, $DQ_7$ will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# pulse. See Figure 20 for Data# Polling timing diagram and Figure 35 for a flowchart. Proper status will not be given using Data# Polling if the address is in the invalid range.

### Toggle Bit ($DQ_6$)

During the internal Program or Erase operation, any consecutive attempts to read $DQ_6$ will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of fourth WE# pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# pulse. See Figure 21 for Toggle Bit timing diagram and Figure 35 for a flowchart.

**Table 10:** Operation Modes Selection (PP Mode)

| Mode | RST# | OE# | WE# | DQ | Address |
|---|---|---|---|---|---|
| Read | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | $D_{OUT}$ | $A_{IN}$ |
| Program | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | $D_{IN}$ | $A_{IN}$ |
| Erase | $V_{IH}$ | $V_{IH}$ | $V_{IL}$ | X[1] | Sector or Block address, XXH for Chip-Erase |
| Reset | $V_{IL}$ | X | X | High Z | X |
| Write Inhibit | $V_{IH}$<br>X | $V_{IL}$<br>X | X<br>$V_{IH}$ | High Z/$D_{OUT}$<br>High Z/$D_{OUT}$ | X<br>X |
| Product Identification | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | Manufacturer's ID (BFH) Device ID[2] | See Table 11 |

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1. X can be $V_{IL}$ or $V_{IH}$, but no other value.
2. Device ID = 5BH for SST49LF080A

## Data Protection (PP Mode)

The SST49LF080A devices provide both hardware and software features to protect nonvolatile data from inadvertent writes.

### Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

$V_{DD}$ Power Up/Down Detection: The Write operation is inhibited when $V_{DD}$ is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

### Software Data Protection (SDP)

The SST49LF080A provides the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of a six-byte load sequence.

# Software Command Sequence

**Table 11:** Software Command Sequence

| Command Sequence | 1st[1] Cycle | | 2nd[1] Cycle | | 3rd[1] Cycle | | 4th[1] Cycle | | 5th[1] Cycle | | 6th[1] Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Addr[2] | Data | Addr[2] | Data | Addr[2] | Data | Addr[2] | Data | Addr[2] | Data | Addr[2] | Data |
| Byte-Program | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | A0H | PA[3] | Data | | | | |
| Sector-Erase | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 80H | YYYY 5555H | AAH | YYYY 2AAAH | 55H | $SA_X$[4] | 30H |
| Block-Erase | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 80H | YYYY 5555H | AAH | YYYY 2AAAH | 55H | $BA_X$[5] | 50H |
| Chip-Erase[6] | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 80H | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 10H |
| Software ID Entry | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | 90H | Read ID[7] | | | | | |
| Software ID Exit[8] | XXXX XXXXH | F0H | | | | | | | | | | |
| Software ID Exit[8] | YYYY 5555H | AAH | YYYY 2AAAH | 55H | YYYY 5555H | F0H | | | | | | |

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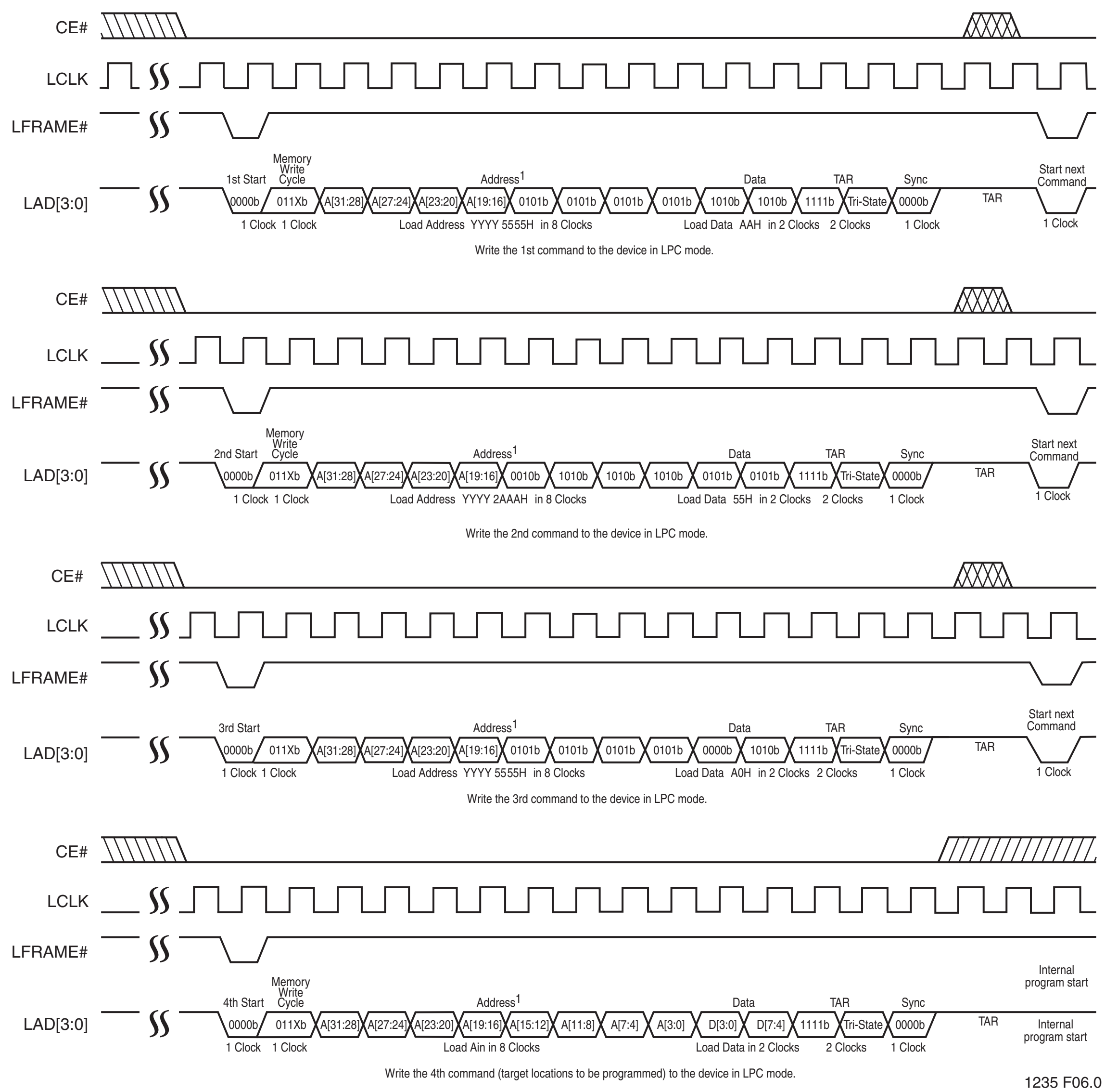
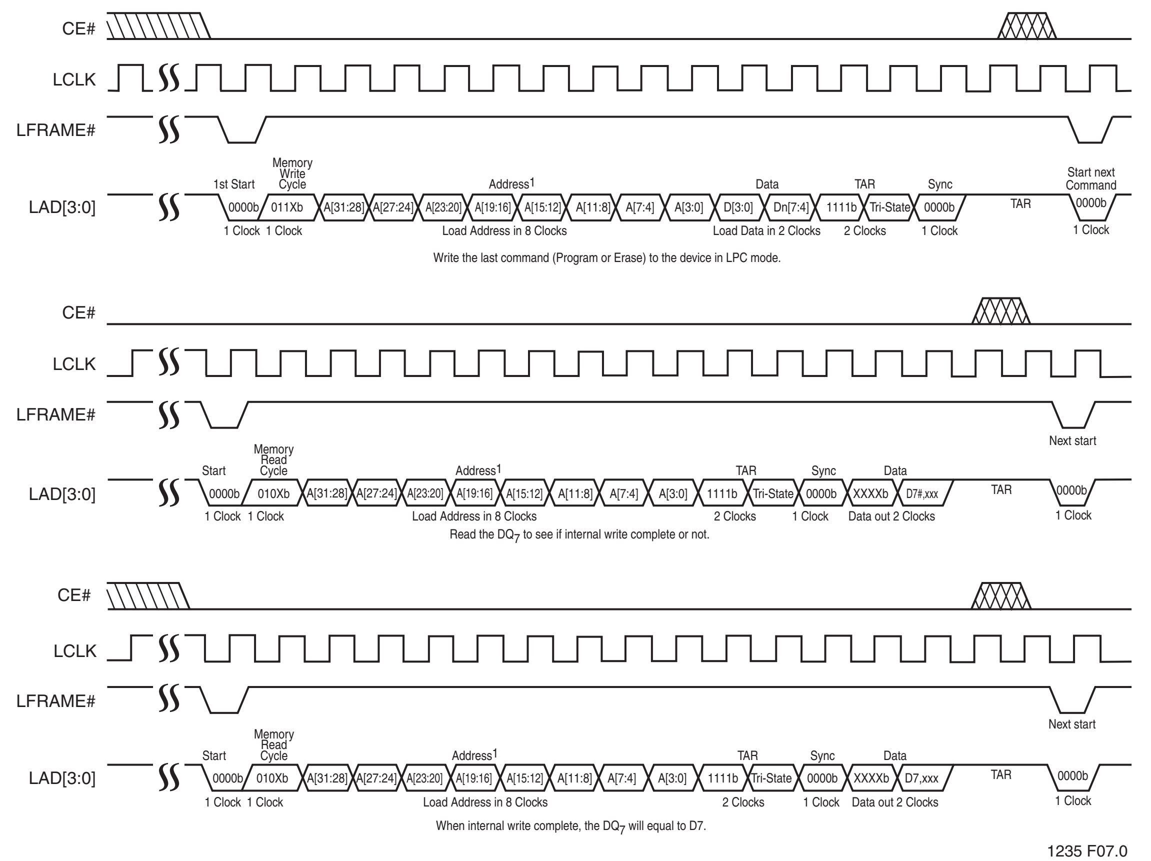
1. LPC mode use consecutive Write cycles to complete a command sequence; PP mode use consecutive bus cycles to complete a command sequence.
2. YYYY = A[31:16]. In LPC mode, during SDP command sequence, YYYY must be within memory address range specified in Table 4. In PP mode, YYYY can be $V_{IL}$ or $V_{IH}$, but no other value.
3. PA = Program Byte address
4. $SA_X$ for Sector-Erase Address
5. $BA_X$ for Block-Erase Address
6. Chip-Erase is supported in PP mode only
7. SST Manufacturer's ID = BFH, is read with $A_0$ = 0.
   With $A_{19}$-$A_1$ = 0; SST49LF080A Device ID = 5BH, is read with $A_0$ = 1.
8. Both Software ID Exit operations are equivalent



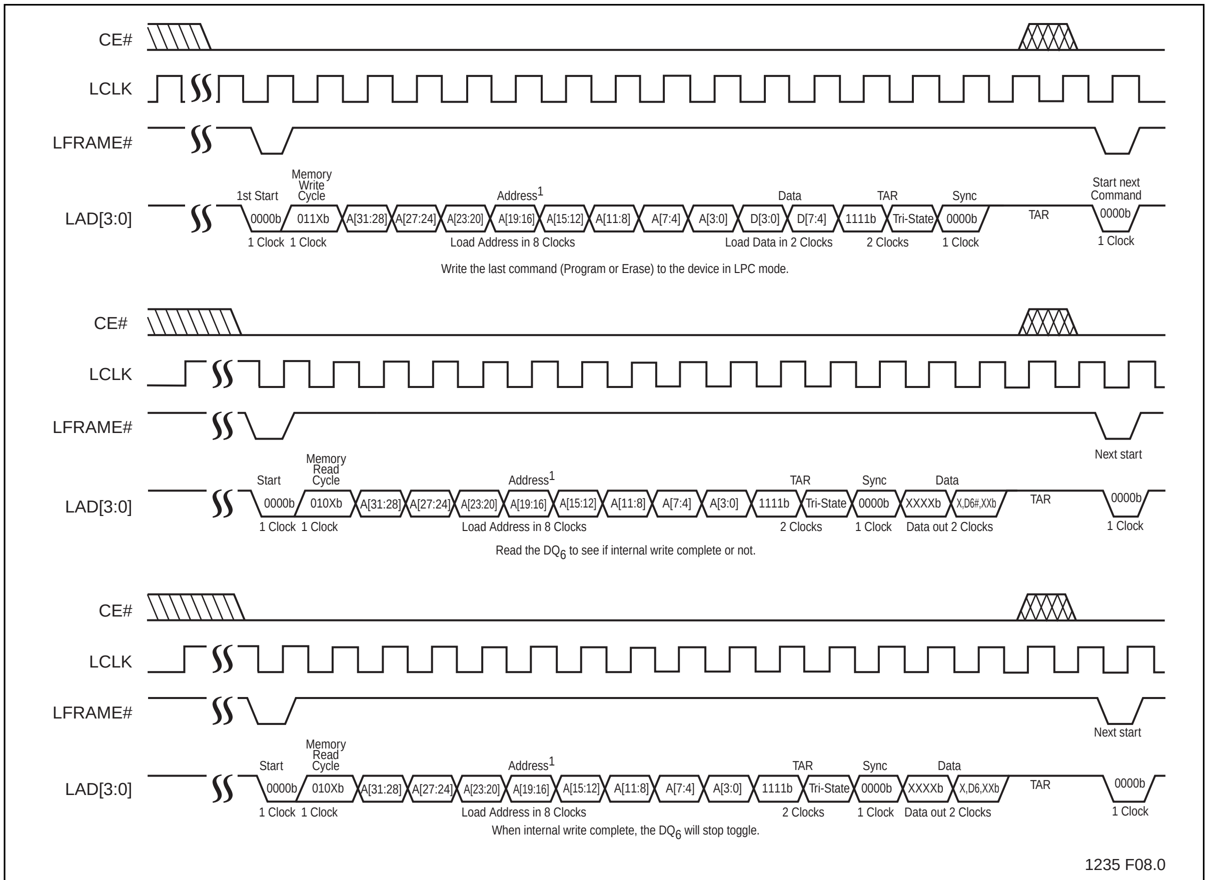

**Note:** 1. Address must be within memory address range specified in Table 4.

**Figure 7:** Program Command Sequence (LPC Mode)




**Note:** 1. Address must be within memory address range specified in Table 4.

**Figure 8:** Data# Polling Command Sequence (LPC Mode)




**Note:** 1. Address must be within memory address range specified in Table 4.

**Figure 9:** Toggle Bit Command Sequence (LPC Mode)

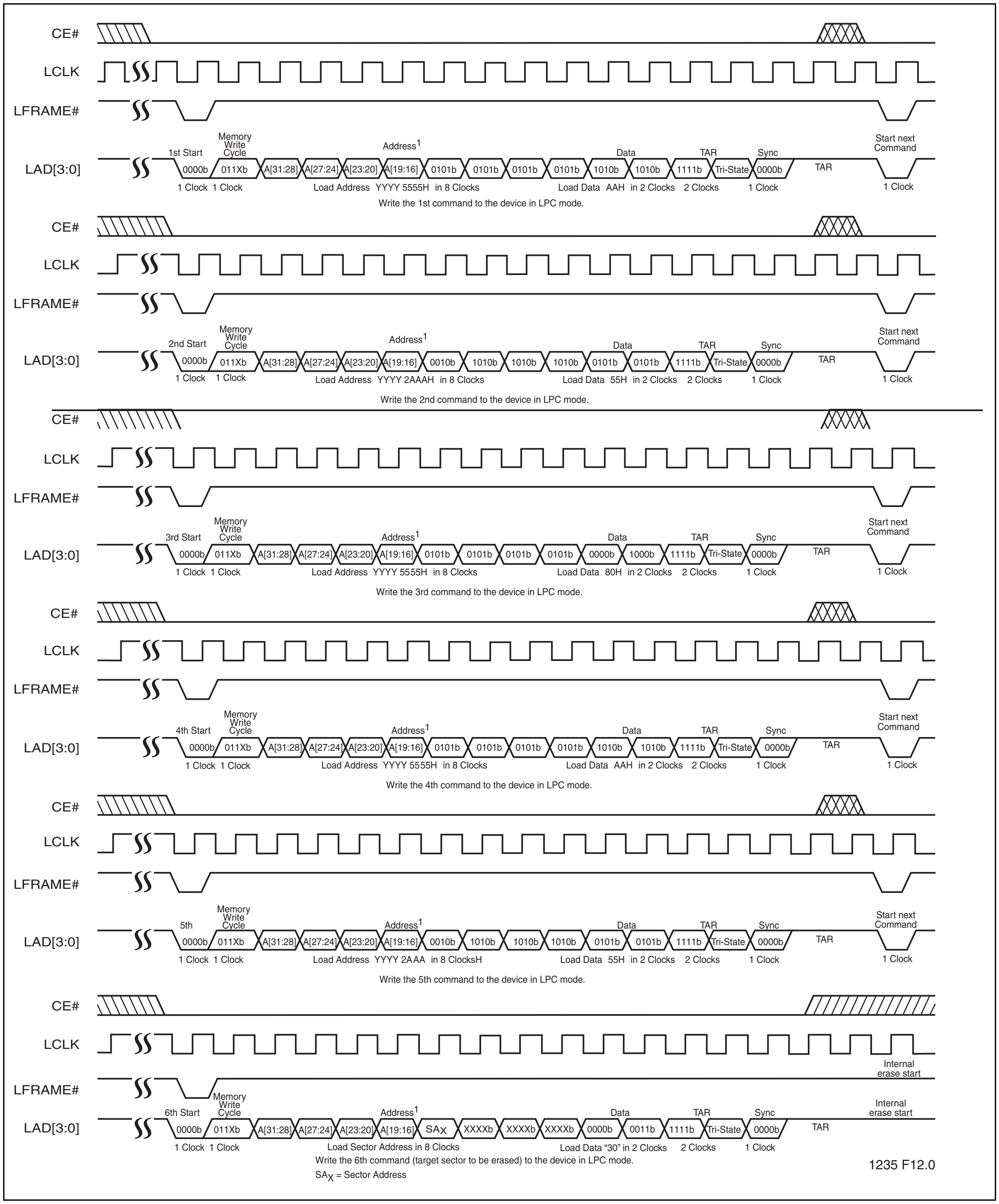
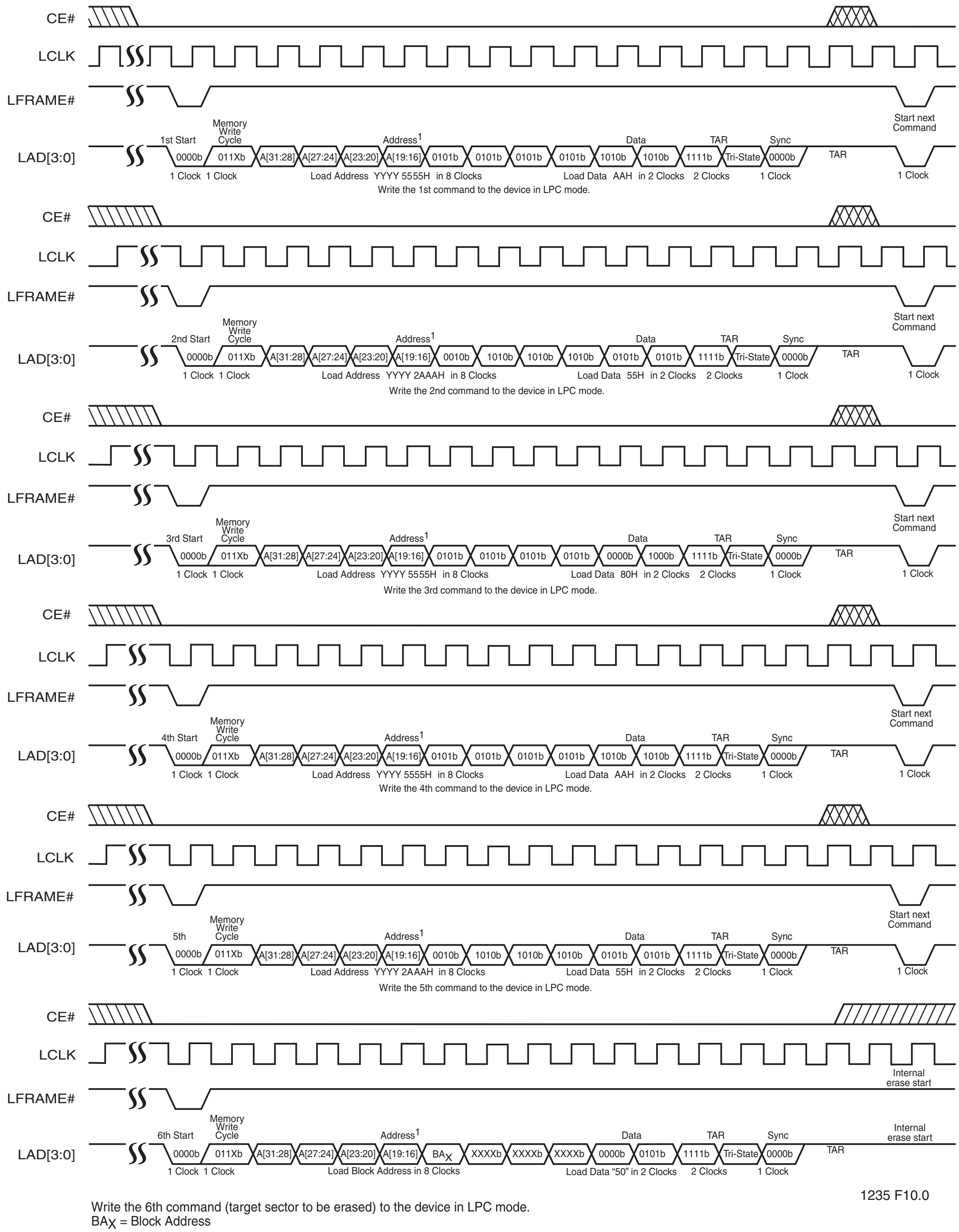
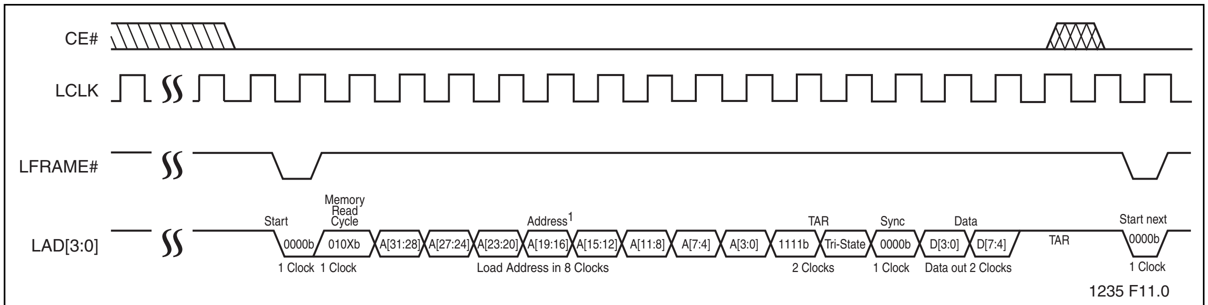



**Figure 10:** Sector-Erase Command Sequence (LPC Mode)




**Note:** 1. Address must be within memory address range specified in Table 4.

**Figure 11:** Block-Erase Command Sequence (LPC Mode)




**Note:** 1. See Table 9 for register addresses.

**Figure 12:** Register Readout Command Sequence (LPC Mode)DS20005086

# Electrical Specifications

The AC and DC specifications for the LPC interface signals (LA0[3:0], LFRAME, LCLCK and RST#) as defined in Section 4.2.2.4 of the PCI local Bus specification, Rev. 2.1. Refer to Table 14 for the DC voltage and current specifications. Refer to Tables 18 through 21 and Tables 23 through 25 for the AC timing specifications for Clock, Read, Write, and Reset operations.

**Absolute Maximum Stress Ratings** (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this datasheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -55°C to +125°C
Storage Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -65°C to +150°C
D.C. Voltage on Any Pin to Ground Potential . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5V to $V_{DD}$+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . . . . . . . . . . . . . . . -2.0V to $V_{DD}$+2.0V
Package Power Dissipation Capability (Ta=25°C) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1.0W
Surface Mount Solder Reflow Temperature[1] . . . . . . . . . . . . . . . . . . . . . . . . . . 260°C for 10 seconds
Output Short Circuit Current[2]. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 50 mA

1. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

**Table 12:** Operating Range

| Range | Ambient Temp | $V_{DD}$ |
|---|---|---|
| Commercial | 0°C to +85°C | 3.0-3.6V |

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**Table 13:** AC Conditions of Test[1]

| Input Rise/Fall Time | Output Load |
|---|---|
| 3 ns | $C_L$ = 30 pF |

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1. See Figures 28 and 29

## DC Characteristics

**Table 14:** DC Operating Characteristics (All Interfaces)

| Symbol | Parameter | Limits | | | Test Conditions |
|---|---|---|---|---|---|
| | | Min | Max | Units | |
| $I_{DD}$[1] | Active $V_{DD}$ Current | | | | LCLK (LPC mode) and Address Input (PP mode)=$V_{ILT}/V_{IHT}$ at f=33 MHz (LPC mode) or 1/$T_{RC\ min}$ (PP Mode) All other inputs=$V_{IL}$ or $V_{IH}$ |
| | Read | | 12 | mA | All outputs = open, $V_{DD}$=$V_{DD}$ Max |
| | Write | | 24 | mA | See Note[2] |
| $I_{SB}$ | Standby $V_{DD}$ Current (LPC Interface) | | 100 | µA | LCLK (LPC mode) and Address Input (PP mode)=$V_{ILT}/V_{IHT}$ at f=33 MHz (LPC mode) or 1/$T_{RC\ min}$ (PP Mode) LFRAME#=0.9 $V_{DD}$, f=33 MHz, CE#=0.9 $V_{DD}$, $V_{DD}$=$V_{DD}$ Max, All other inputs ≥ 0.9 $V_{DD}$ or ≤ 0.1 $V_{DD}$ |
| $I_{RY}$[3] | Ready Mode $V_{DD}$ Current (LPC Interface) | | 10 | mA | LCLK (LPC mode) and Address Input (PP mode)=$V_{ILT}/V_{IHT}$ at f=33 MHz (LPC mode) or 1/$T_{RC\ min}$ (PP Mode) LFRAME#=$V_{IL}$, f=33 MHz, $V_{DD}$=$V_{DD}$ Max All other inputs ≥ 0.9 $V_{DD}$ or ≤ 0.1 $V_{DD}$ |
| $I_I$ | Input Current for Mode and ID[3:0] pins | | 200 | µA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{LI}$ | Input Leakage Current | | 1 | µA | $V_{IN}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $I_{LO}$ | Output Leakage Current | | 1 | µA | $V_{OUT}$=GND to $V_{DD}$, $V_{DD}$=$V_{DD}$ Max |
| $V_{IHI}$ | INIT# Input High Voltage | 1.1 | $V_{DD}$+0.5 | V | $V_{DD}$=$V_{DD}$ Max |
| $V_{ILI}$ | INIT# Input Low Voltage | -0.5 | 0.4 | V | $V_{DD}$=$V_{DD}$ Min |
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.3 $V_{DD}$ | V | $V_{DD}$=$V_{DD}$ Min |
| $V_{IH}$ | Input High Voltage | 0.5 $V_{DD}$ | $V_{DD}$+0.5 | V | $V_{DD}$=$V_{DD}$ Max |
| $V_{OL}$ | Output Low Voltage | | 0.1 $V_{DD}$ | V | $I_{OL}$=1500 µA, $V_{DD}$=$V_{DD}$ Min |
| $V_{OH}$ | Output High Voltage | 0.9 $V_{DD}$ | | V | $I_{OH}$=-500 µA, $V_{DD}$=$V_{DD}$ Min |

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1. $I_{DD}$ active while a Read or Write (Program or Erase) operation is in progress.
2. For PP Mode: OE# = WE# = $V_{IH}$; For LPC Mode: f = 1/$T_{RC}$ min, LFRAME# = $V_{IH}$, CE# = $V_{IL}$.
3. The device is in Ready mode when no activity is on the LPC bus.

**Table 15:** Recommended System Power-up Timings

| Symbol | Parameter | Minimum | Units |
|---|---|---|---|
| $T_{PU\text{-}READ}$[1] | Power-up to Read Operation | 100 | µs |
| $T_{PU\text{-}WRITE}$[1] | Power-up to Write Operation | 100 | µs |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

**Table 16:** Pin Capacitance **($V_{DD}$=3.3V, Ta=25 °C, f=1 Mhz, other pins open)**

| Parameter | Description | Test Condition | Maximum |
|---|---|---|---|
| $C_{I/O}$[1] | I/O Pin Capacitance | $V_{I/O}$=0V | 12 pF |
| $C_{IN}$[1] | Input Capacitance | $V_{IN}$=0V | 12 pF |

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 17:** Reliability Characteristics

| Symbol | Parameter | Minimum Specification | Units | Test Method |
|---|---|---|---|---|
| $N_{END}$[1] | Endurance | 10,000 | Cycles | JEDEC Standard A117 |
| $T_{DR}$[1] | Data Retention | 100 | Years | JEDEC Standard A103 |
| $I_{LTH}$[1] | Latch Up | 100 + $I_{DD}$ | mA | JEDEC Standard 78 |

T17.0 25026

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

**Table 18:** Clock Timing Parameters (LPC Mode)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CYC}$ | LCLK Cycle Time | 30 | | ns |
| $T_{HIGH}$ | LCLK High Time | 11 | | ns |
| $T_{LOW}$ | LCLK Low Time | 11 | | ns |
| - | LCLK Slew Rate (peak-to-peak) | 1 | 4 | V/ns |
| - | RST# or INIT# Slew Rate | 50 | | mV/ns |

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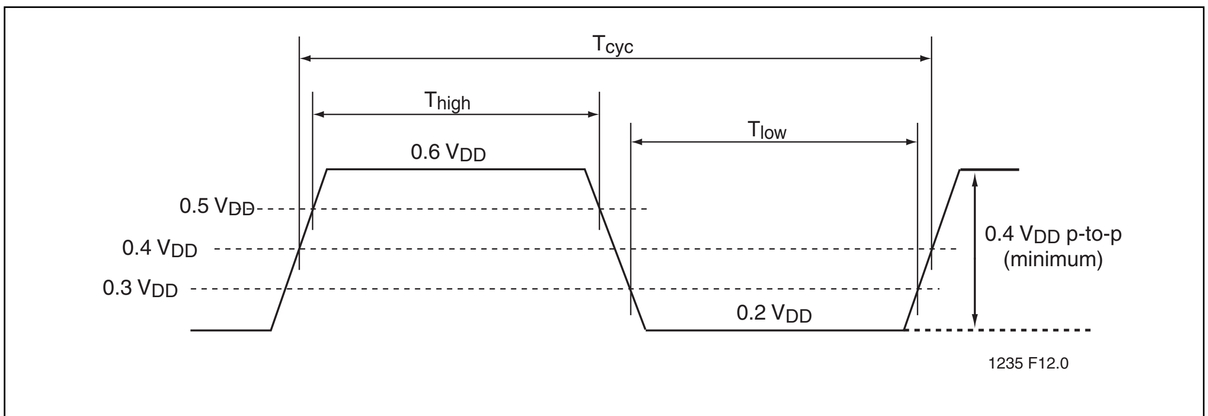


**Figure 13:** LCLK Waveform (LPC Mode)

**Table 19:** Reset Timing Parameters, $V_{DD}$=3.0-3.6V (LPC Mode)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{PRST}$ | $V_{DD}$ stable to Reset Low | 1 | | ms |
| $T_{KRST}$ | Clock Stable to Reset Low | 100 | | µs |
| $T_{RSTP}$ | RST# Pulse Width | 100 | | ns |
| $T_{RSTF}$ | RST# Low to Output Float | | 48 | ns |
| $T_{RST}$[1] | RST# High to LFRAME# Low | 1 | | µs |
| $T_{RSTE}$ | RST# Low to reset during Sector-/Block-Erase or Program | | 10 | µs |

T19.0 25026

1. There may be additional latency due to $T_{RSTE}$ if a reset procedure is performed during a Program or Erase operation.

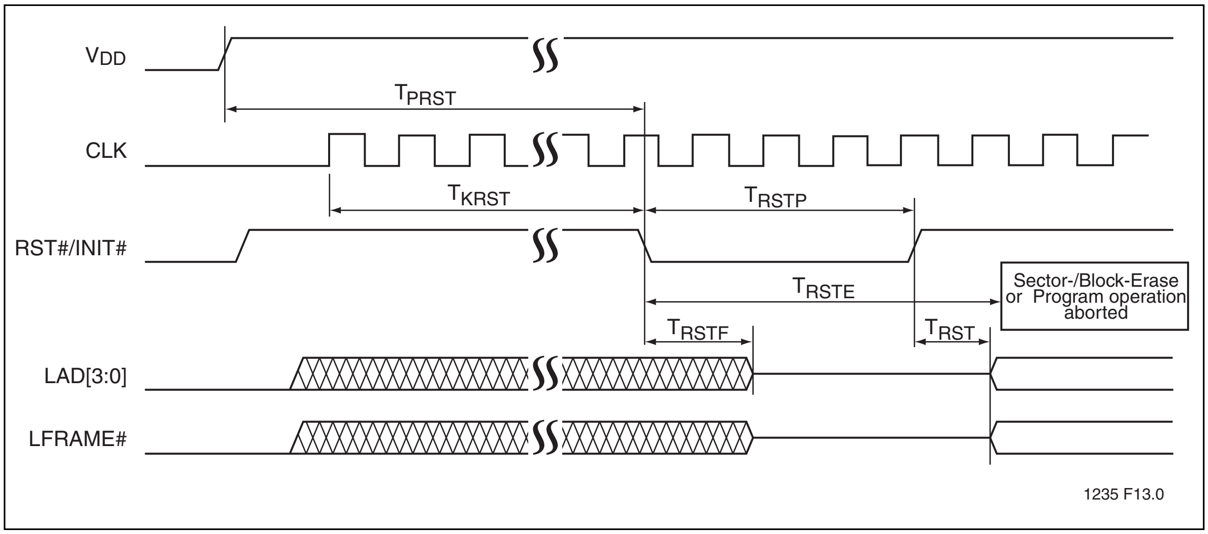


**Figure 14:** Reset Timing Diagram (LPC Mode)

## AC Characteristics

**Table 20:** Read/Write Cycle Timing Parameters, $V_{DD}$=3.0-3.6V (LPC Mode)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CYC}$ | Clock Cycle Time | 30 | | ns |
| $T_{SU}$ | Data Set Up Time to Clock Rising | 7 | | ns |
| $T_{DH}$ | Clock Rising to Data Hold Time | 0 | | ns |
| $T_{VAL}$[1] | Clock Rising to Data Valid | 2 | 11 | ns |
| $T_{BP}$ | Byte Programming Time | | 20 | µs |
| $T_{SE}$ | Sector-Erase Time | | 25 | ms |
| $T_{BE}$ | Block-Erase Time | | 25 | ms |
| $T_{ON}$ | Clock Rising to Active (Float to Active Delay) | 2 | | ns |
| $T_{OFF}$ | Clock Rising to Inactive (Active to Float Delay) | | 28 | ns |

T20.0 25026

1. Minimum and maximum times have different loads. See PCI spec.

**Table 21:** AC Input/Output Specifications (LPC Mode)

| Symbol | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $I_{OH}$(AC) | Switching Current High | -12 $V_{DD}$<br>-17.1($V_{DD}$-$V_{OUT}$) | Equation C[1] | mA<br>mA | 0 < $V_{OUT} \leq$ 0.3 $V_{DD}$<br>0.3 $V_{DD}$ < $V_{OUT}$ < 0.9 $V_{DD}$<br>0.7 $V_{DD}$ < $V_{OUT}$ < $V_{DD}$ |
| | (Test Point) | | -32 $V_{DD}$ | mA | $V_{OUT}$ = 0.7 $V_{DD}$ |
| $I_{OL}$(AC) | Switching Current Low | 16 $V_{DD}$<br>26.7 $V_{OUT}$ | Equation D[1] | mA<br>mA | $V_{DD}$ >$V_{OUT} \geq$ 0.6 $V_{DD}$<br>0.6 $V_{DD}$ > $V_{OUT}$ > 0.1 $V_{DD}$<br>0.18 $V_{DD}$ > $V_{OUT}$ > 0 |
| | (Test Point) | | 38 $V_{DD}$ | mA | $V_{OUT}$ = 0.18 $V_{DD}$ |
| $I_{CL}$ | Low Clamp Current | -25+($V_{IN}$+1)/0.015 | | mA | -3 < $V_{IN} \leq$-1 |
| $I_{CH}$ | High Clamp Current | 25+($V_{IN}$-$V_{DD}$-1)/0.015 | | mA | $V_{DD}$+4 > $V_{IN} \geq V_{DD}$+1 |
| slewr[2] | Output Rise Slew Rate | 1 | 4 | V/ns | 0.2 $V_{DD}$-0.6 $V_{DD}$ load |
| slewf[2] | Output Fall Slew Rate | 1 | 4 | V/ns | 0.6 $V_{DD}$-0.2 $V_{DD}$ load |

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1. See PCI spec.
2. PCI specification output load is used.

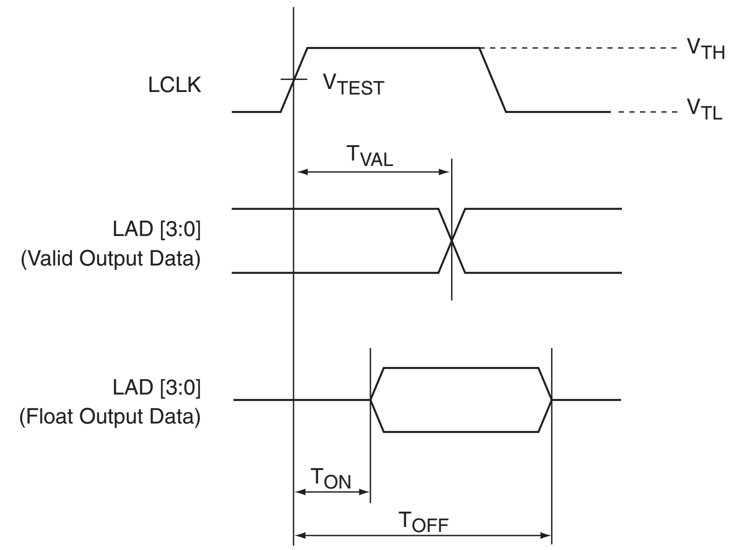


**Figure 15:** Output Timing Parameters (LPC Mode)

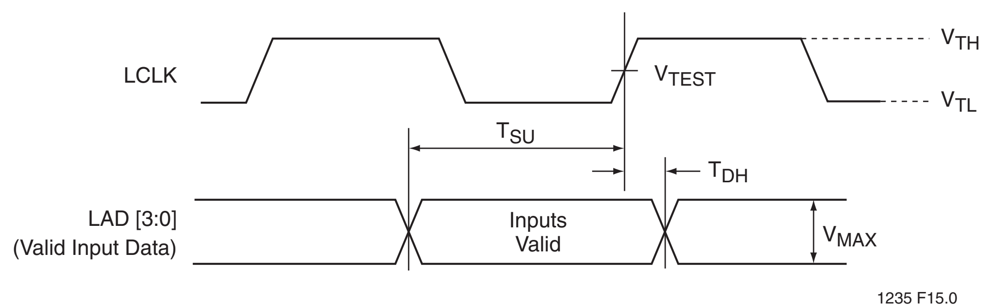


**Figure 16:** Input Timing Parameters (LPC Mode)

**Table 22:** Interface Measurement Condition Parameters (LPC Mode)

| Symbol | Value | Units |
|---|---|---|
| $V_{TH}$[1] | 0.6 $V_{DD}$ | V |
| $V_{TL}$[1] | 0.2 $V_{DD}$ | V |
| $V_{TEST}$ | 0.4 $V_{DD}$ | V |
| $V_{MAX}$[1] | 0.4 $V_{DD}$ | V |
| Input Signal Edge Rate | 1 | V/ns |

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1. The input test environment is done with 0.1 $V_{DD}$ of overdrive over $V_{IH}$ and $V_{IL}$. Timing parameters must be met with no more overdrive than this. $V_{MAX}$ specified the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters

**Table 23:** Read Cycle Timing Parameters, $V_{DD}$=3.0-3.6V (PP Mode)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{RC}$ | Read Cycle Time | 270 | | ns |
| $T_{RST}$ | RST# High to Row Address Setup | 1 | | µs |
| $T_{AS}$ | R/C# Address Set-up Time | 45 | | ns |
| $T_{AH}$ | R/C# Address Hold Time | 45 | | ns |
| $T_{AA}$ | Address Access Time | | 120 | ns |
| $T_{OE}$ | Output Enable Access Time | | 60 | ns |
| $T_{OLZ}$ | OE# Low to Active Output | 0 | | ns |
| $T_{OHZ}$ | OE# High to High-Z Output | | 35 | ns |
| $T_{OH}$ | Output Hold from Address Change | 0 | | ns |

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**Table 24:** Program/Erase Cycle Timing Parameters, $V_{DD}$=3.0-3.6V (PP Mode)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{RST}$ | RST# High to Row Address Setup | 1 | | µs |
| $T_{AS}$ | R/C# Address Setup Time | 50 | | ns |
| $T_{AH}$ | R/C# Address Hold Time | 50 | | ns |
| $T_{CWH}$ | R/C# to Write Enable High Time | 50 | | ns |
| $T_{OES}$ | OE# High Setup Time | 20 | | ns |
| $T_{OEH}$ | OE# High Hold Time | 20 | | ns |
| $T_{OEP}$ | OE# to Data# Polling Delay | | 40 | ns |
| $T_{OET}$ | OE# to Toggle Bit Delay | | 40 | ns |
| $T_{WP}$ | WE# Pulse Width | 100 | | ns |
| $T_{WPH}$ | WE# Pulse Width High | 100 | | ns |
| $T_{DS}$ | Data Setup Time | 50 | | ns |
| $T_{DH}$ | Data Hold Time | 5 | | ns |
| $T_{IDA}$ | Software ID Access and Exit Time | | 150 | ns |
| $T_{BP}$ | Byte Programming Time | | 20 | µs |
| $T_{SE}$ | Sector-Erase Time | | 25 | ms |
| $T_{BE}$ | Block-Erase Time | | 25 | ms |
| $T_{SCE}$ | Chip-Erase Time | | 100 | ms |

T24.0 25026

**Table 25:** Reset Timing Parameters, $V_{DD}$=3.0-3.6V (PP Mode)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{PRST}$ | $V_{DD}$ stable to Reset Low | 1 | | ms |
| $T_{RSTP}$ | RST# Pulse Width | 100 | | ns |
| $T_{RSTF}$ | RST# Low to Output Float | | 48 | ns |
| $T_{RST}$[1] | RST# High to Row Address Setup | 1 | | µs |
| $T_{RSTE}$ | RST# Low to reset during Sector-/Block-Erase or Program | | 10 | µs |
| $T_{RSTC}$ | RST# Low to reset during Chip-Erase | | 50 | µs |

T25.0 25026

1. There may be additional reset latency due to $T_{RSTE}$ or $T_{RSTC}$ if a reset procedure is performed during a Program or Erase operation.

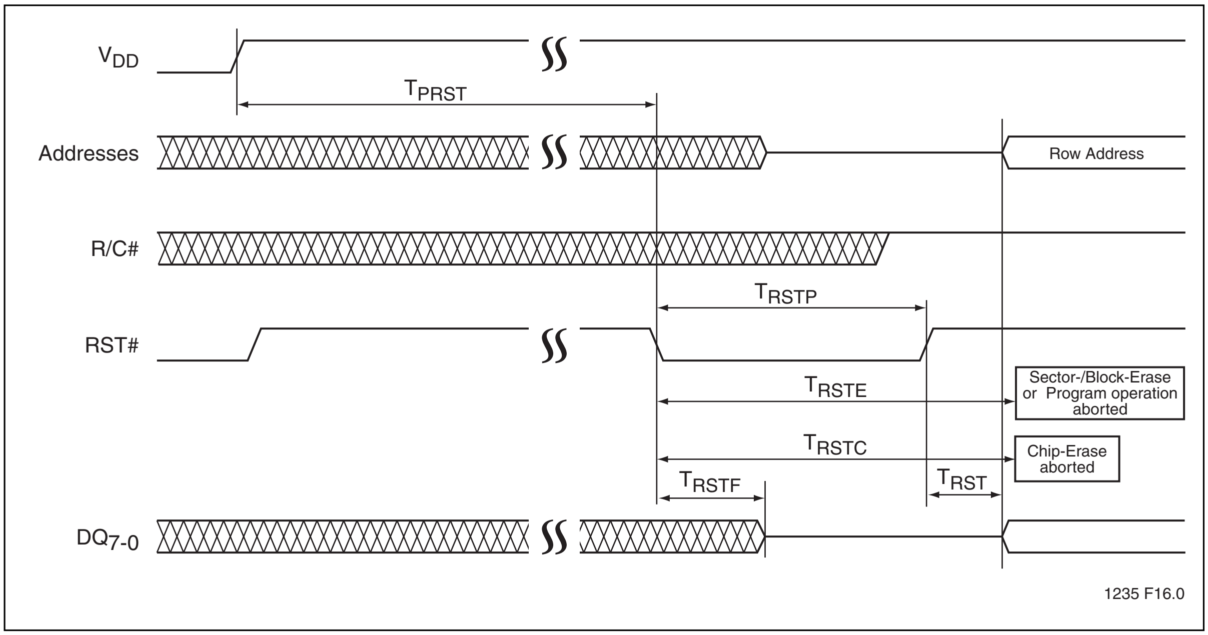



**Figure 17:** Reset Timing Diagram (PP Mode)

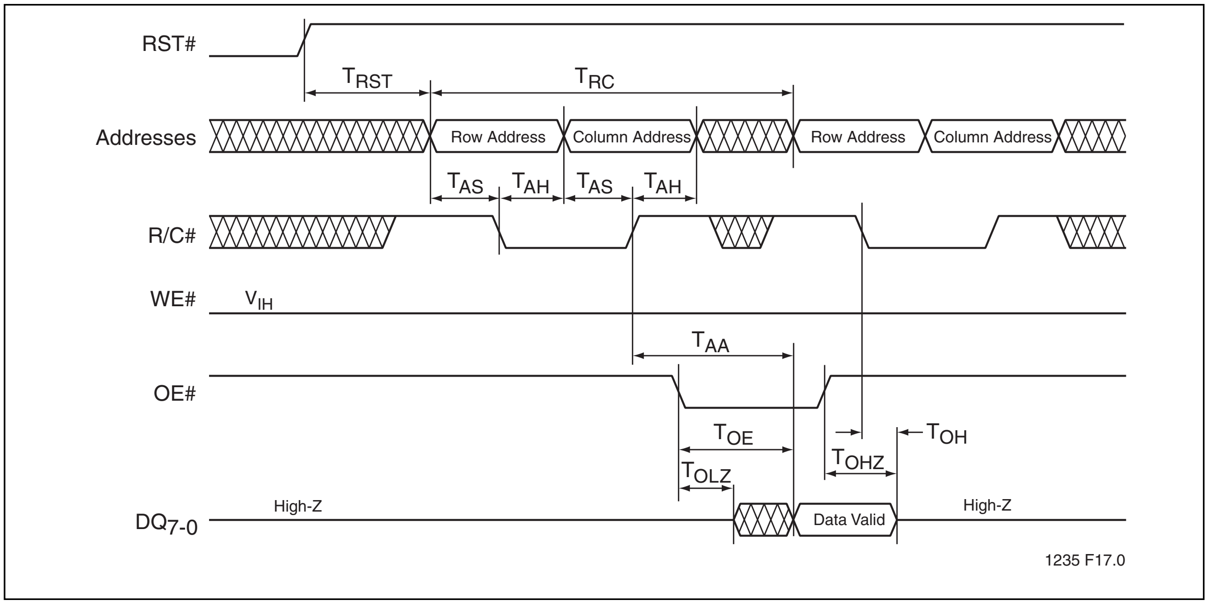



**Figure 18:** Read Cycle Timing Diagram (PP Mode)

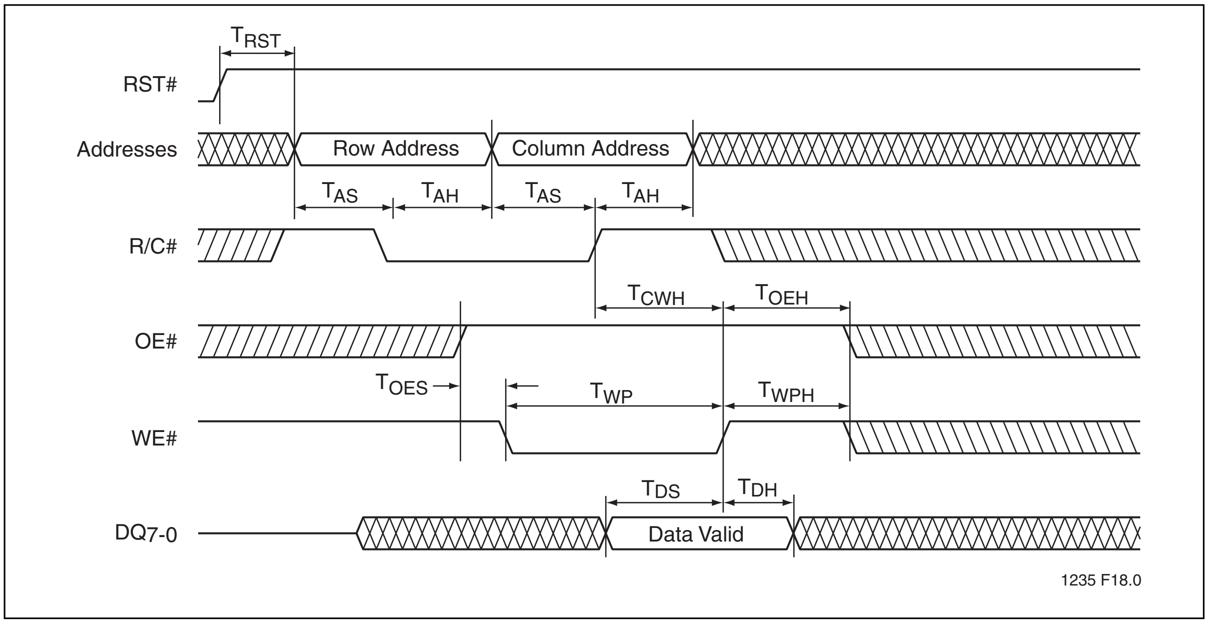



**Figure 19:** Write Cycle Timing Diagram (PP Mode)

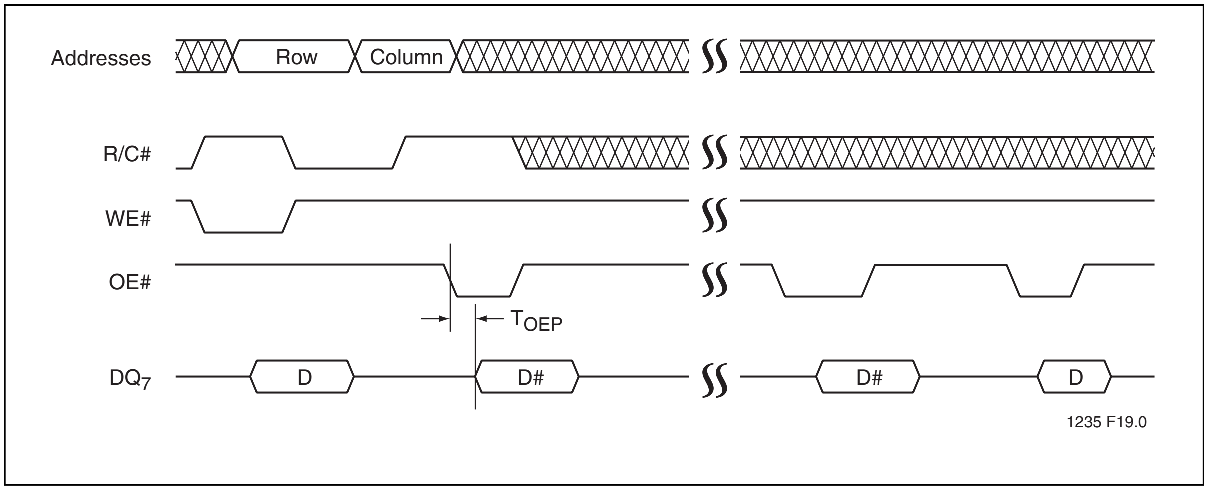



**Figure 20:** Data# Polling Timing Diagram (PP Mode)

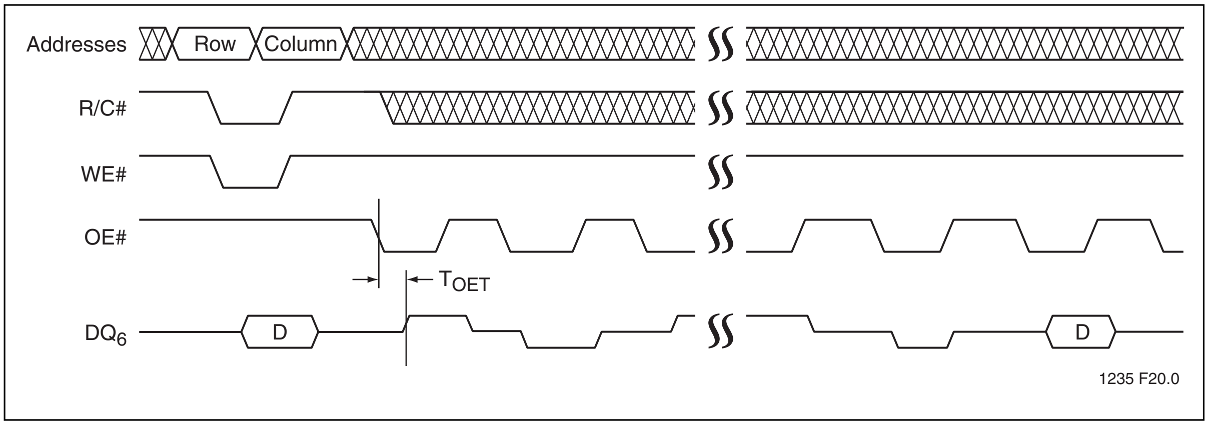



**Figure 21:** Toggle Bit Timing Diagram (PP Mode)

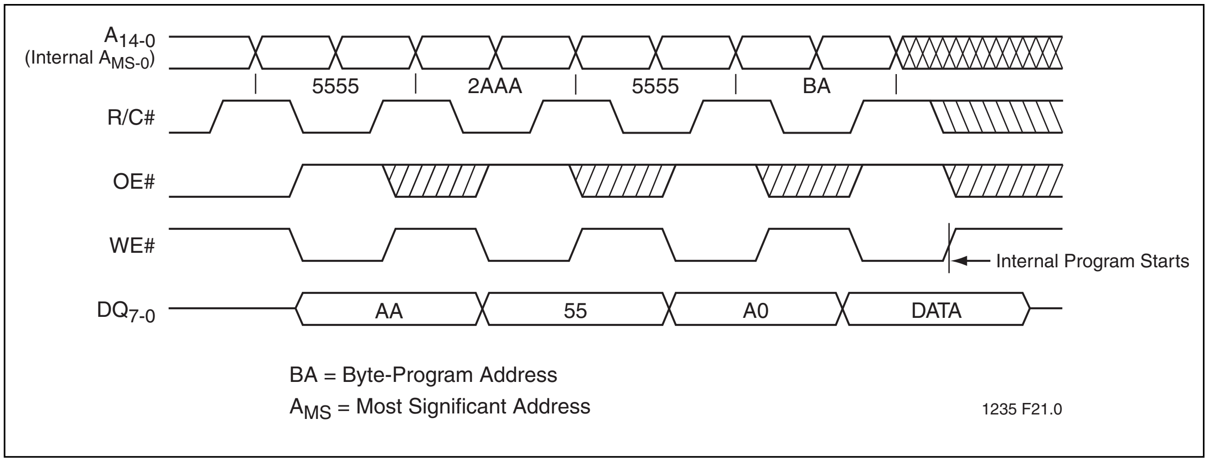



**Figure 22:** Byte-Program Timing Diagram (PP Mode)

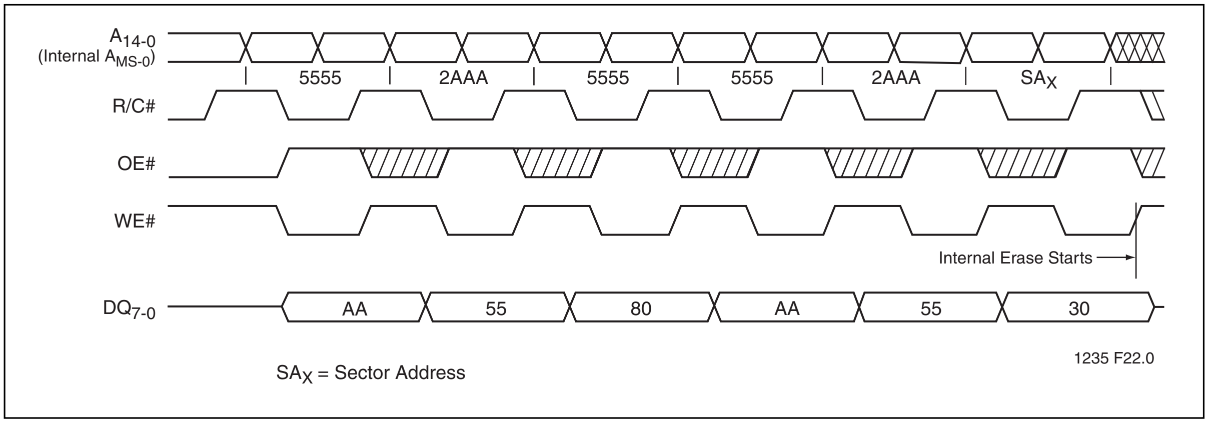



**Figure 23:** Sector-Erase Timing Diagram (PP Mode)

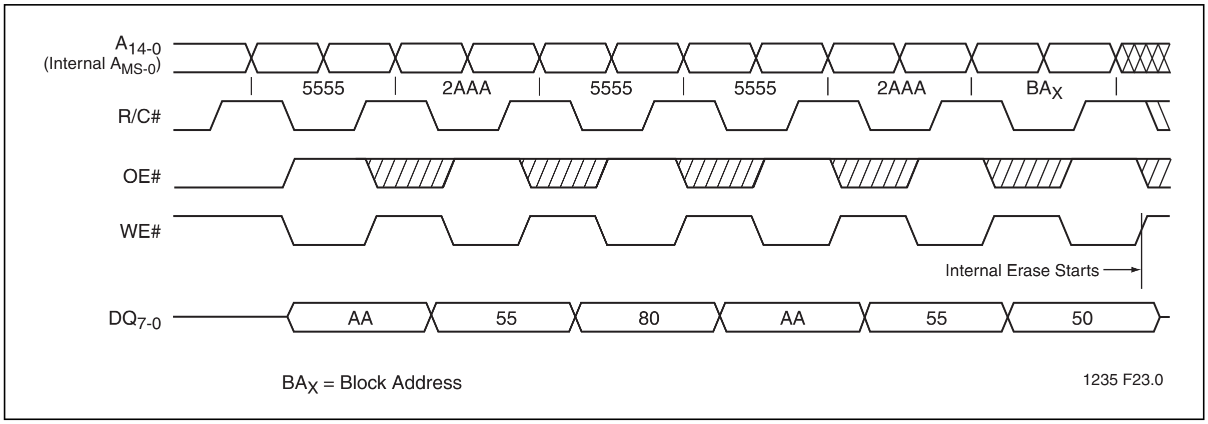



**Figure 24:** Block-Erase Timing Diagram (PP Mode)

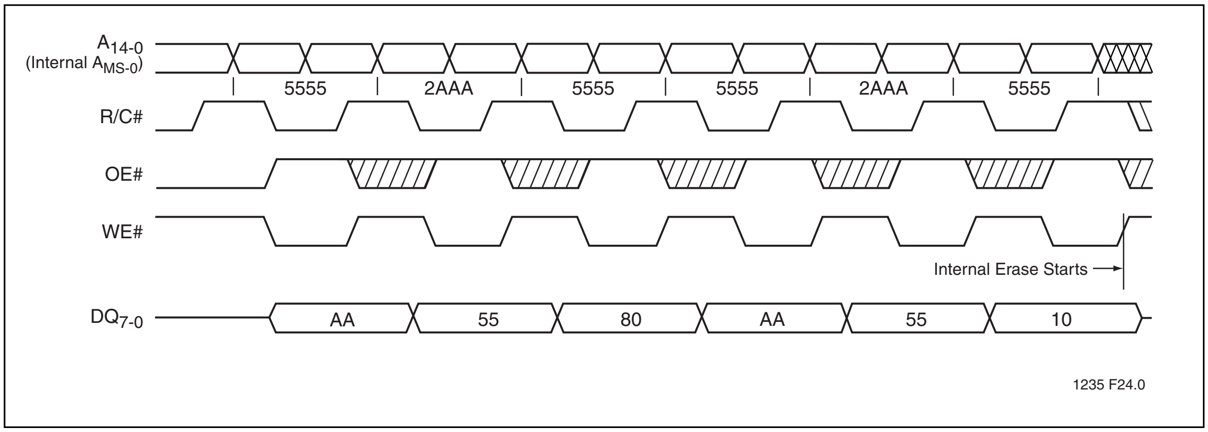



**Figure 25:** Chip-Erase Timing Diagram (PP Mode)

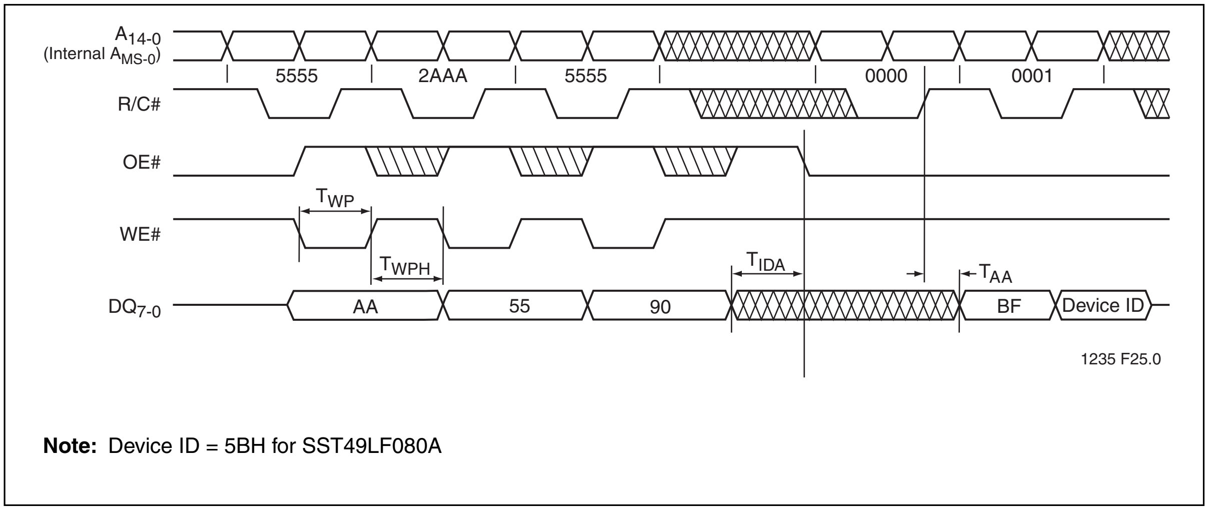



**Figure 26:** Software ID Entry and Read (PP Mode)

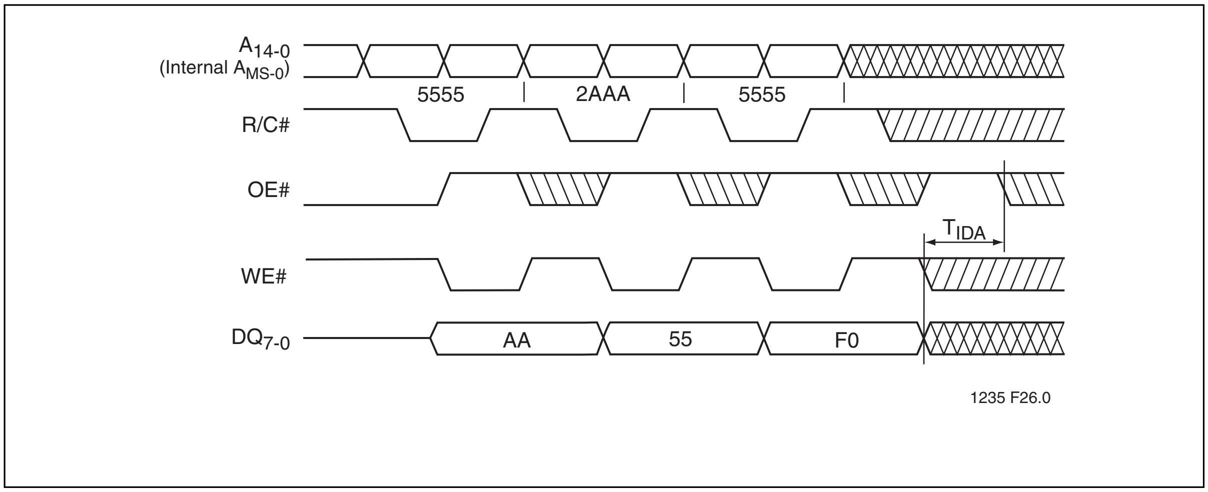
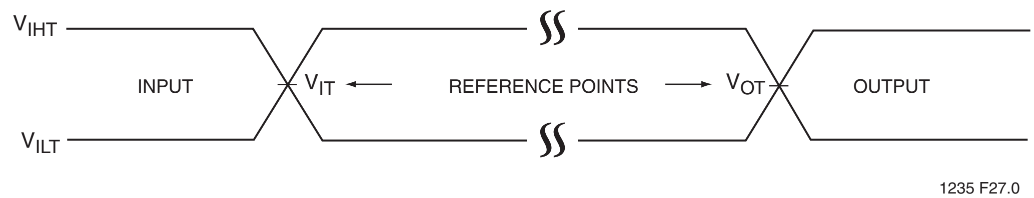



**Figure 27:** Software ID Exit (PP Mode)




AC test inputs are driven at $V_{IHT}$ (0.9 $V_{DD}$) for a logic “1” and $V_{ILT}$ (0.1 $V_{DD}$) for a logic “0”. Measurement reference points for inputs and outputs are $V_{IT}$ (0.5 $V_{DD}$) and $V_{OT}$ (0.5 $V_{DD}$). Input rise and fall times (10% ↔ 90%) are <3 ns.

**Note:** $V_{IT}$ - $V_{INPUT}$ Test
$V_{OT}$ - $V_{OUTPUT}$ Test
$V_{IHT}$ - $V_{INPUT}$ HIGH Test
$V_{ILT}$ - $V_{INPUT}$ LOW Test

**Figure 28:** AC Input/Output Reference Waveforms

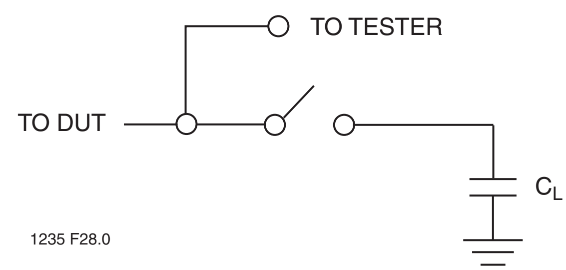



**Figure 29:** A Test Load Example

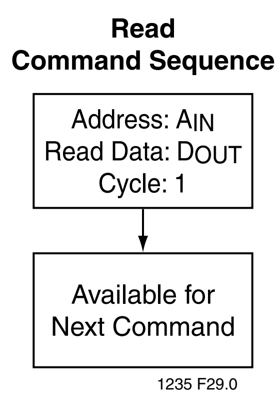



**Figure 30:** Read Flowchart (LPC Mode)

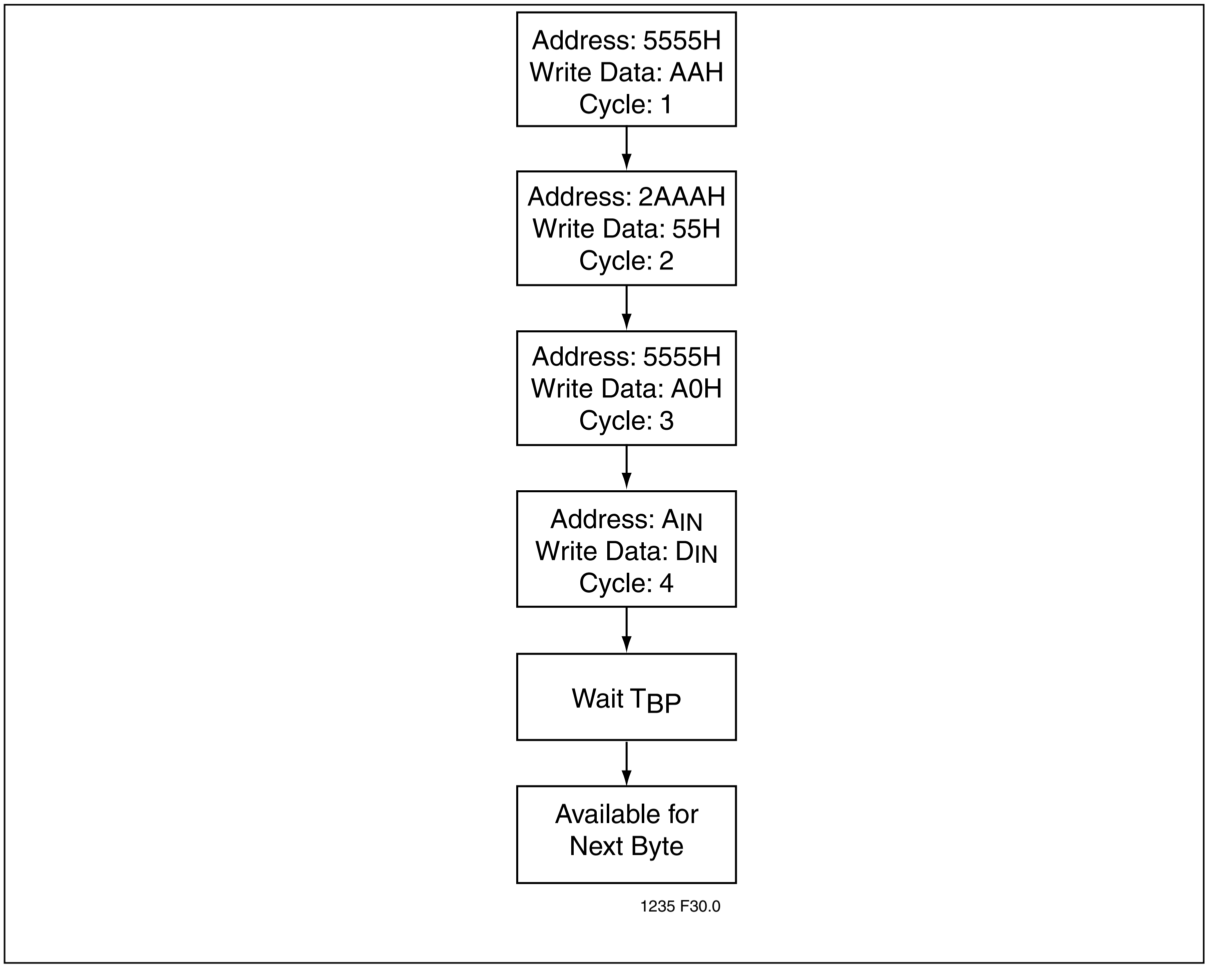



**Figure 31:** Byte-Program Flowchart (LPC Mode)

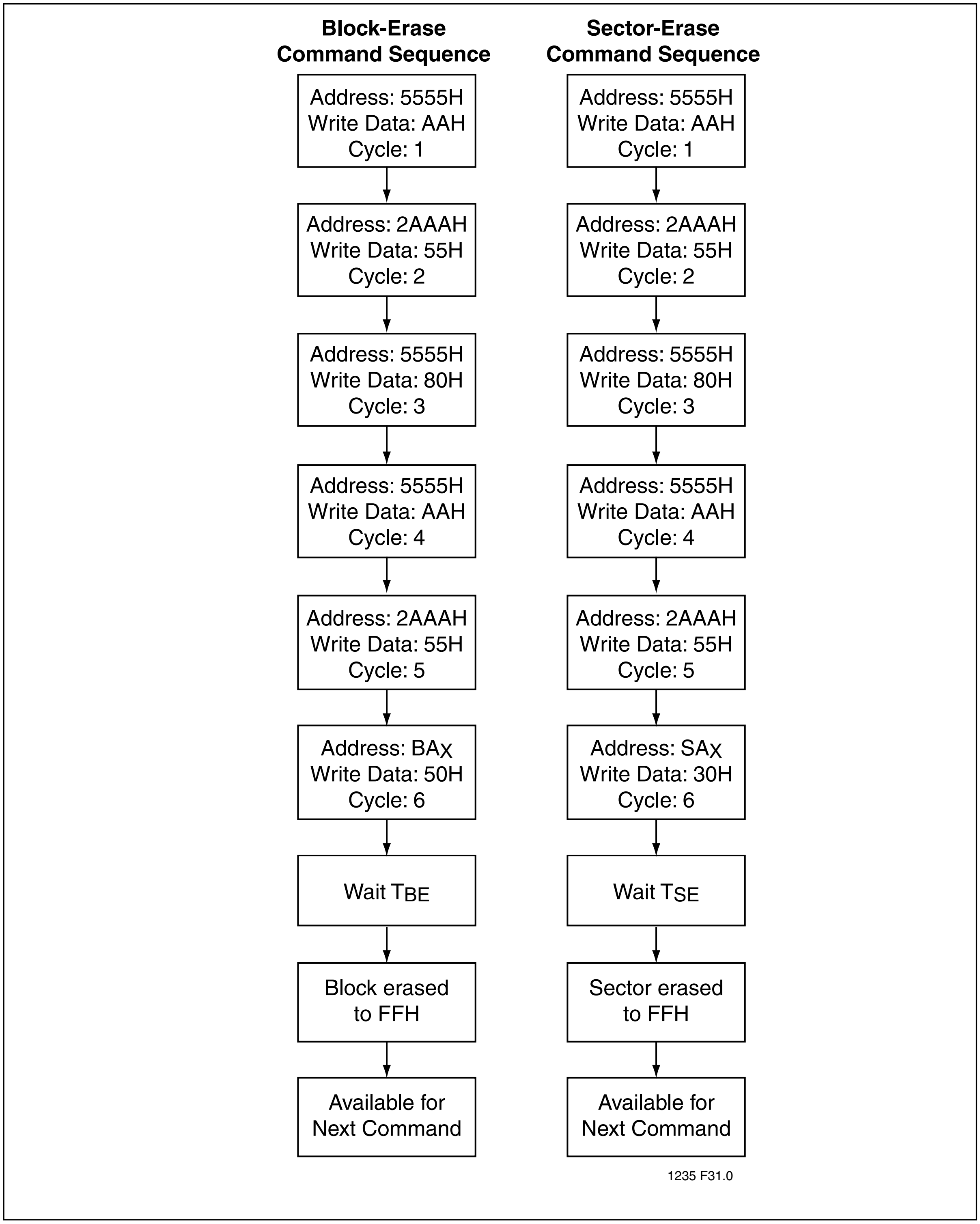



**Figure 32:** Erase Command Sequences Flowchart (LPC Mode)

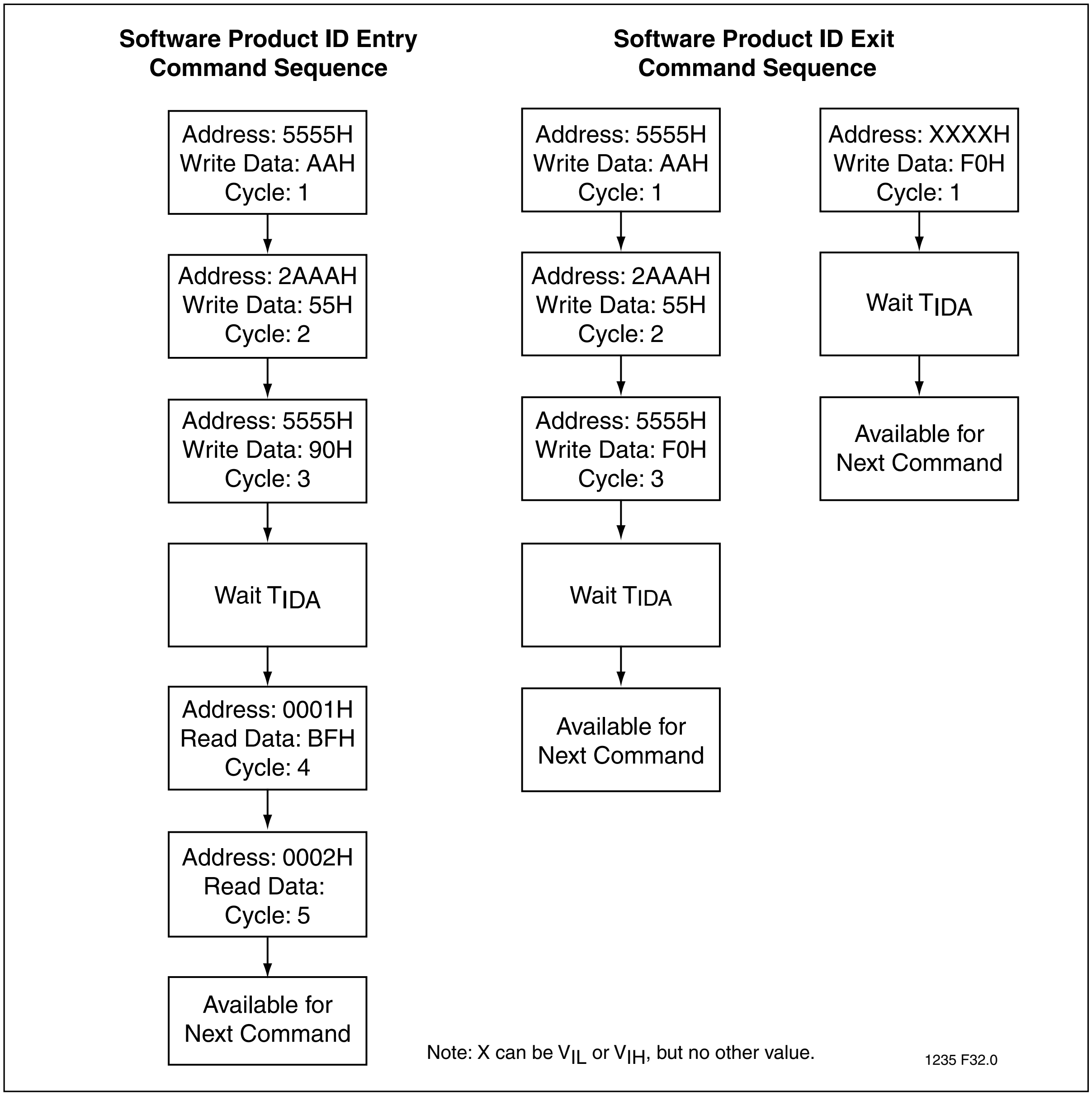



**Figure 33:** Software Product ID Command Sequences Flowchart (LPC Mode)

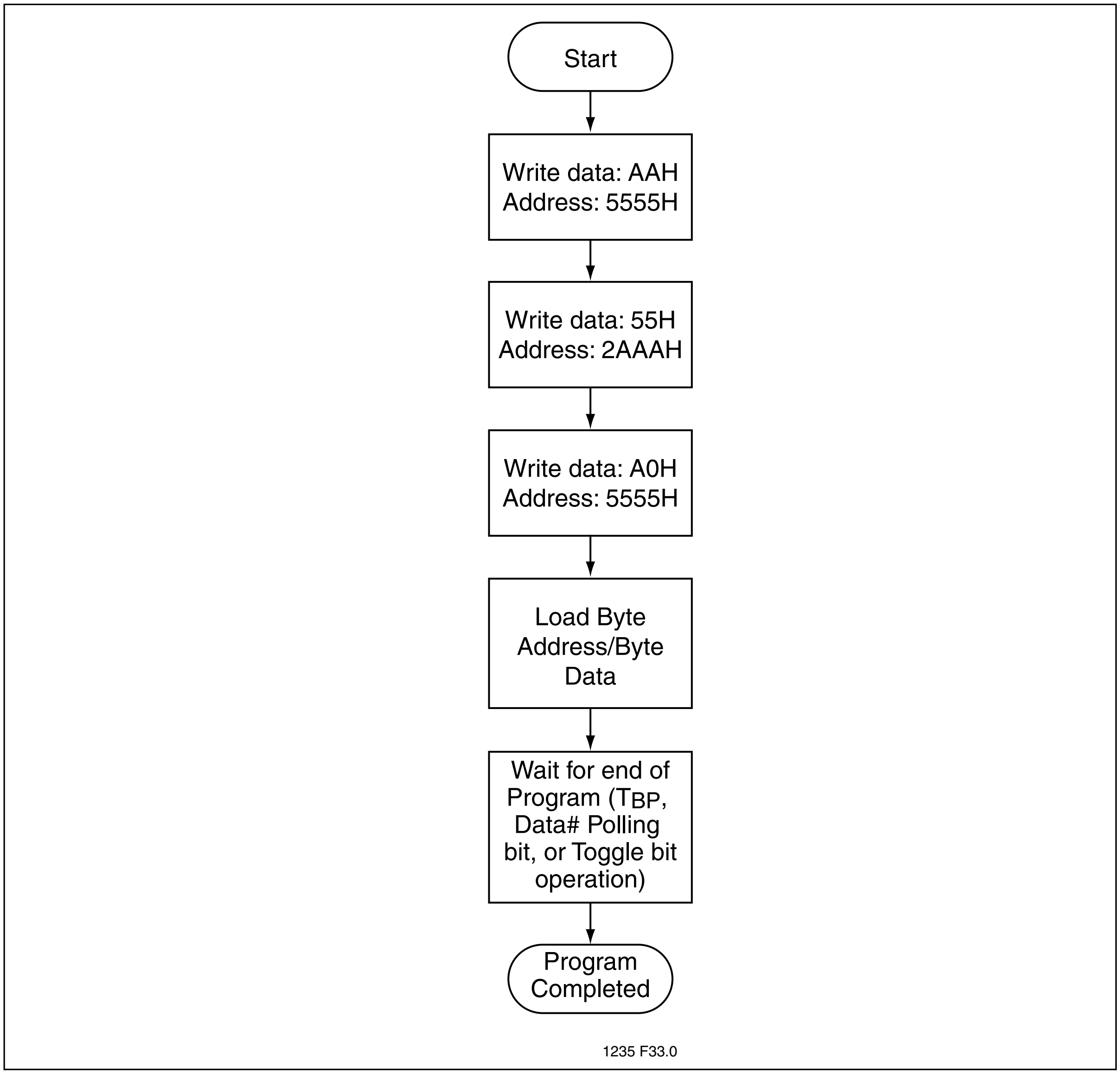



**Figure 34:** Byte-Program Command Sequences Flowchart (PP Mode)

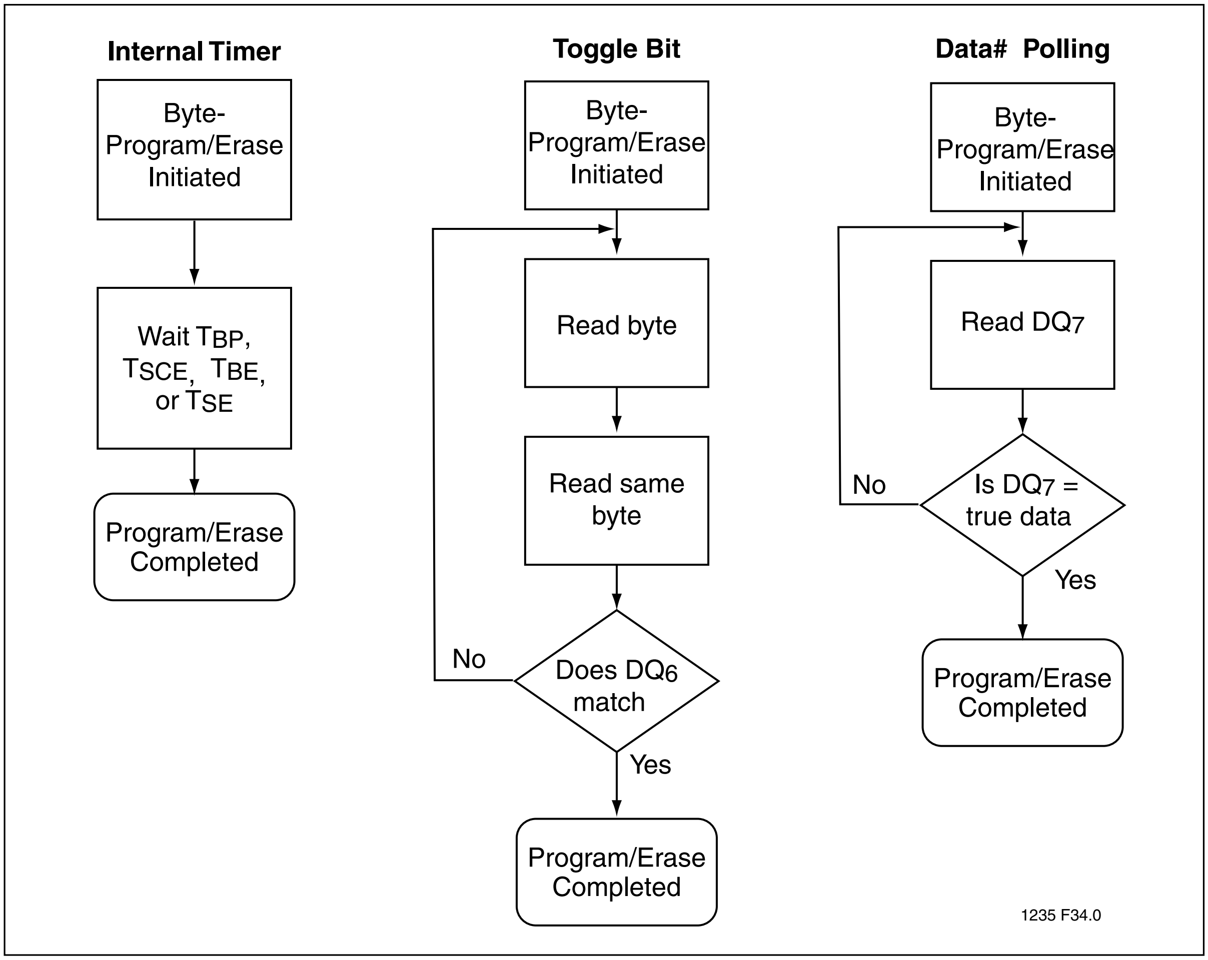



**Figure 35:** Wait Options Flowchart (PP Mode)

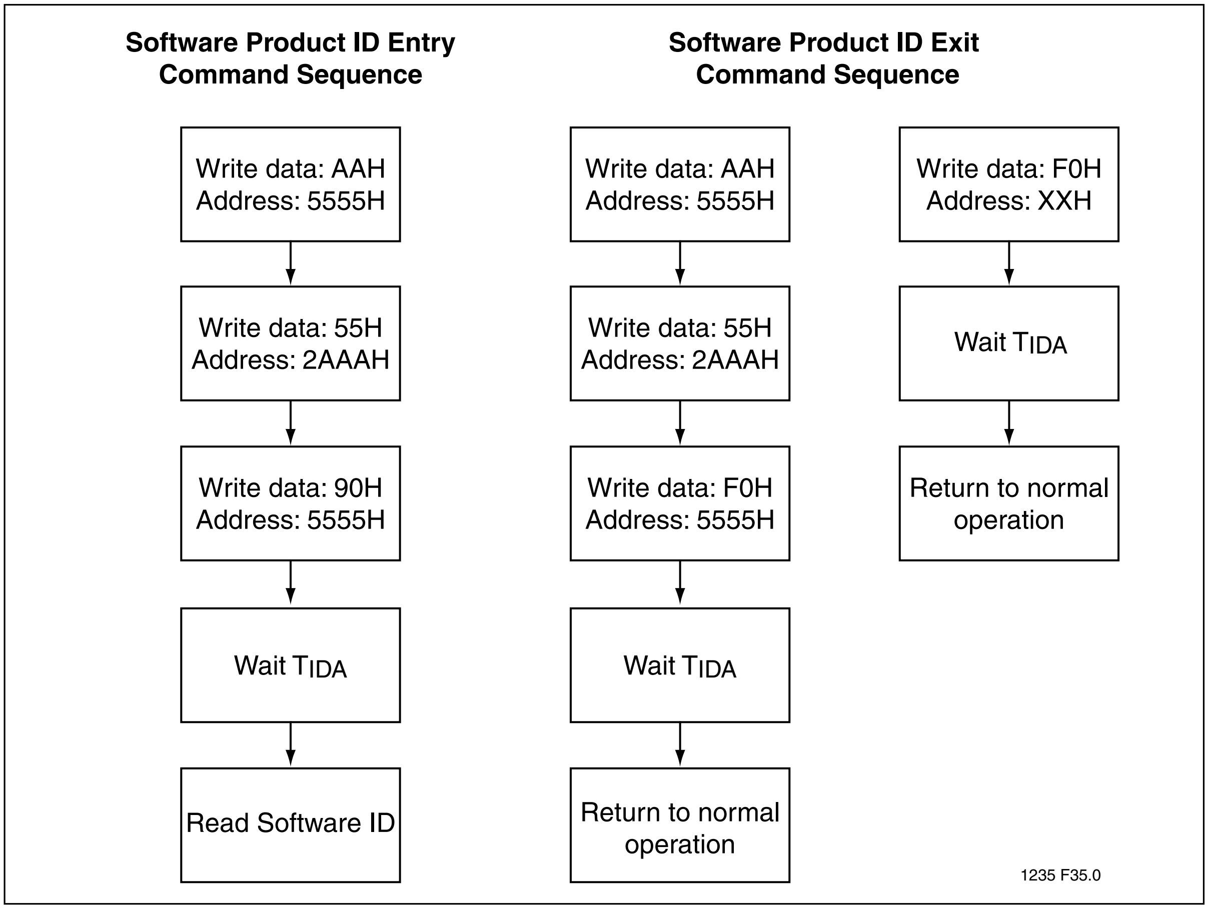



**Figure 36:** Software Product ID Command Sequences Flowchart (PP Mode)

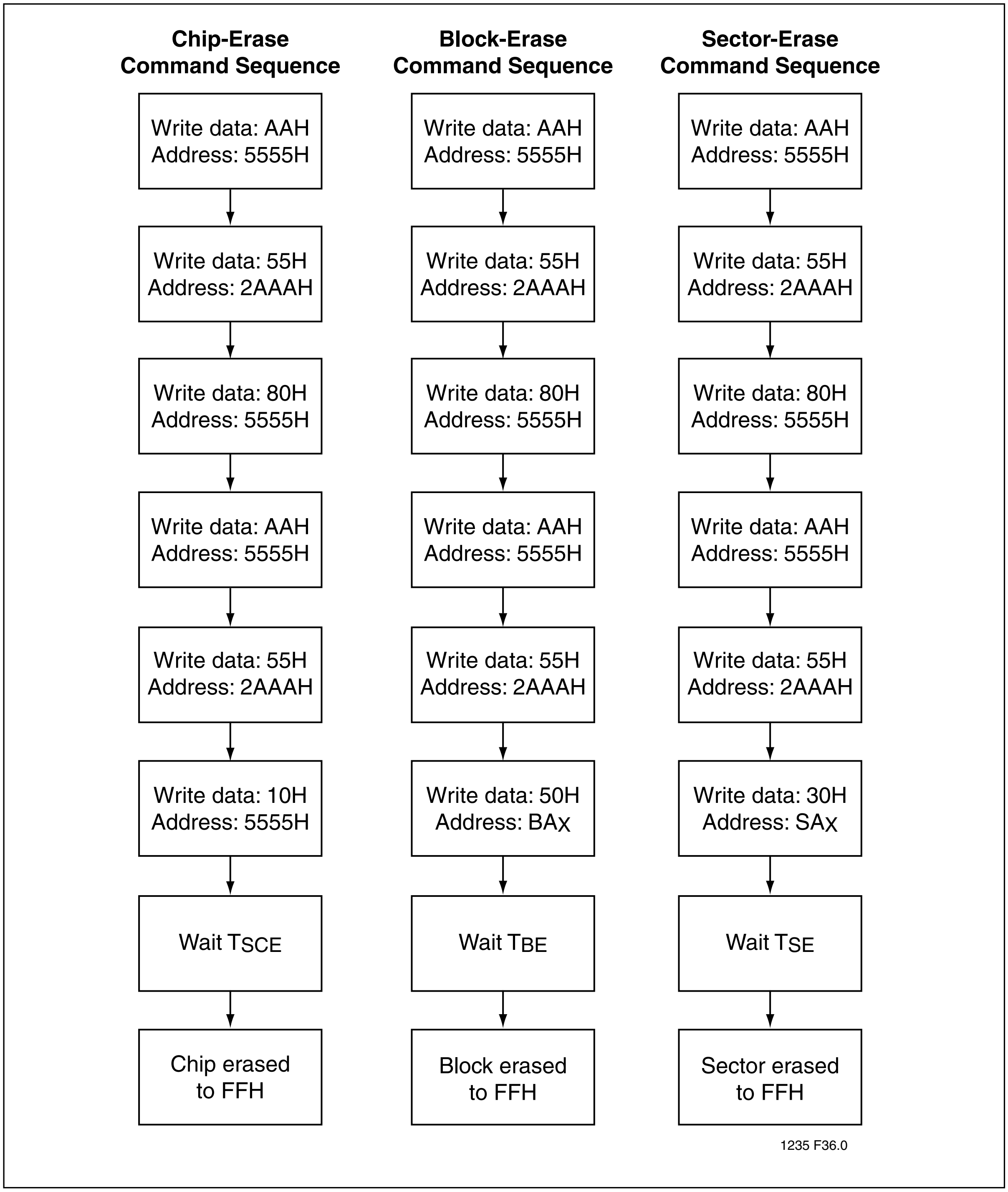



**Figure 37:** Erase Command Sequence Flowchart (PP Mode)

# Product Ordering Information

SST 49 LF 080A - 33 - 4C - NHE
XX XX XXXX - XX - XX - XXX

**Environmental Attribute**
E[1] = non-Pb

**Package Modifier**
H = 32 leads

**Package Type**
N = PLCC
W = TSOP (type 1, die up, 8mm x 14mm)

**Operating Temperature**
C = Commercial = 0°C to +85°C

**Minimum Endurance**
4 = 10,000 cycles

**Serial Access Clock Frequency**
33 = 33 MHz

**Version**

**Device Density**
080 = 8 Mbit

**Voltage Range**
L = 3.0-3.6V

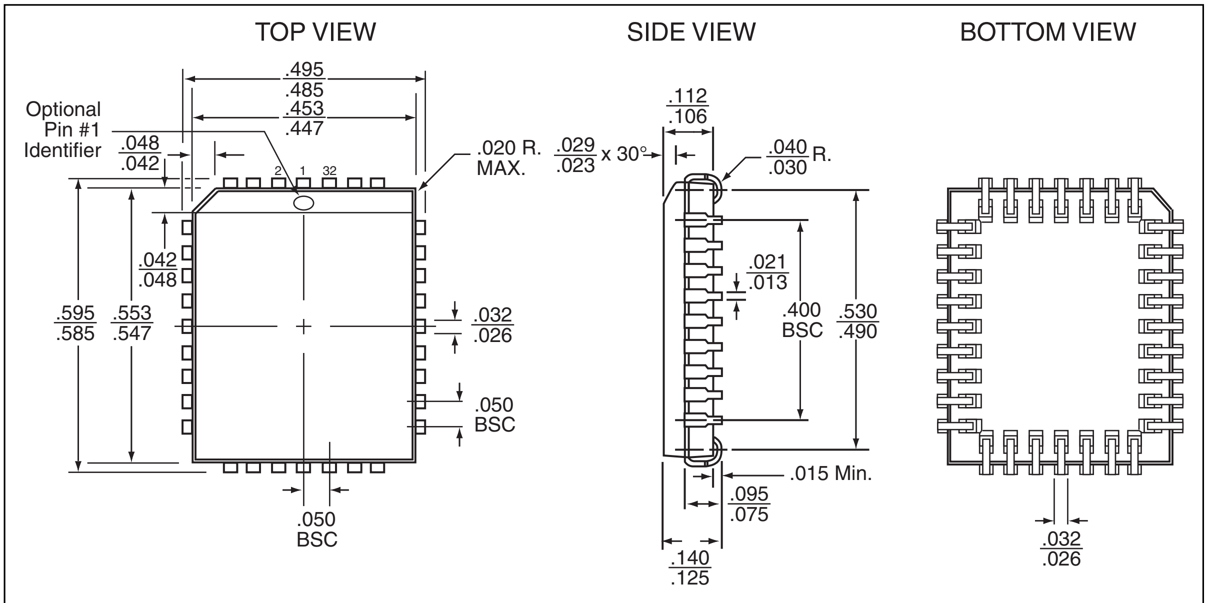
1. Environmental suffix "E" denotes non-Pb solder. SST non-Pb solder devices are "RoHS Compliant".

## Valid combinations for SST49LF080A

SST49LF080A-33-4C-WHE SST49LF080A-33-4C-NHE

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

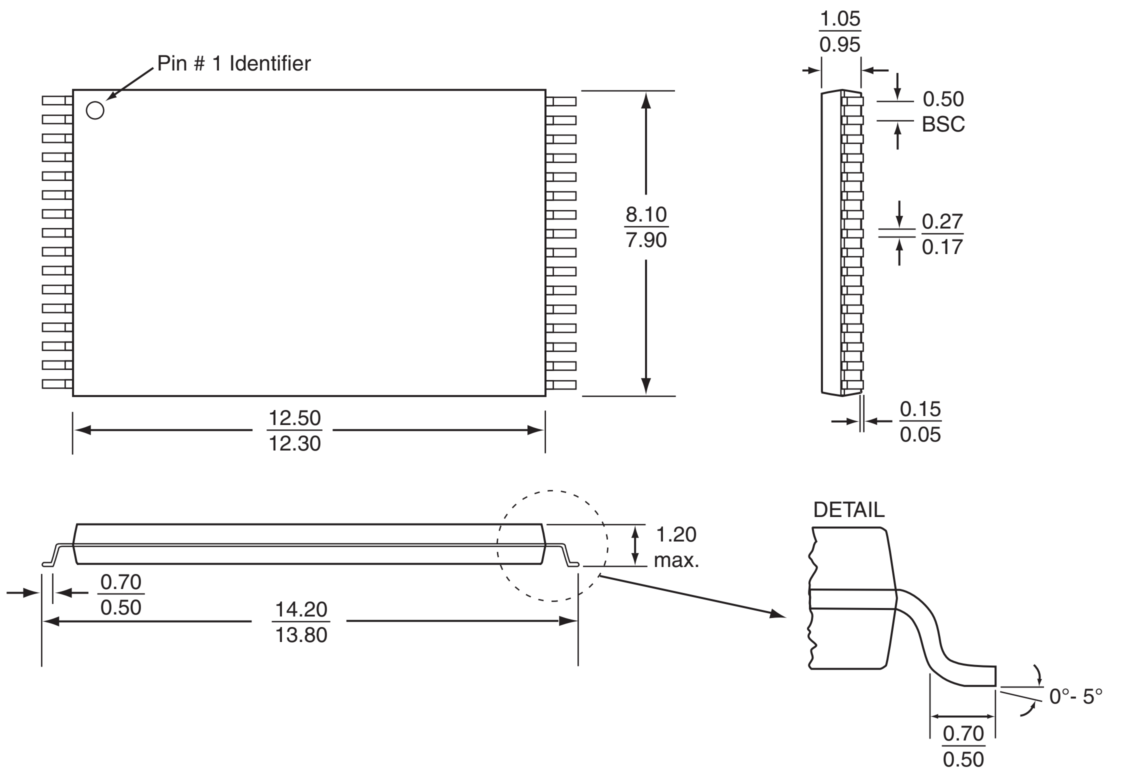
## Packaging Diagrams




Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

32-plcc-NH-3

**Figure 38:** 32-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NH




Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

**Figure 39:** 32-lead Thin Small Outline Package (TSOP) 8mm x 14mm
SST Package Code: WH

**Table 26:** Revision History

| Revision | Description | Date |
|---|---|---|
| 00 | • Initial release<br>(SST49LF080A previously released in data sheet S71206) | Apr 2003 |
| 01 | • Added statement that non-Pb devices are RoHS compliant to Features section<br>• Updated Surface Mount Solder Reflow Temperature information<br>• Added footnote to Product Ordering Information section<br>• Removed leaded part numbers | Jan 2006 |
| 02 | • Updated Table 5 on page 11 | May 2006 |
| A | • Applied new document format<br>• Released document under letter revision system<br>• Updated Spec number from S71235 to DS25086 | Nov 2011 |
| B | • Updated “LFRAME#” on page 9 | Nov 2014 |

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