ABSOLUTE MAXIMUM RATINGS

Input Voltage, V_{IN} . . . . . . 6.5 V
$\overline{SD}$ Input Voltage, $V_{\overline{SD}}$ . . . . . . −0.3 V to V_{IN}
Output Current, I_{OUT} . . . . . . Short Circuit Protected
Output Voltage, V_{OUT} . . . . . . −0.3 V to $V_{O(nom)}$ + 0.3 V
Maximum Junction Temperature, $T_{J(max)}$ . . . . . . 150°C
Storage Temperature, T_{STG} . . . . . . −65°C to 125°C
ESD (Human Body Model) . . . . . . 2 kV

Power Dissipation (Package)[a, b]
5-Pin SOT-23 . . . . . . 555 mW
Thermal Impedance (Θ_{JA})
5-Pin SOT-23 . . . . . . 180 °C/W

Notes
a. Device mounted with all leads soldered or welded to multi-layer (1S2P) JEDEC board, horizontal orientation.
b. Derate 5.5 mW/°C above T_A = 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Input Voltage, V_{IN} . . . . . . 2 V to 6 V
Output Voltage, V_{OUT} (Adjustable Version) . . . . . . 1.5 V to 5 V
$\overline{SD}$ Input Voltage, $V_{\overline{SD}}$ . . . . . . 0 V to V_{IN}

Operating Ambient Temperature, T_A . . . . . . −40°C to 85°C
Operating Junction Temperature, T_J . . . . . . −40°C to 125°C

C_{IN} = 1 μF, C_{OUT} = 2.2 μF (ceramic, X5R or X7R type) , C_{BP} = 0.1 μF (ceramic)
C_{OUT}Range = 1 μF to 10 μF (±20% tolerance, ±20% over temperature; ESR = 0.4 to 4 Ω at dc to 100 kHz, 0 t0 0.4 Ω > 100 kHz))

SPECIFICATIONS (T_A = 25°C)

Parameter	Symbol	Test Conditions Unless Otherwise Specified V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA C_{IN} = 1 μF, C_{OUT} = 2.2 μF, $V_{\overline{SD}}$ = 1.5 V	Temp[a]	Limits −40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Input Voltage Range	V_{IN}		Full	2		6	V
Output Voltage Range	V_{OUT}	Adjustable Version	Full	1.5		5	V
Output Voltage Accuracy (Fixed Versions)	V_{OUT}	1 mA ≤ I_{OUT} ≤ 150 mA	Room	−1.5		1.5	% $V_{O(nom)}$
			Full	−2.5		2.5	
Feedback Voltage (ADJ version)	V_{FB}		Room	1.188	1.215	1.240	V
			Full	1.176		1.252	
Line Regulation (Except 5-V Version)	$\frac{\Delta V_{OUT} \times 100}{V_{IN} \times V_{OUT(nom)}}$	From V_{IN} = $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V	Full	−0.18		0.18	%/V
Line Regulation (5-V Version)		From V_{IN} = 5.5 V to 6 V	Full	−0.18		0.18	
Line Regulation (ADJ Version)		V_{OUT} = 1.5 V, From V_{IN} = 2.5 V to 3.5 V	Full	−0.18		0.18	
		V_{OUT} = 5 V, From V_{IN} = 5.5 V to 6 V	Full	−0.18		0.18	
Dropout Voltage[d] (@V_{OUT} ≥ 2.5 V)	V_{IN} − V_{OUT}	I_{OUT} = 10 mA	Room		1	20	mV
		I_{OUT} = 150 mA	Room		135	170	
			Full		180	220	
Dropout Voltage[d] (@V_{OUT} < 2.5 V, V_{IN} ≥ 2 V)	V_{IN} − V_{OUT}	I_{OUT} = 150 mA	Room		235	320	
			Full			380	
Ground Pin Current	I_{GND}	I_{OUT} = 0 mA	Room		150		μA
		I_{OUT} = 150 mA	Room		500		
			Full			900	
Shutdown Supply Current	$I_{IN(off)}$	$V_{\overline{SD}}$ = 0 V	Full		0.1	1	μA
FB Pin Current	I_{FB}	V_{FB} = 1.2 V	Room		2	100	nA
Peak Output Current	$I_{O(peak)}$	V_{OUT} ≥ 0.95 x $V_{OUT(nom)}$, t_{pw} = 2 ms	Room	250	300		mA
Output Noise Voltage	e_N	BW = 50 Hz to 100 kHz, I_{OUT} = 150 mA, w/o C_{BP}	Room		300		μV (rms)
		BW = 50 Hz to 100 kHz, I_{OUT} = 150 mA, C_{BP} = 0.1 μF	Room		100		

SPECIFICATIONS (T_A = 25°C)								
Parameter	**Symbol**	**Test Conditions Unless Otherwise Specified** $V_{IN} = V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA; C_{IN} = 1 µF, C_{OUT} = 2.2 µF, $V_{\overline{SD}}$ = 1.5 V		**Temp**[a]	**Limits** −40 to 85°C **Min**[b]	**Typ**[c]	**Max**[b]	**Unit**
Ripple Rejection	$\Delta V_{OUT}/\Delta V_{IN}$	I_{OUT} = 150 mA	f = 1 kHz	Room		60		dB
			f = 10 kHz	Room		40		
			f = 100 kHz	Room		30		
Dynamic Line Regulation	$\Delta V_{O(line)}$	V_{IN} : $V_{OUT(nom)}$ + 1 V to $V_{OUT(nom)}$ + 2 V; t_R/t_F = 5 µs, I_{OUT} = 150 mA		Room		10		mV
Dynamic Load Regulation	$\Delta V_{O(load)}$	I_{OUT} : 1 mA to 150 mA, t_R/t_F = 2 µs		Room		30		
V_{OUT} Turn-On-Time	t_{ON}	V_{IN} = 4.3 V; V_{OUT} = 3.3 V	w/o C_{BP} Cap	Room		5		µs
			C_{BP} = 0.1 µF	Room		1000		
Thermal Shutdown								
Thermal Shutdown Junction Temp	$t_{J(s/d)}$			Room		165		°C
Thermal Hysteresis	t_{HYST}			Room		20		
Short Circuit Current	I_{SC}	V_{OUT} = 0 V		Room		400		mA
Shutdown Input								
$\overline{SD}$ Input Voltage	V_{IH}	High = Regulator ON (Rising)		Full	1.2		V_{IN}	V
	V_{IL}	Low = Regulator OFF (Falling)		Full			0.4	
$\overline{SD}$ Input Current[e]	I_{IL}	$V_{\overline{SD}}$ = 0 V, Regulator OFF		Room		0.01		µA
	I_{IH}	$V_{\overline{SD}}$ = 6 V, Regulator ON		Room		1.0		
Shutdown Hysteresis	V_{HYST}			Full		100		mV

Notes
a. Room = 25°C, Full = −40 to 85°C.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. Typical values for dropout voltage at $V_{OUT} \geq 2$ V are measured at V_{OUT} = 2.5 V, while typical values for dropout voltage at V_{OUT} < 2 V are measured at V_{OUT} = 1.8 V.
d. Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 2% below the output voltage measured with a 1-V differential, provided that V_{IN} does not not drop below 2.0 V.
e. The device's shutdown pin includes a typical 6-MΩ internal pull-down resistor connected to ground.
f. V_{OUT} is defined as the output voltage of the DUT at 1 mA.

TIMING WAVEFORMS

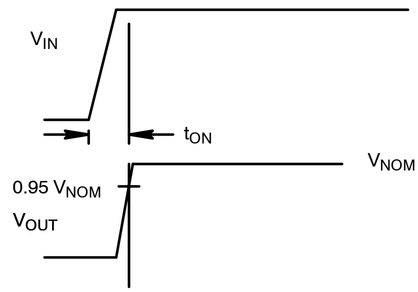
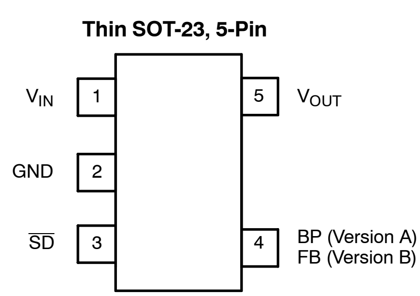


FIGURE 3. Timing Diagram for Power-Up

PIN CONFIGURATION



PIN DESCRIPTION

Pin Number	Name	Function
1	V_{IN}	Input supply pin. Bypass this pin with a 1-µF ceramic or tantalum capacitor to ground.
2	GND	Ground pin. Local ground for C_{BP} and C_{OUT}.
3	$\overline{SD}$	By applying less than 0.4 V to this pin, the device will be turned off. Connect this pin to V_{IN} if unused.
4 (Version A)	BP	Noise bypass pin. For low noise applications, a 0.1-µF or larger ceramic capacitor should be connected from this pin to ground.
4 (Version B)	FB	Connect to divided output voltage to adjust the regulation point.
5	V_{OUT}	Output voltage. Connect C_{OUT} between this pin and ground.

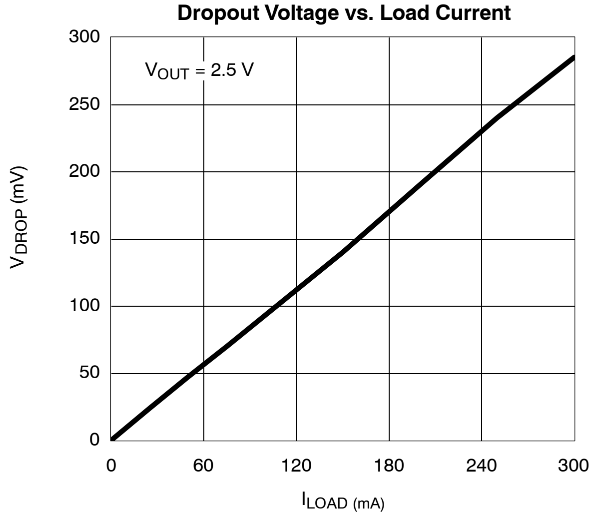
ORDERING INFORMATION					
Part Number	Lead (Pb)-Free Part Number	Marking	Voltage	Temperature Range	Package
Si9183DT-18-T1	Si9183DT-18-T1—E3	A2LL	1.8 V	−40 to 85°C	Thin SOT23-5
Si9183DT-25-T1	Si9183DT-25-T1—E3	A4LL	2.5 V		
Si9183DT-28-T1	Si9183DT-28-T1—E3	A5LL	2.8 V		
Si9183DT-285-T1	Si9183DT-285-T1—E3	B3LL	2.85 V		
Si9183DT-30-T1	Si9183DT-30-T1—E3	A6LL	3.0 V		
Si9183DT-33-T1	Si9183DT-33-T1—E3	A7LL	3.3 V		
Si9183DT-50-T1	Si9183DT-50-T1—E3	A8LL	5.0 V		
Si9183DT-AD-T1	Si9183DT-AD-T1—E3	A9LL	Adjustable		

NOTE: LL = Lot Code

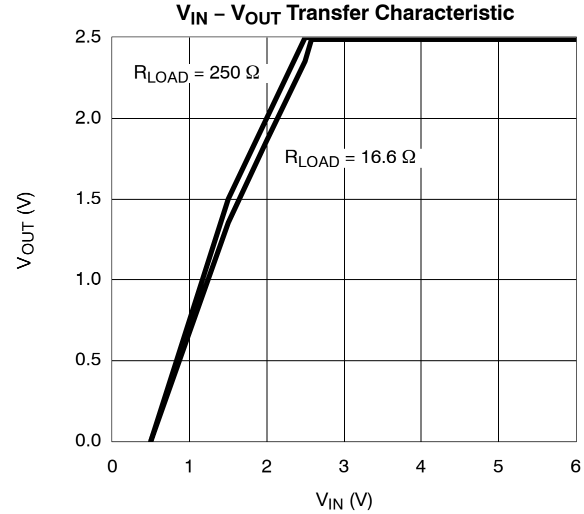
Eval Kit	Temperature Range	Board Type
Si9183DB	−40 to 85°C	Surface Mount

TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

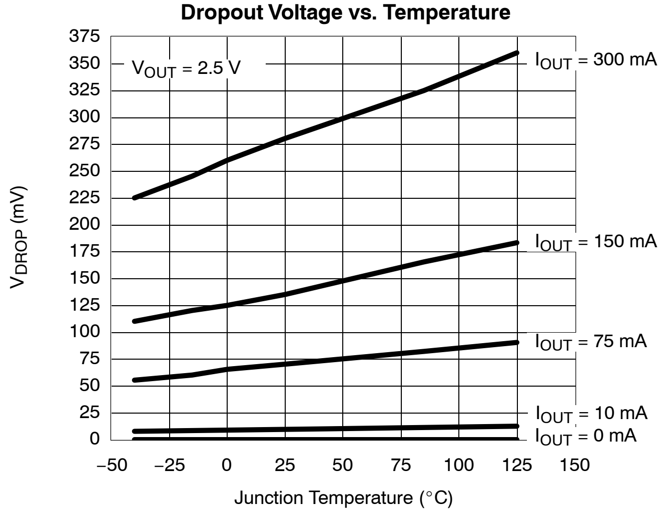
Dropout Voltage vs. Load Current



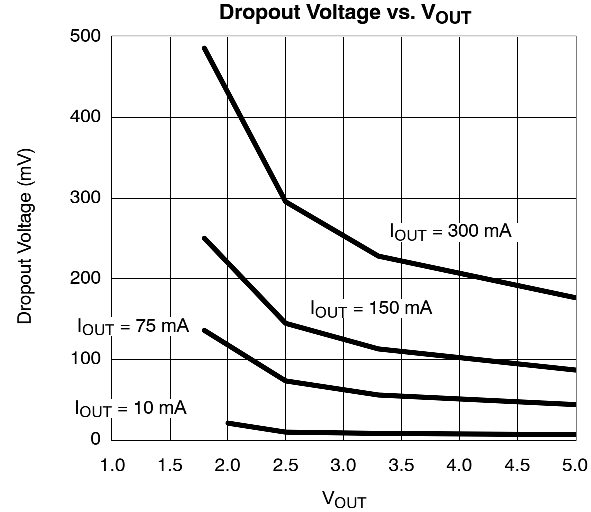
V_{IN} – V_{OUT} Transfer Characteristic



Dropout Voltage vs. Temperature

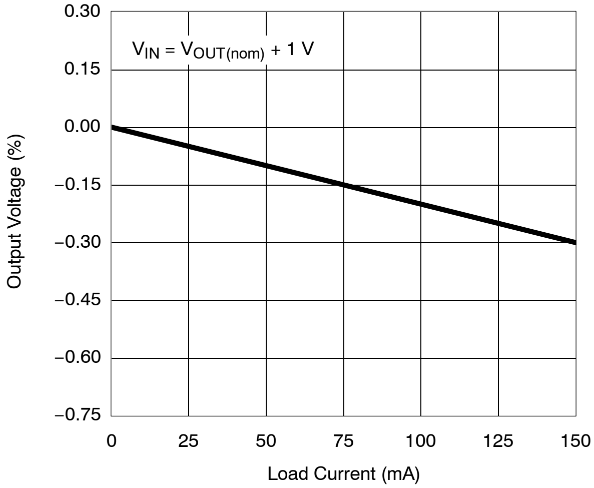


Dropout Voltage vs. V_{OUT}

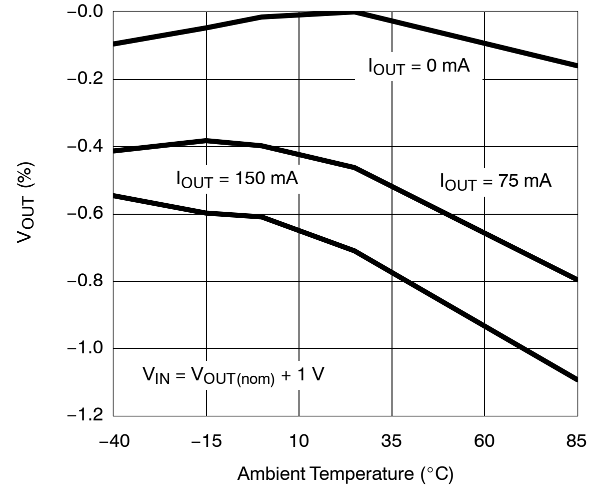


TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

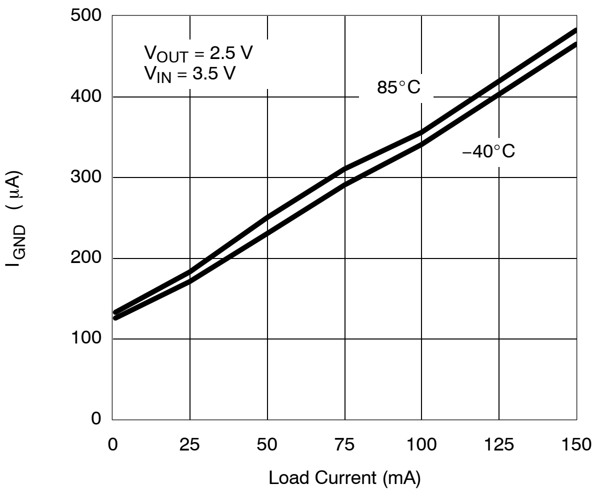
Normalized Output Voltage vs. Load Current



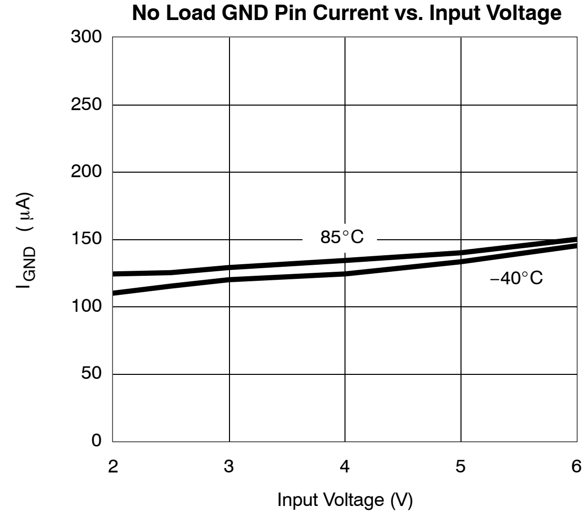
Normalized V_{OUT} vs. Temperature



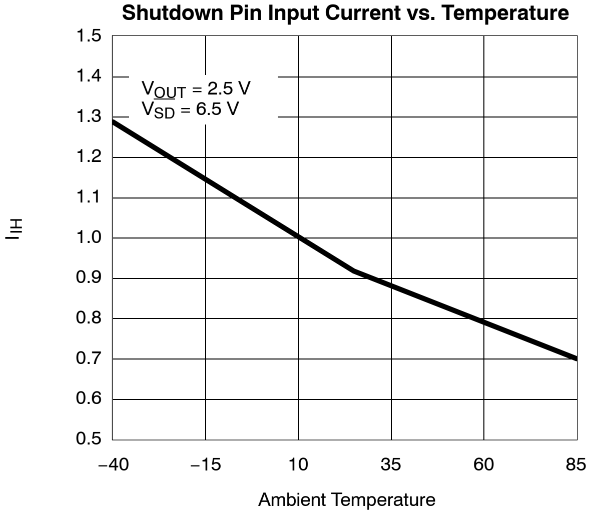
GND Current vs. Load Current



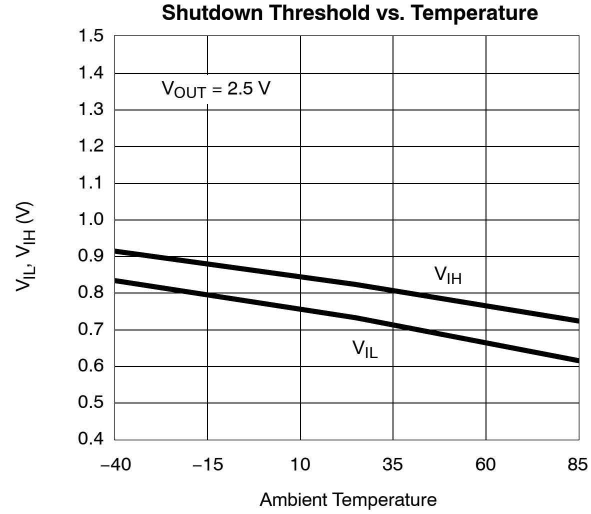
No Load GND Pin Current vs. Input Voltage



Shutdown Pin Input Current vs. Temperature

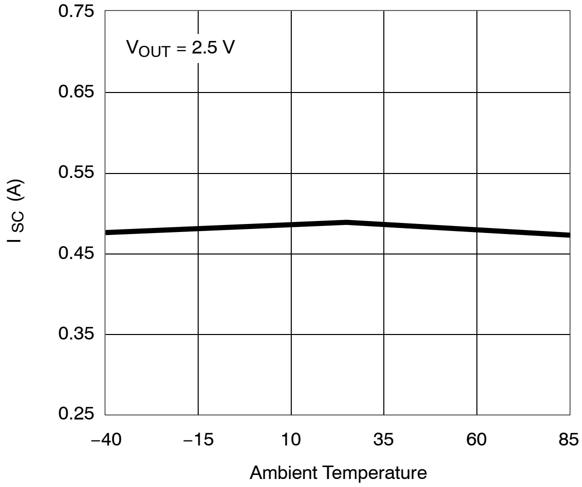


Shutdown Threshold vs. Temperature

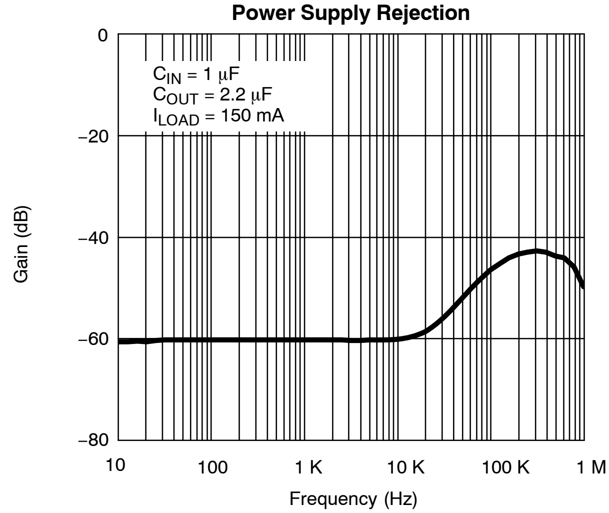


TYPICAL CHARACTERISTICS (INTERNALLY REGULATED, 25°C UNLESS NOTED)

I_{SC} vs. Temperature

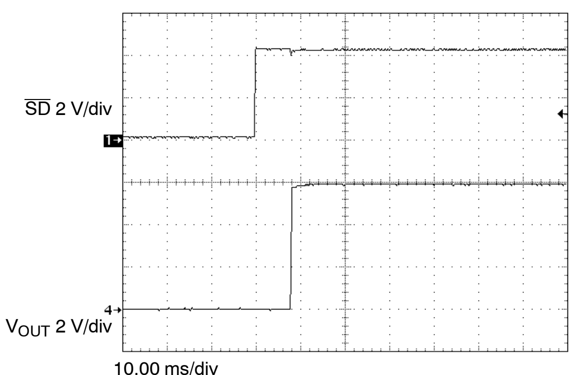


Power Supply Rejection



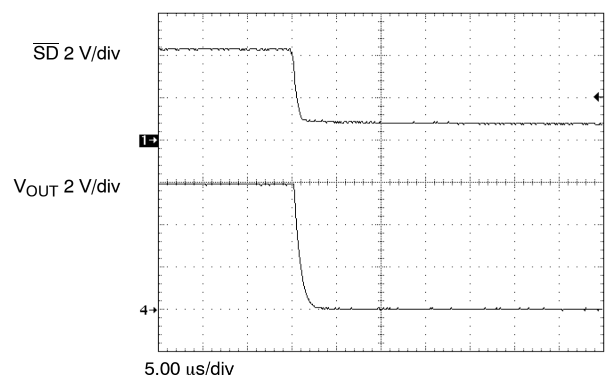
TYPICAL WAVEFORMS

Turn-On Delay



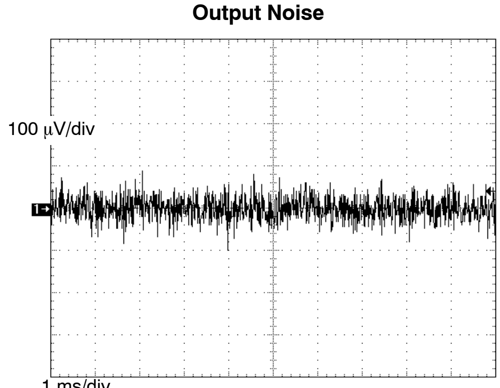
V_{IN} = 4.2 V
V_{OUT} = 3.3 V
C_{BP} = 0.1 µF
I_{LOAD} = 350 mA

Turn-Off Delay



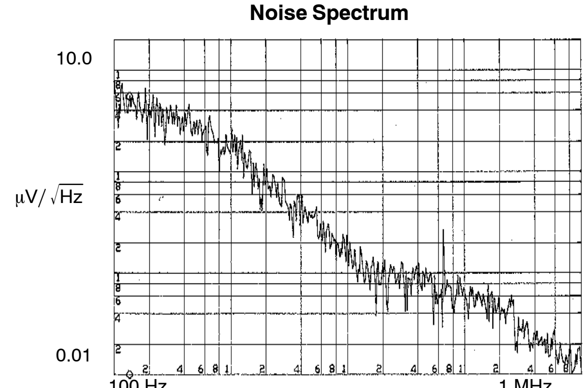
V_{IN} = 4.2 V
V_{OUT} = 3.3 V
C_{BP} = 0.1 µF
I_{LOAD} = 350 mA

Output Noise



V_{IN} = 4 V
V_{OUT} = 3 V
I_{OUT} = 150 mA
C_{IN} = 1 µF
C_{OUT} = 2.2 µF
C_{BP} = 0.1 µF
BW = 10 Hz to 1 MHz

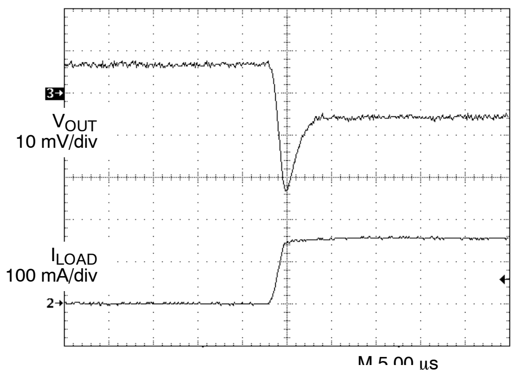
Noise Spectrum



V_{IN} = 4 V
V_{OUT} = 3
I_{OUT} = 150 mA
C_{IN} = 1 µF
C_{OUT} = 2.2 µF
C_{BP} = 0.1 µF

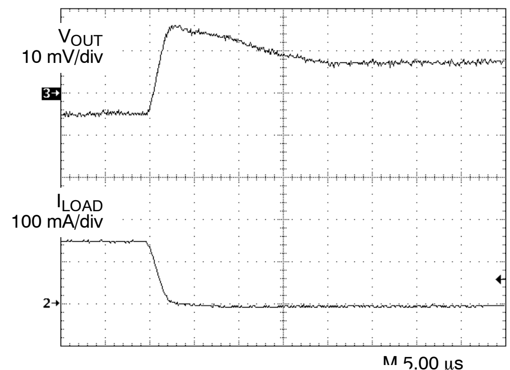
TYPICAL WAVEFORMS

Load Transient Response-1



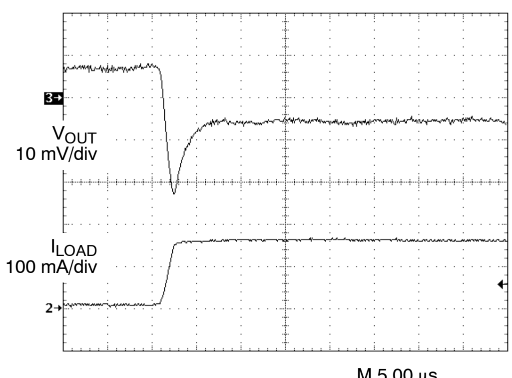
V_{OUT} = 3.0 V
C_{OUT} = 2.2 µF
I_{LOAD} = 1 to 150 mA
t_{rise} = 2 µsec

Load Transient Response-2



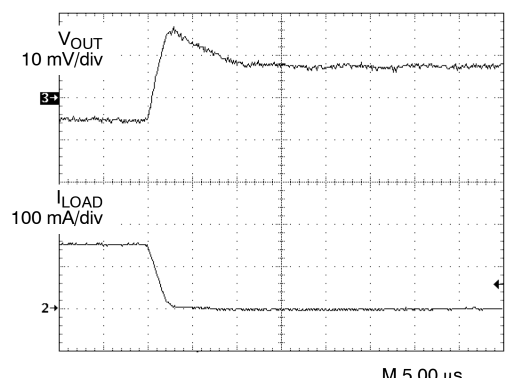
V_{OUT} = 3.0 V
C_{OUT} = 2.2 µF
I_{LOAD} = 150 to 1 mA
t_{fall} = 2 µsec

Load Transient Response-3



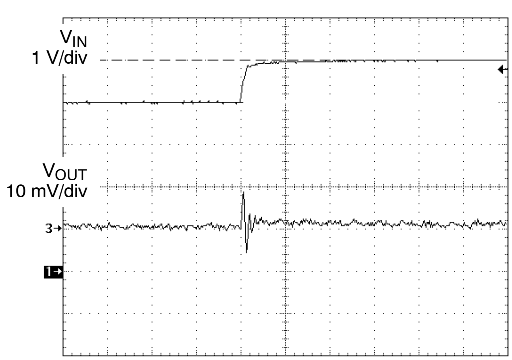
V_{OUT} = 3.0 V
C_{OUT} = 1.0 µF
I_{LOAD} = 1 to 150 mA
t_{rise} = 2 µsec

Load Transient Response-4



V_{OUT} = 3.0 V
C_{OUT} = 1.0 µF
I_{LOAD} = 150 to 1 mA
t_{fall} = 2 µsec

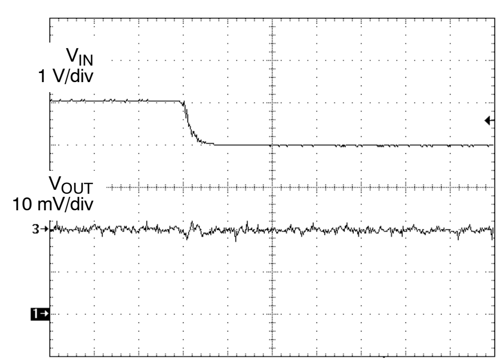
Line Transient Response-1



M 20.0 µs

V_{OUT} = 3.0 V
I_{LOAD} = 150 mA
V_{IN} = 4 to 5 V
C_{OUT} = 2.2 µF
t_{rise} = 5 µsec

Line Transient Response-2



M 20.0 µs

V_{OUT} = 3.0 V
I_{LOAD} = 150 mA
V_{IN} = 5 to 4 V
C_{OUT} = 2.2 µF
t_{fall} = 5 µsec

BLOCK DIAGRAMS

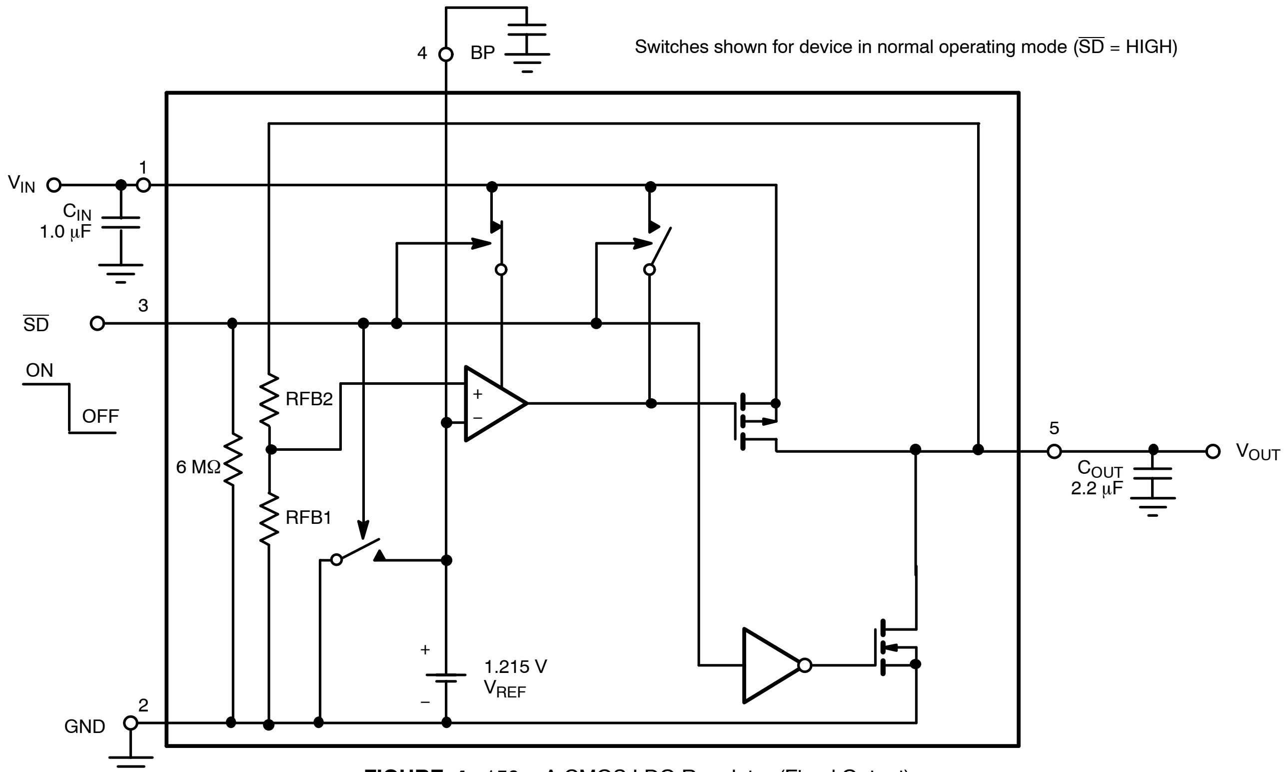


FIGURE 4. 150-mA CMOS LDO Regulator (Fixed Output)

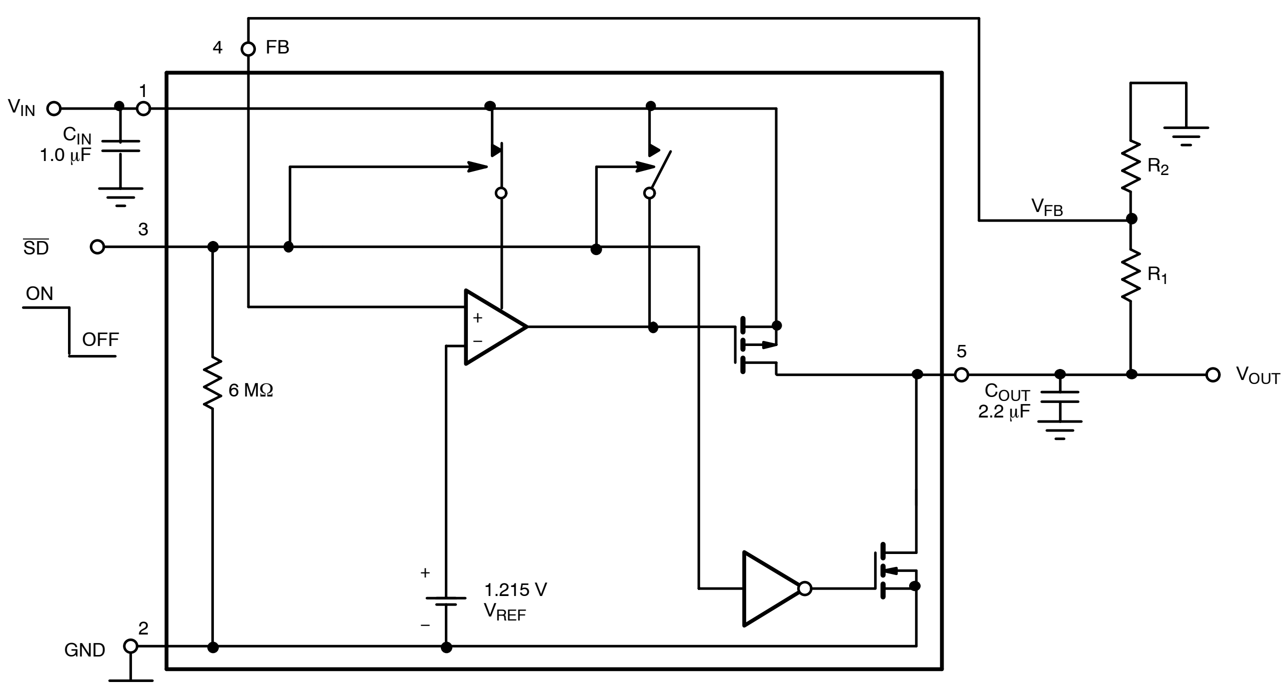


FIGURE 5. 150-mA CMOS LDO Regulator (Adjustable Output)

DETAILED DESCRIPTION

The Si9183 is a low drop out, low quiescent current, linear regulator family with very fast transient response. It is primarily designed for battery powered applications where battery run time is at a premium. The low quiescent current allows extended standby time while low drop out voltage enables the system to fully utilize battery power before recharge. The Si9183 is a very fast regulator with bandwidth exceeding 50 kHz while maintaining low quiescent current at light load conditions. With this bandwidth, the Si9183 is one of the fastest LDO available today. The Si9183 is stable with one of any output capacitor types from 1 μF to 10.0 μF. However, X5R or X7R ceramic capacitors are recommended for best output noise and transient performance.

V_{IN}

V_{IN} is the input supply pin. The bypass capacitor for this pin is not critical as long as the input supply has low enough source impedance. For practical circuits, a 1.0-μF or larger ceramic capacitor is recommended. When the source impedance is not low enough and/or the source is several inches from the Si9183, then a larger input bypass capacitor is needed. It is required that the equivalent impedance (source impedance, wire, and trace impedance in parallel with input bypass capacitor impedance) must be smaller than the input impedance of the Si9183 for stable operation. When the source impedance, wire, and trace impedance are unknown, it is recommended that an input bypass capacitor be used of a value that is equal to or greater than the output capacitor.

V_{OUT}

V_{OUT} is the output voltage of the regulator. Connect a bypass capacitor from V_{OUT} to ground. The output capacitor can be any value from 1.0 μF to 10.0 μF. A ceramic capacitor with X5R or X7R dielectric type is recommended for best output noise, line transient, and load transient performance.

GND

Ground is the common ground connection for V_{IN} and V_{OUT}. It is also the local ground connection for C_{BP}, ADJ, and $\overline{SD}$.

ADJ

For the adjustable output version, use a resistor divider R1 and R2, connect R1 from V_{OUT} to ADJ and R2 from ADJ to ground. R2 should be in the 25-kΩ to 150-kΩ range for low power consumption, while maintaining adequate noise immunity.

The formula below calculates the value of R1, given the desired output voltage and the R2 value,

$$R1 = \frac{(V_{OUT} - V_{ADJ})R2}{V_{ADJ}} \tag{1}$$

V_{ADJ} is nominally 1.215 V.

SHUTDOWN ($\overline{SD}$)

$\overline{SD}$ controls the turning on and off of the Si9183. V_{OUT} is guaranteed to be on when the $\overline{SD}$ pin voltage equals or is greater than 1.2 V. V_{OUT} is guaranteed to be off when the $\overline{SD}$ pin voltage equals or is less than 0.4 V. During shutdown mode, the Si9183 will draw less than 1-μA current from the source. To automatically turn on V_{OUT} whenever the input is applied, tie the $\overline{SD}$ pin to V_{IN}.

C_{BP}

For low noise application, connect a high frequency ceramic capacitor from C_{BP} to ground. A 0.01-μF or a 0.1-μF X5R or X7R is recommended.

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