TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Absolute Maximum Ratings and Thermal Information[1]

Parameter	Symbol	Test Condition	Value	Unit
Operating Temperature Range	T_A		–40 to 85	°C
Storage Temperature Range	T_{STG}		–55 to 150	°C
Thermal Resistance, Typical[2] TQFP-64	θ_{JA}		25	°C/W
Continuous Power Dissipation[3] TQFP-64	P_D	$T_A = 85\ °C$	1.6	W
Thermal Resistance, Typical[2] QFN-40	θ_{JA}		32	°C/W
Continuous Power Dissipation[4] QFN-40	P_D	$T_A = 85\ °C$	1.7	W
Si3226/7				
Supply Voltage	$V_{DD1} – V_{DD4}$		–0.5 to 4.0	V
Digital Input Voltage	V_{IND}		–0.3 to 3.6	V
Si3208				
Supply Voltage	V_{DD}		–0.5 to 4.0	V
Battery Supply Voltage[5]	V_{BAT}	Continuous	+0.4 to –110	V
		Pulse < 10 µs	+0.4 to –118	V
TIP, RING Current	I_{TIP}, I_{RING}		±100	mA
Si3209				
Supply Voltage	V_{DD}		–0.5 to 4.0	V
High Battery Supply Voltage[5]	V_{BAT}	Continuous	+0.4 to –135	V
		Pulse < 10 µs	+0.4 to –143	V
TIP, RING Current	I_{TIP}, I_{RING}		±100	mA

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet.
2. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane.
3. Operation of the Si3226 or Si3227 above 125 °C junction temperature may degrade device reliability.
4. Si3208 and Si3209 are equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold should normally be set to 145 °C; when in the ringing state the thermal shutdown may be set to 200 °C. For optimal reliability long term operation of the Si3208/Si3209 above 150 °C junction temperature should be avoided.
5. The dv/dt of the voltage applied to the VBAT pins must be limited to 10 V/µs.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
Ambient Temperature	T_A	G-grade	–40	25	85	°C
Supply Voltage, Si3226/7	V_{DD1}–V_{DD4}		3.13	3.3	3.47	V
Supply Voltage, Si3208/Si3209	V_{DD}		3.13	3.3	3.47	V
Battery Voltage, Si3208	V_{BAT}		–9	—	–110	V
Battery Voltage, Si3209	V_{BAT}		–9	—	–135	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.

Table 3. 3.3 V Power Supply Characteristics[1]

(V_{DD} = 3.3 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Impedance, Reset	I_{DD}	V_T and V_R = Hi-Z $\overline{RST} = 0$	—	2.4	—	mA
	I_{VBAT}		—	0	—	mA
High Impedance, Open Current	I_{DD}	V_T and V_R = Hi-Z	—	9.7	—	mA
	I_{VBAT}		—	0.6	—	mA
Forward/Reverse Sleep, On-hook Current	I_{DD}	V_{TR} = –48 V	—	15	—	mA
	I_{VBAT}		—	1.2	—	mA
Forward/Reverse Active, On-hook Current	I_{DD}	V_{TR} = –48 V	—	24	—	mA
	I_{VBAT}		—	1.2	—	mA
Forward/Reverse Active, Off-hook Current	I_{DD}	I_{LOOP} = 30 mA R_{LOAD} = 50 Ω	—	43	—	mA
	I_{VBAT}		—	3.1 + I_{LOOP}	—	mA
Forward/Reverse OHT, On-hook Current	I_{DD}	V_{TR} = –48 V	—	43	—	mA
	I_{VBAT}		—	1.6	—	mA
Tip/Ring Open, On-hook Current	I_{DD}	V_T or V_R = –48 V V_R or V_T = Hi-Z	—	23	—	mA
	I_{VBAT}		—	0.6	—	mA
Ringing Current	I_{DD}	V_{TR} = 55 V_{RMS} + 0 V_{DC} balanced, sinusoidal, f = 20 Hz R_{LOAD} = 5 REN = 1400 Ω	—	26	—	mA
	I_{VBAT}		—	2.3 + I_{AVE}	—	mA

Notes:

1. All specifications are for a single channel of Si3226/7 using Si3208/9 linefeed IC and based on measurements with all channels in the same operating state.
2. I_{LOOP} is the dc current in the subscriber loop during the off-hook state.
3. I_{AVE} is the average of the full-wave rectified current in the subscriber loop during ringing ($I_{AVE} = I_{PEAK} \times 2/\pi$).

Table 4. AC Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Level		2.5	—	—	V_{PK}
Overload Compression	2-Wire – PCM	Figure 6	—	—	
Single Frequency Distortion[1]	2-Wire – PCM or PCM – 2-Wire: 200 Hz to 3.4 kHz	—	—	–65	dB
	PCM – 2-Wire – PCM: 200 Hz – 3.4 kHz, 16-bit Linear mode	—	—	–65	dB
Signal-to-(Noise + Distortion) Ratio[2]	200 Hz to 3.4 kHz D/A or A/D 8-bit Active off-hook, and OHT, any Z_T	Figure 5	—	—	
Audio Tone Generator Signal-to-Distortion Ratio[2]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	–41	dB
Gain Accuracy[2]	2-Wire to PCM or PCM to 2-Wire 1014 Hz, Any gain setting $V_{DD1} – V_{DD4}$ = 3.3 V ± 5%	–0.2	—	0.2	dB
Attenuation Distortion vs. Freq.	0 dBm 0	See AN317			
Group Delay vs. Frequency					
Gain Tracking[3]	1014 Hz sine wave, reference level –10 dBm Signal level:	—	—	—	—
	3 dB to –37 dB	—	—	0.25	dB
	–37 dB to –50 dB	—	—	0.5	dB
	–50 dB to –60 dB	—	—	1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
Crosstalk between channels	0 dBm0,				
TX or RX to TX	300 Hz to 3.4 kHz	—	—	–75	dB
TX or RX to RX	300 Hz to 3.4 kHz	—	—	–75	dB
2-Wire Return Loss[4]	200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance[4]	300 Hz to 3.4 kHz	26	30	—	dB
Noise Performance					
Idle Channel Noise[5]	C-Message weighted	—	8	12	dBrnC
	Psophometric weighted	—	–80	–78	dBmP
PSRR from V_{DD1}–V_{DD4}	RX and TX, dc to 3.4 kHz	40	—	—	dB

Notes:

1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DD1}–V_{DD4} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.

Table 4. AC Characteristics (Continued)

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Test Condition	Min	Typ	Max	Unit
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 Hz to 1 kHz	58	60	—	dB
	1 kHz to 3.4 kHz	53	58	—	dB
Metallic/PCM to Longitudinal Balance	200 Hz to 3.4 kHz	40	—	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current per Pin	Active off-hook 200 Hz to 3.4 kHz	—	—	30	mA
DC Current	Differential	—	—	45	mA
	Common Mode	—	—	30	mA
	Differential + Common Mode	—	—	45	mA

Notes:

1. The input signal level should be 0 dBm0 for frequencies greater than 100 Hz. For 100 Hz and below, the level should be –10 dBm0. The output signal magnitude at any other frequency is smaller than the maximum value specified.
2. Analog signal measured as $V_{TIP} – V_{RING}$. Assumes ideal line impedance matching.
3. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to –37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
4. V_{DD1}–V_{DD4} = 3.3 V, V_{BAT} = –52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
5. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed –55 dBm.

Table 5. Linefeed Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum Loop Resistance	R_{LOOP}	$R_{DC,MAX}$ = 430 Ω I_{LOOP} = 18 mA, V_{BAT} = –52V	—	—	2000	Ω
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	—	640	Ω
DC On-Hook Voltage Accuracy—Ground Start	V_{OHTO}	$I_{RING}<I_{LIM}$; V_{RING} wrt ground, V_{RING} = –51 V	—	—	4	V
DC Output Resistance—Ground Start	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	160	—	640	Ω
DC Output Resistance—Ground Start	R_{TOTO}	TIP to ground	400	—	—	kΩ
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ring Trip Threshold Accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80mA	—	—	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	—	—	1	mA
		DC Detection, 48 V DC offset, R_{loop} = 1500 Ω	—	—	3	mA
Ringing Amplitude	V_{RING}	Open circuit, V_{BAT} = –110 V	108	—	—	V_{PK}
		5 REN load, R_{LOOP} = 0 Ω, V_{BAT} = –110 V, R_{DO} = 160 Ω	99	—	—	V_{PK}
		Open Circuit, V_{BAT} = –135 V	133	—	—	V_{PK}
		5 REN load, R_{LOOP} = 0 Ω, V_{BAT} = –130 V, R_{DO} = 160 Ω	121	—	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}		—	2	—	%
Ringing Frequency Accuracy		f = 16 Hz to 100 Hz	—	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	50	ms
Calibration Time		↑CAL to ↓CAL bit	—	—	TBD	ms
Loop Voltage Sense Accuracy		Accuracy of boundaries for each output Code; $V_{TIP} – V_{RING}$ = 48 V	—	2	4	%

***Note:** Ringing amplitude is set for 93 V peak and measured at TIP-RING using no series protection resistance.

Table 5. Linefeed Characteristics (Continued)

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Loop Current Sense Accuracy		Accuracy of boundaries for each output code; I_{LOOP} = 18 mA	—	7	10	%
Power Alarm Threshold Accuracy		Power Threshold = 300 mW	—	—	25	%
***Note:** Ringing amplitude is set for 93 V peak and measured at TIP-RING using no series protection resistance.						

Table 6. Monitor ADC Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Nonlinearity (8-bit resolution)	DNLE		—	—	1	LSB
Integral Nonlinearity (8-bit resolution)	INLE		—	—	1	LSB
Gain Error			—	—	5	%

Table 7. Si3208/Si3209 Characteristics

(V_{DD} = 3.13 to 3.47 V, V_{BAT} = –15 to –130 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TIP/RING Pull-down Transistor Saturation Voltage	V_{CM}	$V_{RING} – V_{BAT}$ (Forward) $V_{TIP} – V_{BAT}$ (Reverse) $V_{AC} = 2.5\ V_{PK}$ I_{OUT} = 22 mA I_{OUT} = 60 mA	— —	3 —	— 3.5	V V
TIP/RING Pull-up Transistor Saturation Voltage	V_{OV}	GND – V_{TIP} (Forward) GND – V_{RING} (Reverse) $V_{AC} = 2.5\ V_{PK}$ I_{OUT} = 22 mA I_{OUT} = 60 mA	— —	3 —	— 3.5	V V
OPEN State TIP/RING Leakage Current	I_{LKG}	$R_L = 0\Omega$	—	—	150	µA

Table 8. DC Characteristics

(V_{DD} = 3.13 to 3.47 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		0.7 x V_{DD}	—	5.25	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{DD}	V
High Level Output Voltage	V_{OH}	I_O = 4 mA	V_{DD} – 0.6	—	—	V
Low Level Output Voltage	V_{OL}	DTX, SDO, $\overline{\text{INT}}$, SDITHRU: I_O = –4 mA	—	—	0.4	V
		GPIO1 a/b, GPIO2 a/b: I_O = –40 mA	—	—	0.72	
SDITHRU internal pullup resistance			35	50	—	kΩ
Relay Driver Source Impedance	R_{OUT}	V_{DD1}–V_{DD4} = 3.13 V IO < 28 mA	—	63	—	Ω
Relay Driver Sink Impedance	R_{IN}	V_{DD1}–V_{DD4} = 3.13 V IO < 85 mA	—	11	—	Ω
Input Leakage Current	I_L		—	—	10	µA

Table 9. Switching Characteristics—General Inputs[1]

(V_{DD} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Rise Time, $\overline{\text{RESET}}$	t_r	—	—	5	ns
$\overline{\text{RESET}}$ Pulse Width, GCI Mode[2,3]	t_{rl}	33/PCLK	—	—	µs
$\overline{\text{RESET}}$ Pulse Width, SPI Daisy Chain Mode[3]	t_{rl}	33/PCLK	—	—	µs

Notes:

1. All timing (except Rise and Fall time) is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DD} – 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
2. The minimum $\overline{\text{RESET}}$ pulse width assumes the SDITHRU pin is tied to ground via a pulldown resistor no greater than 10 kΩ per device.
3. The minimum $\overline{\text{RESET}}$ pulse width is 33/PCLK frequency (i.e. 33/8.192 MHz = 4 µs).

Table 10. Switching Characteristics—SPI

(V_{DDA} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Cycle Time SCLK	t_c		62	—	—	ns
Rise Time, SCLK	t_r		—	—	25	ns
Fall Time, SCLK	t_f		—	—	25	ns
Delay Time, SCLK Fall to SDO Active	t_{d1}		—	—	20	ns
Delay Time, SCLK Fall to SDO Transition	t_{d2}		—	—	20	ns
Delay Time, $\overline{CS}$ Rise to SDO Tri-state	t_{d3}		—	—	20	ns
Setup Time, $\overline{CS}$ to SCLK Fall	t_{su1}		25	—	—	ns
Hold Time, $\overline{CS}$ to SCLK Rise	t_{h1}		20	—	—	ns
Setup Time, SDI to SCLK Rise	t_{su2}		25	—	—	ns
Hold Time, SDI to SCLK Rise	t_{h2}		20	—	—	ns
Delay Time between Chip Selects	t_{cs}		220	—	—	ns
SDI to SDITHRU Propagation Delay	t_{d4}		—	4	10	ns

Note: All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DDD} –0.4 V, V_{IL} = 0.4 V

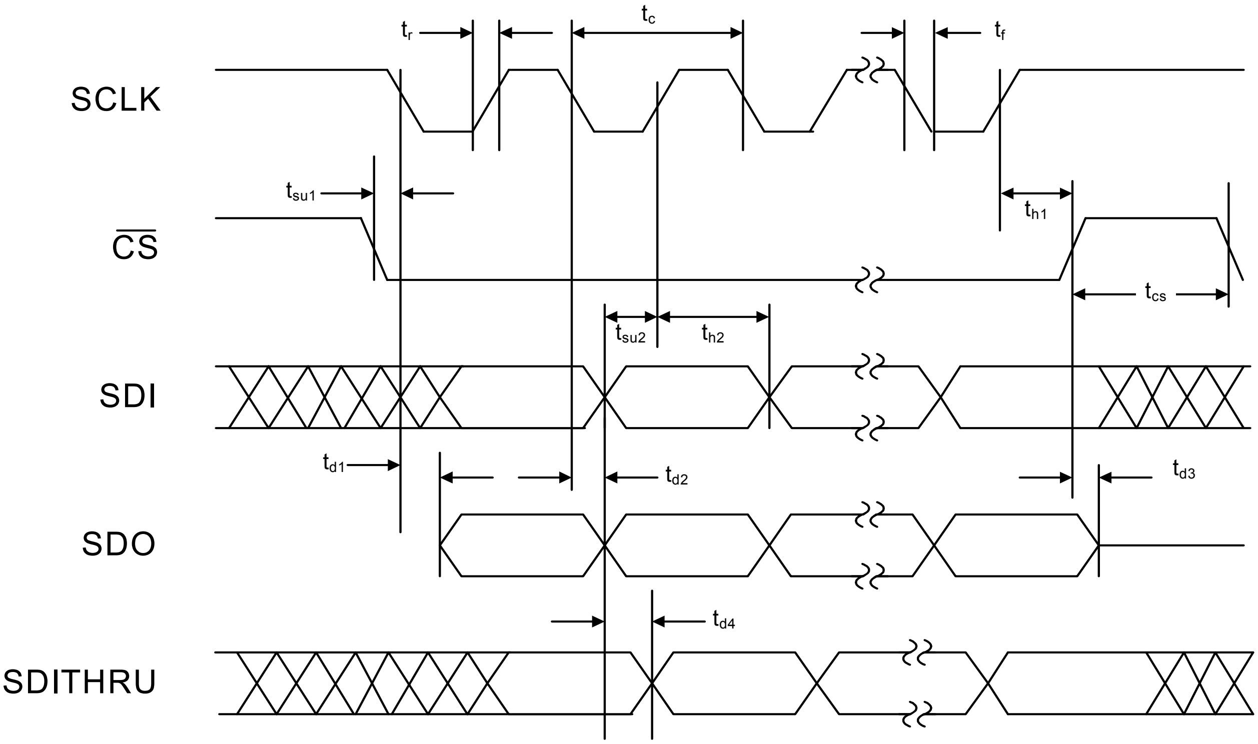


Figure 1. SPI Timing Diagram

Table 11. Switching Characteristics—PCM Highway Interface

(V_{DD} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade, C_L = 20 pF)

Parameter	Symbol	Test Conditions	Min[1]	Typ[1]	Max[1]	Units
PCLK Period	t_p		122	—	3906	ns
Valid PCLK Inputs			— — — — — — — —	512 768 1.024 1.536 1.544 2.048 4.096 8.192	— — — — — — — —	kHz kHz MHz MHz MHz MHz MHz MHz
FSYNC Period[2]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tristate[3]	t_{d3}		—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}		20	—	—	ns
Setup Time, DRX to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, DRX to PCLK Fall	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		t_p	—	125 µs–t_p	

Notes:

1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} – V_{I/O} – 0.4$ V, V_{IL} = 0.4 V.
2. FSYNC source is assumed to be 8 kHz under all operating conditions.
3. Spec applies to PCLK fall to DTX tristate when that mode is selected.

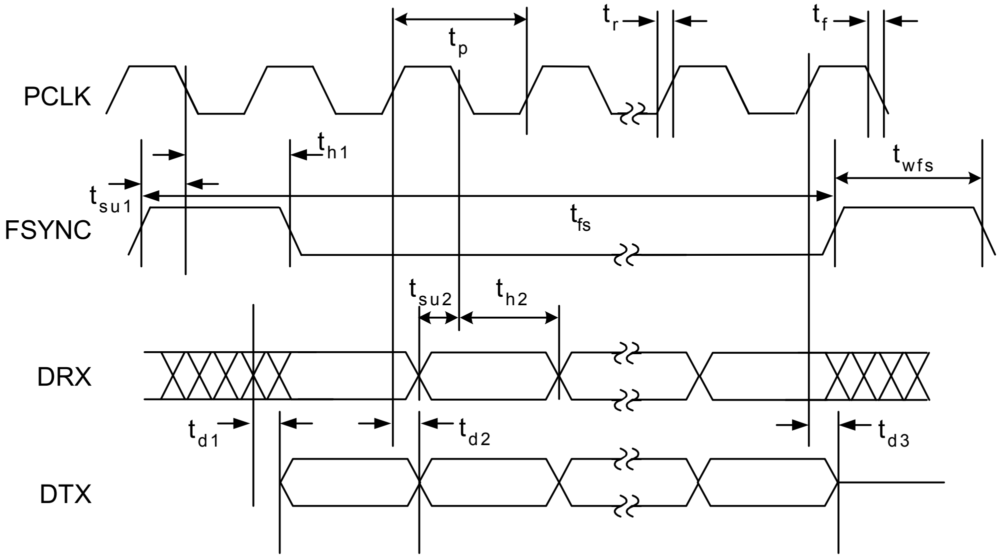


Figure 2. PCM Highway Interface Timing Diagram

Table 12. Switching Characteristics—GCI Highway Serial Interface

(V_{DD} = 3.13 to 5.25 V, T_A = 0 to 70 °C for F-Grade, –40 to 85 °C for G-Grade)

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Units
PCLK Period (2.048 MHz PCLK Mode)	t_p		—	488	—	ns
PCLK Period (4.096 MHz PCLK Mode)	t_p		—	244	—	ns
FSYNC Period[2]	t_{fs}		—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}		40	50	60	%
FSYNC Jitter Tolerance	t_{jitter}		—	—	±120	ns
Rise Time, PCLK	t_r		—	—	25	ns
Fall Time, PCLK	t_f		—	—	25	ns
Delay Time, PCLK Rise to DTX Active	t_{d1}		—	—	20	ns
Delay Time, PCLK Rise to DTX Transition	t_{d2}		—	—	20	ns
Delay Time, PCLK Rise to DTX Tristate[3]	t_{d3}		—	—	20	ns
Setup Time, $\overline{\text{FSYNC}}$ Rise to PCLK Fall	t_{su1}		25	—	—	ns
Hold Time, PCLK Fall to FSYNC Fall	t_{h1}		20	—	—	ns
Setup Time, DRX Transition to PCLK Fall	t_{su2}		25	—	—	ns
Hold Time, PCLK Falling to DRX Transition	t_{h2}		20	—	—	ns
FSYNC Pulse Width	t_{wfs}		$t_p/2$	—	—	ns

Notes:

1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_O - 0.4$ V and $V_{IL} = 0.4$ V. Rise and fall times are referenced to the 20% and 80% levels of the waveform.
2. FSYNC source is assumed to be 8 kHz under all operating conditions.
3. Specification applies to PCLK fall to DTX tristate when that mode is selected.

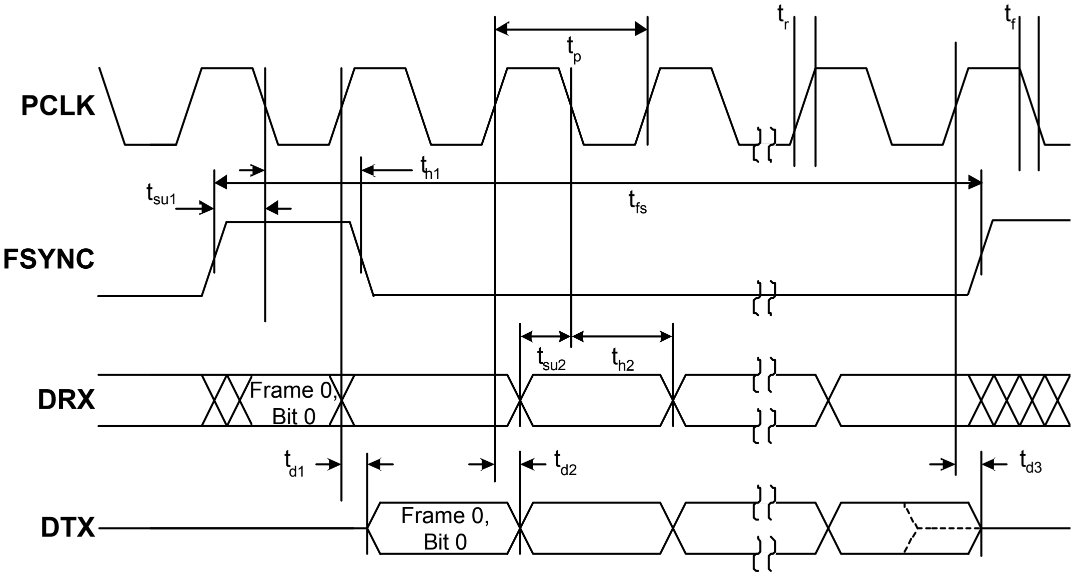


Figure 3. GCI Highway Interface Timing Diagram (2.048 MHz PCLK Mode)

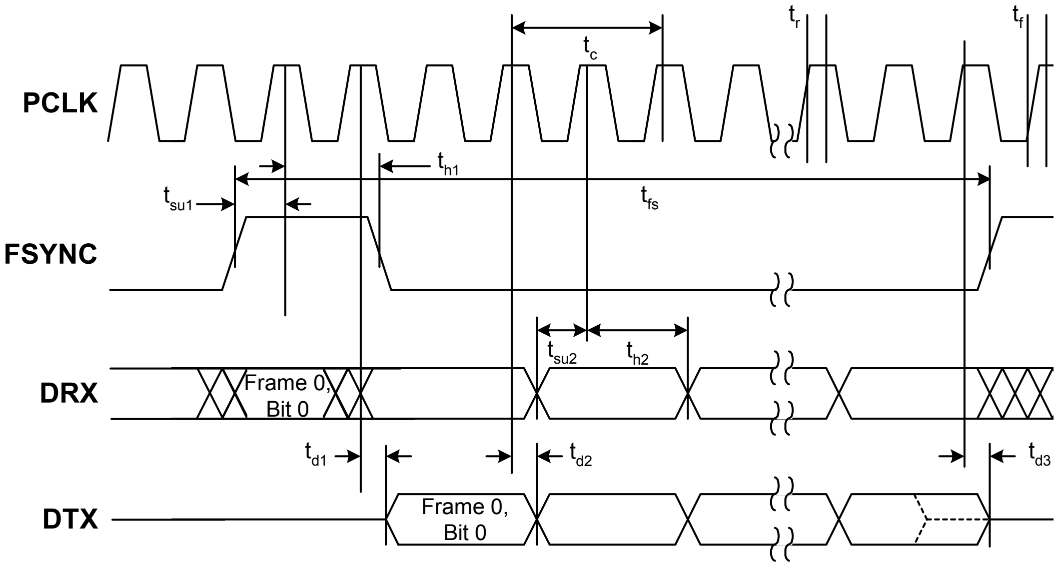


Figure 4. GCI Highway Interface Timing Diagram (4.096 MHz PCLK Mode)

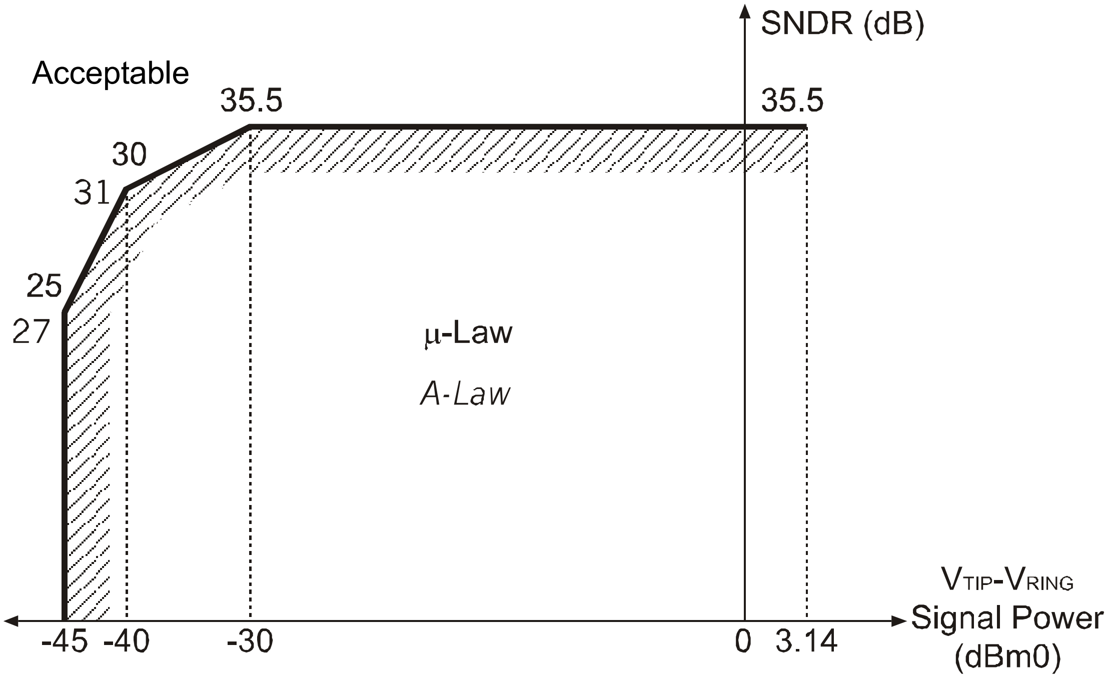


Figure 5. Transmit and Receive Path SNDR

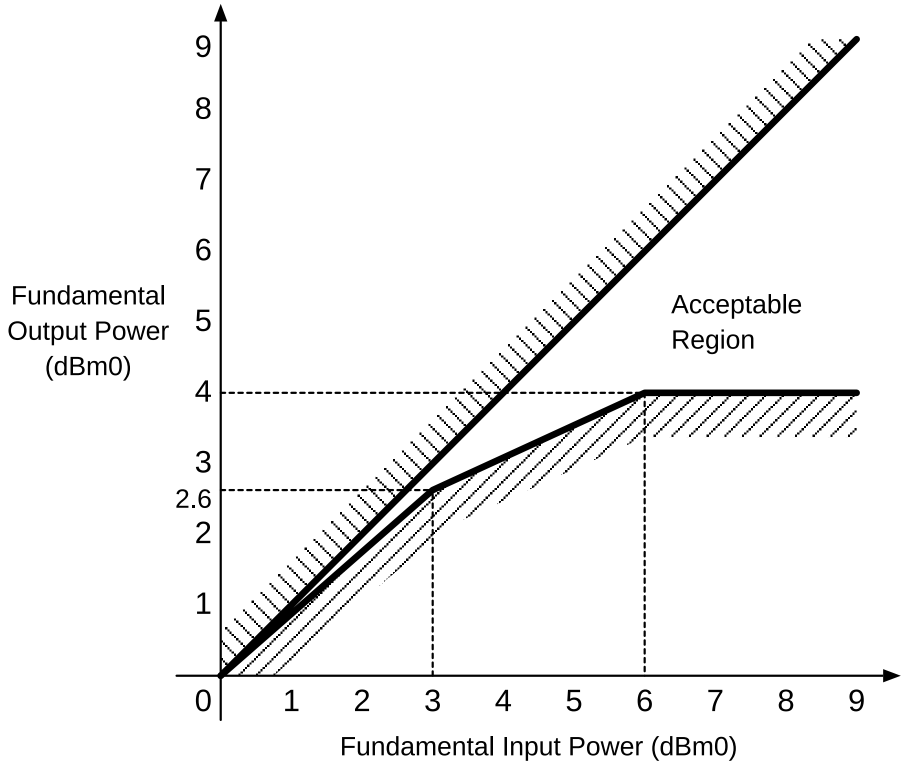
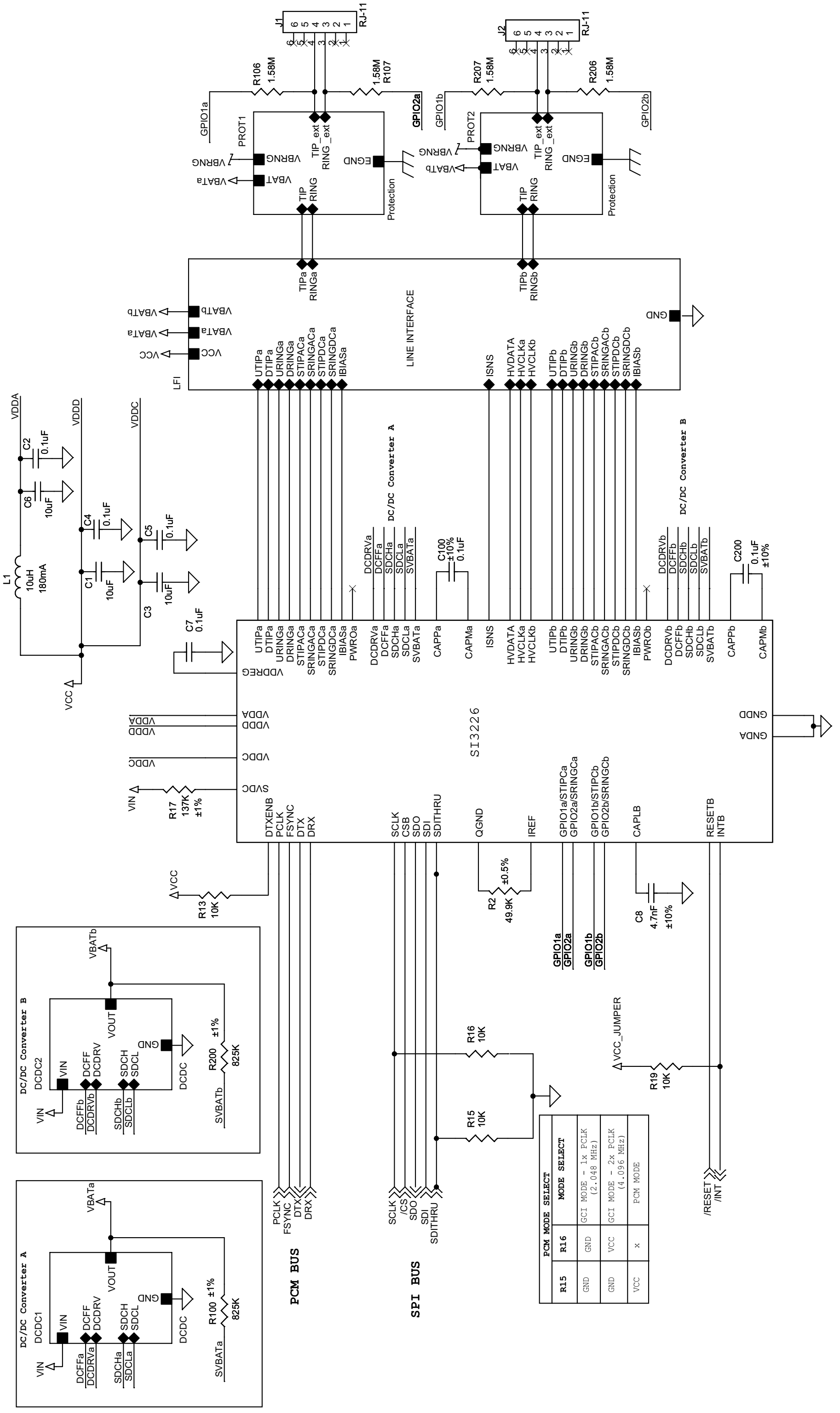


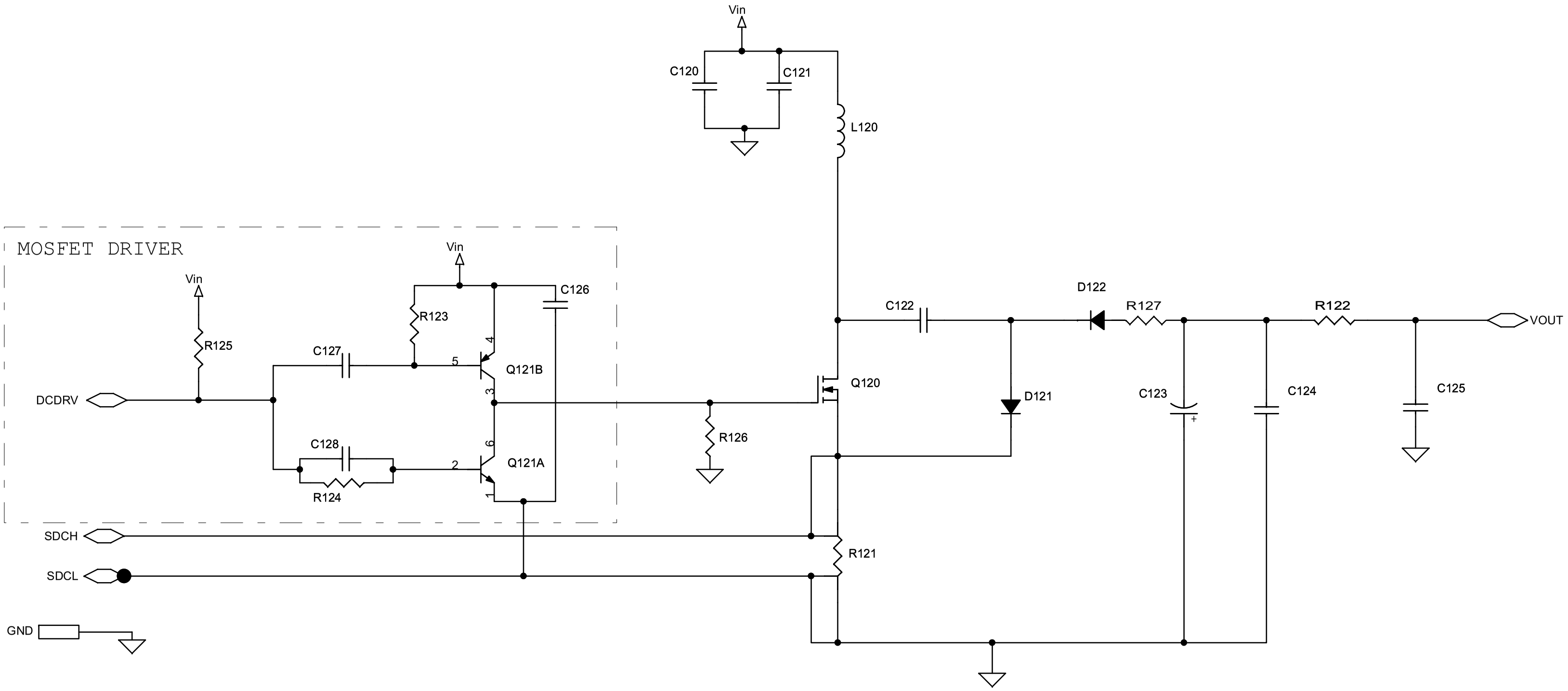
Figure 6. Overload Compression Performance

2. Typical Application Circuits



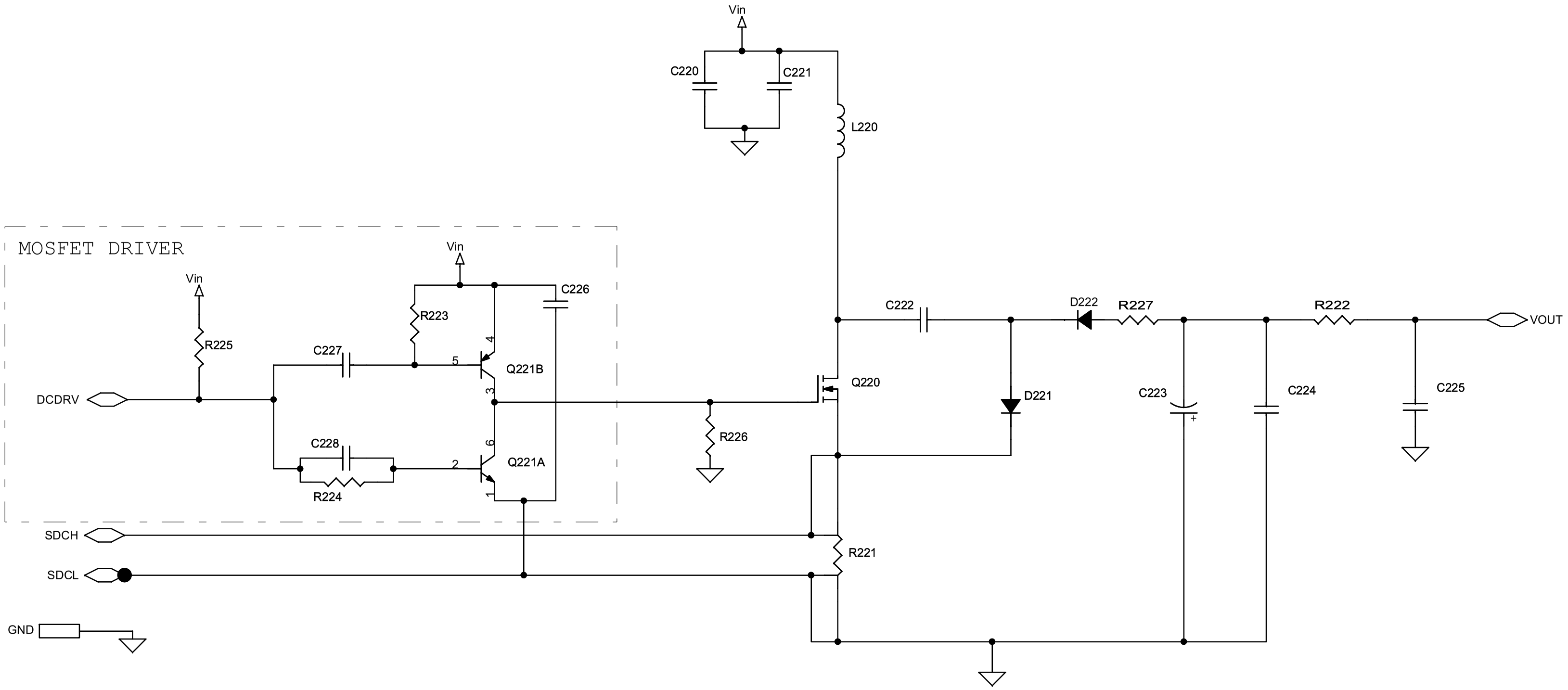
PCM MODE SELECT		
R15	R16	MODE SELECT
GND	GND	GCI MODE - 1x PCLK (2.048 MHz)
GND	VCC	GCI MODE - 2x PCLK (4.096 MHz)
VCC	x	PCM MODE

Figure 7. Si3226/7 (2 Lines)



Notes:
1) Component values and ratings are shown in the bill of materials.
2) Vin and Vout are defined in the bill of materials.

Figure 8. DC-DC Converter (A)



Notes:
1) Component values and ratings are shown in the bill of materials.
2) Vin and Vout are defined in the bill of materials.

Figure 9. DC-DC Converter (B)

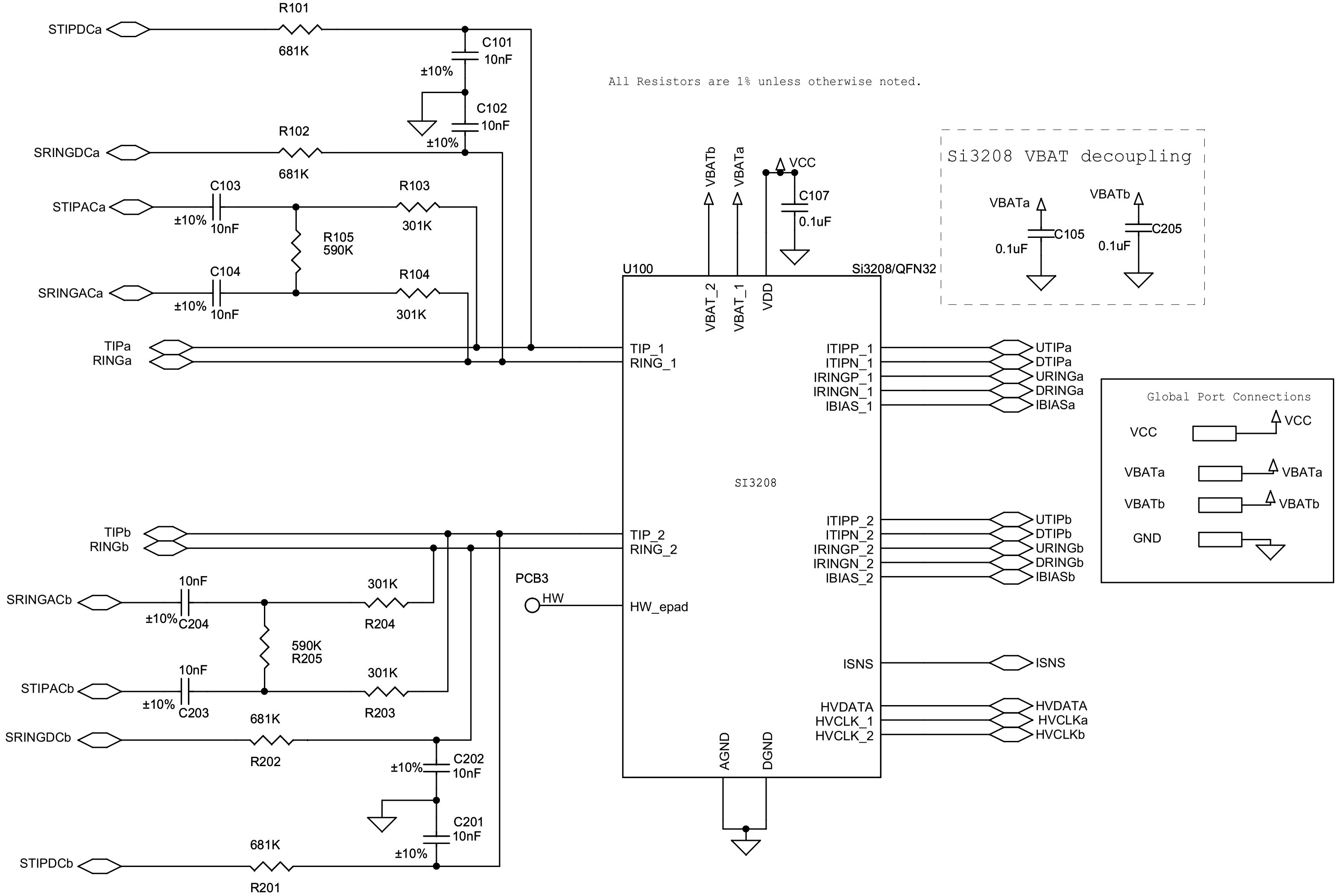


Figure 10. Linefeed (2 Lines)

3. Bill of Materials

Table 13. Bill of Materials for Si3226/7 (2 Lines)

Quantity	Reference	Value	Rating	Tolerance	Dielectric	PCB Footprint	Manufacturer
2	C1, C6	10 µF	6.3 V	±20%	Y5V	CC1210	Venkel
2	C100, C200	0.1 µF	6.3 V	±10%	X7R	CC0603	Venkel
4	C2, C4, C5, C7	0.1µF	6.3 V	±20%	X7R	CC0603	Venkel
1	C3*	10µF	6.3 V	±20%	Y5V	CC1210	Venkel
1	C8	4.7 nF	6.3 V	±10%	X7R	CC0603	Venkel
1	L1*	10 µH	180 mA	±10%		IND-NLC3225	TDK
1	R2	49.9 kΩ	1/16 W	±0.5%		RC0603	Venkel
4	R13, R15, R16, R19	10 kΩ	1/10 W	±5%		RC0603	Venkel
1	R17	137 kΩ	1/16 W	±1%		RC0603	Venkel
2	R100, R200	825 kΩ	1/10 W, 100 V	±1%		RC0805	Venkel
4	R106*, R107*, R206*, R207*	1.58 MΩ	1/10 W, 100 V	±5%		RC0805	Venkel
1	U1	Si3226				TQFP64	SiLabs

***Note:** Denotes optional component.

Table 14. Bill of Materials for Linefeed and DC-DC Converters with $|V_{OUT}| < 90$ V (2 Lines)

V_{IN} = +12 V nominal, |Vout| < 90 V

Quantity	Reference	Value	Rating	Tolerance	Dielectric	PCB Footprint	Manufacturer
1	C120	10 µF	25 V	±20%	X7R	CC1210	Venkel
1	C220*	10 µF	25 V	±20%	X7R	CC1210	Venkel
2	C121, C221	0.1 µF	25 V	±10%	X7R	CC0603	Venkel
2	C126, C226	0.1 µF	25 V	±20%	X7R	CC0603	Venkel
2	C124, C224	0.1 µF	100 V	±20%	X7R	CC1210	Venkel
2	C125*, C225*	0.1 µF	100 V	±20%	X7R	CC1210	Venkel
2	C122, C222	0.22 µF	100 V	±20%	X7R	CC1812	Venkel
2	C123, C223	3.3 µF	100 V	±20%	Al	C2.5X6.3MM-RAD	Panasonic
4	C127, C128, C227, C228	470 pF	25 V	±10%	X7R	CC0402	Venkel
2	D122, D222	BAS21HT1	250 V,200 mA			SOD-323	ON SEMI
2	D121, D221	STPS2150A	150 V, 2.0 A			DO-214AC	STMicro
2	L120, L220	15 µH				CDR74	SUMIDA
2	Q120, Q220	FQT7N10	100 V, 2 W			SOT-223	Fairchild
2	Q121, Q221	MMDT3946				SOT-363	Diodes Inc.
2	R121, R221	0.1 Ω	1/4 W	±1%		RC1210	Venkel
2	R122, R222	15 Ω	1/4 W	±5%		RC1206	Venkel
2	R123, R223	220 Ω	1/16 W	±5%		RC0402	Venkel
2	R124, R224	1 kΩ	1/16 W	±5%		RC0402	Venkel
2	R125, R225	150 kΩ	1/16 W	±5%		RC0402	Venkel
2	R126, R226	100 kΩ	1/16 W	±5%		RC0402	Venkel
2	R127, R227	2 Ω	1/8 W	±5%		RC0402	Venkel
1	C107	0.1 µF	25 V	±10%	X7R	CC0603	Venkel

***Note:** Denotes optional component.

Table 14. Bill of Materials for Linefeed and DC-DC Converters with $|V_{OUT}| < 90$ V (2 Lines) (Continued)

V_{IN} = +12 V nominal, |Vout| < 90 V

Quantity	Reference	Value	Rating	Tolerance	Dielectric	PCB Footprint	Manufacturer
4	C101, C102, C201, C202	10 nF	100 V	±10%	X7R	CC0805	Venkel
4	C103, C104, C203, C204	10 nF	100 V	±10%	X7R	CC0805	Venkel
2	C105, C205	0.1 µF	100 V	±20%	X7R	CC1210	Venkel
4	R101, R102, R201, R202	681 kΩ	1/10 W, 150 V	±1%		RC0805	Venkel
4	R103, R104, R203, R204	301 kΩ	1/16 W, 75 V	±1%		RC0603	Venkel
2	R105, R205	590 kΩ	1/10 W, 150 V	±1%		RC0805	Venkel
1	U100	Si3208 or Si3209				QFN-40	Silicon Laboratories

***Note:** Denotes optional component.

Table 15. Bill of Materials for Linefeed and DC-DC Converters with $|V_{OUT}| < 135$ V (2 Lines)

V_{IN} = +12 V nominal, |Vout| < 135 V

Quantity	Reference	Value	Rating	Tolerance	Dielectric	PCB Footprint	Manufacturer
1	C120	10 µF	25 V	±20%	X7R	CC1210	Venkel
1	C220*	10 µF	25 V	±20%	X7R	CC1210	Venkel
2	C121,C221	0.1 µF	25 V	±10%	X7R	CC0603	Venkel
2	C126,C226	0.1 µF	25 V	±20%	X7R	CC0603	Venkel
2	C124,C224	0.1 µF	200 V	±20%	X7R	CC1210	Venkel
2	C125*,C225*	0.1 µF	200 V	±20%	X7R	CC1210	Venkel
2	C122,C222	0.22 µF	200 V	±20%	X7R	CC1812	Venkel
2	C123,C223	3.3 µF	160 V	±20%	Al	C2.5X6.3MM-RAD	Panasonic
4	C127, C128, C227, C228	470 pF	25 V	±10%	X7R	CC0402	Venkel
2	D122, D222	BAS21HT1	250 V,200 mA			SOD-323	ON SEMI
2	D121, D221	STPS2150A	150 V, 2.0 A			DO-214AC	STMicro
2	L120, L220	15 µH				CDRH125	SUMIDA
2	Q120, Q220	FQD7N20L	200 V, 2.5 W			D-PAK	Fairchild
2	Q121, Q221	MMDT3946				SOT-363	Diodes Inc.
2	R121, R221	0.1 Ω	1/4 W	±1%		RC1210	Venkel
2	R122, R222	15 Ω	1/4 W	±5%		RC1206	Venkel
2	R123, R223	220 Ω	1/16 W	±5%		RC0402	Venkel
2	R124, R224	1 kΩ	1/16 W	±5%		RC0402	Venkel
2	R125, R225	150 kΩ	1/16 W	±5%		RC0402	Venkel
2	R126, R226	100 kΩ	1/16 W	±5%		RC0402	Venkel
2	R127, R227	2 Ω	1/8 W	±5%		RC0402	Venkel
1	C107	0.1 µF	25 V	±10%	X7R	CC0603	Venkel

***Note:** Denotes optional component.

Table 15. Bill of Materials for Linefeed and DC-DC Converters with $|V_{OUT}|$ < 135 V (2 Lines) (Continued)

V_{IN} = +12 V nominal, |Vout| < 135 V

Quantity	Reference	Value	Rating	Tolerance	Dielectric	PCB Footprint	Manufacturer
4	C101, C102, C201, C202	10 nF	200 V	±10%	X7R	CC0805	Venkel
4	C103, C104, C203, C204	10 nF	100 V	±10%	X7R	CC0805	Venkel
2	C105, C205	0.1 µF	200 V	±20%	X7R	CC1210	Venkel
4	R101, R102, R201, R202	681 kΩ	1/10 W, 150 V	±1%		RC0805	Venkel
4	R103, R104, R203, R204	301 kΩ	1/16 W, 75 V	±1%		RC0603	Venkel
2	R105, R205	590 kΩ	1/10 W, 150 V	±1%		RC0805	Venkel
1	U100	Si3209				QFN-40	Silicon Laboratories
***Note:** Denotes optional component.							

4. Functional Description

The Dual ProSLIC® chipset includes the Si3226/7 low-voltage IC and the Si3208/9 high-voltage linefeed IC. The Dual ProSLIC provides all SLIC, codec, DTMF detection, and signal generation functions needed for two complete analog telephone interfaces. The Dual ProSLIC performs all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions; it also supports extensive metallic loop testing capabilities.

The Si3226 provides a standard voice-band (200 Hz–3.4 kHz) audio codec. The Si3227 provides an audio CODEC with both wideband (50 Hz–7 kHz) and standard voice-band (200 Hz– 3.4 kHz) modes. The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality while the standard voice-band mode provides standard telephony audio compatibility. The Si3226/7 provides two independent, programmable, dc-dc converter controllers, each of which reacts to line conditions to provide the optimal battery voltage required for each line-state.

The linefeed chips (Si3208/9) provide programmable on-hook voltage, programmable off-hook loop current, reverse battery operation, loop or ground start operation, and on-hook transmission. Loop current and voltage are continuously monitored using an A/D converter in the Si3226/7. The Si3208 supports battery voltages up to 110 V, sufficient for most ringing signals. The Si3209 supports battery voltages up to 130 V for higher-voltage ringing applications.

The Dual ProSLIC supports balanced 5 REN ringing with or without a programmable dc offset. The available offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements. Digital voice data transfer occurs over a standard PCM bus. Control data is transferred using a standard SPI.

The Si3226/7 is available in a 64-pin TQFP; the Si3208 is available in a 32-pin QFN, and the Si3209 is available in a 40-pin QFN or a 48-pin eTQFP.

4.1. DC Feed Characteristics

Dual ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics. Linefeed characteristics for each channel are independently configurable.

When in the active state, each ProSLIC channel operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in Figure 11. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

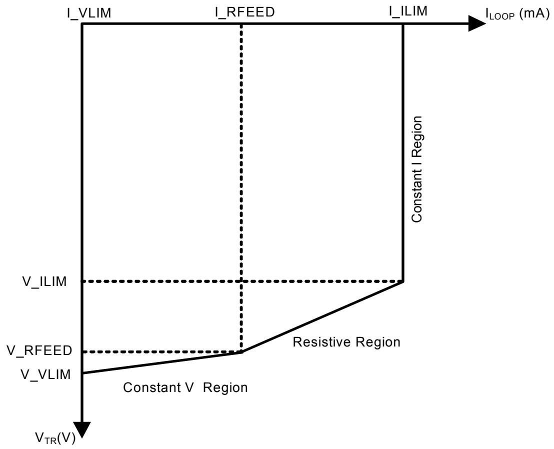


Figure 11. Dual ProSLIC DC Feed Characteristics

4.2. Linefeed Operating States

The linefeed interface includes eight different register-programmable operating states as listed in Table 16. The Open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

4.3. Line Voltage and Current Monitoring

The Dual ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip ADC and stores the resulting values in individual register addresses. Additionally, the loop voltage (V_{TIP}–V_{RING}), loop current, and longitudinal current values are calculated based on the TIP and RING measurements and are stored in unique register locations for further processing. The ADC updates all registers at a rate of 2 kHz or greater.

4.4. Power Monitoring and Power Fault Detection

The Dual ProSLIC's line monitoring functions are used to continuously protect the linefeed IC (LFIC) against excessive power conditions. The LFIC contains an on-chip, analog sensing diode that provides real-time temperature data to the Si3226/7 and turns off the LFIC when a preset threshold is exceeded. The LFIC status is reflected in a Si3226/7 register bit.

If the Si3226/7 detects a fault condition or overpower condition on any channel, it automatically sets that channel to the open state and generates a "power alarm" interrupt. The interrupt can be masked, but the automatic transition to open cannot be masked. The various power alarms and linefeed faults supporting automatic intervention are described below.

1. LFIC total power exceeded.
2. Power exceeded in one or more transistors of a LFIC internal transistor group (if capable of measuring individual power consumption).
3. Excessive foreign current or voltage on TIP and/or RING.
4. LFIC thermal shutdown event; this event is automatically performed, and no intervention by the Si3226/7 is required.

4.5. Thermal Overload Shutdown

If the LFIC die temperature exceeds the maximum junction temperature threshold, TJmax, of 145 °C or 200 ºC or other programmed temperature threshold range, the LFIC has the ability to shut itself down to a low-power state without any assistance from the Si3226/7. The thermal shutdown circuit contains a sufficient amount of hysteresis and/or turn-on delay time so as to remain shut down during a power cross event, where 50 Hz or 60 Hz, 600 V, is connected to TIP and/ or RING.

Table 16. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance, and all line supervision functions are powered down. Audio is powered down. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high-Z state during linefeed testing. A power fault condition may also force the device into the open state.
Forward Active Reverse Active	Linefeed circuitry and audio are active. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead. Loop closure and ground key detect circuitry are active.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.
TIP Open	Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (>400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
RING Open	Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (>400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto TIP and RING leads with or without dc offset.
Line Diagnostics	The channel selected is put into diagnostic mode. In this mode, the selected channel has special diagnostic resources available.

4.6. Power Dissipation Considerations

The Dual ProSLIC is designed to source loops up to 20 kft as well as short loop applications. The LFIC provides all battery sourcing functions and is, therefore, the determining factor regarding power dissipation in a specific application. The Dual ProSLIC provides an on-chip dc-dc controller that can dynamically reduce the battery supply to ideally match the required line feed voltage.

4.7. Loop Closure Detection

The Dual ProSLIC provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two unique thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

4.8. Ground Key Detection

The Dual ProSLIC provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two unique thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

4.9. Ringing Generation

The Dual ProSLIC provides the ability to generate a programmable sinusoidal or trapezoidal ringing waveform, with or without dc offset. The ringing frequency, wave shape, cadence, and offset are all register-programmable. Using a balanced ringing scheme, the ringing signal is applied to both the TIP and RING leads using dual ringing waveforms that are 180° out of phase with each other. The resulting ringing signal seen across TIP-RING is twice the amplitude of the ringing waveform on either the TIP or RING lead, which allows the ringing circuitry to be forced to withstand only half the total ringing amplitude seen across TIP-RING.

4.10. Polarity Reversal

The Dual ProSLIC supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

4.11. Two-Wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Dual ProSLIC to the impedance of the subscriber loop and minimize the receive path signal reflected back onto the transmit path. Most real or complex two-wire impedances can be generated by using the coefficient generator software to simulate the desired line conditions and generate the required register coefficients.

4.12. Transhybrid Balance Filter

The trans-hybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path. The coefficient generator software is used to optimize the filter coefficients.

4.13. Tone Generators

The Dual ProSLIC includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

4.14. DTMF Detection

In DTMF, two tones generate a DTMF digit. One tone is chosen from the four possible row tones, and one tone is chosen from the four possible column tones. The sum of these tones constitutes one of 16 possible DTMF digits. The Dual ProSLIC performs DTMF detection using an algorithm to compute the DFT for each of the eight DTMF frequencies and their second harmonics. At the end of the DFT computation, the squared magnitudes of the DFT results for the 8 DTMF fundamental tones are computed. The row and column results are sorted to determine the strongest tones, and checks are made to determine if the strongest row and column tones constitute a DTMF digit.

4.15. DC-DC Controller

The controller converts a single positive dc input voltage into an independent negative battery voltage for each channel. The controller operates a dc-dc converter circuit that converts a single positive dc input voltage into an independent negative battery voltage for each channel. In addition to eliminating external high-voltage power supplies, the dc-dc controller allows the Dual ProSLIC to dynamically control the battery voltage to the minimum required for any given operating state according to the programmed linefeed parameters.

4.16. Wideband Audio

The Si3226 supports a narrowband (200 Hz–3.4 kHz) audio codec. The Si3227 supports a software-selectable wideband (50 Hz–7 kHz) and narrowband (200 Hz–3.4 kHz) audio codec. The Si3227 wideband mode provides an expanded audio band at a 16-bit, 16 kHz sample rate for enhanced audio quality while maintaining standard telephony audio compatibility. Wideband audio samples are transmitted and received on the PCM interface using two consecutive 8 kHz frames.

4.17. SPI Control Interface

The controller interface to the Dual ProSLIC is a 4-wire interface modeled after microcontroller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CS), serial data input (SDI), and serial data output (SDO). In addition, the Dual ProSLIC devices feature a serial data through output (SDITHRU) to support operation of up to eight devices (up to 16 channels) using a single chip select line. The device operates with both 8-bit and 16-bit SPI controllers.

4.18. PCM Interface and Companding

The Dual ProSLIC contains a flexible, programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCM clock (PCLK) and frame sync (FSYNC) inputs as well as the PCM Mode Select, PCM Transmit Start, and PCM Receive Start settings.

The interface can be configured to support from four to 128 8-bit time slots in each 125 µs frame, corresponding to a PCM clock (PCLK) frequency range of 256 kHz to 8.192 MHz. 1.544 MHz is also supported.

The Dual ProSLIC supports both µ-255 Law (µ-Law) and A-law companding formats in addition to 16-bit linear data mode with no companding.

4.19. General Circuit Interface

The Dual ProSLIC supports an alternative communication interface to the SPI and PCM control and data interface. The General Circuit Interface (GCI) is used for transmission and reception of both control and data information onto a GCI bus. The PCM and GCI interfaces are both 4-wire interfaces and share the same pins. In GCI mode, the four-wire SPI control interface is used as hard-wired channel selector pins. The selection between PCM and GCI modes is performed when coming out of reset using the SDITHRU pin.

4.20. Metallic Loop Testing

The Dual ProSLIC includes the ability to detect multiple fault conditions within the line card as well as on the T/R pair.

1. Hazardous Potential Test—This test checks for ac voltage >50 V_{rms} or dc voltage >135 V on T-G or R-G. If a hazardous voltage is encountered, test access MUST release within two seconds of the time when it was initiated using a preset threshold.
2. Foreign ElectroMotive Force Test—Checks T-G or R-G for ac voltage >10 V_{rms}, dc voltage >6 V. Uses same threshold as for hazardous voltage test.
3. Resistive Faults Test—Checks for dc resistance from T-R, T-G or R-G. Any measurement <150 kΩ is considered a resistive fault.
4. Receiver-Off-Hook Test—Distinguishes between a T-R resistive fault and an off-hook condition.
5. Ringers Test—Checks for the presence of REN across T-R. Result are >0.175REN and <5REN for a valid load.
6. AC Line Impedance (line length)—T-R, T-G, and R-G. Generate a tone at several specific frequencies (audio band) and measure the reflected signal amplitude (complex spectrum) that comes back (with transhybrid balance filter disabled). The reflected signal is then used to calculate the line impedance based on certain assumptions of wire gauge, etc.
7. Line Capacitance—T-R, T-G, R-G. Generate a linear ramp function with polarity reversal, and measure the time constant.
8. Ringer Capacitance—This test uses the same procedure as the ringer test above but also measures the V/I phase relationship of the received signal (dc path) and then subtracts the delay to calculate the ringer capacitance.
9. Ringing Voltage Verification—Uses current voltage sensing capability.
10. Test-In Diagnostics—The Dual ProSLIC can switch in a preset load impedance to test the SLIC/codec functionality using a known set of conditions.

5. Pin Descriptions: Si3226/7

Table 17. Si3226/7 Pin Descriptions

Pin Number	Symbol	I/O	Description
1	SRINGDCa	I	RING DC Sense Input.
2	SRINGACa	I	RING AC Sense Input.
3	STIPACa	I	TIP AC Sense Input.
4	STIPDCa	I	TIP DC Sense Input.
5	CAPPa	I/O	Metallic Loop Filter Capacitor-Positive Terminal.
6	CAPMa	I/O	Metallic Loop Filter Capacitor-Negative Terminal.
7	SVBATa	I	Battery Sensing Input.
8	SVDC	I	DC-DC Input Power Rail Sensor.
9	GPIO3a / PWROa	I/O	General Purpose I/O / Power Offloading Output.
10	GPIO2a / SRINGCa / TRD2a	I/O	General Purpose I/O / TIP Course Sense Input / Test Relay Driver.
11	GPIO1a / STIPCa / TRD1a	I/O	General Purpose I/O / TIP Course Sense Input / Test Relay Driver.
12	$\overline{\text{CS}}$	I	Chip Select Input.
13	FSYNC	I	Frame Sync Clock Input.
14	SDI	I	Serial Port Data Input.
15	HVCLKa	O	Line-Driver IC Clock Output.
16	SCLK	I	Serial Port Bit Clock Input.
17	HVDATA	O	Line-Driver IC Data Output
18	SDITHRU	O	Serial Data Daisy Chain Output.
19	SDO	O	Serial Port Data Output.
20	DCFFa	I/O	DC-DC BJT Drive Monitor.
21	SDCHa	I	DC-DC Current Monitor Input-High Terminal.
22	SDCLa	I	DC-DC Current Monitor Input-Low Terminal.
23	DCDRVa	I/O	DC-DC Drive Output.
24	VDDC	PWR	DC-DC Switch Driver Power Supply.
25	DCDRVb	O	DC-DC Drive Output.
26	SDCLb	I	DC-DC Current Monitor Input-Low Terminal.
27	SDCHb	I	DC-DC Current Monitor Input-High Terminal.
28	DCFFb	I/O	DC-DC BJT Drive Monitor.
29	GNDD	GND	Digital Ground.
30	VDDD	PWR	Digital Supply Voltage.
31	PCLK	I	PCM Bus Clock Input.
32	HVCLKb	O	Line-Driver IC Clock Output.

Table 17. Si3226/7 Pin Descriptions (Continued)

Pin Number	Symbol	I/O	Description
33	$\overline{\text{DTXEN}}$	O	Transmit PCM Enable Output.
34	DTX	O	Transmit PCM Data Output.
35	DRX	I	Receive PCM Data Input.
36	$\overline{\text{INT}}$	O	Interrupt Output.
37	$\overline{\text{RST}}$	I	Reset Input.
38	VDDREG	I/O	Regulated Core Power Supply.
39	GPIO1b / STIPCb / TRD1b	I/O	General Purpose I/O / TIP Course Sense Input / Test Relay Driver.
40	GPIO2b / SRINGCb / TRD2b	I/O	General Purpose I/O / TIP Course Sense Input / Test Relay Driver.
41	GPIO3b / PWROb	I/O	General Purpose I/O / Power Offloading Output.
42	SVBATb	I	Battery Sensing Input.
43	CAPMb	I/O	Differential Loop Filter Capacitor-Negative Term.
44	CAPPb	I/O	Differential Loop Filter Capacitor-Positive Term.
45	STIPDCb	I	TIP DC Sense Input.
46	STIPACb	I	TIP AC Sense Input.
47	SRINGACb	I	RING AC Sense Input.
48	SRINGDCb	I	RING DC Sense Input.
49	DRINGb	O	RING Pull-Down Current Driver Output.
50	URINGb	O	RING Pull-Up Current Driver Output.
51	DTIPb	O	TIP Pull-Down Current Driver Output.
52	UTIPb	O	TIP Pull-Up Current Driver Output.
53	IBIASb	O	Line Driver IC Bias Current Output.
54	CAPLB	O	Longitudinal Balance Calibration Capacitor.
55	IREF	I	Current Reference Input.
56	QGND	I	Quiet Ground Reference Input.
57	GNDA	GND	Analog Ground.
58	VDDA	PWR	Analog Supply Voltage.
59	ISNS	I/O	Line Current Sense Input.
60	IBIASa	O	Line Driver IC Bias Current Output.
61	UTIPa	O	TIP Pull-Up Current Driver Output.
62	DTIPa	O	TIP Pull-Down Current Driver Output.
63	URINGa	O	RING Pull-Up Current Driver Output.
64	DRINGa	O	RING Pull-Down Current Driver Output.

6. Pin Descriptions: Si3208/9

Table 18. Si3208/9 Pin Descriptions

QFN Pin #	Symbol	I/O	Description
1	IC		Internal connection; leave to float.
2	NC		No Connect.
3	RING_1	I/O	Ring Channel 1 Input/Output.
4	NC		No Connect.
5	TIP_1	I/O	Tip Channel 1 Input/Output.
6	NC		No Connect.
7	IC		Internal connection; leave to float.
8	IRINGN_1	I	Negative Ring Current Control Channel 1 Input.
9	IRINGP_1	I	Positive Ring Current Control Channel 1 Input.
10	ITIPN_1	I	Negative Tip Current Control Channel 1 Input.
11	ITIPP_1	I	Positive Tip Current Control Channel 1 Input.
12	IBIAS_1	I	Current Bias Channel 1 Input.
13	ISNS	O	Current Sense Output.
14	VDD	I	IC Supply Voltage Input.
15	HVCLK_1	I	High-Voltage IC Clock Channel 1 Input.
16	HVDATA	I/O	High-Voltage IC Data Input/Output.
17	HVCLK_2	I	High-Voltage IC Clock Channel 2 Input.
18	DGND	I	Digital Ground.
19	IBIAS_2	I	Current Bias Channel 2 Input.
20	ITIPP_2	I	Positive Tip Current Control Channel 1 Input.
21	ITIPN_2	I	Negative Tip Current Control Channel 2 Input.
22	IRINGP_2	I	Positive Ring Current Control Channel 2 Input.
23	IRINGN_2	I	Negative Ring Current Control Channel 2 Input.
24	IC		Internal connection; leave to float.
25	NC		No Connect.
26	TIP_2	I/O	Tip Channel 2 Input/Output.
27	NC		No Connect.
28	RING_2	I/O	Ring Channel 2 Input/Output.
29	NC		No Connect.
30	IC		Internal connection; leave to float.
31	IC		Internal connection; leave to float.
32	VBAT_2	I	Operating Battery Voltage Channel 2 Input.
33	NC		No Connect.
34	IC		Internal connection; leave to float.

Table 18. Si3208/9 Pin Descriptions (Continued)

QFN Pin #	Symbol	I/O	Description
35	NC		No Connect.
36	AGND	I	Analog Ground.
37	IC		Internal connection; leave to float.
38	IC		Internal connection; leave to float.
39	VBAT_1	I	Operating Battery Voltage Channel 1 Input.
40	IC		Internal connection; leave to float.
epad			Exposed Die Attach Paddle. For adequate thermal management, the exposed die paddle should be soldered to a printed circuit board pad that is connected to an electrically-isolated low-impedance inner layer and/or back-side thermal plane(s) using multiple thermal vias. Do not connect this pad to ground.

7. Ordering Guide

Device	Description	Wideband Audio	Package	Temp Range
Si3226-X-FQ	Dual ProSLIC	No	TQFP-64	0 to 70 °C
Si3226-X-GQ	Dual ProSLIC	No	TQFP-64	–40 to 85 °C
Si3227-X-FQ	Dual ProSLIC	Yes	TQFP-64	0 to 70 °C
Si3227-X-GQ	Dual ProSLIC	Yes	TQFP-64	–40 to 85 °C
Si3208-X-FM	110 V Dual LFIC	—	QFN-40	0 to 70 °C
Si3208-X-GM	110 V Dual LFIC	—	QFN-40	–40 to 85 °C
Si3209-X-FM	135 V Dual LFIC	—	QFN-40	0 to 70 °C
Si3209-X-GM	135 V Dual LFIC	—	QFN-40	–40 to 85 °C

Notes:

1. All devices are lead-free and RoHS compliant.
2. “X” denotes product revision (A, B, C, etc.).
3. Add an R at the end of the device to denote tape and reel options.

8. Package Outline: 64-Pin TQFP

Figure 12 illustrates the package details for the Si3226/7. Table 19 lists the values for the dimensions shown in the illustration.

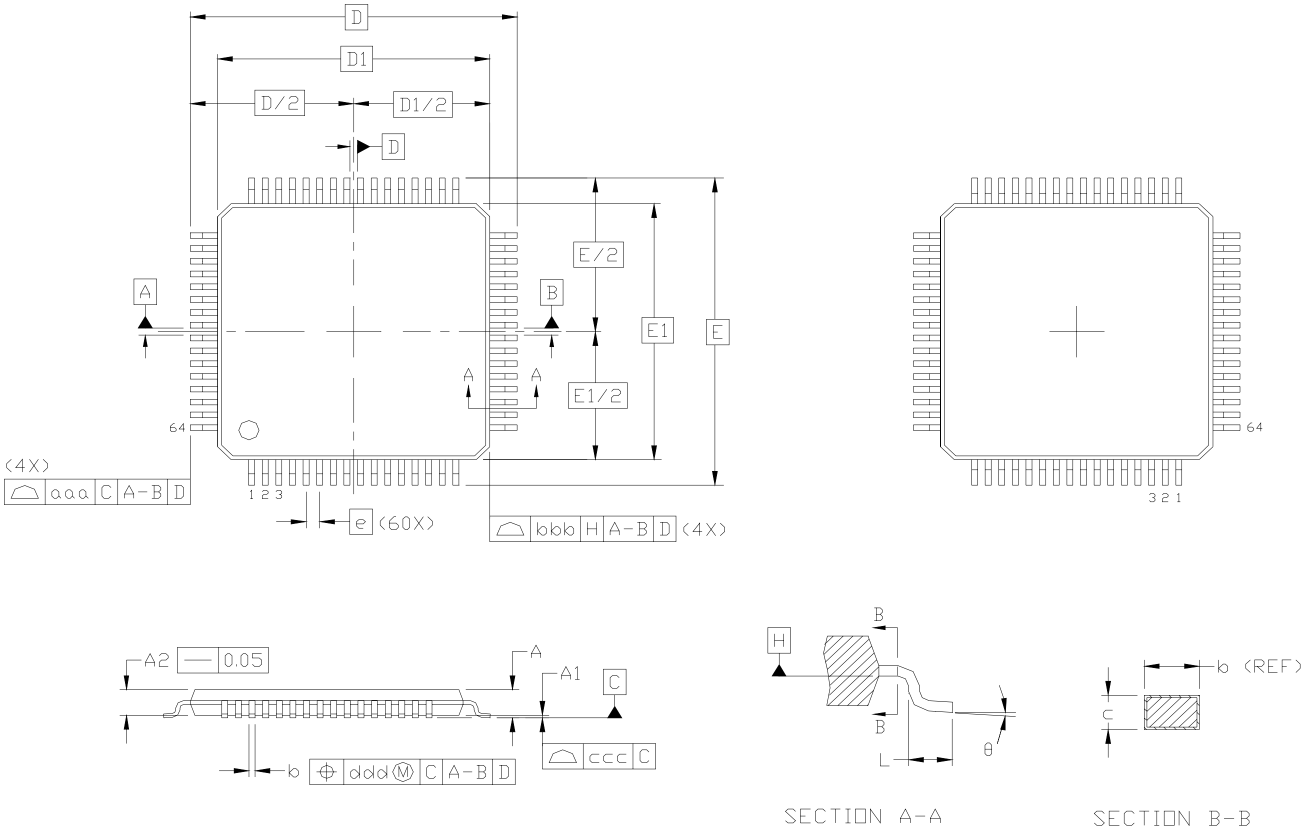


Figure 12. 64-Pin Thin Quad Flat Package (TQFP)

Table 19. 64-Pin TQFP Package Dimensions

Dimension	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC.		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08
Q	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This package outline conforms to JEDEC MS-026, variant ACD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

9. Package Outline: 40-Pin QFN

Figure 13 illustrates the package details for the Si3208/9. Table 20 lists the values for the dimensions shown in the illustration.

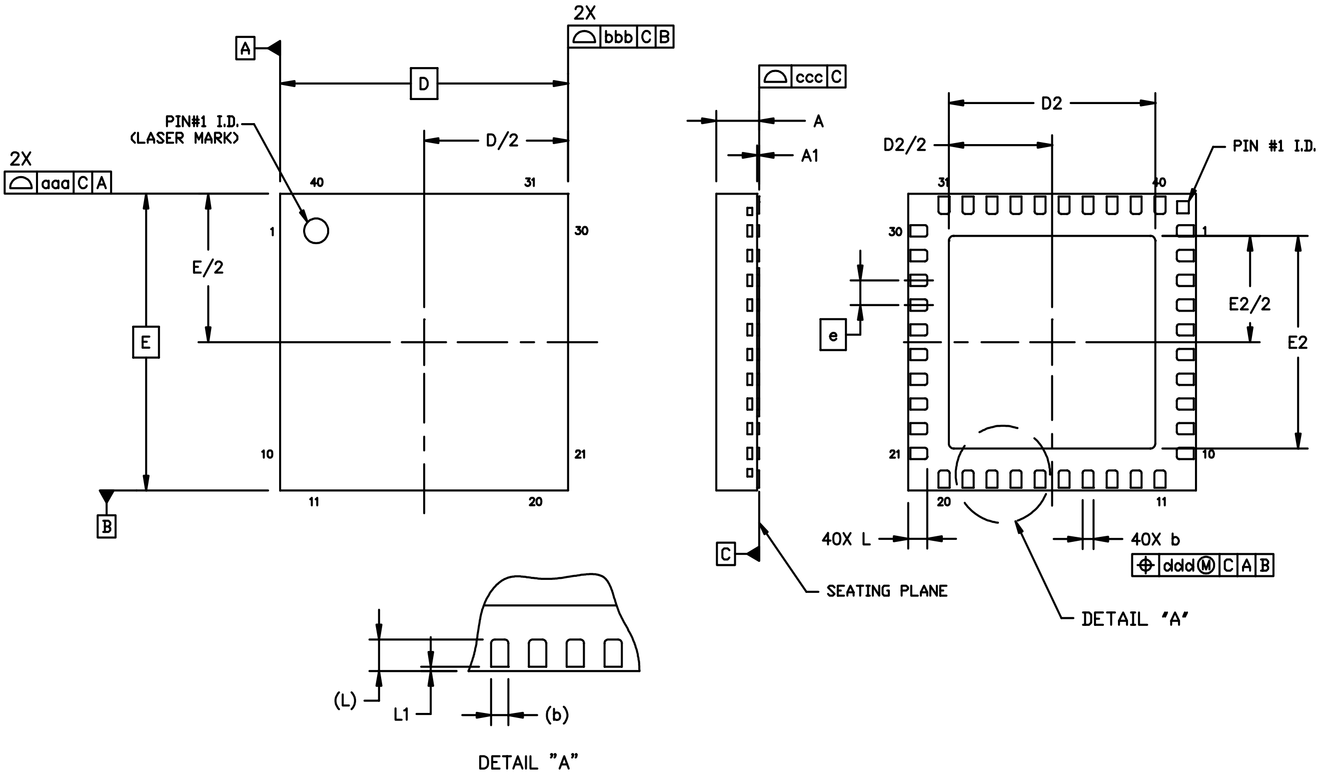


Figure 13. 40-Pin QFN Package

Table 20. 40-Pin QFN Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	0.80	0.90	1.00	E2	4.10	4.30	4.40
A1	0.00	0.02	0.05	L	0.30	0.40	0.50
b	0.18	0.25	0.30	L1	0.03	0.05	0.08
D	6.00 BSC.			aaa	—	—	0.10
D2	4.10	4.30	4.40	bbb	—	—	0.10
e	0.50 BSC.			ccc	—	—	0.08
E	6.00 BSC.			ddd	—	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD-2.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for small body components.

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.32

- Added Si3208 and Si3209.
- Removed Si3203, Si3205, and Si3206.
- Added pin-outs and package drawings for Si3208 and Si3209.
- Updated pin-out for Si3226.
- Updated bill of materials.
- Updated “2. Typical Application Circuits” and added dc-dc converter schematics.
- Updated tables.

Revision 0.32 to Revision 0.33

- Changed package type for Si3208.
- Deleted QFN-32 drawing.
- Updated dc-dc converter schematic.
- Updated bills of materials.
- Updated max V_{BAT} values.
- Updated thermal shutdown thresholds.
- Updated Si3208/9 pin descriptions.

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: ProSLICinfo@silabs.com
Internet: www.silabs.com

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories, Silicon Labs, and ProSLIC are trademarks of Silicon Laboratories Inc.

Other products or brand names mentioned herein are trademarks or registered trademarks of their respective holders.

Downloaded from Arrow.com.