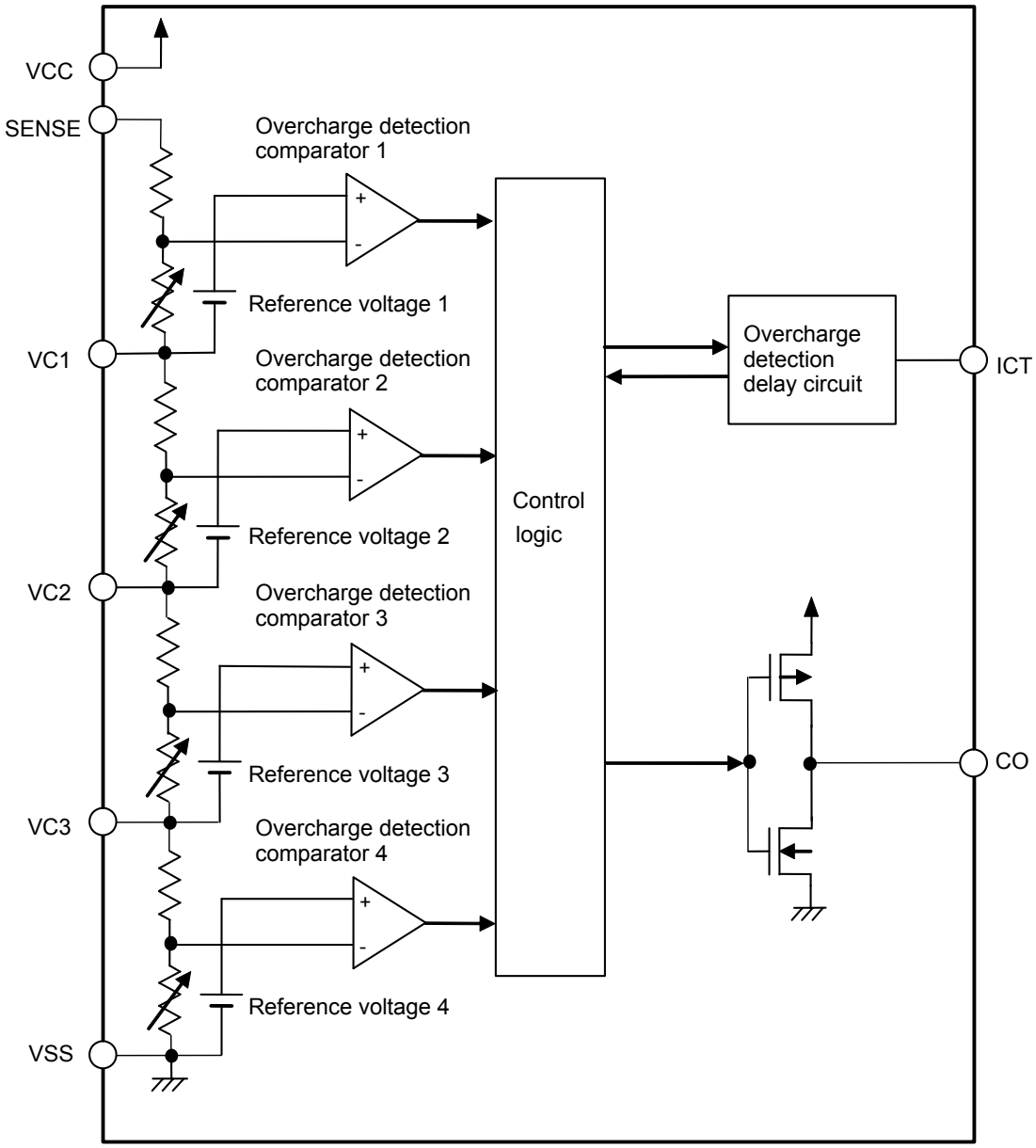
## ■ Block Diagram



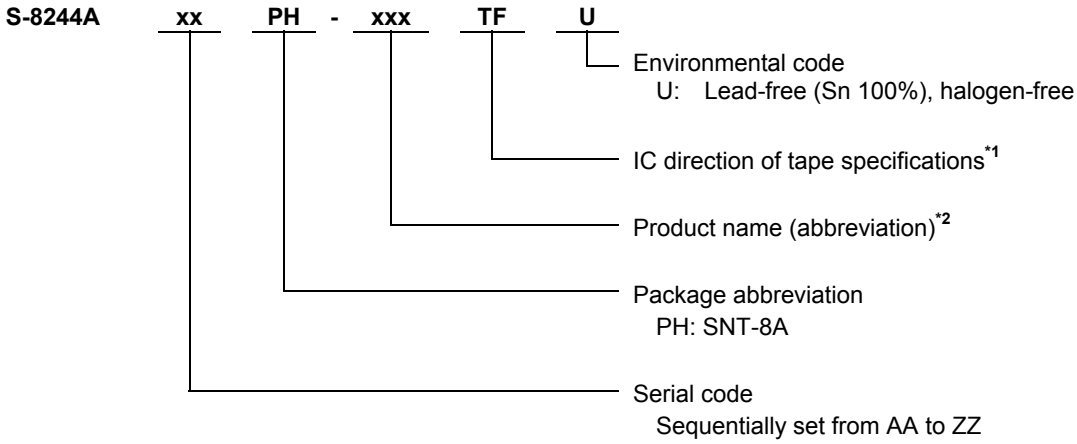

**Remark** In the case of Nch open-drain output, only the Nch transistor will be connected to the CO pin.
In the case of Pch open-drain output, only the Pch transistor will be connected to the CO pin.

**Figure 1**

## ■ Product Name Structure

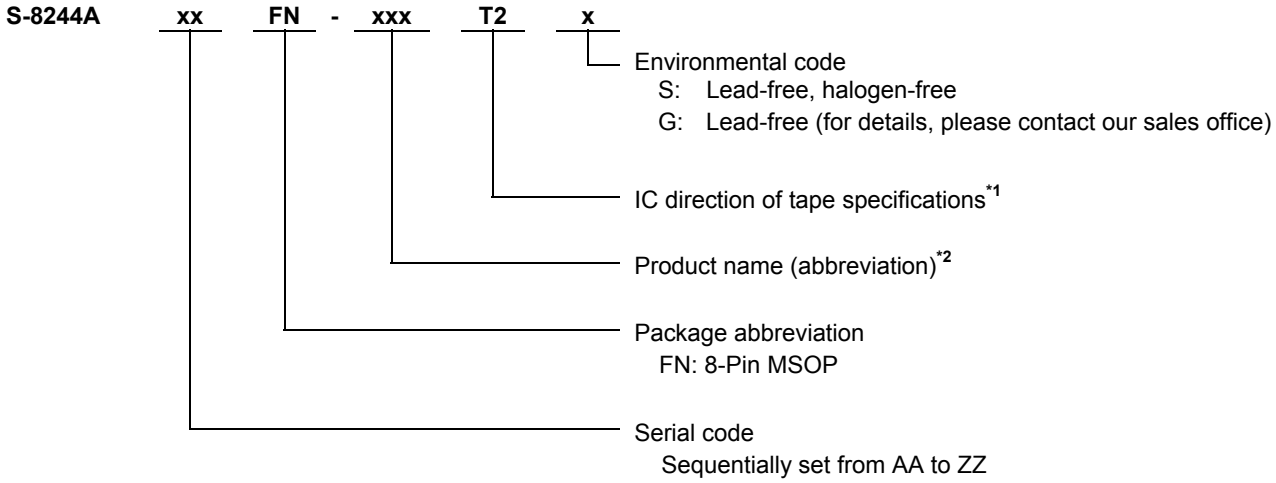
### 1. Product Name

#### (1) SNT-8A



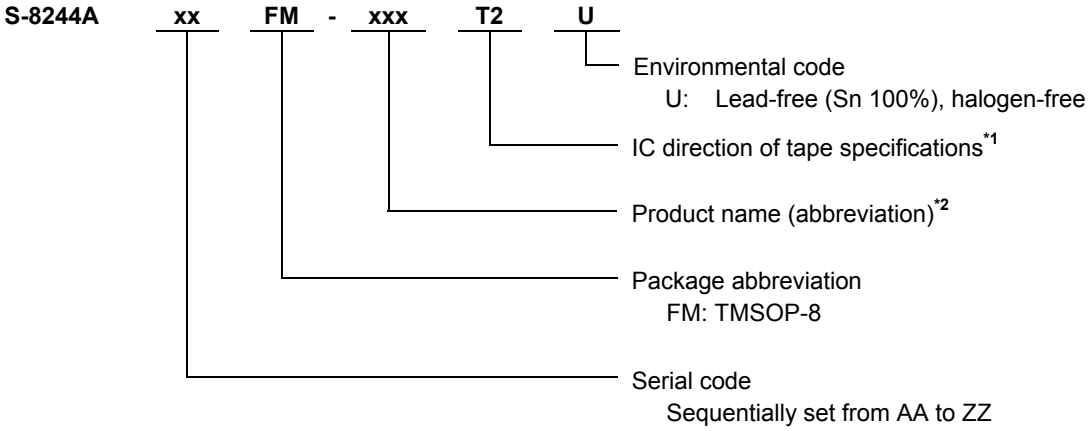

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product Name List**".

#### (2) 8-Pin MSOP




***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product Name List**".

### (3) TMSOP-8




***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product Name List**".

## 2. Packages

| Package name | Drawing code | | | |
|---|---|---|---|---|
| | Package | Tape | Reel | Land |
| SNT-8A | PH008-A-P-SD | PH008-A-C-SD | PH008-A-R-SD | PH008-A-L-SD |
| 8-Pin MSOP | FN008-A-P-SD | FN008-A-C-SD | FN008-A-R-SD | — |
| TMSOP-8 | FM008-A-P-SD | FM008-A-C-SD | FM008-A-R-SD | — |

## 3. Product Name List

### (1) SNT-8A

**Table 1**

| Product name | Overcharge detection voltage [$V_{CU}$] | Overcharge hysteresis voltage [$V_{CD}$] | Output form |
|---|---|---|---|
| S-8244AAAPH-CEATFU | 4.450 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active "H" |
| S-8244AABPH-CEBTFU | 4.200 ± 0.025 V | 0 V | Nch open drain active "H" |
| S-8244AADPH-CEDTFU | 4.200 ± 0.025 V | 0 V | Pch open drain active "L" |
| S-8244AAFPH-CEFTFU | 4.350 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active "H" |
| S-8244AAGPH-CEGTFU | 4.450 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active "H" |
| S-8244AAJPH-CEJTFU | 4.500 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active "H" |
| S-8244AASPH-CESTFU | 4.350 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active "H" |
| S-8244AATPH-CETTFU | 4.200 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active "H" |
| S-8244AAVPH-CEVTFU | 4.275 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active "H" |
| S-8244AAYPH-CEYTFU | 4.300 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active "H" |
| S-8244AAZPH-CEZTFU | 4.280 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active "H" |
| S-8244ABBPH-CFBTFU | 4.380 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active "H" |
| S-8244ABDPH-CFDTFU | 4.150 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active "L" |
| S-8244ABEPH-CFETFU | 4.215 ± 0.025 V | 0 V | Nch open drain active "L" |
| S-8244ABHPH-CFHTFU | 4.280 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active "H" |
| S-8244ABMPH-CFMTFU | 4.100 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active "H" |
| S-8244ABOPH-CFOTFU | 4.550 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active "H" |

**Remark** Please contact our sales office for the products with the detection voltage value other than those specified above.

**(2) 8-Pin MSOP**

**Table 2**

| Product name | Overcharge detection voltage [$V_{CU}$] | Overcharge hysteresis voltage [$V_{CD}$] | Output form |
|---|---|---|---|
| S-8244AAAFN-CEAT2z | 4.450 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active “H” |
| S-8244AABFN-CEBT2z | 4.200 ± 0.025 V | 0 V | Nch open drain active “H” |
| S-8244AACFN-CECT2z | 4.115 ± 0.025 V | 0.13 ± 0.04 V | CMOS output active “H” |
| S-8244AADFN-CEDT2z | 4.200 ± 0.025 V | 0 V | Pch open drain active “L” |
| S-8244AAEFN-CEET2z | 4.225 ± 0.025 V | 0 V | Nch open drain active “H” |
| S-8244AAFFN-CEFT2z | 4.350 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244AAGFN-CEGT2z | 4.450 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244AAHFN-CEHT2z | 4.300 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAIFN-CEIT2z | 4.400 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244AAJFN-CEJT2z | 4.500 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active “H” |
| S-8244AAKFN-CEKT2z | 4.475 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active “H” |
| S-8244AALFN-CELT2z | 4.350 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAMFN-CEMT2z | 4.300 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “L” |
| S-8244AANFN-CENT2z | 4.150 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAOFN-CEOT2z | 4.250 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAPFN-CEPT2z | 4.050 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAQFN-CEQT2z | 4.150 ± 0.025 V | 0 V | Nch open drain active “H” |
| S-8244AARFN-CERT2z | 4.300 ± 0.025 V | 0.25 ± 0.07 V | Nch open drain active “H” |
| S-8244AATFN-CETT2z | 4.200 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAUFN-CEUT2z | 3.825 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAWFN-CEWT2z | 4.500 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active “L” |
| S-8244AAXFN-CEXT2z | 4.025 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAZFN-CEZT2S | 4.280 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244ABAFN-CFAT2z | 4.220 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244ABCFN-CFCT2z | 3.750 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244ABGFN-CFGT2S | 4.225 ± 0.025 V | 0.045 ± 0.02 V | Nch open drain active “L” |
| S-8244ABIFN-CFIT2S | 4.100 ± 0.025 V | 0 V | Nch open drain active “L” |
| S-8244ABJFN-CFJT2S | 4.325 ± 0.025 V | 0.045 ± 0.02 V | Nch open drain active “L” |
| S-8244ABKFN-CFKT2S | 4.175 ± 0.025 V | 0 V | Nch open drain active “L” |

**Remark 1.** Please contact our sales office for the products with the detection voltage value other than those specified above.
**2.** z: G or S

**(3) TMSOP-8**

**Table 3**

| Product name | Overcharge detection voltage [$V_{CU}$] | Overcharge hysteresis voltage [$V_{CD}$] | Output form |
|---|---|---|---|
| S-8244AAAFM-CEAT2U | 4.450 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active “H” |
| S-8244AABFM-CEBT2U | 4.200 ± 0.025 V | 0 V | Nch open drain active “H” |
| S-8244AAFFM-CEFT2U | 4.350 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244AAGFM-CEGT2U | 4.450 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244AAHFM-CEHT2U | 4.300 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAIFM-CEIT2U | 4.400 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244AAJFM-CEJT2U | 4.500 ± 0.025 V | 0.38 ± 0.1 V | CMOS output active “H” |
| S-8244AALFM-CELT2U | 4.350 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AANFM-CENT2U | 4.150 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAPFM-CEPT2U | 4.050 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAQFM-CEQT2U | 4.150 ± 0.025 V | 0 V | Nch open drain active “H” |
| S-8244AAUFM-CEUT2U | 3.825 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244AAVFM-CEVT2U | 4.275 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244AAXFM-CEXT2U | 4.025 ± 0.025 V | 0.25 ± 0.07 V | CMOS output active “H” |
| S-8244ABAFM-CFAT2U | 4.220 ± 0.025 V | 0.045 ± 0.02 V | CMOS output active “H” |
| S-8244ABGFM-CFGT2U | 4.225 ± 0.025 V | 0.045 ± 0.02 V | Nch open drain active “L” |
| S-8244ABIFM-CFIT2U | 4.100 ± 0.025 V | 0 V | Nch open drain active “L” |
| S-8244ABJFM-CFJT2U | 4.325 ± 0.025 V | 0.045 ± 0.02 V | Nch open drain active “L” |
| S-8244ABKFM-CFKT2U | 4.175 ± 0.025 V | 0 V | Nch open drain active “L” |
| S-8244ABNFM-CFNT2U | 4.225 ± 0.025 V | 0.38 ± 0.1 V | Nch open drain active “L” |

**Remark** Please contact our sales office for the products with the detection voltage value other than those specified above.

## ■ Pin Configurations

SNT-8A
Top view

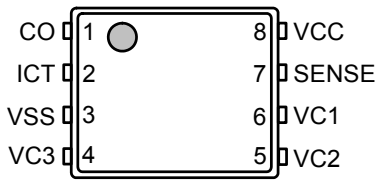



**Figure 2**

**Table 4**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | CO | FET gate connection pin for charge control |
| 2 | ICT | Capacitor connection pin for overcharge detection delay |
| 3 | VSS | Input pin for negative power supply,<br>Connection pin for battery 4's negative voltage |
| 4 | VC3 | Connection pin for battery 3's negative voltage,<br>Connection pin for battery 4's positive voltage |
| 5 | VC2 | Connection pin for battery 2's negative voltage,<br>Connection pin for battery 3's positive voltage |
| 6 | VC1 | Connection pin for battery 1's negative voltage,<br>Connection pin for battery 2's positive voltage |
| 7 | SENSE | Connection pin for battery 1's positive voltage |
| 8 | VCC | Input pin for positive power supply |

8-Pin MSOP
Top view

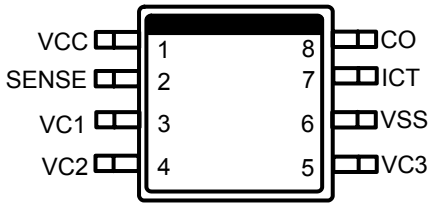



**Figure 3**

**Table 5**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VCC | Input pin for positive power supply |
| 2 | SENSE | Connection pin for battery 1's positive voltage |
| 3 | VC1 | Connection pin for battery 1's negative voltage,<br>Connection pin for battery 2's positive voltage |
| 4 | VC2 | Connection pin for battery 2's negative voltage,<br>Connection pin for battery 3's positive voltage |
| 5 | VC3 | Connection pin for battery 3's negative voltage,<br>Connection pin for battery 4's positive voltage |
| 6 | VSS | Input pin for negative power supply,<br>Connection pin for battery 4's negative voltage |
| 7 | ICT | Capacitor connection pin for overcharge detection delay |
| 8 | CO | FET gate connection pin for charge control |

TMSOP-8
Top view

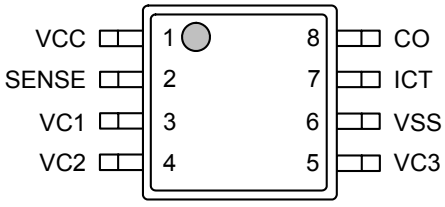



**Figure 4**

**Table 6**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | VCC | Input pin for positive power supply |
| 2 | SENSE | Connection pin for battery 1's positive voltage |
| 3 | VC1 | Connection pin for battery 1's negative voltage,<br>Connection pin for battery 2's positive voltage |
| 4 | VC2 | Connection pin for battery 2's negative voltage,<br>Connection pin for battery 3's positive voltage |
| 5 | VC3 | Connection pin for battery 3's negative voltage,<br>Connection pin for battery 4's positive voltage |
| 6 | VSS | Input pin for negative power supply,<br>Connection pin for battery 4's negative voltage |
| 7 | ICT | Capacitor connection pin for overcharge detection delay |
| 8 | CO | FET gate connection pin for charge control |

## ■ Absolute Maximum Ratings

**Table 7**

(Ta = 25°C unless otherwise specified)

| Item | | Symbol | Applied pin | Absolute maximum rating | Unit |
|---|---|---|---|---|---|
| Input voltage between VCC and VSS | | $V_{DS}$ | VCC | $V_{SS}$−0.3 to $V_{SS}$ +26 | V |
| Delay capacitor connection pin voltage | | $V_{ICT}$ | ICT | $V_{SS}$ −0.3 to $V_{CC}$ +0.3 | V |
| Input pin voltage | | $V_{IN}$ | SENSE, VC1, VC2, VC3 | $V_{SS}$ −0.3 to $V_{CC}$ +0.3 | V |
| CO output pin voltage | (CMOS output) | $V_{CO}$ | CO | $V_{SS}$ −0.3 to $V_{CC}$ +0.3 | V |
| | (Nch open drain output) | | | $V_{SS}$ −0.3 to 26 | V |
| | (Pch open drain output) | | | $V_{CC}$ −26 to $V_{CC}$ +0.3 | V |
| Power dissipation | SNT-8A | $P_D$ | — | 450[*1] | mW |
| | 8-Pin MSOP | | | 500[*1] | mW |
| | TMSOP-8 | | | 650[*1] | mW |
| Operating ambient temperature | | $T_{opr}$ | — | −40 to +85 | °C |
| Storage temperature | | $T_{stg}$ | — | −40 to +125 | °C |

***1.** When mounted on board

**[Mounted board]**

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Name : JEDEC STANDARD51-7

**Caution** **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

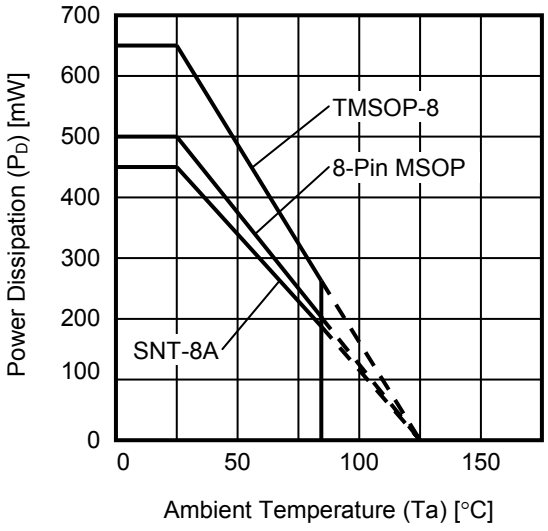



**Figure 5 Power Dissipation of Package (When Mounted on Board)**

## ■ Electrical Characteristics

**Table 8**

(Ta = 25 °C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test condition | Test circuit |
|---|---|---|---|---|---|---|---|---|
| **DETECTION VOLTAGE** | | | | | | | | |
| Overcharge detection voltage 1 *1 | $V_{CU1}$ | 3.7 V to 4.55 V Adjustment | $V_{CU1}$ −0.025 | $V_{CU1}$ | $V_{CU1}$ +0.025 | V | 1 | 1 |
| Overcharge detection voltage 2 *1 | $V_{CU2}$ | 3.7 V to 4.55 V Adjustment | $V_{CU2}$ −0.025 | $V_{CU2}$ | $V_{CU2}$ +0.025 | V | 2 | 1 |
| Overcharge detection voltage 3 *1 | $V_{CU3}$ | 3.7 V to 4.55 V Adjustment | $V_{CU3}$ −0.025 | $V_{CU3}$ | $V_{CU3}$ +0.025 | V | 3 | 1 |
| Overcharge detection voltage 4 *1 | $V_{CU4}$ | 3.7 V to 4.55 V Adjustment | $V_{CU4}$ −0.025 | $V_{CU4}$ | $V_{CU4}$ +0.025 | V | 4 | 1 |
| Overcharge hysteresis voltage 1 *2 | $V_{CD1}$ | — | 0.28 | 0.38 | 0.48 | V | 1 | 1 |
| Overcharge hysteresis voltage 2 *2 | $V_{CD2}$ | — | 0.28 | 0.38 | 0.48 | V | 2 | 1 |
| Overcharge hysteresis voltage 3 *2 | $V_{CD3}$ | — | 0.28 | 0.38 | 0.48 | V | 3 | 1 |
| Overcharge hysteresis voltage 4 *2 | $V_{CD4}$ | — | 0.28 | 0.38 | 0.48 | V | 4 | 1 |
| Detection voltage temperature coefficient *3 | $T_{COE}$ | Ta = −40°C to +85°C*4 | −0.4 | 0.0 | +0.4 | mV/°C | — | — |
| **DELAY TIME** | | | | | | | | |
| Overcharge detection delay time | $t_{CU}$ | C = 0.1 µF | 1.0 | 1.5 | 2.0 | s | 5 | 2 |
| **OPERATING VOLTAGE** | | | | | | | | |
| Operating voltage between VCC and VSS *5 | $V_{DSOP}$ | — | 3.6 | — | 24 | V | — | — |
| **CURRENT CONSUMPTION** | | | | | | | | |
| Current consumption during normal operation | $I_{OPE}$ | V1 = V2 = V3 = V4 = 3.5 V | — | 1.5 | 3.0 | µA | 6 | 3 |
| Current consumption at power down | $I_{PDN}$ | V1 = V2 = V3 = V4 = 2.3 V | — | 1.2 | 2.4 | µA | 6 | 3 |
| VC1 sink current | $I_{VC1}$ | V1 = V2 = V3 = V4 = 3.5 V | −0.3 | — | 0.3 | µA | 6 | 3 |
| VC2 sink current | $I_{VC2}$ | V1 = V2 = V3 = V4 = 3.5 V | −0.3 | — | 0.3 | µA | 6 | 3 |
| VC3 sink current | $I_{VC3}$ | V1 = V2 = V3 = V4 = 3.5 V | −0.3 | — | 0.3 | µA | 6 | 3 |
| **OUTPUT VOLTAGE*6** | | | | | | | | |
| CO “H” voltage | $V_{CO(H)}$ | at $I_{OUT}$ = 10 µA | $V_{CC}$ −0.05 | — | — | V | 7 | 4 |
| CO “L” voltage | $V_{CO(L)}$ | at $I_{OUT}$ = 10 µA | — | — | $V_{SS}$ +0.05 | V | 7 | 4 |

***1.** ± 50 mV when Ta = −40°C to +85°C.
***2.** 0.25 ± 0.07 V, 0.13 ± 0.04 V, 0.045 ± 0.02 V except for 0.38 V hysteresis models.
***3.** Overcharge detection voltage or overcharge hysteresis voltage.
***4.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.
***5.** After detecting the overcharge, the delay circuit operates normally in the range of operating voltage.
***6.** Output logic and CMOS or open drain output can be selected.

## ■ Test Circuits

### (1) Test Condition 1, Test Circuit 1

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active “H”, Nch open drain output active “H”

  The overcharge detection voltage 1 ($V_{CU1}$) is a voltage at V1; when the CO pin’s voltage is set to “H” by increasing V1 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V1’s voltage to set CO = “L”, and the difference of this V1’s voltage and $V_{CU1}$ is the overcharge hysteresis voltage 1 ($V_{CD1}$).

- Product with CMOS output active “L”, Nch open drain output active “L”, Pch open drain output active “L”

  The overcharge detection voltage 1 ($V_{CU1}$) is a voltage at V1; when the CO pin’s voltage is set to “L” by increasing V1 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V1’s voltage to set CO = “H”, and the difference of this V1’s voltage and $V_{CU1}$ is the overcharge hysteresis voltage 1 ($V_{CD1}$).

### (2) Test Condition 2, Test Circuit 1

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active “H”, Nch open drain output active “H”

  The overcharge detection voltage 2 ($V_{CU2}$) is a voltage at V2; when the CO pin’s voltage is set to “H” by increasing V2 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V2’s voltage to set CO = “L”, and the difference of this V2’s voltage and $V_{CU2}$ is the overcharge hysteresis voltage 2 ($V_{CD2}$).

- Product with CMOS output active “L”, Nch open drain output active “L”, Pch open drain output active “L”

  The overcharge detection voltage 2 ($V_{CU2}$) is a voltage at V2; when the CO pin’s voltage is set to “L” by increasing V2 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V2’s voltage to set CO = “H”, and the difference of this V2’s voltage and $V_{CU2}$ is the overcharge hysteresis voltage 2 ($V_{CD2}$).

### (3) Test Condition 3, Test Circuit 1

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active “H”, Nch open drain output active “H”

  The overcharge detection voltage 3 ($V_{CU3}$) is a voltage at V3; when the CO pin’s voltage is set to “H” by increasing V3 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V3’s voltage to set CO = “L”, and the difference of this V3’s voltage and $V_{CU3}$ is the overcharge hysteresis voltage 3 ($V_{CD3}$).

- Product with CMOS output active “L”, Nch open drain output active “L”, Pch open drain output active “L”

  The overcharge detection voltage 3 ($V_{CU3}$) is a voltage at V3; when the CO pin’s voltage is set to “L” by increasing V3 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V3’s voltage to set CO = “H”, and the difference of this V3’s voltage and $V_{CU3}$ is the overcharge hysteresis voltage 3 ($V_{CD3}$).

**(4) Test Condition 4, Test Circuit 1**

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active “H”, Nch open drain output active “H”

  The overcharge detection voltage 4 ($V_{CU4}$) is a voltage at V4; when the CO pin’s voltage is set to “H” by increasing V4 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V4’s voltage to set CO = “L”, and the difference of this V4’s voltage and $V_{CU4}$ is the overcharge hysteresis voltage 4 ($V_{CD4}$).

- Product with CMOS output active “L”, Nch open drain output active “L”, Pch open drain output active “L”

  The overcharge detection voltage 4 ($V_{CU4}$) is a voltage at V4; when the CO pin’s voltage is set to “L” by increasing V4 gradually, after setting V1 = V2 = V3 = V4 = 3.5 V. After that, gradually decreasing V4’s voltage to set CO = “H”, and the difference of this V4’s voltage and $V_{CU4}$ is the overcharge hysteresis voltage 4 ($V_{CD4}$).

**(5) Test Condition 5, Test Circuit 2**

Set switches 1 and 2 to OFF for CMOS output product.
Set switch 1 to ON and switch 2 to OFF for Nch open drain product.
Set switch 1 to OFF and switch 2 to ON for Pch open drain product.

- Product with CMOS output active “H”, Nch open drain output active “H”

  Rise V1 to 4.7 V momentarily within 10 μs after setting V1 = V2 = V3 = V4 = 3.5 V. The period from V1 having reached 4.7 V to CO = “H” is the overcharge detection delay time ($t_{CU}$).

- Product with CMOS output active “L”, Nch open drain output active “L”, Pch open drain output active “L”

  Rise V1 to 4.7 V momentarily within 10 μs after setting V1 = V2 = V3 = V4 = 3.5 V. The period from V1 having reached 4.7 V to CO = “L” is the overcharge detection delay time ($t_{CU}$).

**(6) Test Condition 6, Test Circuit 3**

Measure current consumption (I1) setting V1 = V2 = V3 = V4 = 2.3 V. This I1 is current consumption at power-down ($I_{PDN}$).
Measure current consumption (I1) setting V1 = V2 = V3 = V4 = 3.5 V. This I1 is current consumption during normal operation ($I_{OPE}$), I2 is the VC1 sink current ($I_{VC1}$), I3 is the VC2 sink current ($I_{VC2}$), I4 is the VC3 sink current ($I_{VC3}$).

### (7) Test Condition 7, Test Circuit 4

Measure setting switch 1 to OFF and switch 2 to ON.

- Product with CMOS output active “H”

  Decrease V6 from $V_{CC}$ gradually after setting V1 = V2 = V3 = V4 = 4.6 V, the V6’s voltage when flowing I2 = −10 μA is the $V_{CO(H)}$ voltage.
  Increase V6 from 0 V gradually after setting V1 = V2 = V3 = V4 = 3.5 V, the V6’s voltage when flowing I2 = 10 μA is the $V_{CO(L)}$ voltage.

- Product with CMOS output active “L”

  Decrease V6 from $V_{CC}$ gradually after setting V1 = V2 = V3 = V4 = 3.5 V, the V6’s voltage when flowing I2 = −10 μA is the $V_{CO(H)}$ voltage.
  Increase V6 from 0 V gradually after setting V1 = V2 = V3 = V4 = 4.6 V, the V6’s voltage when flowing I2 = 10 μA is the $V_{CO(L)}$ voltage.

- Product with Pch open drain output active “L”

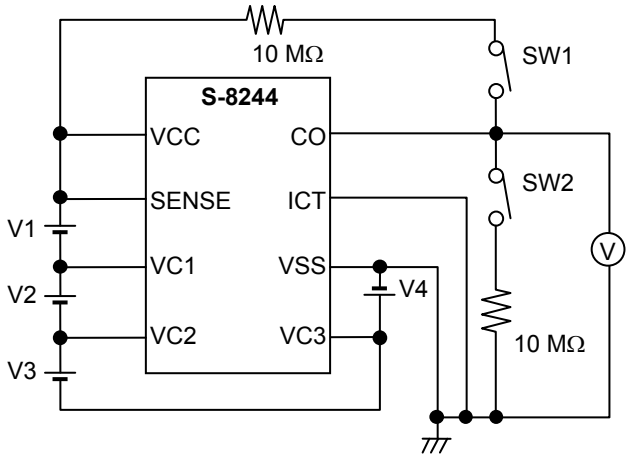
  Decrease V6 from $V_{CC}$ gradually after setting V1 = V2 = V3 = V4 = 3.5 V, the V6’s voltage when flowing I2 = −10 μA is the $V_{CO(H)}$ voltage.

- Product with Nch open drain output active “H”

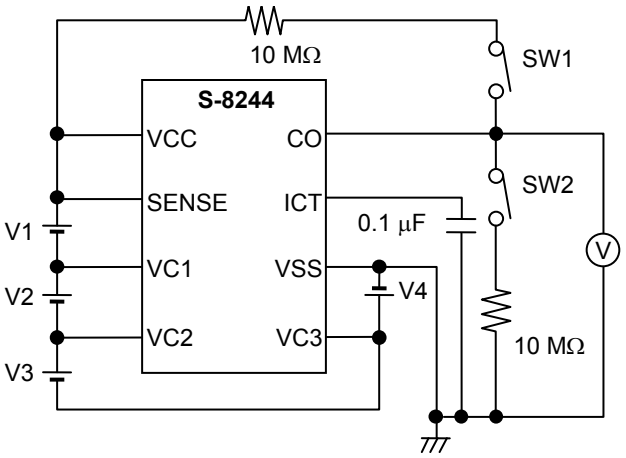
  Increase V6 from 0 V gradually after setting V1 = V2 = V3 = V4 = 3.5 V, the V6’s voltage when flowing I2 = 10 μA is the $V_{CO(L)}$ voltage.

- Product with Nch open drain output active “L”

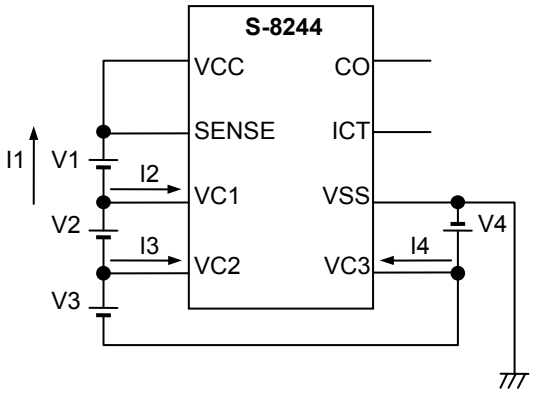
  Increase V6 from 0 V gradually after setting V1 = V2 = V3 = V4 = 4.6 V, the V6’s voltage when flowing I2 = 10 μA is the $V_{CO(L)}$ voltage.



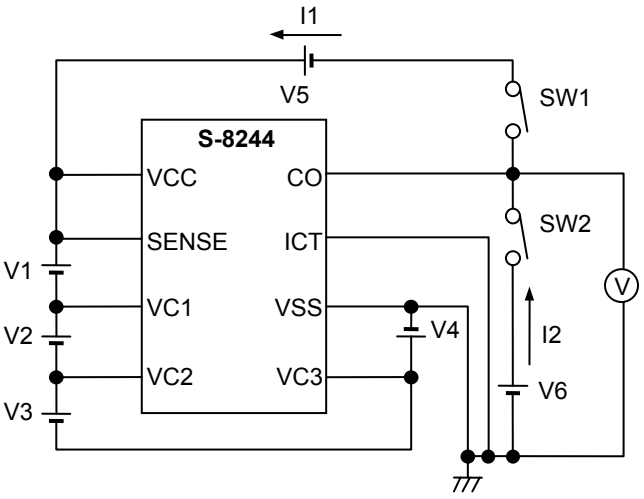

Test Circuit 1




Test Circuit 2




Test Circuit 3




Test Circuit 4

**Figure 6**

## ■ Operation

**Remark** Refer to " ■ **Battery Protection IC Connection Example**".

### 1. Overcharge Detection

- Product with CMOS output active "H", Nch open drain output active "H"

  During charging in the normal status, the voltage of one of the batteries exceeds overcharge detection voltage ($V_{CU}$), and this status is maintained for overcharge detection delay time ($t_{CU}$) or longer, CO gets "H". This is overcharge status. Connecting a FET to the CO pin enables charge-control and the second protect.
  In this case, the IC maintains the overcharge status until the voltage of each of the batteries decreases, to the overcharge hysteresis voltage ($V_{CD}$) from the overcharge detection voltage ($V_{CU}$).

- Product with CMOS output active "L", Nch open drain output active "L", Pch open drain output active "L"

  During charging in the normal status, the voltage of one of the batteries exceeds overcharge detection voltage ($V_{CU}$), and this status is maintained for overcharge detection delay time ($t_{CU}$) or longer, CO gets "L". This is overcharge status. Connecting a FET to the CO pin enables charge-control and the second protect.
  In this case, the IC maintains the overcharge status until the voltage of each of the batteries decreases, to the overcharge hysteresis voltage ($V_{CD}$) from the overcharge detection voltage ($V_{CU}$).

### 2. Delay Circuit

The delay circuit rapidly charges the capacitor connected to the delay capacitor connection pin up to a specified voltage when the voltage of one of the batteries exceeds the overcharge detection voltage ($V_{CU}$). Then, the delay circuit gradually discharges the capacitor at 100 nA and inverts the CO output when the voltage at the delay capacitor connection pin goes below a specified level. Overcharge detection delay time ($t_{CU}$) varies depending upon the external capacitor.

Each delay time is calculated using the following equation.

| | | Min. | Typ. | Max. | |
|---|---|---|---|---|---|
| $t_{CU}$[s] | = Delay Coefficient | (10, | 15, | 20) | $\times C_{ICT}$ [μF] |

Because the delay capacitor is rapidly charged, the smaller the capacitance, the larger the difference between the maximum voltage and the specified value of delay capacitor pin (ICT pin). This will cause a deviation between the calculated delay time and the resultant delay time. Also, delay time is internally set in this IC to prevent the CO output from inverting until the charge to delay capacitor pin is reached to the specified voltage. If large capacitance is used, output may be enabled without delay time because charge is disabled within the internal delay time.
Please note that the maximum capacitance connected to the delay capacitor pin (ICT pin) is 1 μF.

## ■ Timing Chart

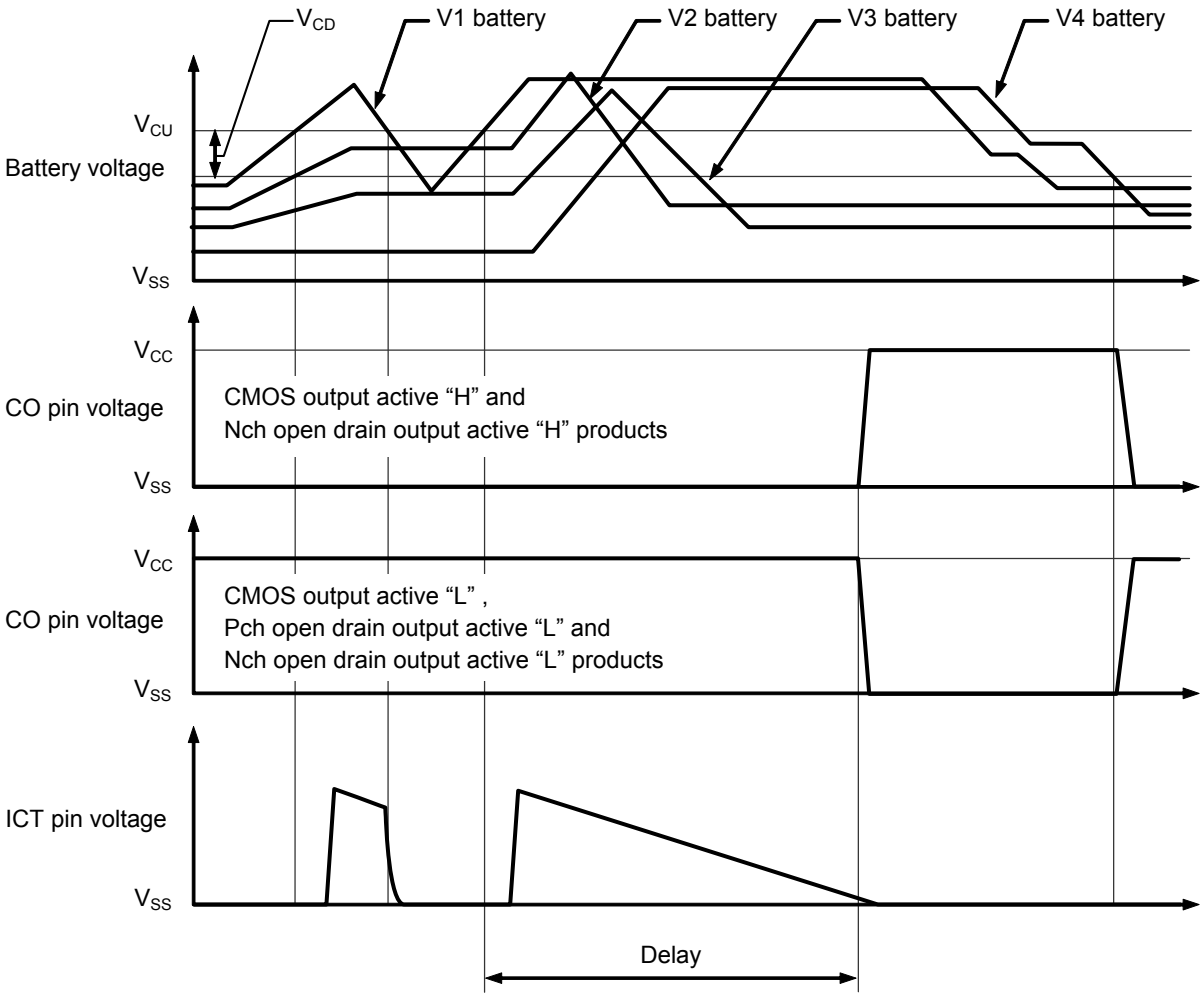



**Figure 7**

## ■ Battery Protection IC Connection Example

### (1) Connection Example 1

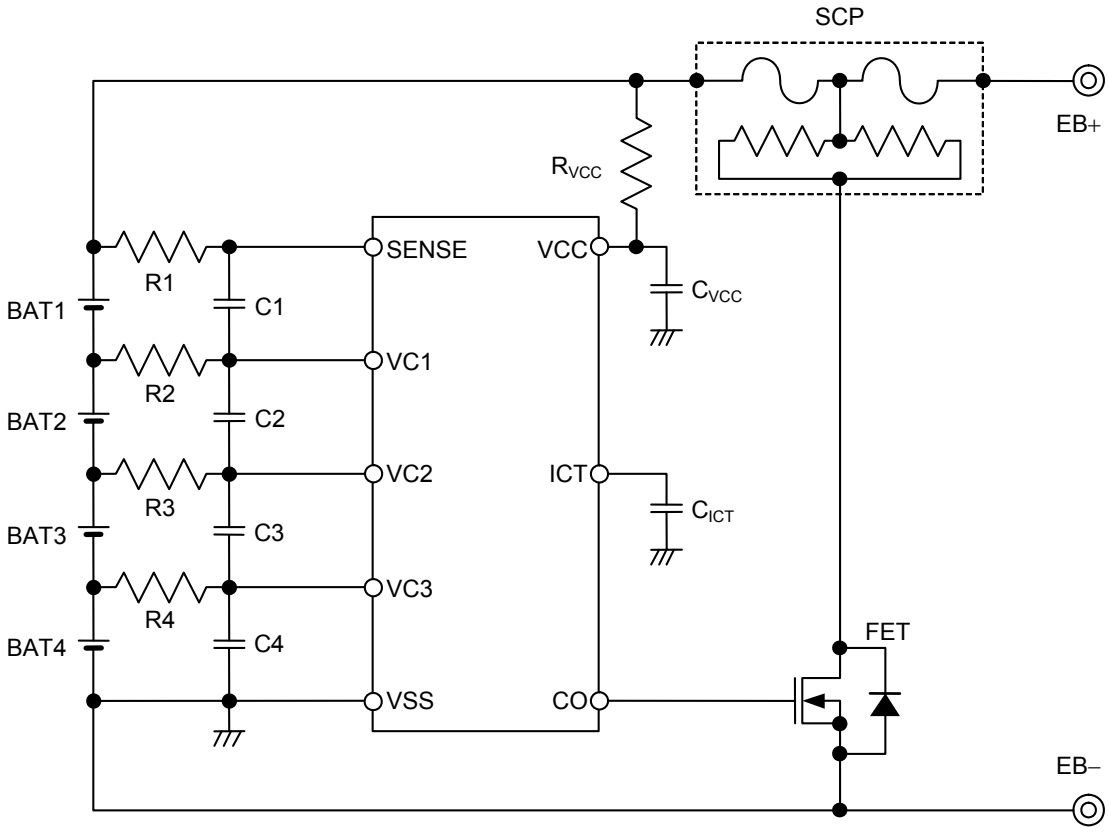



**Figure 8**

**Table 9 Constants for External Components 1**

| Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| R1 to R4 | 0 | 1 k | 10 k | Ω |
| C1 to C4 | 0 | 0.1 | 1 | μF |
| $R_{VCC}$ | 0 | 100 | 1 k | Ω |
| $C_{VCC}$ | 0 | 0.1 | 1 | μF |
| $C_{ICT}$ | 0 | 0.1 | 1 | μF |

**Caution1. The above constants may be changed without notice.**

**2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.**

**[For SCP, contact]**

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Contact Us: http://www.dexerials.jp/en/

**(2) Connection Example 2 (for 3-cells)**

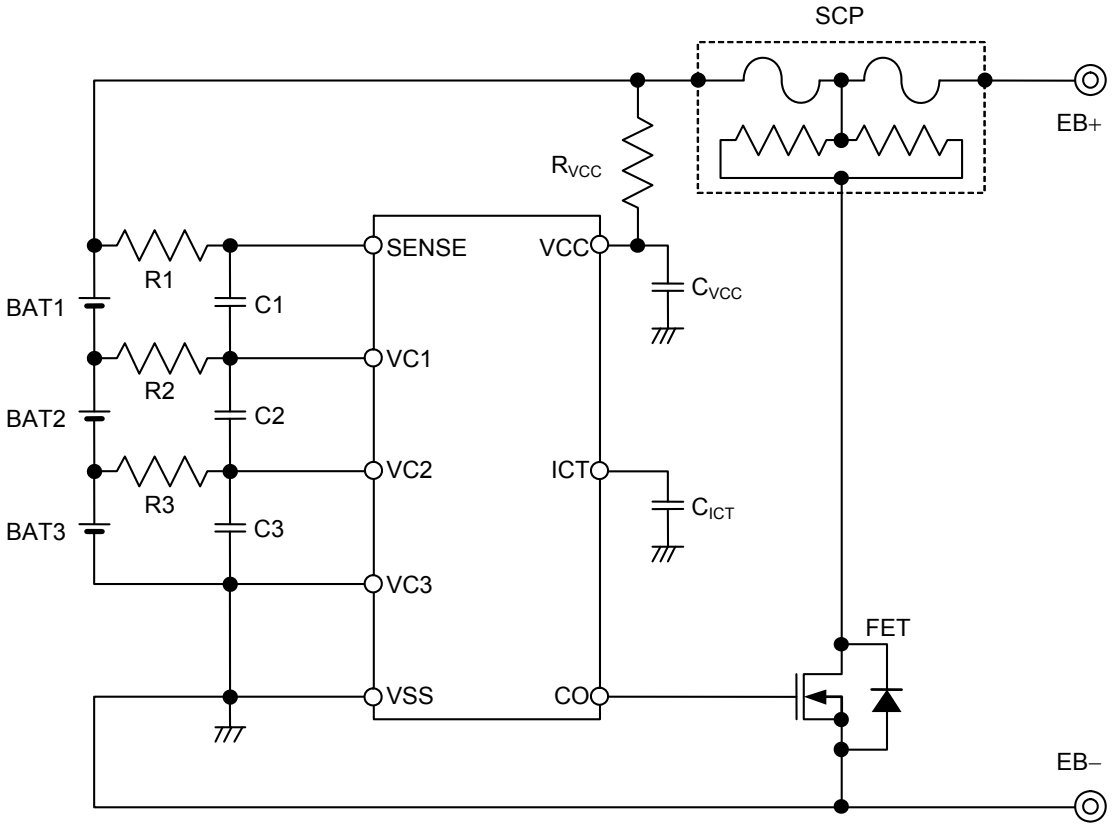



**Figure 9**

**Table 10 Constants for External Components 2**

| Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| R1 to R3 | 0 | 1 k | 10 k | Ω |
| C1 to C3 | 0 | 0.1 | 1 | μF |
| $R_{VCC}$ | 0 | 100 | 1 k | Ω |
| $C_{VCC}$ | 0 | 0.1 | 1 | μF |
| $C_{ICT}$ | 0 | 0.1 | 1 | μF |

**Caution1. The above constants may be changed without notice.**

**2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.**

### (3) Connection Example 3 (for 2-cells)

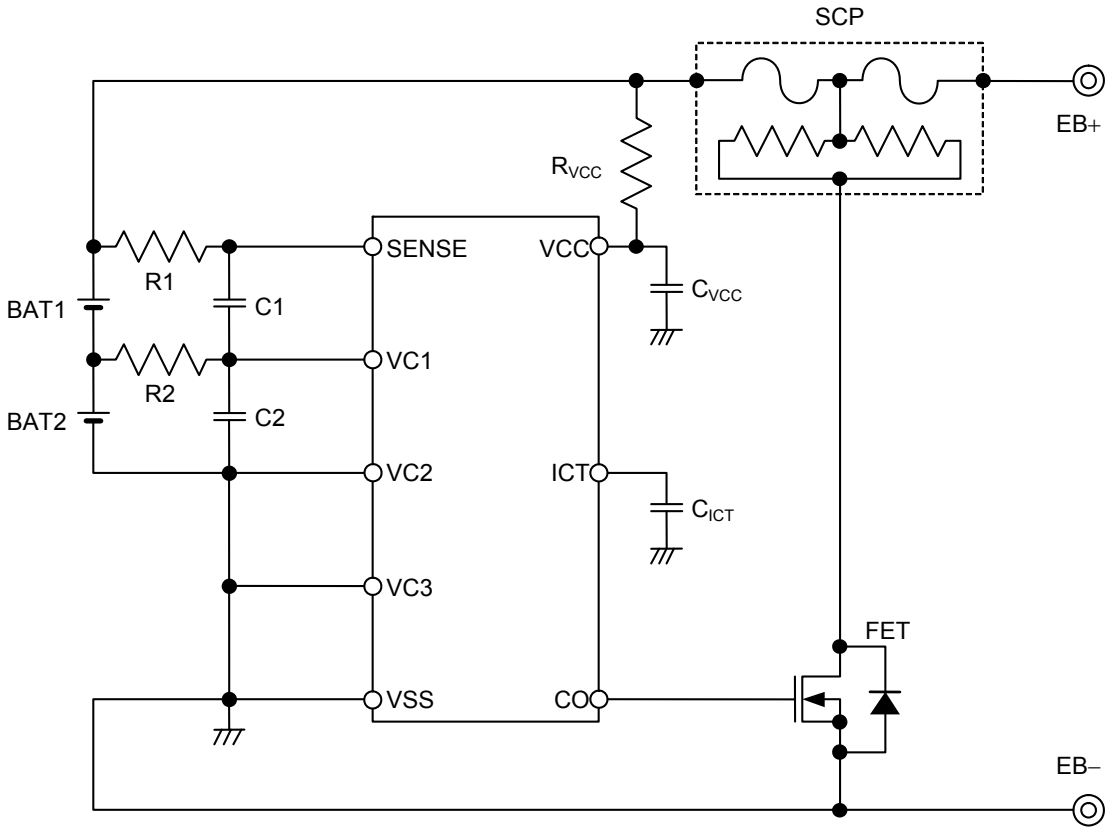



**Figure 10**

**Table 11 Constants for External Components 3**

| Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| R1, R2 | 0 | 1 k | 10 k | Ω |
| C1, C2 | 0 | 0.1 | 1 | μF |
| $R_{VCC}$ | 0 | 100 | 1 k | Ω |
| $C_{VCC}$ | 0 | 0.1 | 1 | μF |
| $C_{ICT}$ | 0 | 0.1 | 1 | μF |

**Caution1. The above constants may be changed without notice.**

**2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.**

### (4) Connection Example 4 (for 1-cell)

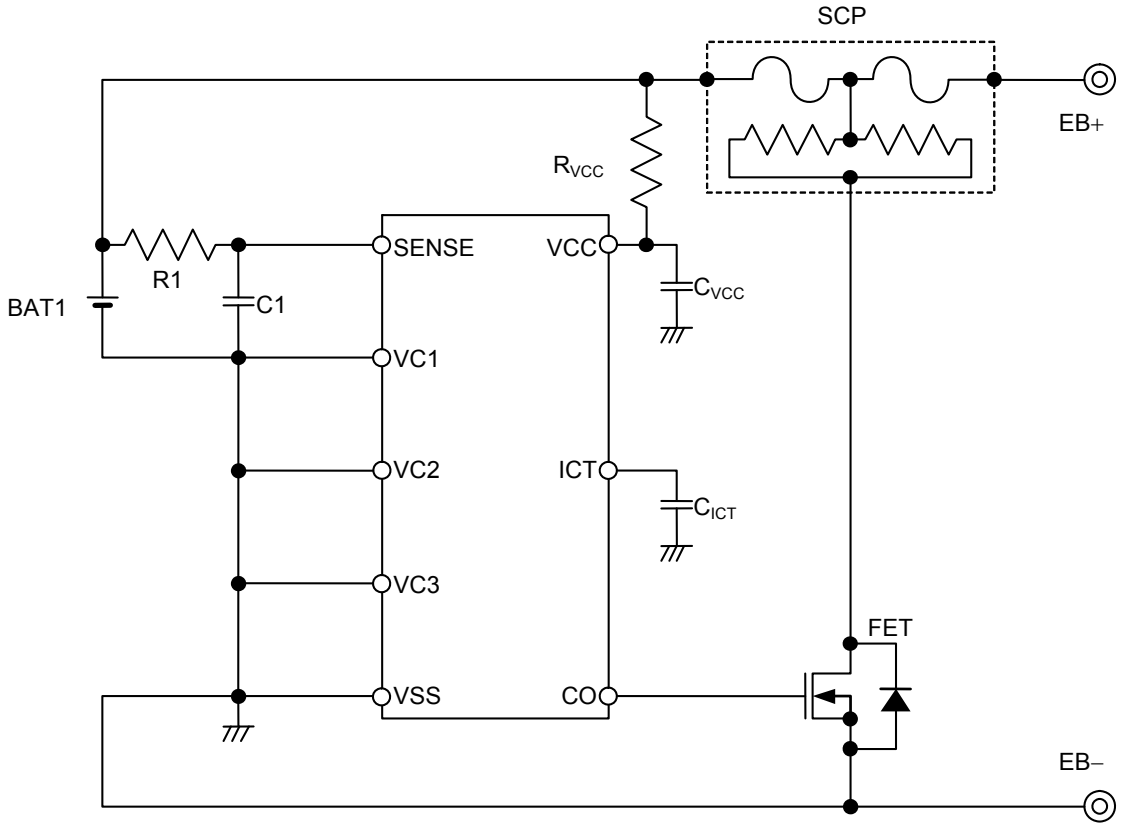



**Figure 11**

**Table 12 Constants for External Components 4**

| Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| R1 | 0 | 1 k | 10 k | Ω |
| C1 | 0 | 0.1 | 1 | μF |
| $R_{VCC}$ | 0 | 100 | 1 k | Ω |
| $C_{VCC}$ | 0 | 0.1 | 1 | μF |
| $C_{ICT}$ | 0 | 0.1 | 1 | μF |

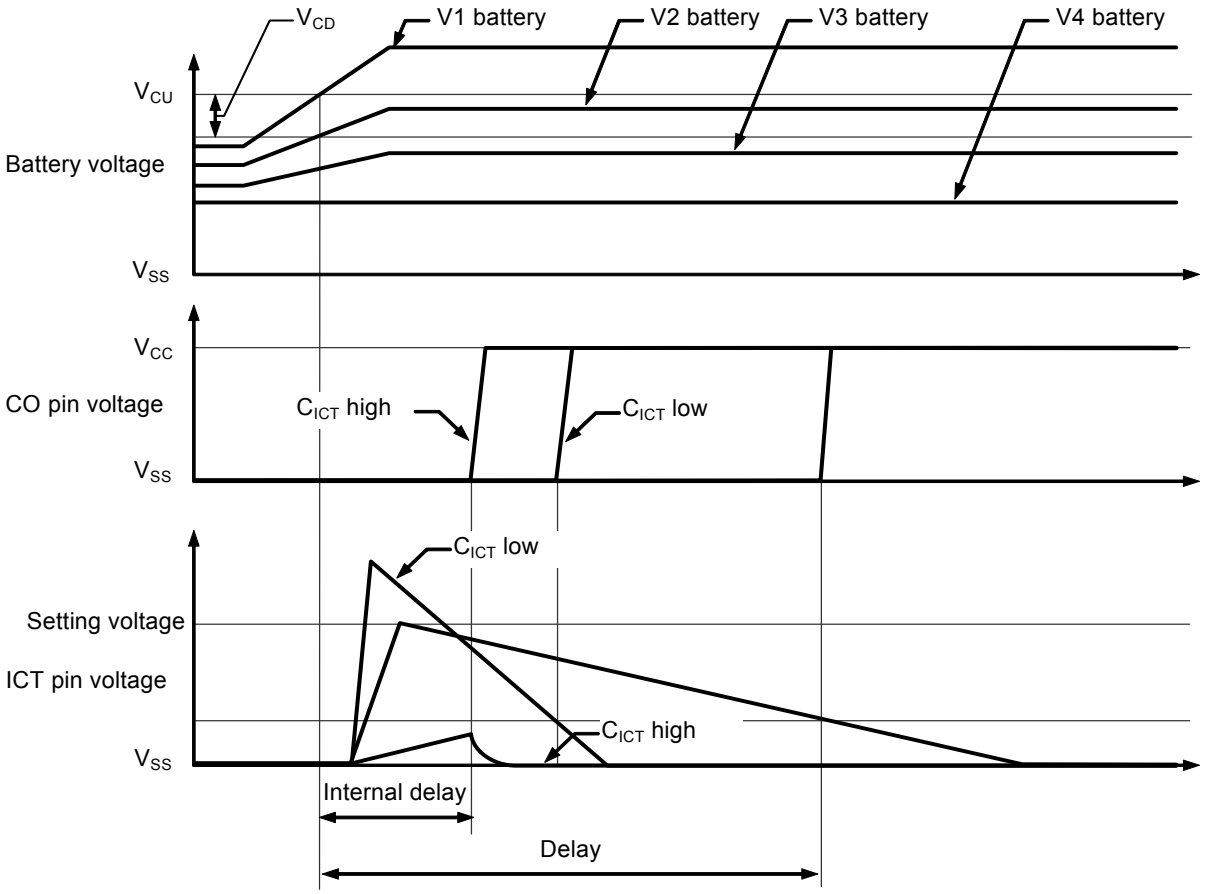
**Caution1. The above constants may be changed without notice.**

**2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Precautions

- This IC charges the delay capacitor through the delay capacitor pin (ICT pin) immediately when the voltage of one of batteries V1 to V4 reaches the overcharge voltage. Therefore, setting the resistor connected to the VCC pin to any value greater than the recommended level causes a reduction in the IC power supply voltage because of charge current of the delay capacitor. This may lead to a malfunction. Set up the resistor NOT to exceed the typical value. If you change the resistance, please consult us.
- DO not connect any of overcharged batteries. Even if only one overcharged battery is connected to this IC, the IC detects overcharge, then charge current flows to the delay capacitor through the parasitic diode between pins where the battery is not connected yet. This may lead to a malfunction. Please perform sufficient evaluation in the case of use. Depending on an application circuit, even when the fault charge battery is not contained, the connection turn of a battery may be restricted in order to prevent the output of CO detection pulse at the time of battery connection.

CMOS output active “H” and Nch open drain output active “H” products

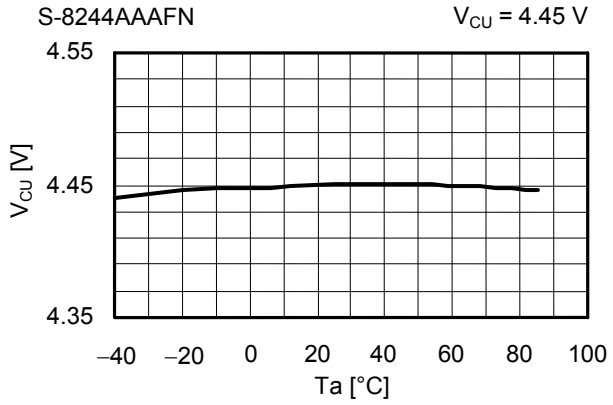



- In this IC, the output logic of the CO pin is inverted after several milliseconds of internal delay if this IC is under the overcharge condition even ICT pin is either “$V_{SS}$–short circuit,” “$V_{DD}$–short circuit” or “Open” status.
- Any position from V1 to V4 can be used when applying this IC for a one to three-cell battery. However, be sure to short circuit between pins not in use (SENSE–VC1, VC1–VC2, VC2–VC3, or VC3–VSS).
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

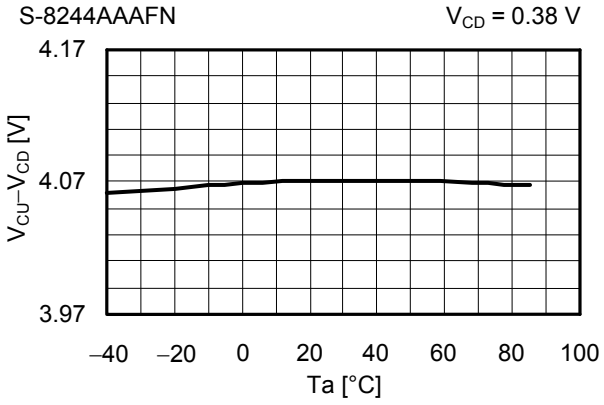
## ■ Characteristics (Typical Data)

### 1. Detection Voltage vs. Temperature

Overcharge Detection Voltage vs. Temperature

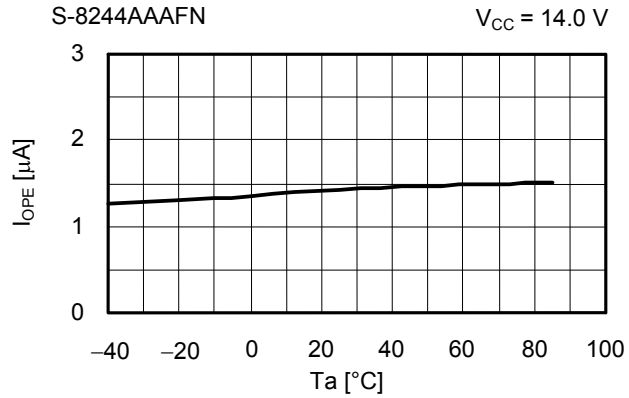



Overcharge Release Voltage vs. Temperature

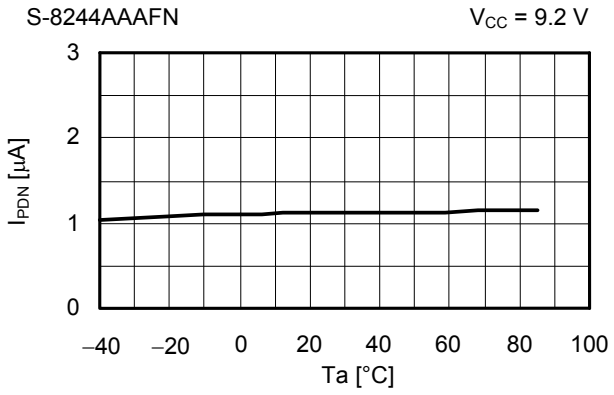



### 2. Current Consumption vs. Temperature

Current Consumption during Normal Operation vs. Temperature

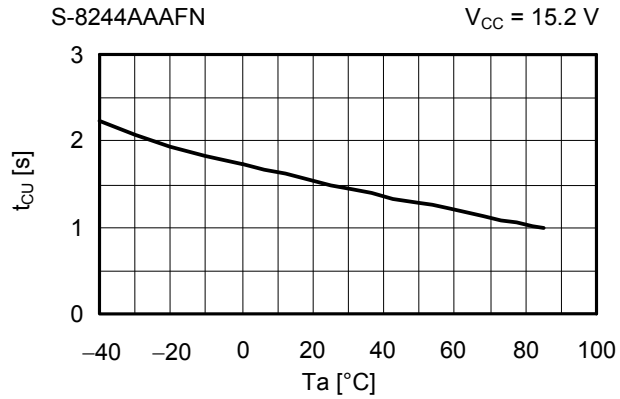



Current Consumption at Power Down vs. Temperature

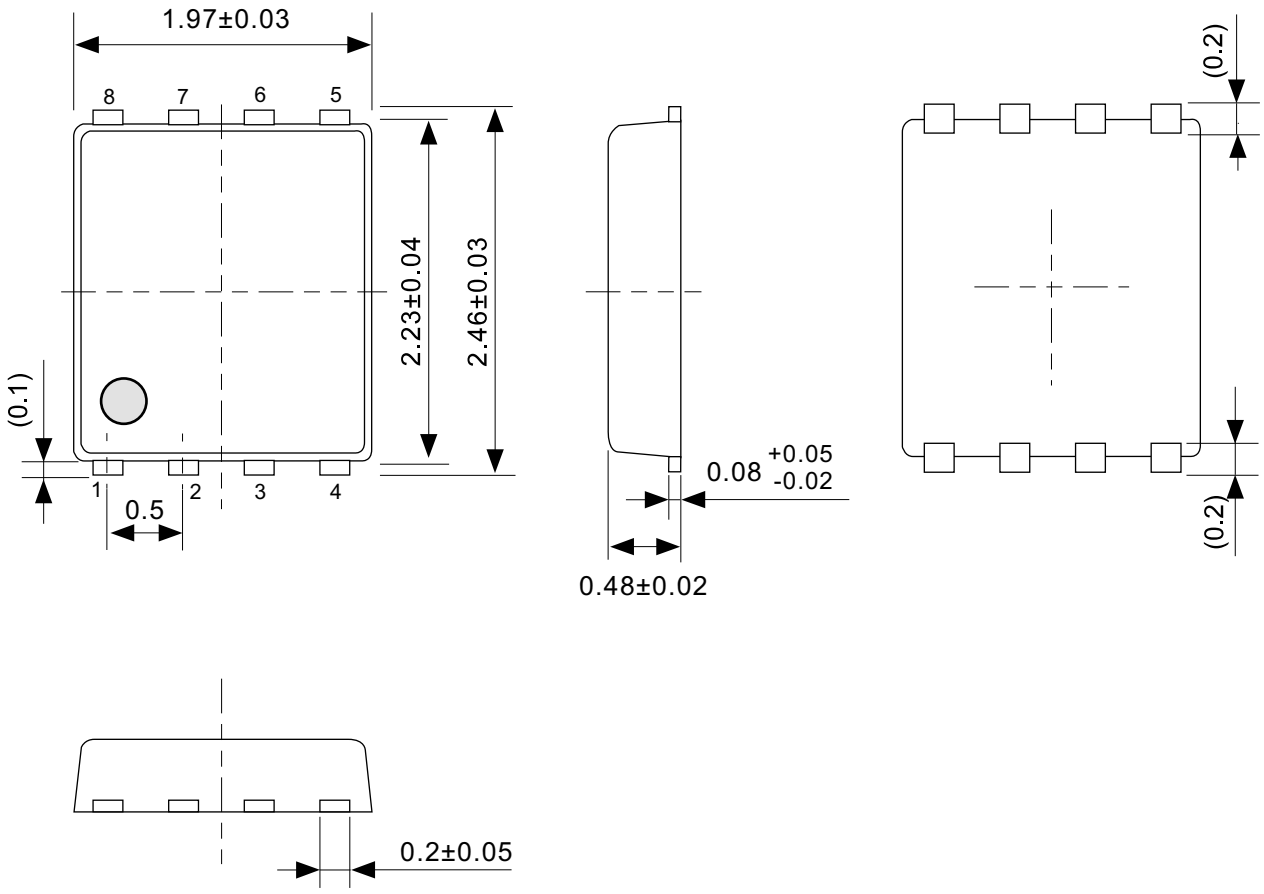



### 3. Delay Time vs. Temperature

Overcharge Detection Delay Time vs. Temperature




**Caution Please design all applications of the S-8244 Series with safety in mind.**




No. PH008-A-P-SD-2.1

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| UNIT | mm |
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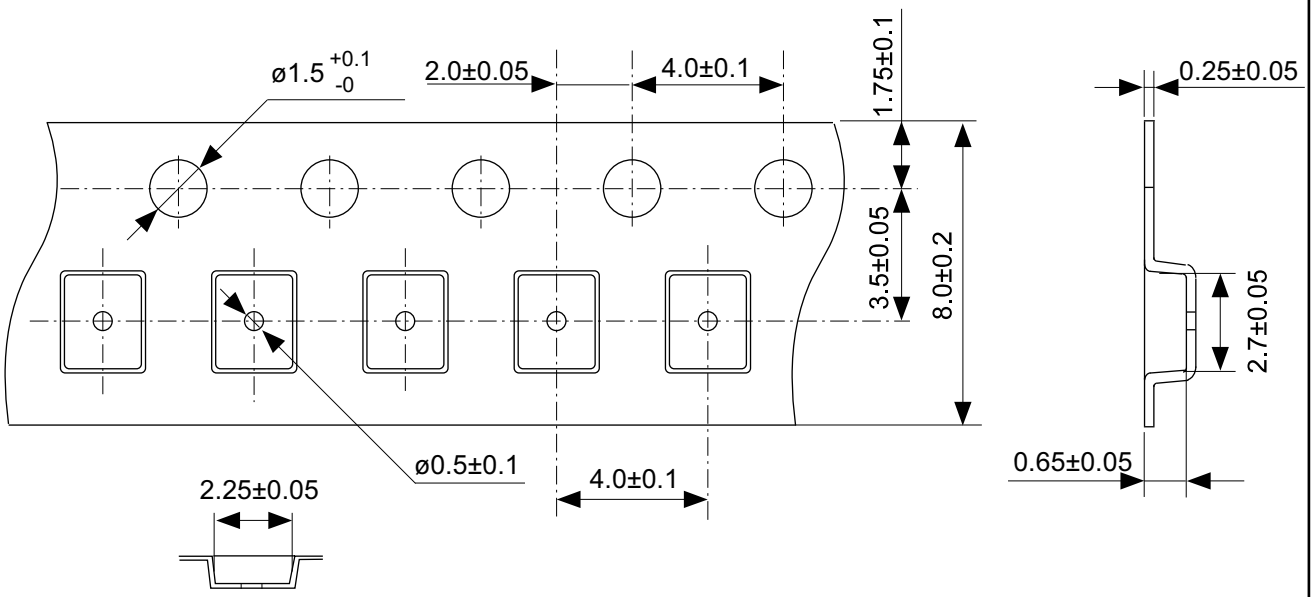
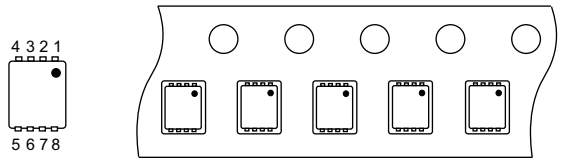
| **ABLIC Inc.** | |




Feed direction

No. PH008-A-C-SD-2.0

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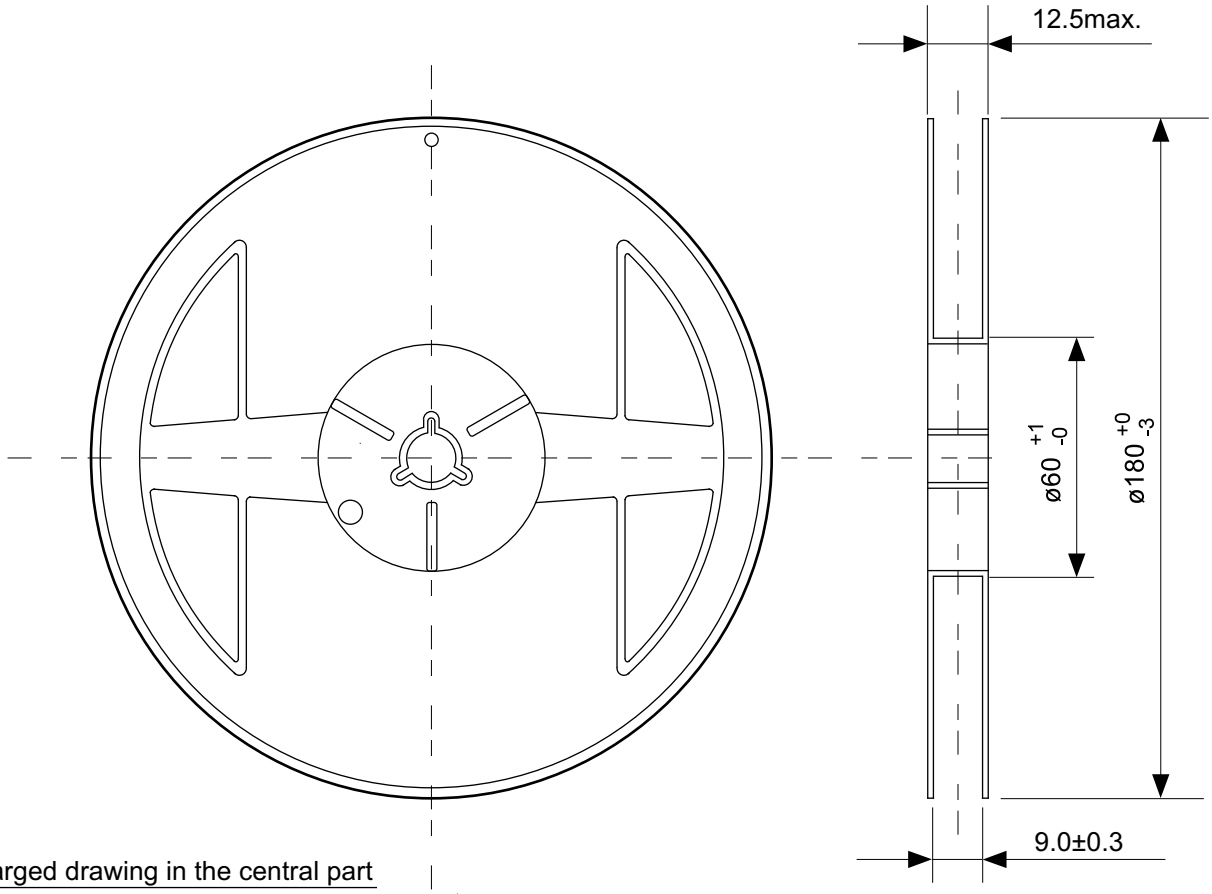
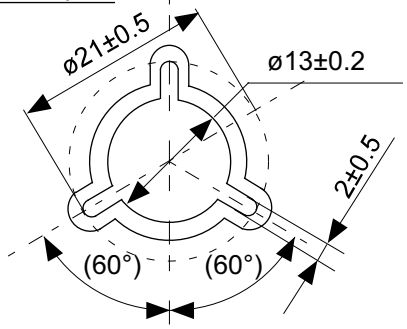



Enlarged drawing in the central part

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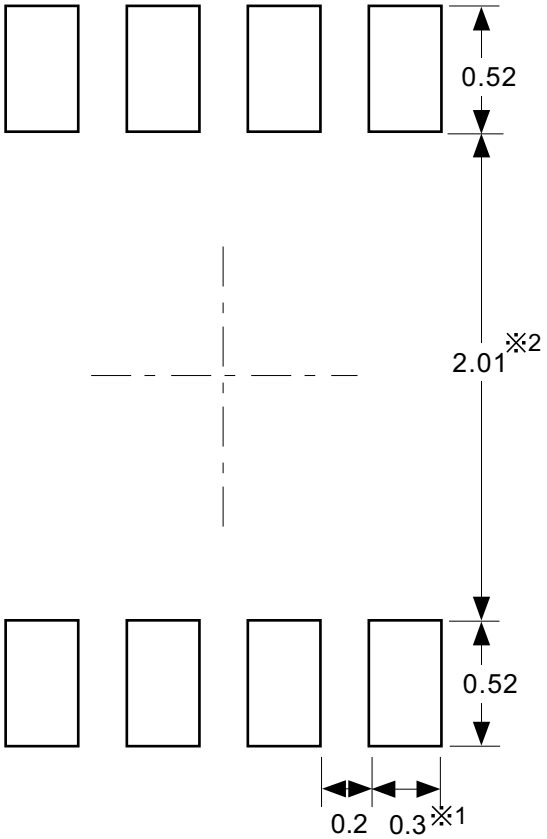


※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

**注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。**
**2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。**
**3. マスク開口サイズと開口位置はランドパターンと合わせてください。**
**4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。**

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

**Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.**
**2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.**
**3. Match the mask aperture size and aperture position with the land pattern.**
**4. Refer to "SNT Package User's Guide" for details.**

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

**注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。**
**2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。**
**3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。**
**4. 详细内容请参阅 "SNT 封装的应用指南"。**

No. PH008-A-L-SD-4.1

| | |
|---|---|
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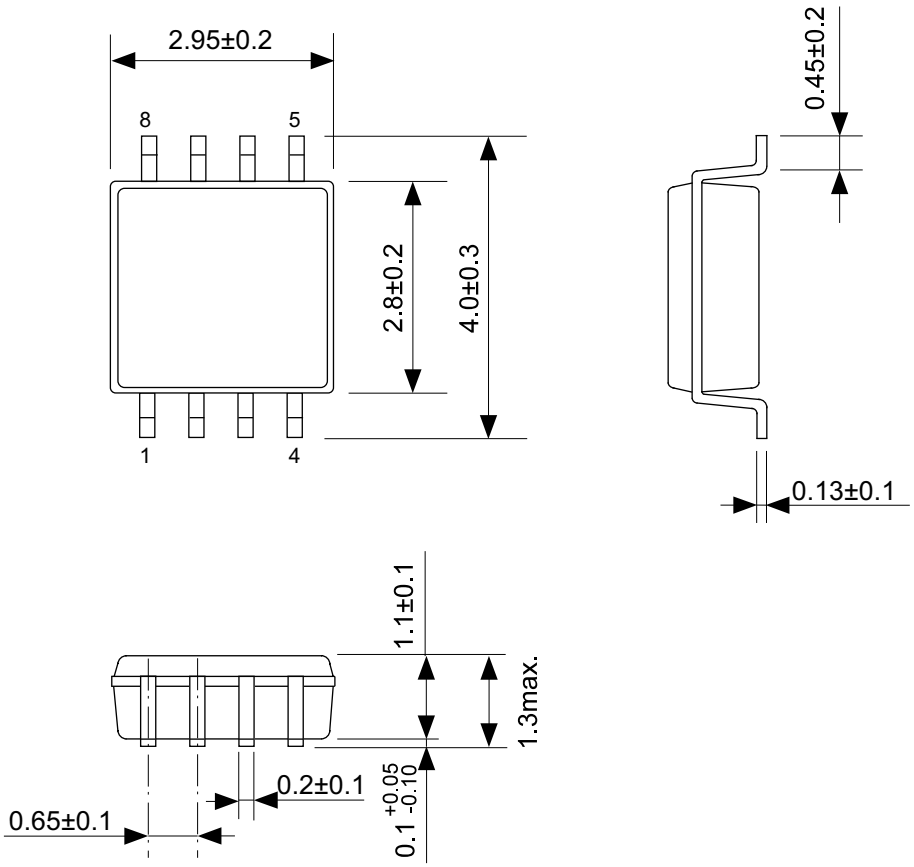


No. FN008-A-P-SD-1.2

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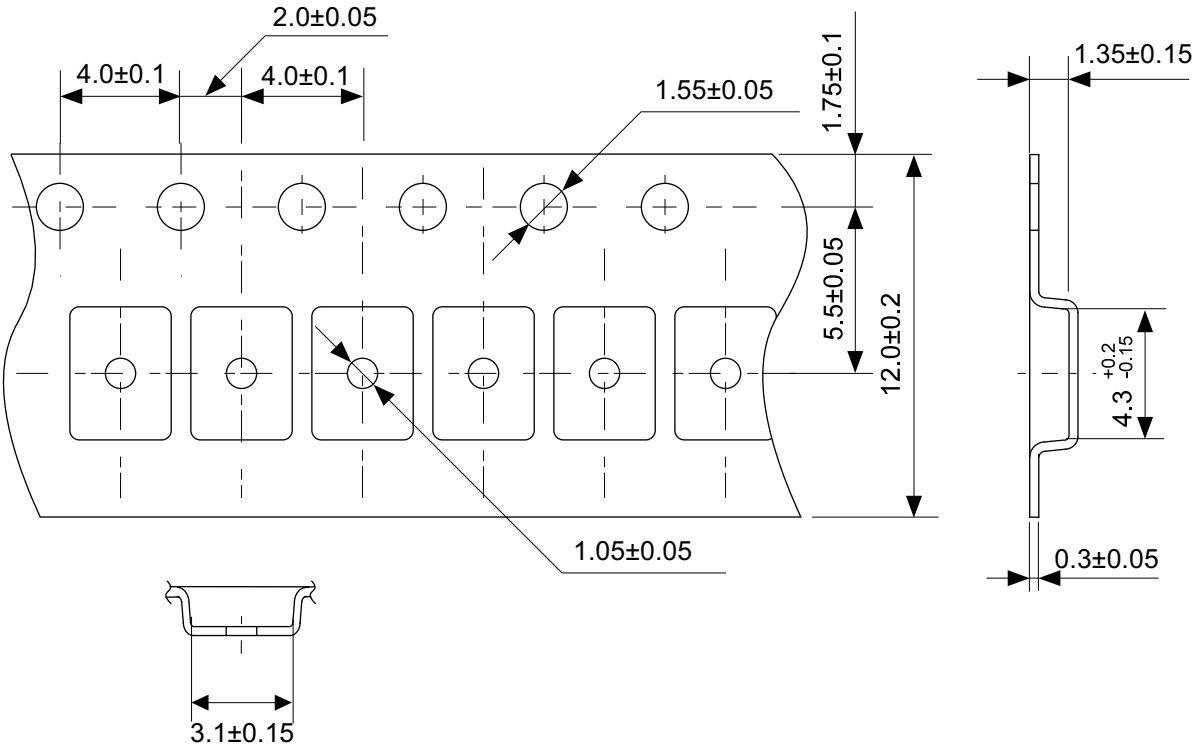
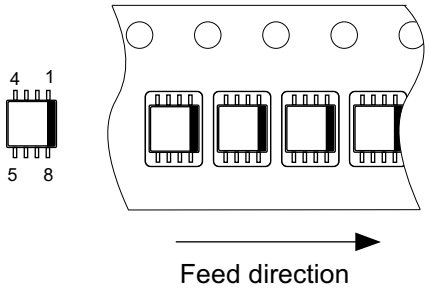
| **ABLIC Inc.** | |




No. FN008-A-C-SD-1.1

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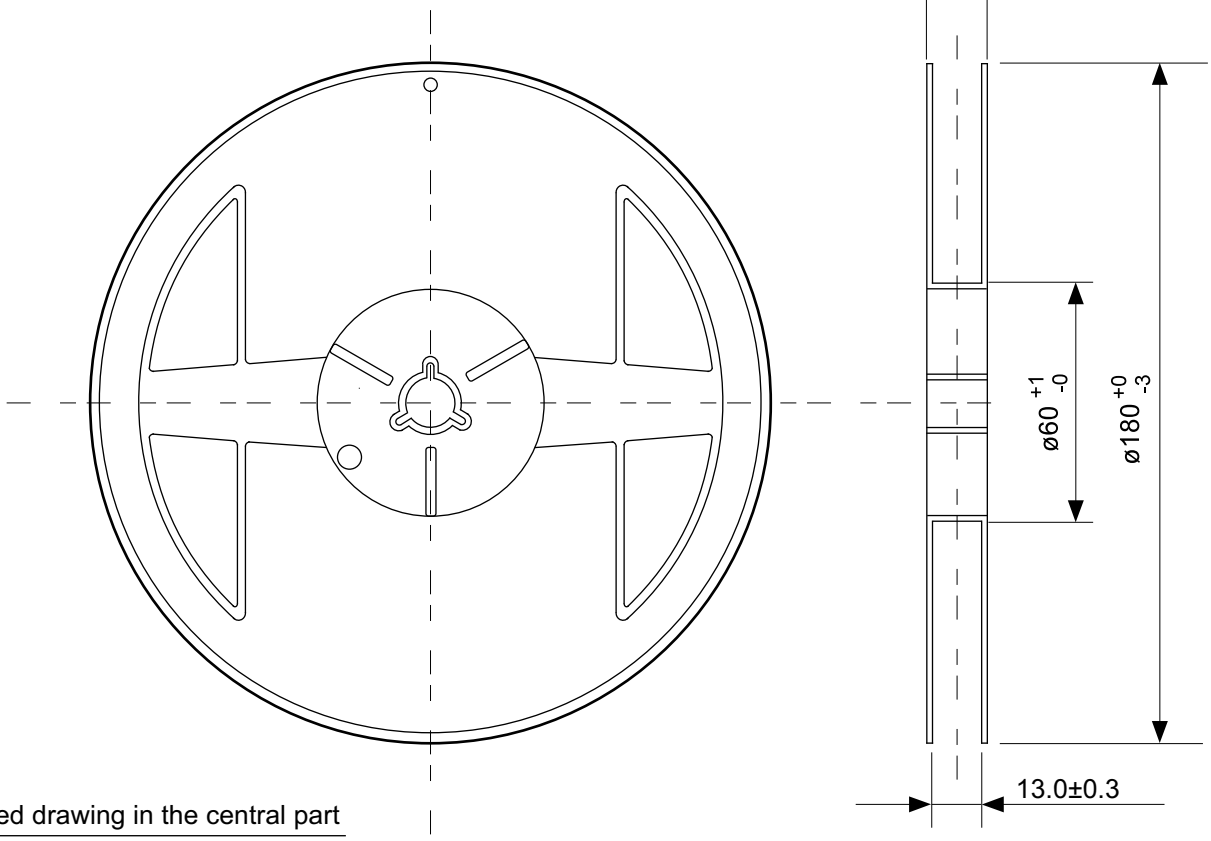
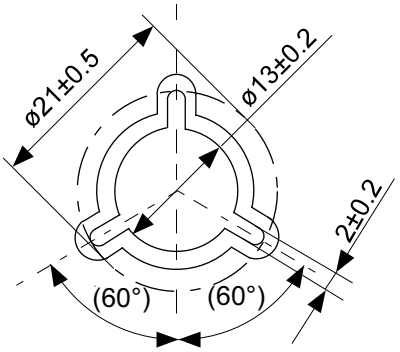
| ABLIC Inc. | |




Enlarged drawing in the central part




No. FN008-A-R-SD-1.1

| | | | |
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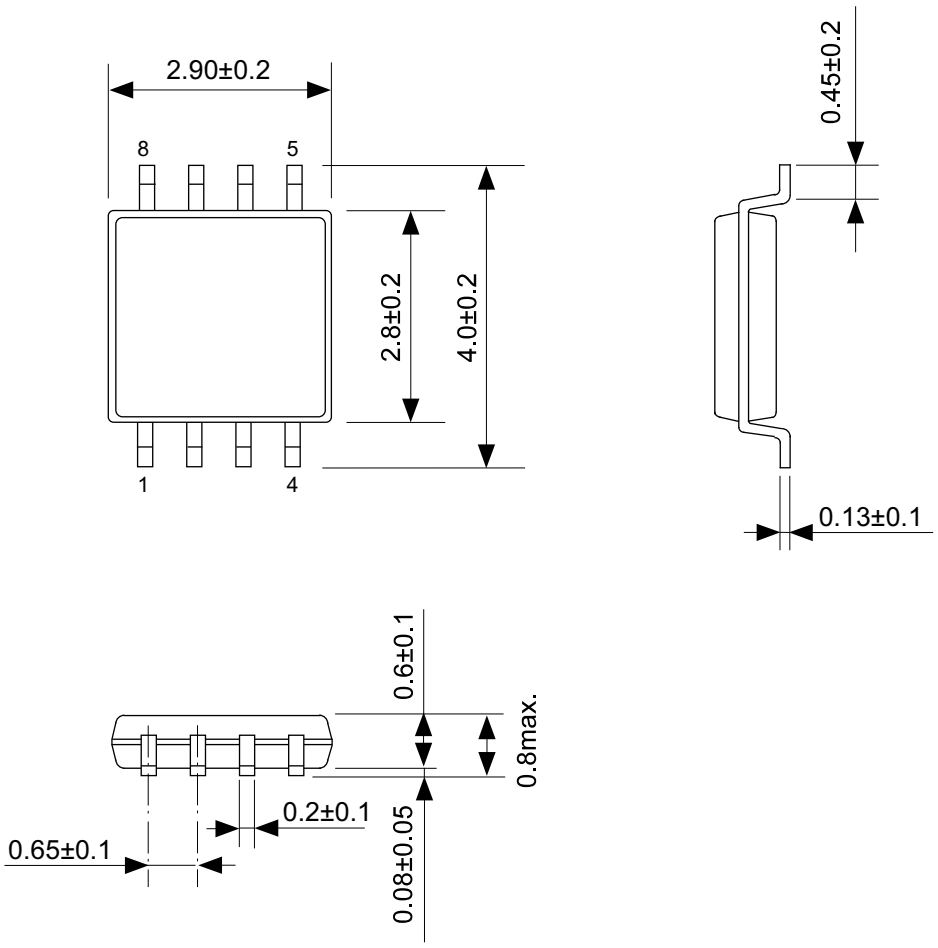
| **ABLIC Inc.** | | | |




No. FM008-A-P-SD-1.2

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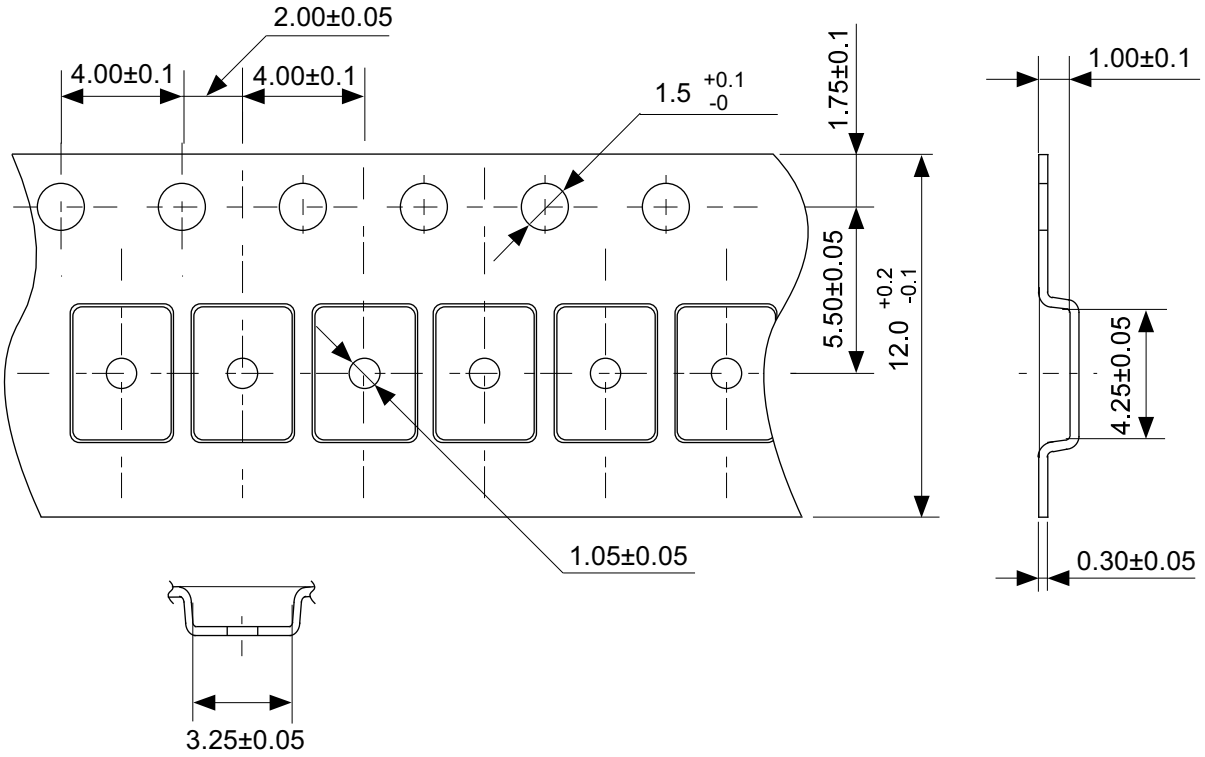
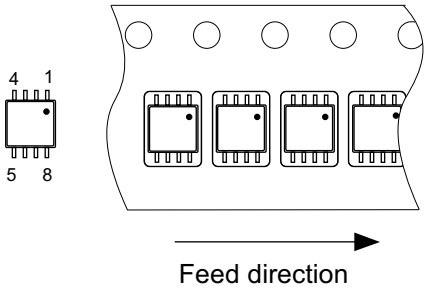
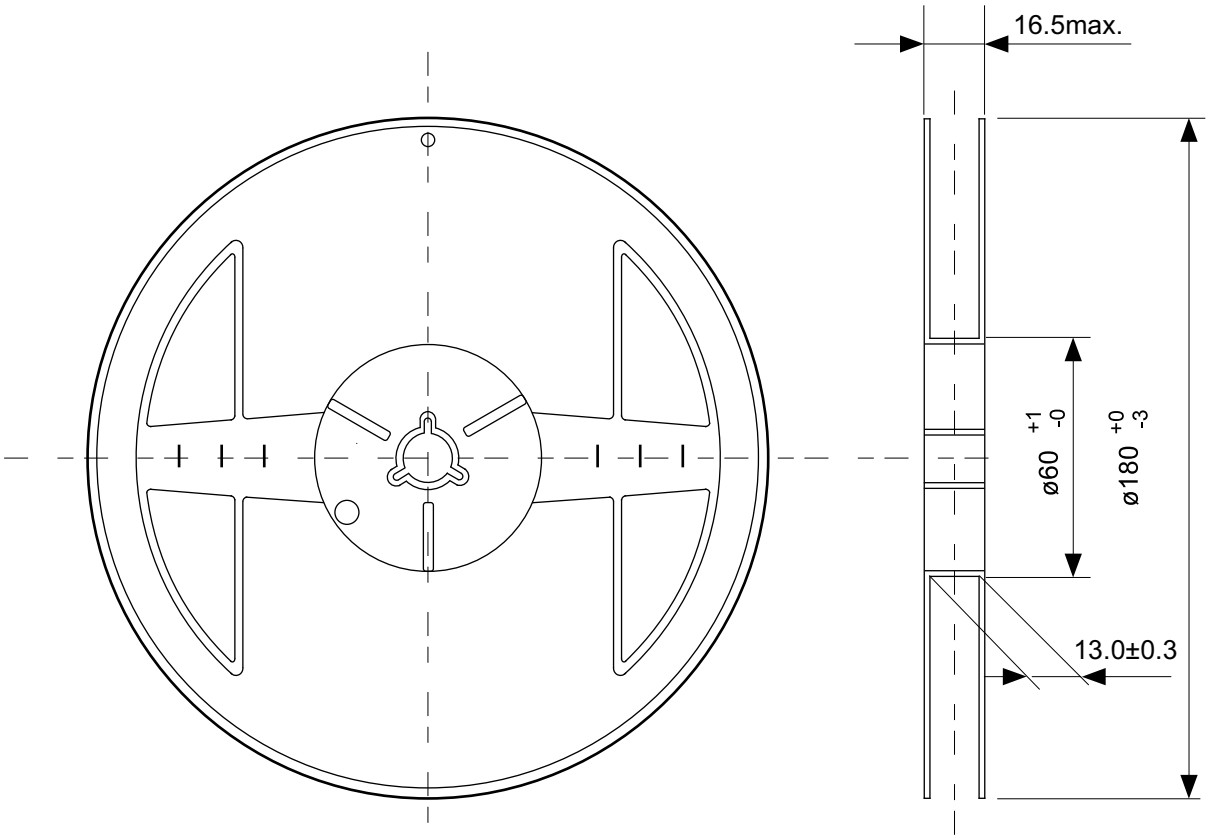
| **ABLIC Inc.** | |



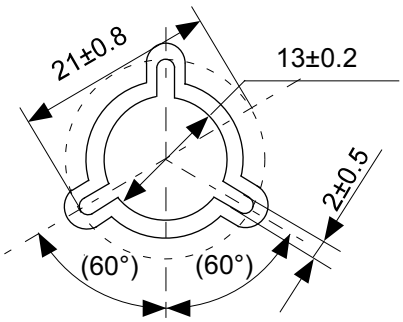




No. FM008-A-C-SD-2.0

| | |
|---|---|
| TITLE | TMSOP8-A-Carrier Tape |
| No. | FM008-A-C-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |




Enlarged drawing in the central part




No. FM008-A-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | TMSOP8-A-Reel | | |
| No. | FM008-A-R-SD-1.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

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