## GENERAL DESCRIPTION (continued)

semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

The PALCE29MA16 uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to 29 array inputs and 16 outputs. It incorporates our unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as combinatorial, registered, or latched with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the system designer to tailor the device to particular application requirements.

Increased logic power has been built into the PALCE29MA16 by providing a varied number of logic product terms per output. Of the 16 outputs, 8 outputs have 4 product terms each, 4 outputs have 8 product terms each, and the other 4 outputs have 12 product terms each. This varied product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by a common Output Enable pin or Output Enable product term. Each output can also be permanently enabled or disabled.

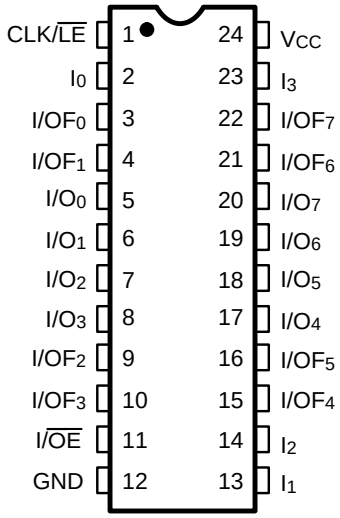
System operation has been enhanced by the addition of common asynchronous-Preset and Reset product terms and a power-up Reset feature. The PALCE29MA16 also incorporates Preload and Observability functions which permit full logic verification of the design.

The PALCE29MA16 is offered in the space-saving 300-mil SKINNYDIP package as well as the plastic leaded chip carrier package.

## CONNECTION DIAGRAMS

### Top View

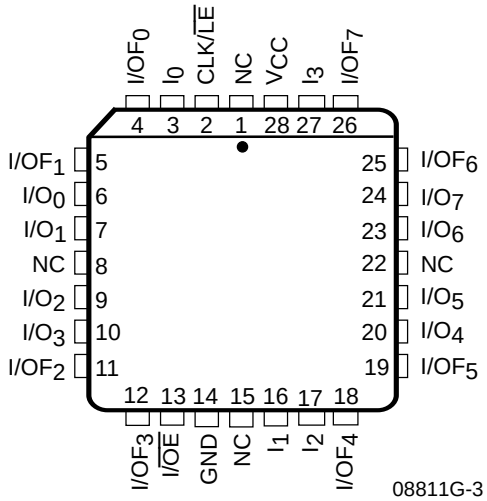
#### SKINNYDIP




08811G-2

***Note:***
*Pin 1 is marked for orientation.*

#### PLCC




08811G-3

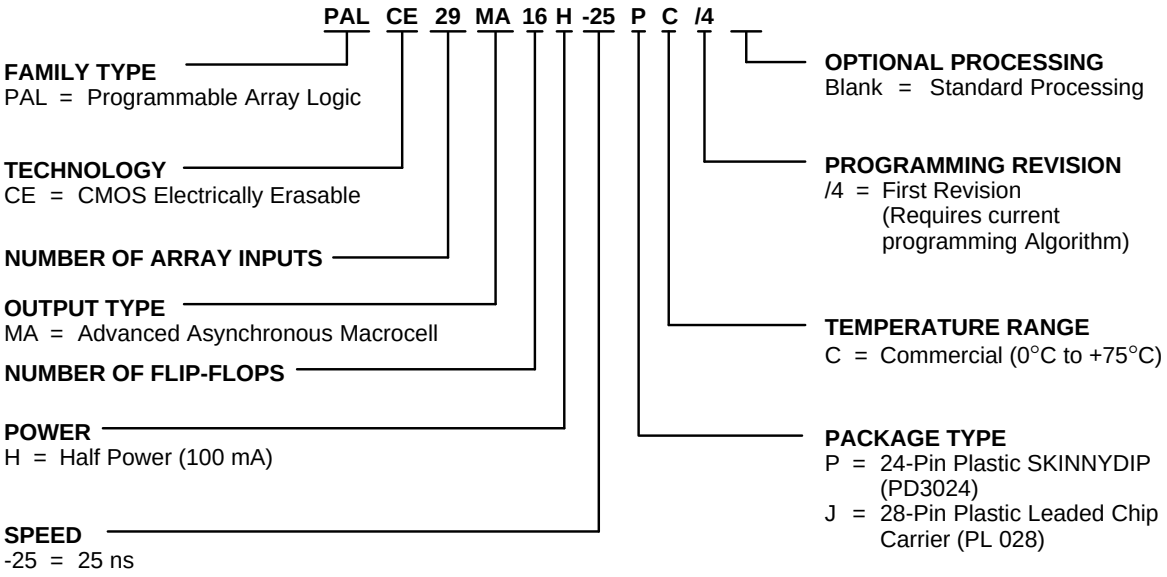
## PIN DESIGNATIONS

| | | |
|---|---|---|
| CLK/$\overline{LE}$ | = | Clock or Latch Enable |
| GND | = | Ground |
| I | = | Input |
| I/O | = | Input/Output |
| I/OF | = | Input/Output with Dual Feedback |
| $V_{CC}$ | = | Supply Voltage |
| NC | = | No Connection |

## ORDERING INFORMATION

### Commercial Products

Programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:




| Valid Combinations | | |
|---|---|---|
| PALCE29MA16H-25 | PC, JC | /4 |

**Valid Combinations**

Valid Combinations lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

## FUNCTIONAL DESCRIPTION

### Inputs

The PALCE29MA16 has 29 inputs to drive each product term (up to 58 inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram in Figure 1. Of these 29 inputs, 4 are dedicated inputs, 16 are from eight I/O logic macrocells with two feedbacks, 8 are from other I/O logic macrocells with single feedback and one is the I/$\overline{OE}$ input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE for the AND array. By selectively programming the EE cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

### Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The PALCE29MA16 has 178 product terms; 112 of these product terms provide logic capability and others are architectural product terms. Among the control product terms, one is for Observability, and one is for Preload. The Output Enable of each macrocell can be programmed to be controlled by a common Output Enable pin or an individual product term. It may also be permanently disabled. In addition, independent product terms for each macrocell control Preset, Reset and CLK/$\overline{LE}$.

Each product term on the PALCE29MA16 consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a varied distribution across the device ranging from 4 to 12 wide, with an average of 7 logic product terms per output. An increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Individual asynchronous-Preset and Reset product terms are connected to all Registered or Latched I/Os.

When the asynchronous-Preset product term is asserted (HIGH) the register or latch will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-Reset product term is asserted (HIGH) the register or latch will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the Reset, Preset, Preload, and power-up Reset modes to be meaningful.

### Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The PALCE29MA16 has 16 macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 2). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers and Latches are used in synchronous logic applications. Registers and Latches with product term controlled clocks can also be used in asychronous application.

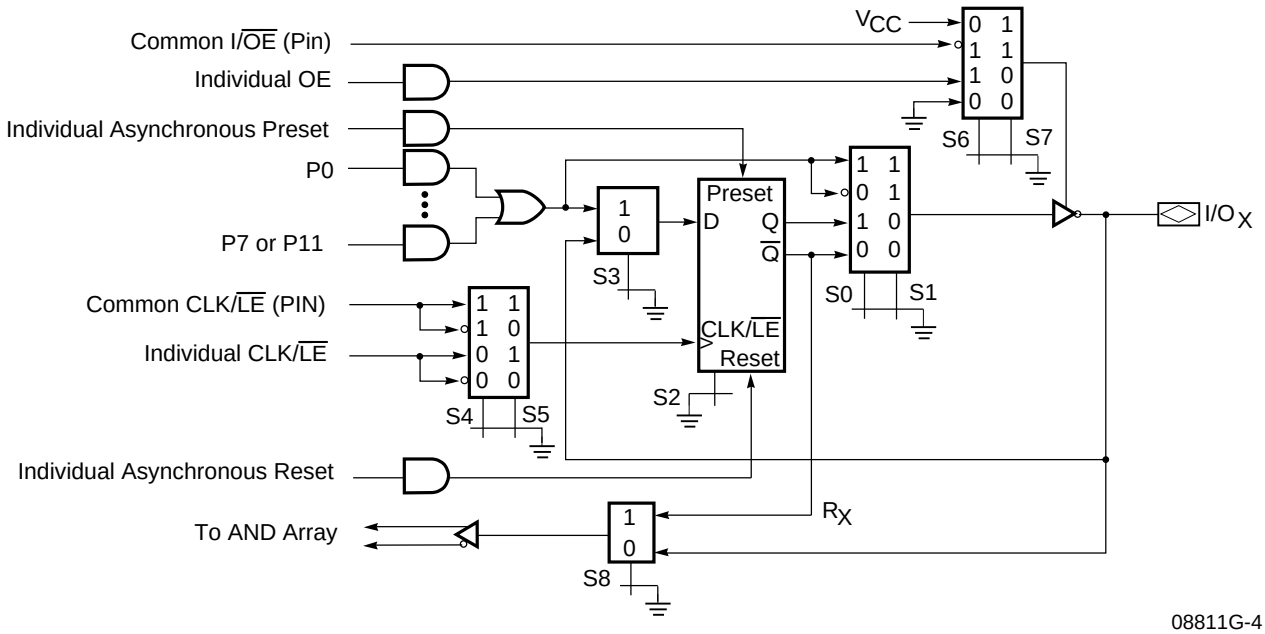



**Figure 2a. PALCE29MA16 Macrocell (Single Feedback)**

The output polarity for each macrocell in each of the three modes of operation is user-selectable, allowing complete flexibility of the macrocell configuration.

Eight of the macrocells ($I/OF_0$–$I/OF_7$) have two independent feedback paths to the AND array (see Figure 2b). The first is a dedicated I/O pin feedback to the AND array for combinatorial input. The second path consists of a direct register/latch feedback to the array. If the pin is used as a dedicated input using the first feedback path, the register/latch feedback path is still available to the AND array. This path provides the capability of using the register/latch as a buried state register/latch. The other eight macrocells have a single feedback path to the AND array. This feedback is user-selectable as either an I/O pin or a register/latch feedback (see Figure 2a).

Each macrocell can provide true input/output capability. The user can select each macrocell register/latch to be driven by either the signal generated by the AND-OR array or the corresponding I/O pin. When the I/O pin is selected as the input, the feedback path provides the register/latch input to the array. When used as an input, each macrocell is also user-programmable for registered, latched, or combinatorial input.

The PALCE29MA16 has a dedicated CLK/$\overline{LE}$ pin and one individual CLK/$\overline{LE}$ product term or macrocell. All macrocells have a programmable switch to choose between the CLK/$\overline{LE}$ pin and the CLK/$\overline{LE}$ product term as the clock or latch enable signal. These signals are clock signals for macrocells configured as registers and latch enable signals for macrocells configured as latches. The polarity of these CLK/$\overline{LE}$ signals is also individually programmable. Thus different registers or latches can be driven by different clocks and clock phases.

The Output-Enable mode of each of the macrocells can be selected by the user. The I/O pin can be configured as an output pin (permanently enabled) or as an input pin (permanently disabled). It can also be configured as a dynamic I/O controlled by the Output Enable pin or by a product term.

## I/O Logic Macrocell Configuration

Our unique I/O macrocell offers major benefits through its versatile, programmable input/output cell structure, multiple clock choices, flexible Output Enable and feedback selection. Eight I/O macrocells with single feedback contain 9 EE cells, while the other eight macrocells contain 8 EE cells for programming the input/output functions (see Table 1).

EE cell $S_1$ controls whether the macrocell will be combinatorial or registered/latched. $S_0$ controls the output polarity (active-HIGH or active-LOW). $S_2$ determines whether the storage element is a register or a latch. $S_3$ allows the use of the macrocell as an input register/latch or as an output register/latch. It selects the direction of the data path through the register/latch. If connected to the usual AND-OR array output, the register/latch is an output connected to the I/O pin. If connected to the I/O pin, the register/latch becomes an input register/latch to the AND array using the feedback data path.

Programmable EE cells $S_4$ and $S_5$ allow the user to select one of the four CLK/$\overline{LE}$ signals for each macrocell. $S_6$ and $S_7$ are used to control Output Enable as pin controlled, product-term controlled, permanently enabled or permanently disabled. $S_8$ controls a feedback multiplexer for the macrocells with a single feedback path only.

Using the programmable EE cells $S_0$–$S_8$ various input and output configurations can be selected. Some of the possible configuration options are shown in Figure 3.

In the erased state (charged, disconnected), an architectural cell is said to have a value of “1”; in the programmed state (discharged, connected to GND), an architectural cell is said to have a value of “0.”

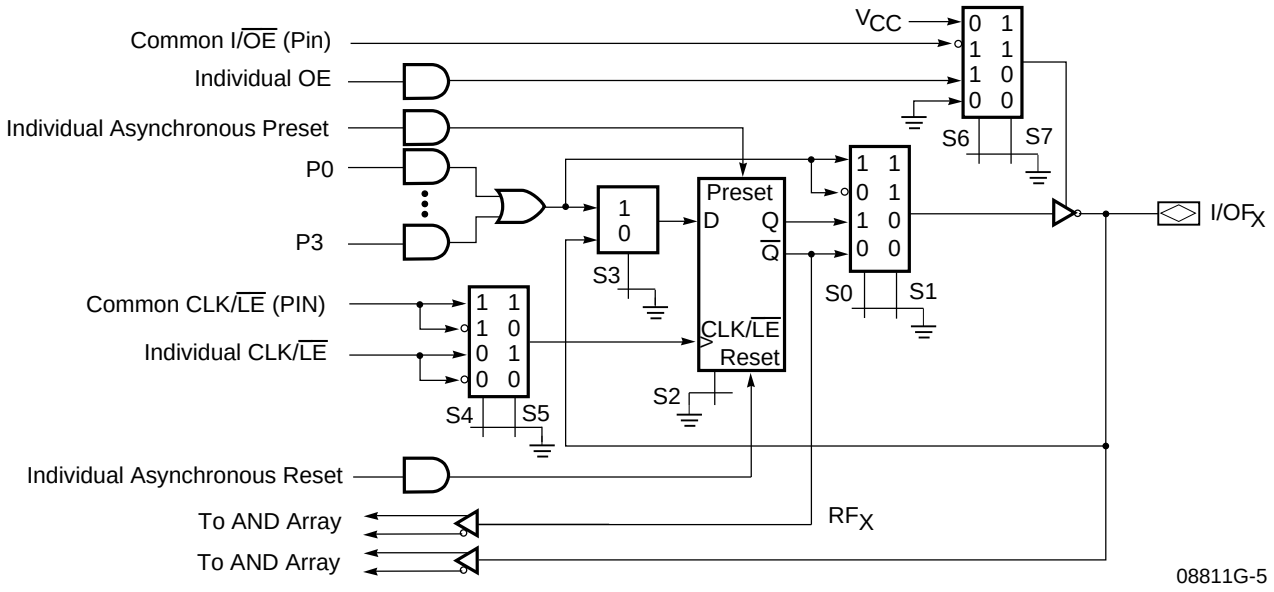



**Figure 2b. PALCE29MA16 Macrocell (Dual Feedback)**

## Table 1a. PALCE29MA16 I/O Logic Macrocell Architecture Selections

| $S_3$ | I/O Cell |
|---|---|
| 1 | Output Cell |
| 0 | Input Cell |

| $S_2$ | Storage Element |
|---|---|
| 1 | Register |
| 0 | Latch |

| $S_1$ | Output Type |
|---|---|
| 1 | Combinatorial |
| 0 | Register/Latch |

| $S_0$ | Output Polarity |
|---|---|
| 1 | Active LOW |
| 0 | Active HIGH |

| $S_8$ | Feedback* |
|---|---|
| 1 | Register/Latch |
| 0 | I/O |

**Applies to macrocells with single feedback only.*

## Table 1b. PALCE29MA16 I/O Logic Macrocell Clock Polarity and Output Enable Selections

| $S_4$ | $S_5$ | Clock Edge/Latch Enable Level |
|---|---|---|
| 1 | 1 | CLK/$\overline{LE}$ pin positive-going edge, active-LOW LE* |
| 1 | 0 | CLK/$\overline{LE}$ pin negative-going edge, active-HIGH LE* |
| 0 | 1 | CLK/$\overline{LE}$ PT positive-going edge, active-LOW LE* |
| 0 | 0 | CLK/$\overline{LE}$ PT negative-going edge, active-HIGH LE* |

| $S_6$ | $S_7$ | Output Buffer Control |
|---|---|---|
| 1 | 1 | Pin-Controlled Three-State Enable |
| 1 | 0 | PT-Controlled Three-State Enable |
| 0 | 1 | Permanently Enabled (Output only) |
| 0 | 0 | Permanently Disabled (Input only) |

***Notes:***

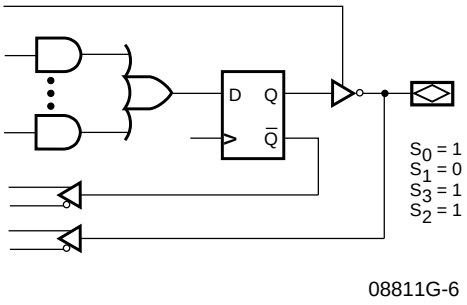
*1 = Erased State (Charged or disconnected).*

*0 = Programmed State (Discharged or connected).*

**Active-LOW LE means that data is stored when the $\overline{LE}$ pin is HIGH, and the latch is transparent when the $\overline{LE}$ pin is LOW. Active-HIGH LE means the opposite.*

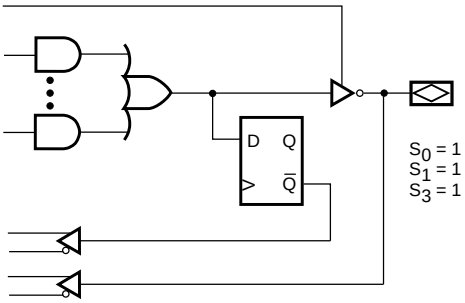
## SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

(For other useful configurations, please refer to the macrocell diagrams in Figure 2. All macrocell architecture cells are independently programmable).



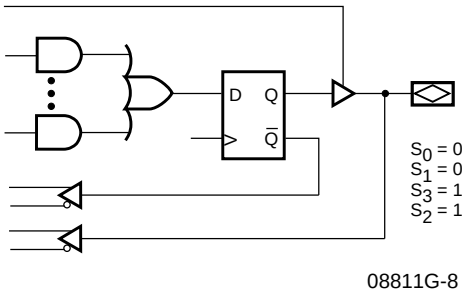

08811G-6

**Output Registered/Active Low**



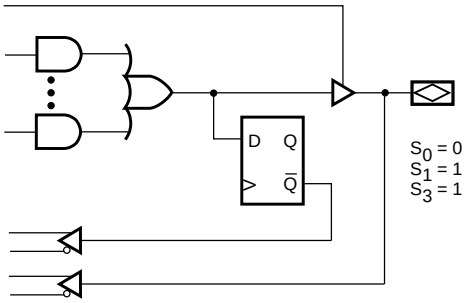

08811G-7

**Output Combinatorial/Active Low**




08811G-8

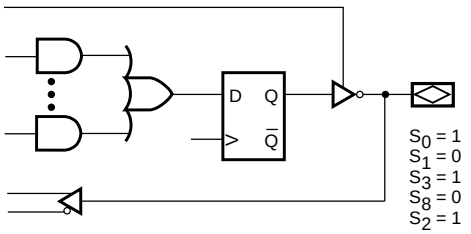
**Output Registered/Active High**




08811G-9

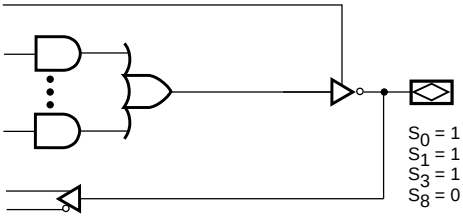
**Output Combinatorial/Active High**

**Figure 3a. Dual Feedback Macrocells**



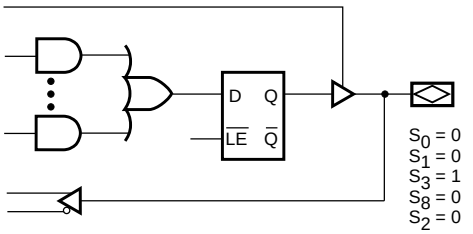

08811G-10

**Output Registered/Active Low, I/O Feedback**



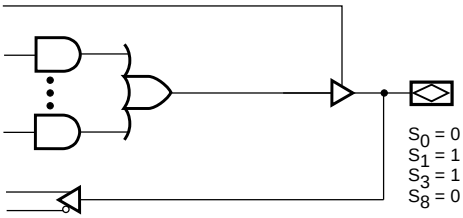

08811G-11

**Output Combinatorial/Active Low, I/O Feedback**




08811G-12

**Output Latched/Active High, I/O Feedback**

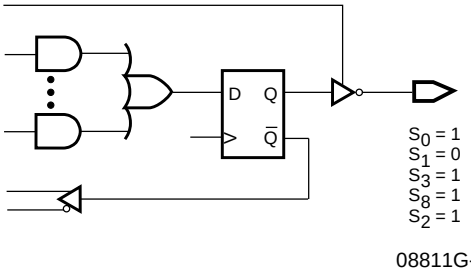



08811G-13

**Output Combinatorial/Active High, I/O Feedback**

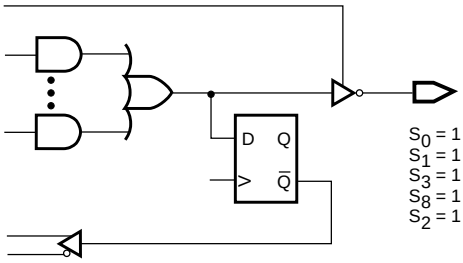
**Figure 3b. Single Feedback Macrocells**

## SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL



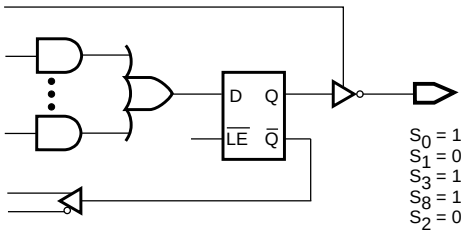

08811G-14

**Output Registered/Active Low, Register Feedback**



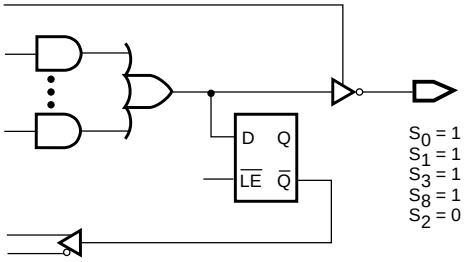

08811G-15

**Output Combinatorial/Active Low, Latched Feedback**




08811G-16

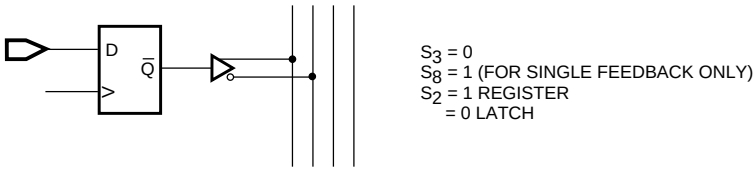
**Output Latched/Active Low, Latched Feedback**




08811G-17

**Output Combinatorial/Active Low, Latched Feedback**

**Figure 3b. Single Feedback Macrocells (Continued)**




08811G-18

**Programmable-AND Array**

**Figure 3c. All Macrocells**

## Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. The outputs of the PALCE29MA16 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW if programmed as active LOW and HIGH if programmed as active HIGH. If combinatorial is selected, the output will be a function of the logic.

## Preload

To simplify testing, the PALCE29MA16 is designed with preload circuitry that provides an easy method for testing logical functionality. Both product-term-controlled and supervoltage-enabled preload modes are available. The TTL-level preload product term can be useful during debugging, where supervoltages may not be available.

Preload allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the device's inputs into an arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state," which can be checked to validate the transition from the "present state." In this way any transition can be checked.

Since preload can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

## Observability

The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

## Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, preload, and the observability modes. The only way to erase the protection cell is by erasing the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

## Programming and Erasing

The PALCE29MA16 can be programmed on standard logic programmers. It may also be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erasure operation is required.

## Quality and Testability

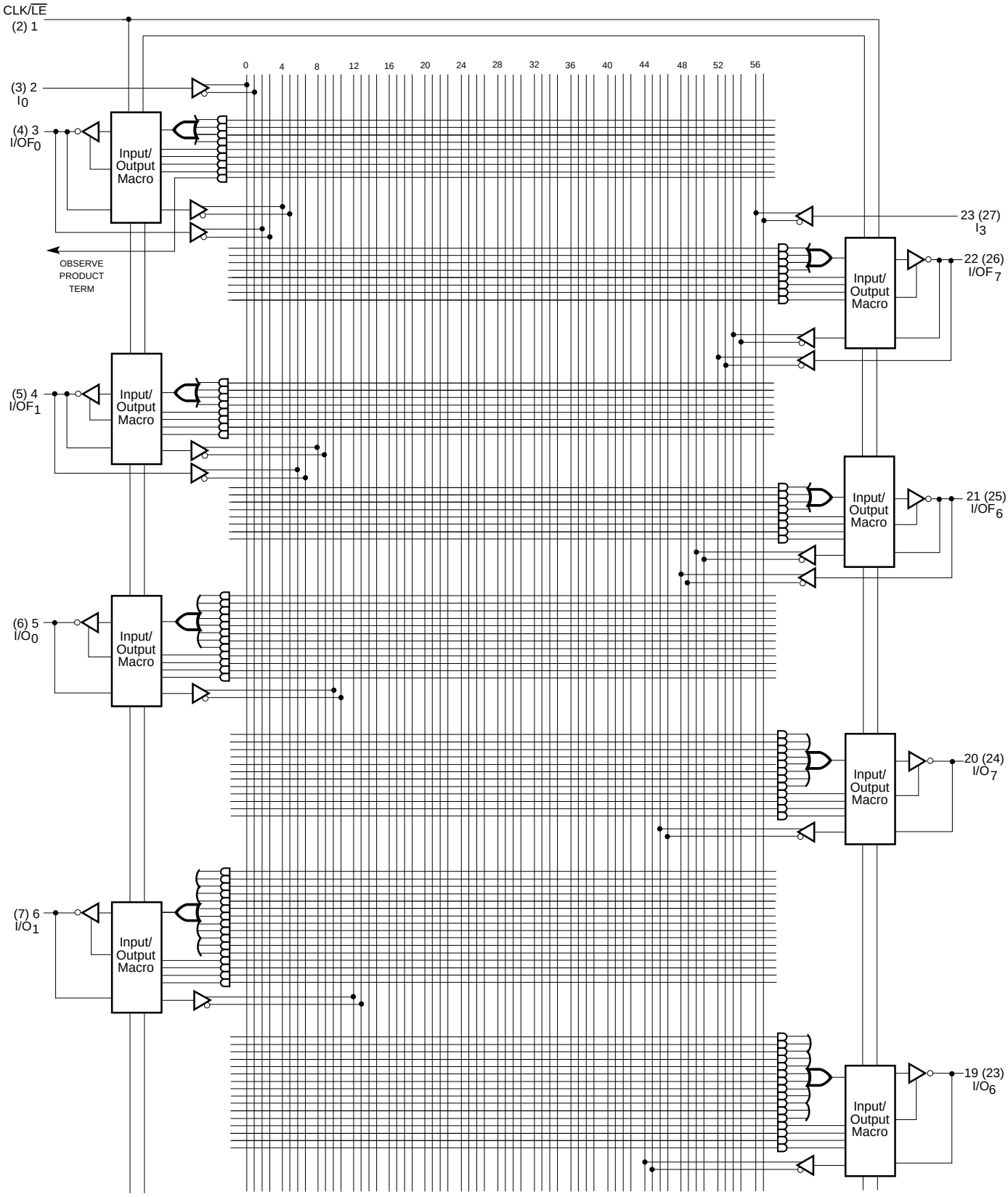
The PALCE29MA16 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all the AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to yield the highest programming yield and post-programming functional yield in the industry.

## Technology

The high-speed PALCE29MA16 is fabricated with our advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

## LOGIC DIAGRAM

## SKINNY DIP (PLCC) Pinouts

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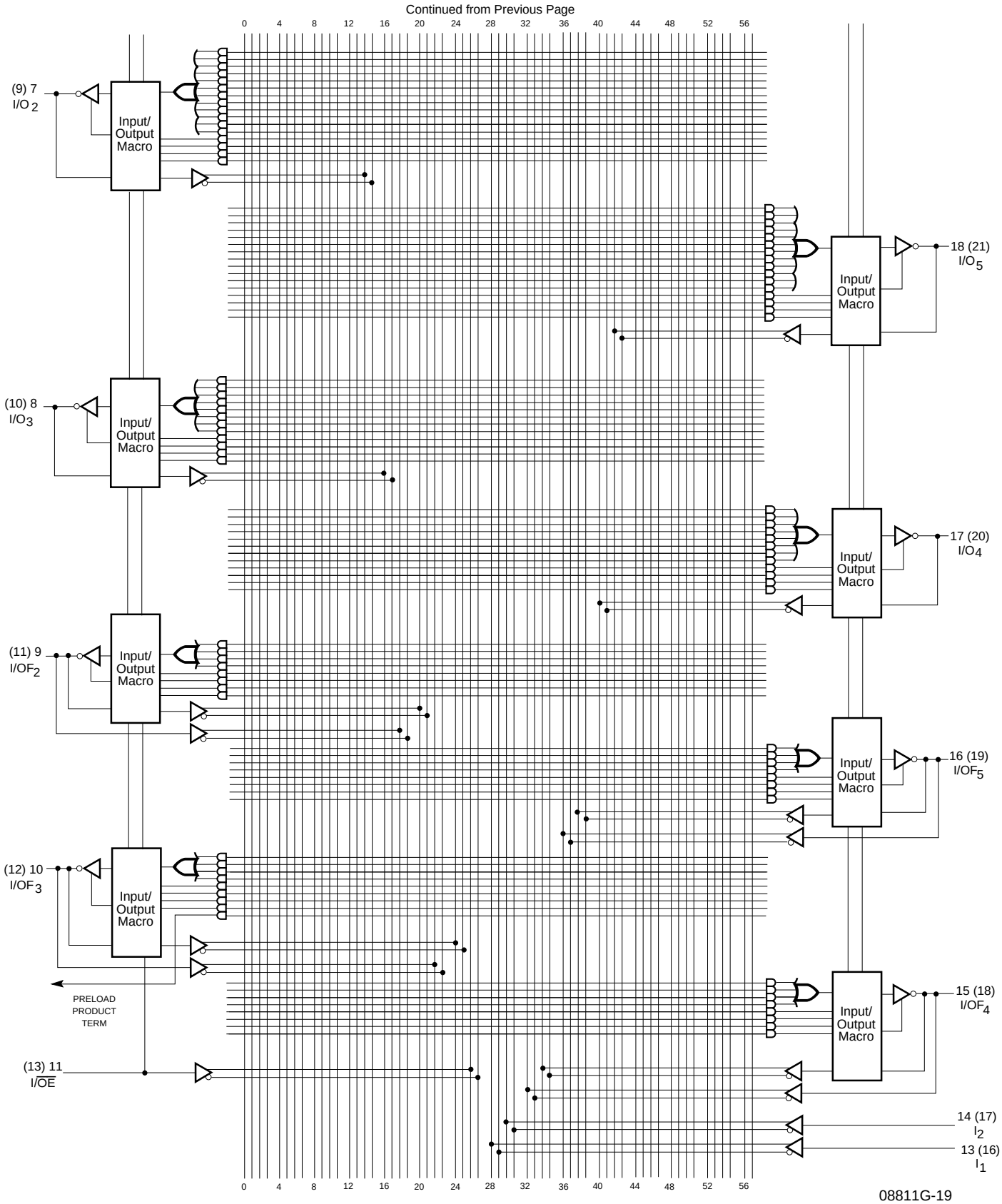
08811G-19

## LOGIC DIAGRAM
## SKINNY DIP (PLCC) Pinouts




08811G-19
(concluded)

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current ($T_A$ = 0°C to +75°C) . . . . . 100 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Ambient Temperature ($T_A$) Operating in Free Air . . . . . 0°C to +75°C

Supply Voltage ($V_{CC}$) with Respect to Ground . . . . . +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –2 mA | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 8 mA | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 0.5 | V |
| | | $I_{OL}$ = 4 mA | $V_{CC}$ = Min | | 0.33 | |
| | | $I_{OL}$ = 20 µA | | | 0.1 | |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max (Note 2) | | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max (Note 2) | | | –10 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.5 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 5.5 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | –10 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | | –30 | –130 | mA |
| $I_{CC}$ | Supply Current | $V_{IN}$ = 0 V, Outputs Open ($I_{OUT}$ = 0 mA)<br>$V_{CC}$ = Max | | | 100 | mA |

***Notes:***

1. *These are absolute values with respect to device ground all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

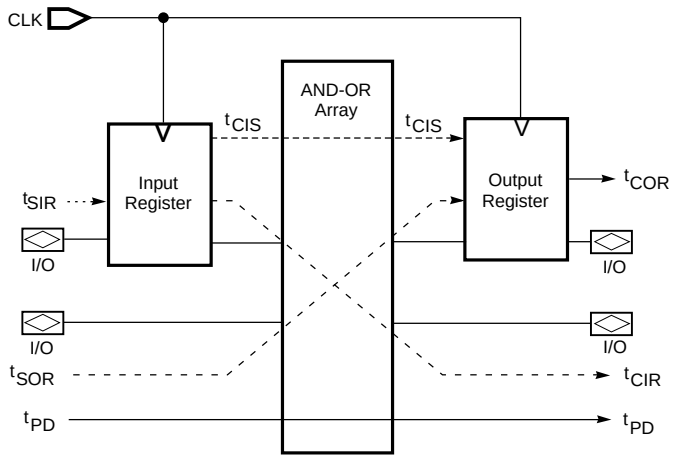
| Parameter Symbol | Parameter Description | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 V | f = 1 MHz | 8 | pF |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

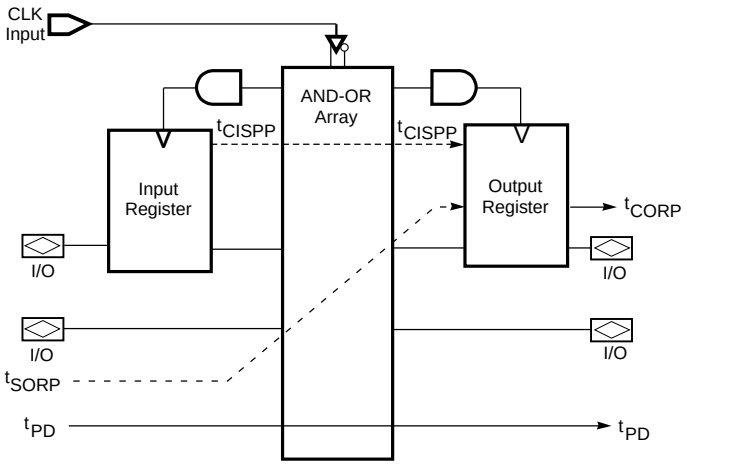
## SWITCHING CHARACTERISTICS
## Registered Operation

| Parameter Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| **Combinatorial Output** | | | | |
| $t_{PD}$ | Input or I/O Pin to Combinatorial Output | | 25 | ns |
| **Output Register – Pin Clock** | | | | |
| $t_{SOR}$ | Input or I/O Pin to Output Register Setup | 15 | | ns |
| $t_{COR}$ | Output Register Clock to Output | | 15 | ns |
| $t_{HOR}$ | Data Hold Time for Output Register | 0 | | ns |
| **Output Register – Product Term Clock** | | | | |
| $t_{SORP}$ | I/O Pin or Input to Output Register Setup | 4 | | ns |
| $t_{CORP}$ | Output Register Clock to Output | | 29 | ns |
| $t_{HORP}$ | Data Hold Time for Output Register | 10 | | ns |
| **Input Register – Pin Clock** | | | | |
| $t_{SIR}$ | I/O Pin to Input Register Setup | 2 | | ns |
| $t_{CIR}$ | Register Feedback Clock to Combinatorial Output | | 28 | ns |
| $t_{HIR}$ | Data Hold time for Input Register | 6 | | ns |
| **Clock and Frequency** | | | | |
| $t_{CIS}$ | Register Feedback (Pin Driven Clock) to Output Register/Latch (Pin Driven) Setup | 20 | | ns |
| $t_{CISPP}$ | Register Feedback (PT Driven Clock) to Output Register/Latch (PT Driven) Setup | 25 | | ns |
| $f_{MAX}$ | Maximum Frequency (Pin Driven) $1/(t_{SOR} + t_{COR})$ | 33.3 | | MHz |
| $f_{MAXI}$ | Maximum Internal Frequency (Pin Driven) $1/t_{CIS}$ | 50 | | MHz |
| $f_{MAXP}$ | Maximum Frequency (PT Driven) $1/(t_{SORP} + t_{CORP})$ | 30 | | MHz |
| $f_{MAXIPP}$ | Maximum Internal Frequency (PT Driven) $1/t_{CISPP}$ | 40 | | MHz |
| $t_{CWH}$ | Pin Clock Width HIGH | 8 | | ns |
| $t_{CWL}$ | Pin Clock Width LOW | 8 | | ns |
| $t_{CWHP}$ | PT Clock Width HIGH | 12 | | ns |
| $t_{CWLP}$ | PT Clock Width LOW | 12 | | ns |




08811G-20

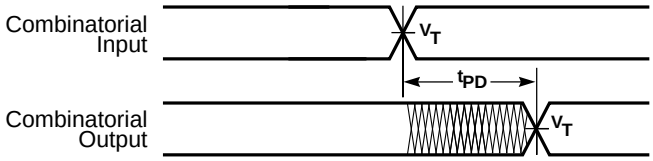
**Input/Output Register Specs (Pin CLK Reference)**




08811G-21

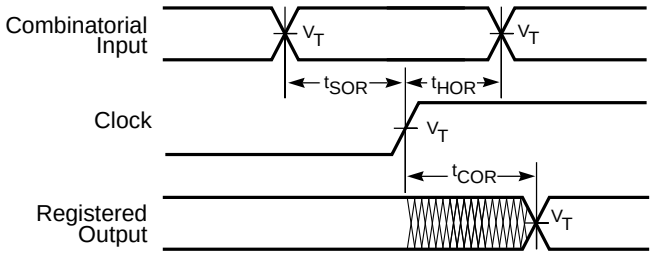
**Input/Output Register Specs (PT CLK Reference)**

## SWITCHING WAVEFORMS



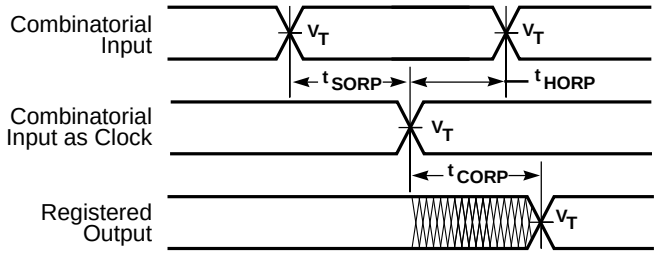

08811G-22

**Combinatorial Output**



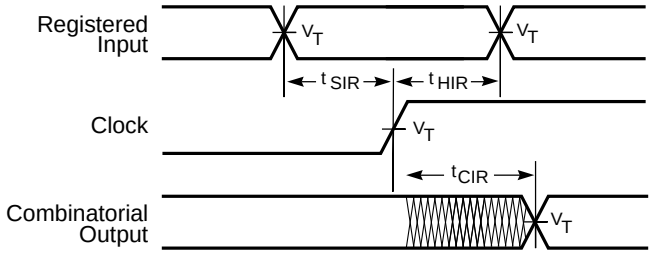

08811G-23

**Output Register (Pin Clock)**




08811G-24

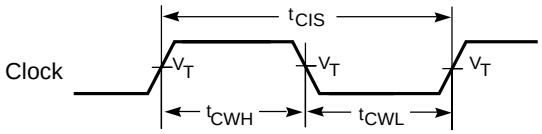
**Output Register (PT Clock)**




08811G-25

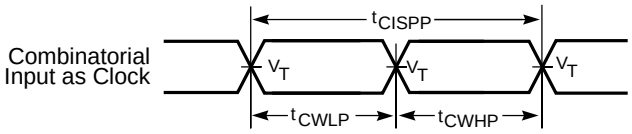
**Input Register**

## SWITCHING WAVEFORMS




08811G-26

**Pin Clock Width**



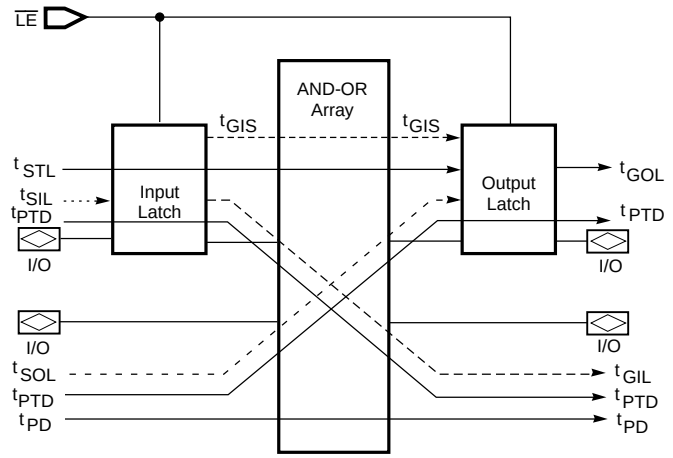

08811G-27

**PT Clock Width**

## SWITCHING CHARACTERISTICS

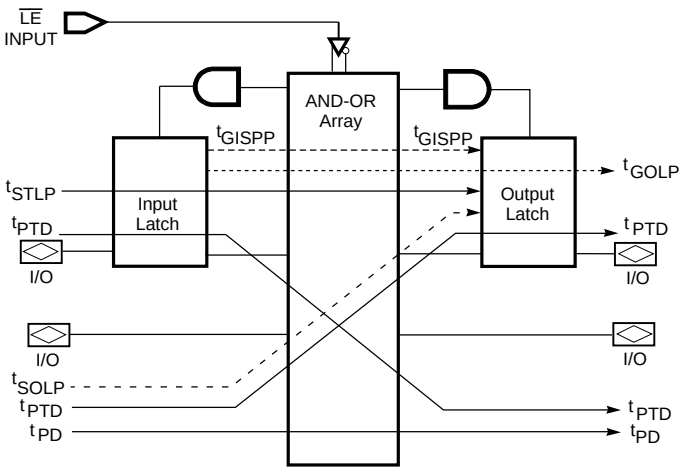
### Latched Operation

| Parameter Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| **Combinatorial Output** | | | | |
| $t_{PD}$ | Input or I/O Pin to Combinatorial Output | | 25 | ns |
| $t_{PTD}$ | Input or I/O Pin to Output via Transparent Latch | | 28 | ns |
| **Output Latch – Pin LE** | | | | |
| $t_{SOL}$ | Input or I/O Pin to Output Register Setup | 15 | | ns |
| $t_{GOL}$ | Latch Enable to Transparent Mode Output | | 15 | ns |
| $t_{HOL}$ | Data Hold Time for Output Latch | 0 | | ns |
| $t_{STL}$ | Input or I/O Pin to Output Latch Setup via Transparent Input Latch | 18 | | ns |
| **Output Latch – Product Term LE** | | | | |
| $t_{SOLP}$ | Input or I/O Pin to Output Latch Setup | 4 | | ns |
| $t_{GOLP}$ | Latch Enable to Transparent Mode Output | | 29 | ns |
| $t_{HOLP}$ | Data Hold Time for Output Latch | 10 | | ns |
| $t_{STLP}$ | Input or I/O Pin to Output Latch Setup via Transparent Input Latch | 10 | | ns |
| **Input Latch – Pin LE** | | | | |
| $t_{SIL}$ | I/O Pin to Input Latch Setup | 2 | | ns |
| $t_{GIL}$ | Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output | | 28 | ns |
| $t_{HIL}$ | Data Hold Time for Input Latch | 6 | | ns |
| **Latch Enable** | | | | |
| $t_{GIS}$ | Latch Feedback (Pin Driven) to Output Register/Latch (Pin Driven) Setup | 20 | | ns |
| $t_{GISPP}$ | Latch Feedback (PT Driven) to Output Register/Latch (PT Driven) Setup | 25 | | ns |
| $t_{GWH}$ | Pin Enable Width HIGH | 8 | | ns |
| $t_{GWL}$ | Pin Enable Width LOW | 8 | | ns |
| $t_{GWHP}$ | PT Enable Width HIGH | 12 | | ns |
| $t_{GWLP}$ | PT Enable Width LOW | 12 | | ns |




08811G-28

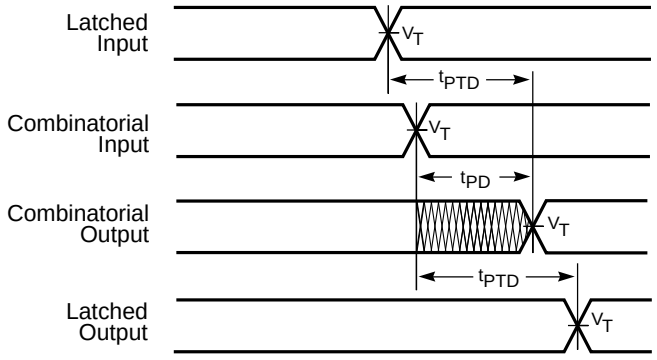
**Input/Output Latch Specs (Pin $\overline{LE}$ Reference)**




08811G-29

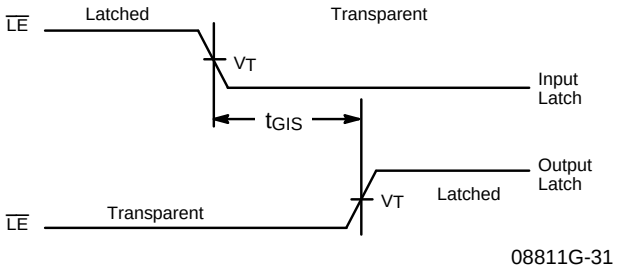
**Input/Output Latch Specs (PT $\overline{LE}$ Reference)**

## SWITCHING WAVEFORMS



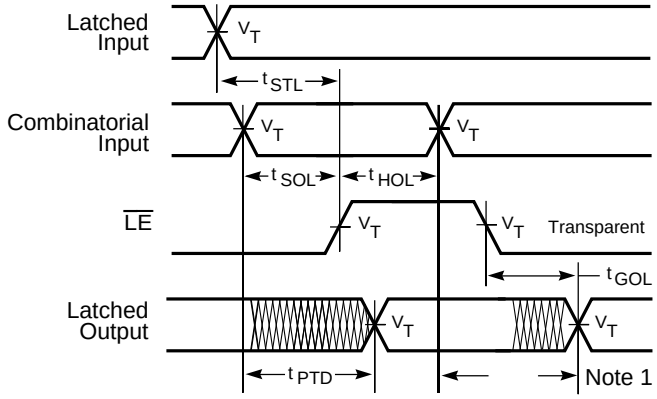

08811G-30

**Latch (Transparent Mode)**



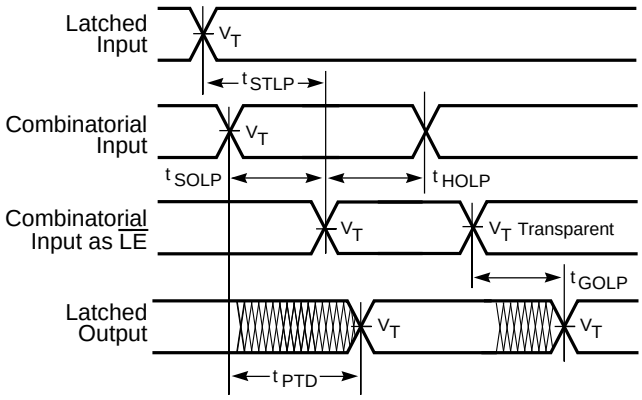

08811G-31

**Input and Output Latch Relationship**



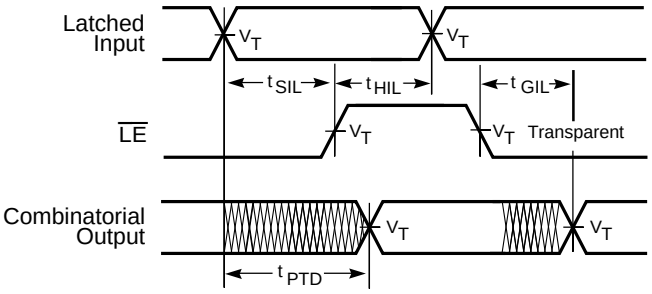

08811G-32

**Output Latch (Pin $\overline{LE}$)**



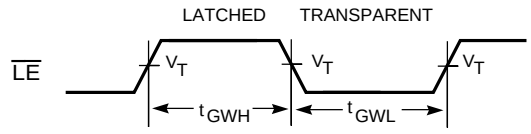

08811G-33

**Output Latch (PT $\overline{LE}$)**



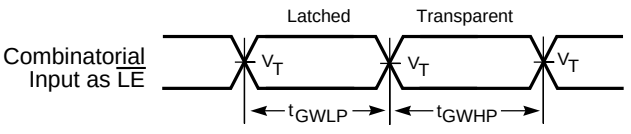

08811G-34

**Input Latch (Pin $\overline{LE}$)**




08811G-35

**Pin $\overline{LE}$ Width**




08811G-36

**PT $\overline{LE}$ Width**

***Note:***

1. *If the combinatorial input changes while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode after $t_{PTD}$ ns has elasped, the corresponding latched output will change $t_{GOL}$ ns after $\overline{LE}$ goes into the transparent mode. If the combinatorial input changes while $\overline{LE}$ is in the latched mode and $\overline{LE}$ goes into the transparent mode before $t_{PTD}$ ns has elapsed, the corresponding latched output will change at the later of the following – $t_{PTD}$ ns after the combinatorial input changes or $t_{GOL}$ ns after $\overline{LE}$ goes into the latched mode.*

## SWITCHING CHARACTERISTICS

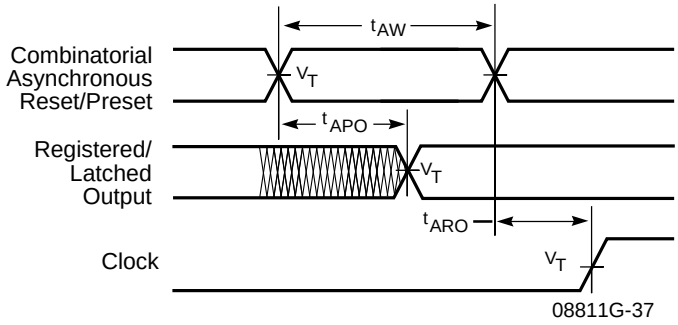
### Reset/Preset, Enable

| Parameter Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{APO}$ | Input or I/O Pin to Output Register/Latch Reset/Preset | | 30 | ns |
| $t_{AW}$ | Asynchronous Reset/Preset Pulse Width | 15 | | ns |
| $t_{ARO}$ | Asynchronous Reset/Preset to Output Register/Latch Recovery | 15 | | ns |
| $t_{ARI}$ | Asynchronous Reset/Preset to Input Register/Latch Recovery | 12 | | ns |
| $t_{ARPO}$ | Asynchronous Reset/Preset to Output Register/Latch Recovery PT Clock/LE | 4 | | ns |
| $t_{ARPI}$ | Asynchronous Reset/Preset to Input Register/Latch Recovery PT Clock/LE | 6 | | ns |
| **Output Enable Operation** | | | | |
| $t_{PZX}$ | I/$\overline{OE}$ Pin to Output Enable | | 20 | ns |
| $t_{PXZ}$ | I/$\overline{OE}$ Pin to Output Disable (Note 1) | | 20 | ns |
| $t_{EA}$ | Input or I/O to Output Enable via PT | | 25 | ns |
| $t_{ER}$ | Input or I/O to Output Disable via PT (Note 1) | | 25 | ns |

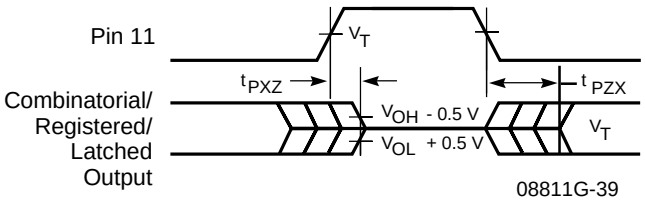
***Note:***

*1. Output disable times do not include test load RC time constants.*

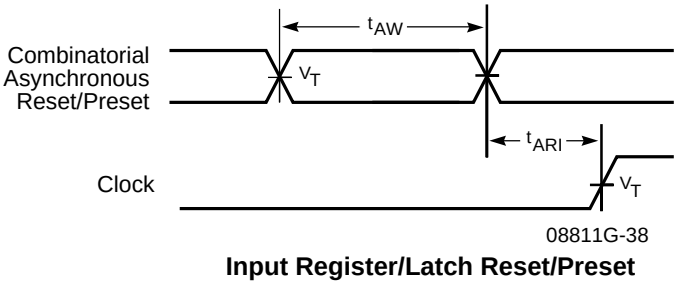
## SWITCHING WAVEFORMS



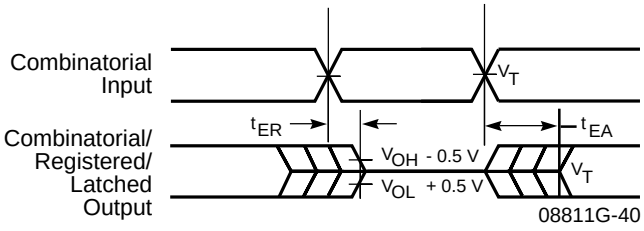

**Output Register/Latch Reset/Preset**




**Pin 11 to Output Disable/Enable**

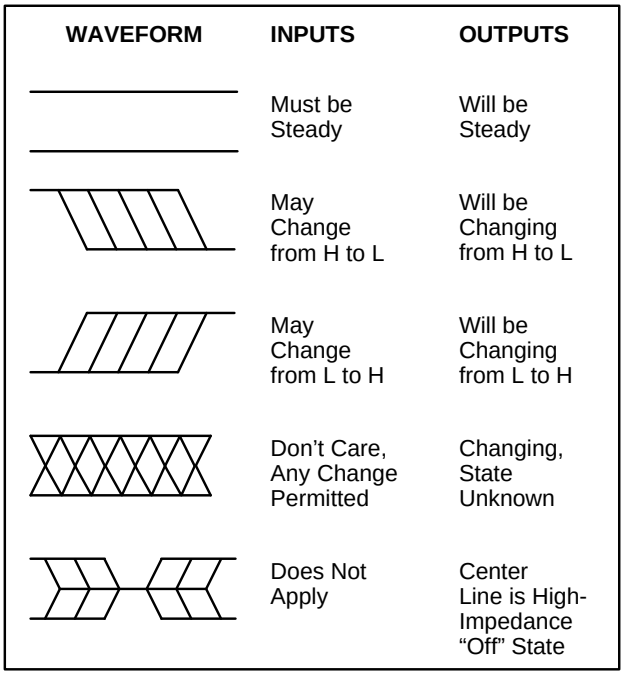



**Input Register/Latch Reset/Preset**



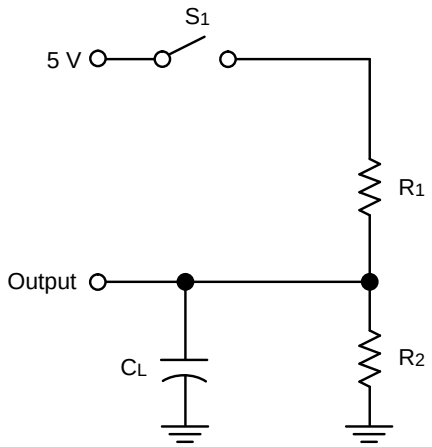

**Input to Output Disable/Enable**

## KEY TO SWITCHING WAVEFORMS




KS000010-PAL

## SWITCHING TEST CIRCUIT




08811G-41

| Specification | Switch $S_1$ | $C_L$ | $R_1$ | $R_2$ | Measured Output Value |
|---|---|---|---|---|---|
| $t_{PD}$, $t_{CO}$, $t_{GOL}$ | Closed | 35 pF | 470 Ω | 390 Ω | 1.5 V |
| $t_{EA}$, $t_{PZX}$ | Z→H: open<br>Z→L: closed | | | | 1.5 V |
| $t_{ER}$, $t_{PXZ}$ | H→Z: open<br>L→Z: closed | 5 pF | | | H→Z: $V_{OH}$ –0.5 V<br>L→Z: $V_{OL}$ +0.5 V |

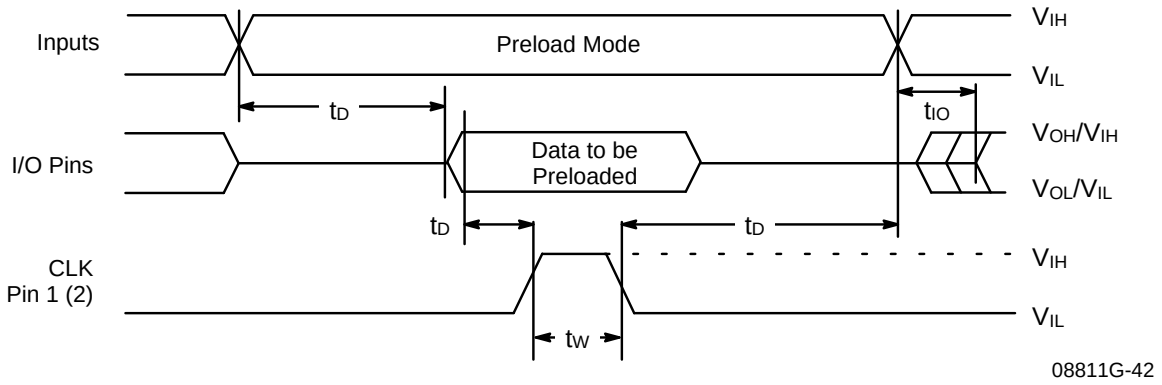
## PRELOAD

The PALCE29MA16 has the capability for product-term Preload. When the global-preload product term is true, the PALCE29MA16 will enter the preload mode. This feature aids functional testing by allowing direct setting of register states. The procedure for Preload is as follows:

- Set the selected input pins to the user selected preload condition.
- Apply the desired register value to the I/O pins. This sets Q of the register. The value seen on the I/O pin, after Preload, will depend on whether the macrocell is active high or active low.
- Pulse the clock pin (pin 1).
- Remove the inputs to the I/O pins.
- Remove the Preload condition.
- Verify $V_{OL}/V_{OH}$ for all output pins as per programmed pattern.

Because the Preload command is a product term, any input to the array can be used to set Preload (including I/O pins and registers). Preload itself will change the values of the I/O pins and registers. This will have unpredictable results. Therefore, only dedicated input pins should be used for the Preload command.

| Parameter Symbol | Parameter Description | Min | Rec. | Max | Unit |
|---|---|---|---|---|---|
| $t_D$ | Delay Time | 0.5 | 1.0 | 5.0 | µs |
| $t_W$ | Pulse Width | 250 | 500 | 700 | ns |
| $t_{I/O}$ | Valid Output | 100 | | 500 | ns |




**Preload Waveform**

## OBSERVABILITY

The PALCE29MA16 has the capability for product-term Observability. When the global-Observe product term is true, the PALCE29MA16 will enter the Observe mode. This feature aids functional testing by allowing direct observation of register states.

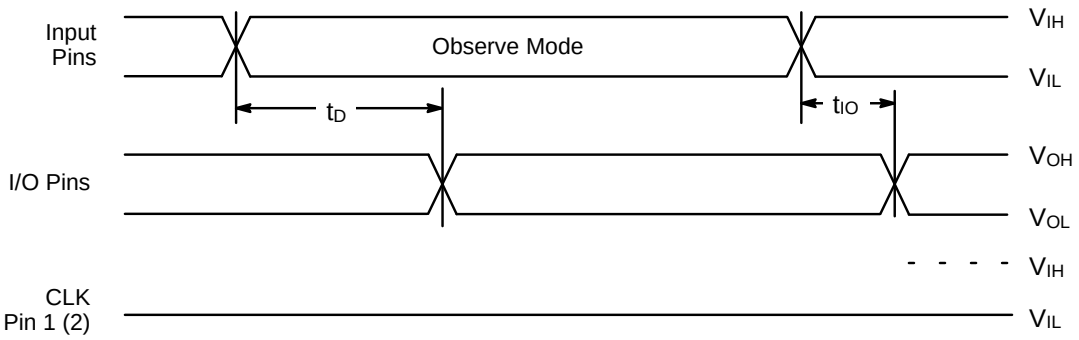
When the PALCE29MA16 is in the Observe mode, the output buffer is enabled and the I/O pin value will be Q of the corresponding register. This overrides any $\overline{OE}$ inputs.

The procedure for Observe is:

- Remove the inputs to all the I/O pins.
- Set the inputs to the, user selected, Observe configuration.
- The register values will be sent to the corresponding I/O pins.
- Remove the Observe configuration from the selected I/O pins.

Because the Observe command is a product term, any input to the array can be used to set Observe (including I/O pins and registers). If I/O pins are used, the observe mode could cause a value change, which would cause the device to oscillate in and out of the Observe mode. Therefore, only dedicated input pins should be used for the Observe command.

| Parameter Symbol | Parameter Description | Min | Rec. | Max | Unit |
|---|---|---|---|---|---|
| $t_D$ | Delay Time | 0.5 | 1.0 | 5.0 | µs |
| $t_{I/O}$ | Valid Output | 100 | | 500 | ns |




08811G-43

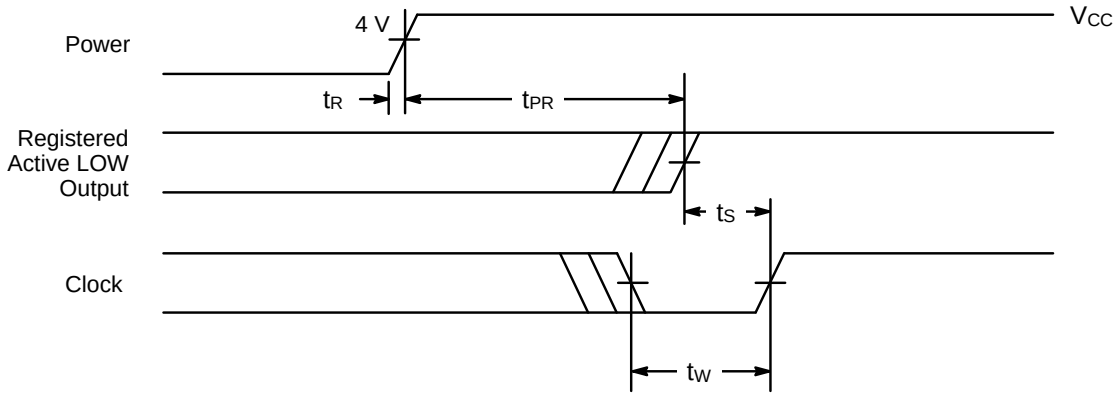
**Observability Waveform**

## POWER-UP RESET

The registered devices in the PAL Family have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways $V_{CC}$ can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- The $V_{CC}$ rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

| Parameter Symbol | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PR}$ | Power-Up Reset Time | | 10 | µs |
| $t_S$ | Input or Feedback Setup Time | See Switching Characteristics | | |
| $t_W$ | Clock Width | | | |
| $t_R$ | $V_{CC}$ Rise Time | 500 | | µs |




08811G-44

**Power-Up Reset Waveform**

## TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

| Parameter Symbol | Parameter Description | | Typ | | Unit |
|---|---|---|---|---|---|
| | | | SKINNYDIP | PLCC | |
| $\theta_{jc}$ | Thermal impedance, junction to case | | 17 | 11 | °C/W |
| $\theta_{ja}$ | Thermal impedance, junction to ambient | | 63 | 51 | °C/W |
| $\theta_{jma}$ | Thermal impedance, junction to ambient with air flow | 200 lfpm air | 60 | 43 | °C/W |
| | | 400 lfpm air | 52 | 38 | °C/W |
| | | 600 lfpm air | 43 | 34 | °C/W |
| | | 800 lfpm air | 39 | 30 | °C/W |

***Plastic θjc Considerations***

*The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.*