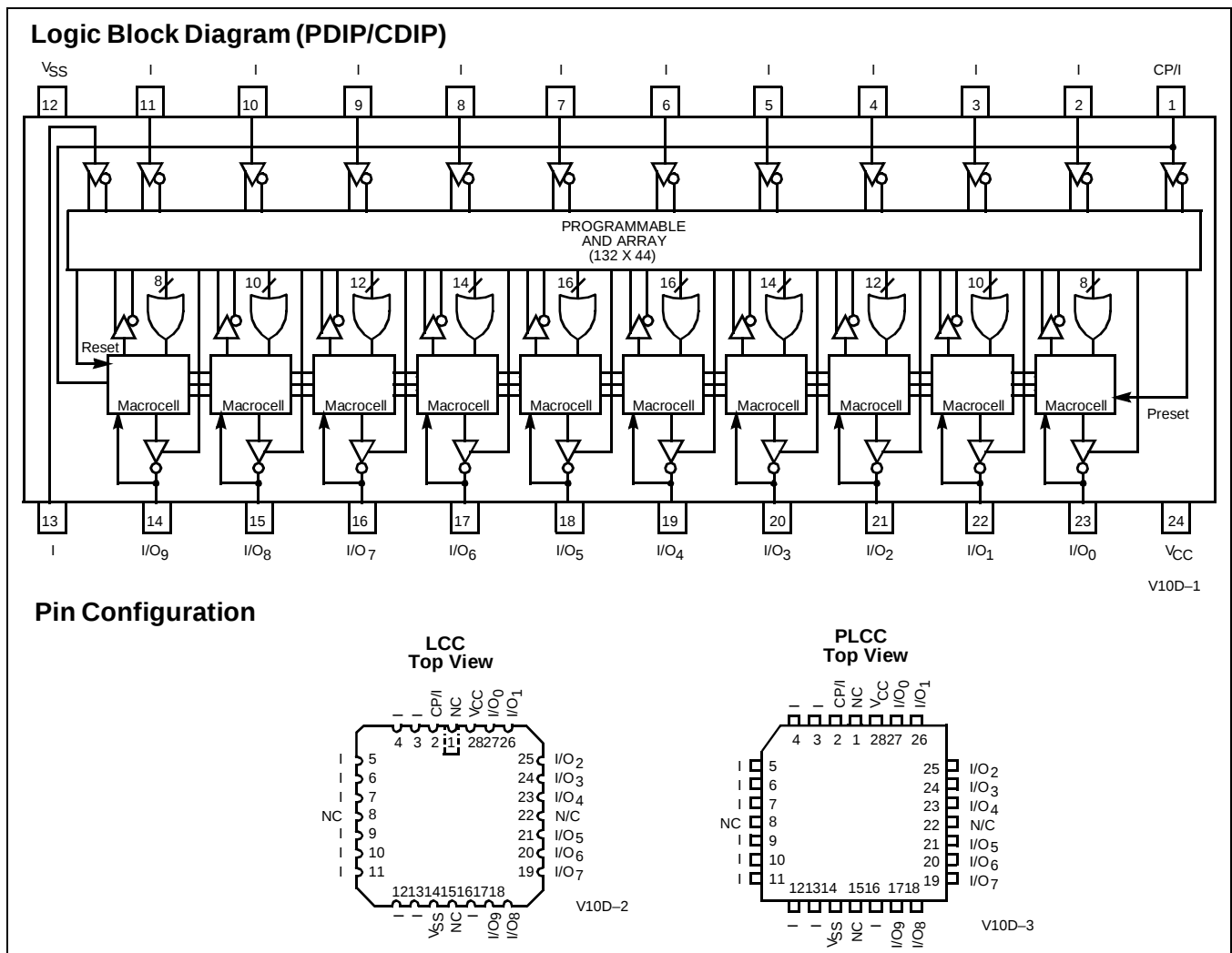
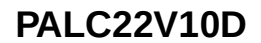




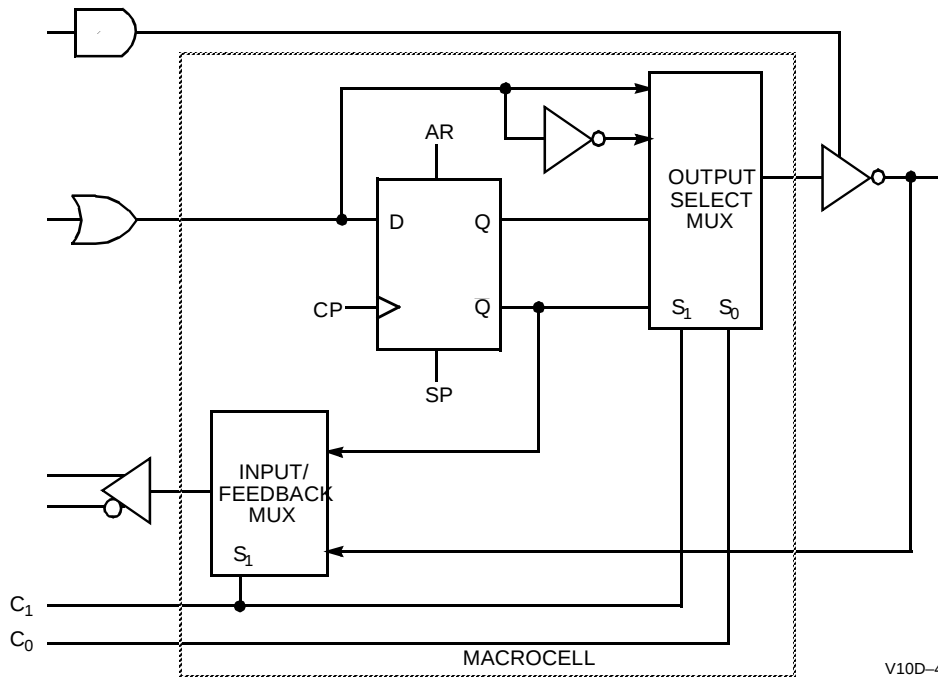
## Configuration Table

| Registered/Combinatorial |       |                        |
|--------------------------|-------|------------------------|
| $C_1$                    | $C_0$ | Configuration          |
| 0                        | 0     | Registered/Active LOW  |
| 0                        | 1     | Registered/Active HIGH |

## Configuration Table

| Registered/Combinatorial |       |                           |
|--------------------------|-------|---------------------------|
| $C_1$                    | $C_0$ | Configuration             |
| 1                        | 0     | Combinatorial/Active LOW  |
| 1                        | 1     | Combinatorial/Active HIGH |

## Macrocell



## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential  
(Pin 24 to Pin 12) ..... -0.5V to +7.0V

DC Voltage Applied to Outputs  
in High Z State ..... -0.5V to +7.0V

DC Input Voltage ..... -0.5V to +7.0V

Output Current into Outputs (LOW) ..... 16 mA

DC Programming Voltage ..... 12.5V

Latch-Up Current ..... >200 mA

Static Discharge Voltage  
(per MIL-STD-883, Method 3015) ..... >2001V

## Operating Range

| Range                   | Ambient Temperature | V <sub>CC</sub> |
|-------------------------|---------------------|-----------------|
| Commercial              | 0°C to +75°C        | 5V ±5%          |
| Military <sup>[1]</sup> | -55°C to +125°C     | 5V ±10%         |
| Industrial              | -40°C to +85°C      | 5V ±10%         |

### Note:

1. T<sub>A</sub> is the "instant on" case temperature.

## Electrical Characteristics Over the Operating Range<sup>[2]</sup>

| Parameter                      | Description                  | Test Conditions                                                                 |                           |         | Min. | Max. | Unit |
|--------------------------------|------------------------------|---------------------------------------------------------------------------------|---------------------------|---------|------|------|------|
| V <sub>OH</sub>                | Output HIGH Voltage          | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OH</sub> = -3.2 mA | Com'l   | 2.4  |      | V    |
|                                |                              |                                                                                 | I <sub>OH</sub> = -2 mA   | Mil/Ind |      |      |      |
| V <sub>OL</sub>                | Output LOW Voltage           | V <sub>CC</sub> = Min.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> | I <sub>OL</sub> = 16 mA   | Com'l   |      | 0.5  | V    |
|                                |                              |                                                                                 | I <sub>OL</sub> = 12 mA   | Mil/Ind |      |      |      |
| V <sub>IH</sub>                | Input HIGH Level             | Guaranteed Input Logical HIGH Voltage for All Inputs <sup>[3]</sup>             |                           |         | 2.0  |      | V    |
| V <sub>IL</sub> <sup>[2]</sup> | Input LOW Level              | Guaranteed Input Logical LOW Voltage for All Inputs <sup>[3]</sup>              |                           |         | -0.5 | 0.8  | V    |
| I <sub>Ix</sub>                | Input Leakage Current        | V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , V <sub>CC</sub> = Max.    |                           |         | -10  | 10   | μA   |
| I <sub>OZ</sub>                | Output Leakage Current       | V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub>    |                           |         | -40  | 40   | μA   |
| I <sub>SC</sub>                | Output Short Circuit Current | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0.5V <sup>[5,6]</sup>                |                           |         | -30  | -90  | mA   |

**Electrical Characteristics Over the Operating Range<sup>[2]</sup>**

| Parameter       | Description                    | Test Conditions                                                                                                                                        | Min.          | Max.    | Unit |
|-----------------|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|---------|------|
| $I_{CC1}$       | Standby Power Supply Current   | $V_{CC} = \text{Max.}, V_{IN} = \text{GND},$<br>Outputs Open in<br>Unprogrammed De-<br>vice                                                            | 10, 15, 25 ns | Com'l   |      |
|                 |                                |                                                                                                                                                        | 7.5 ns        | Com'l   |      |
|                 |                                |                                                                                                                                                        | 15, 25 ns     | Mil/Ind |      |
|                 |                                |                                                                                                                                                        | 10 ns         | Mil/Ind |      |
| $I_{CC2}^{[6]}$ | Operating Power Supply Current | $V_{CC} = \text{Max.}, V_{IL} = 0\text{V}, V_{IH} = 3\text{V},$<br>Output Open, De-<br>vice Programmed<br>as a 10-Bit Counter,<br>$f = 25 \text{ MHz}$ | 10, 15, 25 ns | Com'l   |      |
|                 |                                |                                                                                                                                                        | 7.5 ns        | Com'l   |      |
|                 |                                |                                                                                                                                                        | 15, 25 ns     | Mil/Ind |      |
|                 |                                |                                                                                                                                                        | 10 ns         | Mil/Ind |      |

**Notes:**

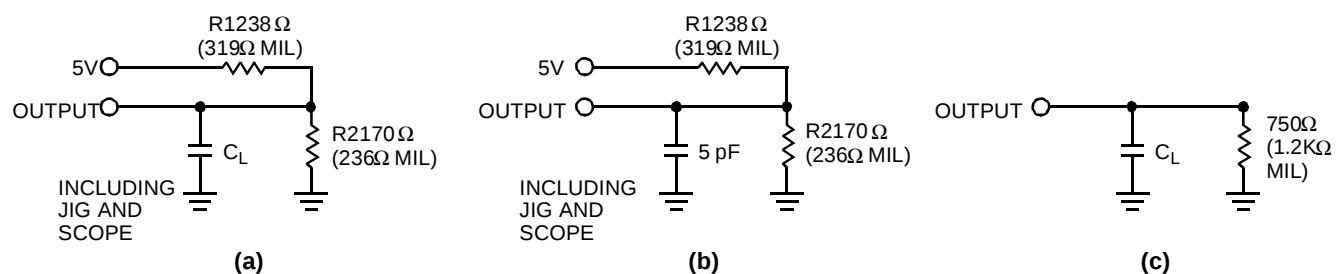
- See the last page of this specification for Group A subgroup testing information.
- These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
- $V_{IL}$  (Min.) is equal to -3.0V for pulse durations less than 20 ns.
- Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second.  $V_{OUT} = 0.5\text{V}$  has been chosen to avoid test problems caused by tester ground degradation.
- Tested initially and after any design or process changes that may affect these parameters.

**Capacitance<sup>[6]</sup>**

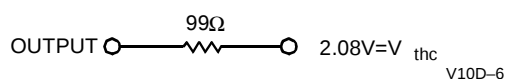
| Parameter | Description        | Test Conditions                             | Min. | Max. | Unit |
|-----------|--------------------|---------------------------------------------|------|------|------|
| $C_{IN}$  | Input Capacitance  | $V_{IN} = 2.0\text{V} @ f = 1 \text{ MHz}$  |      | 10   | pF   |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 2.0\text{V} @ f = 1 \text{ MHz}$ |      | 10   | pF   |

**Endurance Characteristics<sup>[6]</sup>**

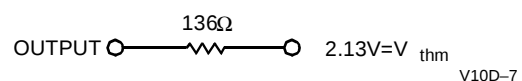
| Parameter | Description                  | Test Conditions               | Min. | Max. | Unit   |
|-----------|------------------------------|-------------------------------|------|------|--------|
| N         | Minimum Reprogramming Cycles | Normal Programming Conditions | 100  |      | Cycles |

**AC Test Loads and Waveforms**


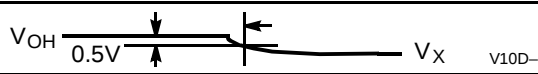
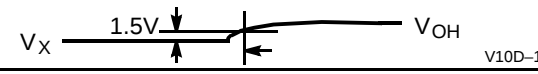
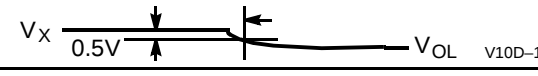
Equivalent to: THÉVENIN EQUIVALENT(Commercial)



Equivalent to: THÉVENIN EQUIVALENT(Military)



|                    |       |                       |
|--------------------|-------|-----------------------|
| Load Speed         | $C_L$ | Package               |
| 7.5, 10, 15, 25 ns | 50 pF | PDIP, CDIP, PLCC, LCC |

| Parameter    | $V_X$     | Output Waveform Measurement Level                                                 |
|--------------|-----------|-----------------------------------------------------------------------------------|
| $t_{ER} (-)$ | 1.5V      |  |
| $t_{ER} (+)$ | 2.6V      |  |
| $t_{EA} (+)$ | 0V        |  |
| $t_{EA} (-)$ | $V_{thc}$ |  |

(e) Test Waveforms

**Commercial Switching Characteristics PALC22V10D<sup>[2, 7]</sup>**

| Parameter  | Description                                                                   | 22V10D-7 |      | 22V10D-10 |      | 22V10D-15 |      | 22V10D-25 |      | Unit |
|------------|-------------------------------------------------------------------------------|----------|------|-----------|------|-----------|------|-----------|------|------|
|            |                                                                               | Min.     | Max. | Min.      | Max. | Min.      | Max. | Min.      | Max. |      |
| $t_{PD}$   | Input to Output Propagation Delay <sup>[8, 9]</sup>                           | 3        | 7.5  | 3         | 10   | 3         | 15   | 3         | 25   | ns   |
| $t_{EA}$   | Input to Output Enable Delay <sup>[10]</sup>                                  |          | 8    |           | 10   |           | 15   |           | 25   | ns   |
| $t_{ER}$   | Input to Output Disable Delay <sup>[11]</sup>                                 |          | 8    |           | 10   |           | 15   |           | 25   | ns   |
| $t_{CO}$   | Clock to Output Delay <sup>[8, 9]</sup>                                       | 2        | 5    | 2         | 7    | 2         | 8    | 2         | 15   | ns   |
| $t_{S1}$   | Input or Feedback Set-Up Time                                                 | 5        |      | 6         |      | 10        |      | 15        |      | ns   |
| $t_{S2}$   | Synchronous Preset Set-Up Time                                                | 6        |      | 7         |      | 10        |      | 15        |      | ns   |
| $t_H$      | Input Hold Time                                                               | 0        |      | 0         |      | 0         |      | 0         |      | ns   |
| $t_P$      | External Clock Period ( $t_{CO} + t_S$ )                                      | 10       |      | 12        |      | 20        |      | 30        |      | ns   |
| $t_{WH}$   | Clock Width HIGH <sup>[6]</sup>                                               | 3        |      | 3         |      | 6         |      | 13        |      | ns   |
| $t_{WL}$   | Clock Width LOW <sup>[6]</sup>                                                | 3        |      | 3         |      | 6         |      | 13        |      | ns   |
| $f_{MAX1}$ | External Maximum Frequency ( $1/(t_{CO} + t_S)$ ) <sup>[12]</sup>             | 100      |      | 76.9      |      | 55.5      |      | 33.3      |      | MHz  |
| $f_{MAX2}$ | Data Path Maximum Frequency ( $1/(t_{WH} + t_{WL})$ ) <sup>[6, 13]</sup>      | 166      |      | 142       |      | 83.3      |      | 35.7      |      | MHz  |
| $f_{MAX3}$ | Internal Feedback Maximum Frequency ( $1/(t_{CF} + t_S)$ ) <sup>[6, 14]</sup> | 133      |      | 111       |      | 68.9      |      | 38.5      |      | MHz  |
| $t_{CF}$   | Register Clock to Feedback Input <sup>[6, 15]</sup>                           |          | 2.5  |           | 3    |           | 4.5  |           | 13   | ns   |
| $t_{AW}$   | Asynchronous Reset Width                                                      | 8        |      | 10        |      | 15        |      | 25        |      | ns   |
| $t_{AR}$   | Asynchronous Reset Recovery Time                                              | 5        |      | 6         |      | 10        |      | 25        |      | ns   |
| $t_{AP}$   | Asynchronous Reset to Registered Output Delay                                 |          | 12   |           | 13   |           | 20   |           | 25   | ns   |
| $t_{SPR}$  | Synchronous Preset Recovery Time                                              | 6        |      | 8         |      | 10        |      | 15        |      | ns   |
| $t_{PR}$   | Power-Up Reset Time <sup>[6, 16]</sup>                                        | 1        |      | 1         |      | 1         |      | 1         |      | μs   |

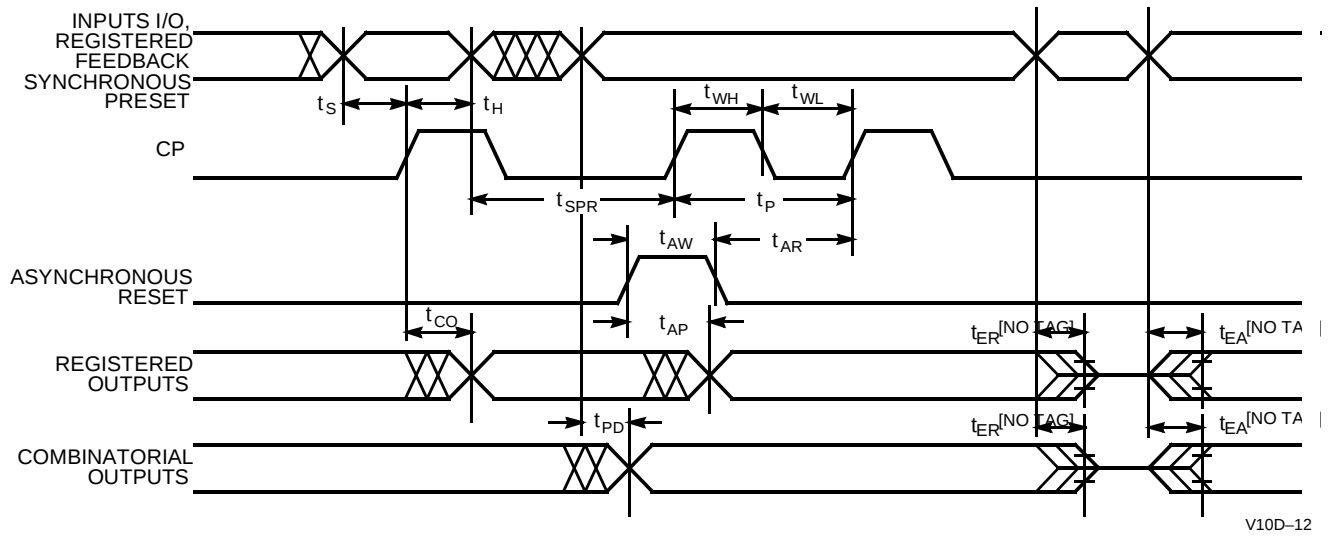
**Notes:**

7. Part (a) of AC Test Loads and Waveforms is used for all parameters except  $t_{ER}$  and  $t_{EA(+)}$ . Part (b) of AC Test Loads and Waveforms is used for  $t_{ER}$ . Part (c) of AC Test Loads and Waveforms is used for  $t_{EA(+)}$ .
8. Min. times are tested initially and after any design or process changes that may affect these parameters.
9. This specification is guaranteed for all device outputs changing state in a given access cycle.
10. The test load of part (a) of AC Test Loads and Waveforms is used for measuring  $t_{EA(-)}$ . The test load of part (c) of AC Test Loads and Waveforms is used for measuring  $t_{EA(+)}$  only. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
11. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below  $V_{OH}$  min. or a previous LOW level has risen to 0.5 volts above  $V_{OL}$  max. Please see part (e) of AC Test Loads and Waveforms for enable and disable test waveforms and measurement reference levels.
12. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
13. This specification indicates the guaranteed maximum frequency at which the device can operate in data path mode.
14. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate.
15. This parameter is calculated from the clock period at  $f_{MAX}$  internal ( $1/f_{MAX3}$ ) as measured (see Note above) minus  $t_S$ .
16. The registers in the PALC22V10D have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in  $V_{CC}$  must be monotonic and the timing constraints depicted in Power-Up Reset Waveform must be satisfied.

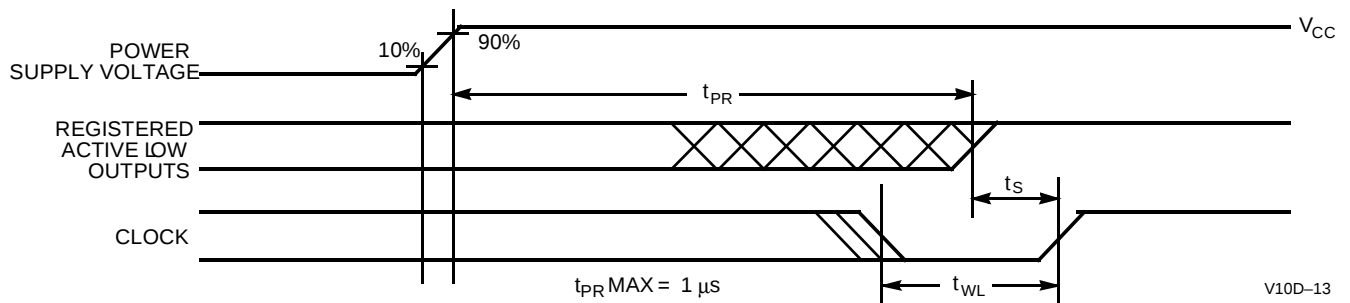
**Military and Industrial Switching Characteristics PALC22V10D<sup>[2, 7]</sup>**

| Parameter  | Description                                                                   | 22V10D-10 |      | 22V10D-15 |      | 22V10D-25 |      | Unit    |
|------------|-------------------------------------------------------------------------------|-----------|------|-----------|------|-----------|------|---------|
|            |                                                                               | Min.      | Max. | Min.      | Max. | Min.      | Max. |         |
| $t_{PD}$   | Input to Output Propagation Delay <sup>[8, 9]</sup>                           | 3         | 10   | 3         | 15   | 3         | 25   | ns      |
| $t_{EA}$   | Input to Output Enable Delay <sup>[10]</sup>                                  |           | 10   |           | 15   |           | 25   | ns      |
| $t_{ER}$   | Input to Output Disable Delay <sup>[11]</sup>                                 |           | 10   |           | 15   |           | 25   | ns      |
| $t_{CO}$   | Clock to Output Delay <sup>[8, 9]</sup>                                       | 2         | 7    | 2         | 8    | 2         | 15   | ns      |
| $t_{S1}$   | Input or Feedback Set-Up Time                                                 | 6         |      | 10        |      | 18        |      | ns      |
| $t_{S2}$   | Synchronous Preset Set-Up Time                                                | 7         |      | 10        |      | 18        |      | ns      |
| $t_H$      | Input Hold Time                                                               | 0         |      | 0         |      | 0         |      | ns      |
| $t_P$      | External Clock Period ( $t_{CO} + t_S$ )                                      | 12        |      | 20        |      | 33        |      | ns      |
| $t_{WH}$   | Clock Width HIGH <sup>[6]</sup>                                               | 3         |      | 6         |      | 14        |      | ns      |
| $t_{WL}$   | Clock Width LOW <sup>[6]</sup>                                                | 3         |      | 6         |      | 14        |      | ns      |
| $f_{MAX1}$ | External Maximum Frequency ( $1/(t_{CO} + t_S)$ ) <sup>[12]</sup>             | 76.9      |      | 50.0      |      | 30.3      |      | MHz     |
| $f_{MAX2}$ | Data Path Maximum Frequency ( $1/(t_{WH} + t_{WL})$ ) <sup>[6, 13]</sup>      | 142       |      | 83.3      |      | 35.7      |      | MHz     |
| $f_{MAX3}$ | Internal Feedback Maximum Frequency ( $1/(t_{CF} + t_S)$ ) <sup>[6, 14]</sup> | 111       |      | 68.9      |      | 32.2      |      | MHz     |
| $t_{CF}$   | Register Clock to Feedback Input <sup>[6, 15]</sup>                           |           | 3    |           | 4.5  |           | 13   | ns      |
| $t_{AW}$   | Asynchronous Reset Width                                                      | 10        |      | 15        |      | 25        |      | ns      |
| $t_{AR}$   | Asynchronous Reset Recovery Time                                              | 6         |      | 12        |      | 25        |      | ns      |
| $t_{AP}$   | Asynchronous Reset to Registered Output Delay                                 |           | 12   |           | 20   |           | 25   | ns      |
| $t_{SPR}$  | Synchronous Preset Recovery Time                                              | 8         |      | 20        |      | 25        |      | ns      |
| $t_{PR}$   | Power-Up Reset Time <sup>[6, 16]</sup>                                        | 1         |      | 1         |      | 1         |      | $\mu$ s |

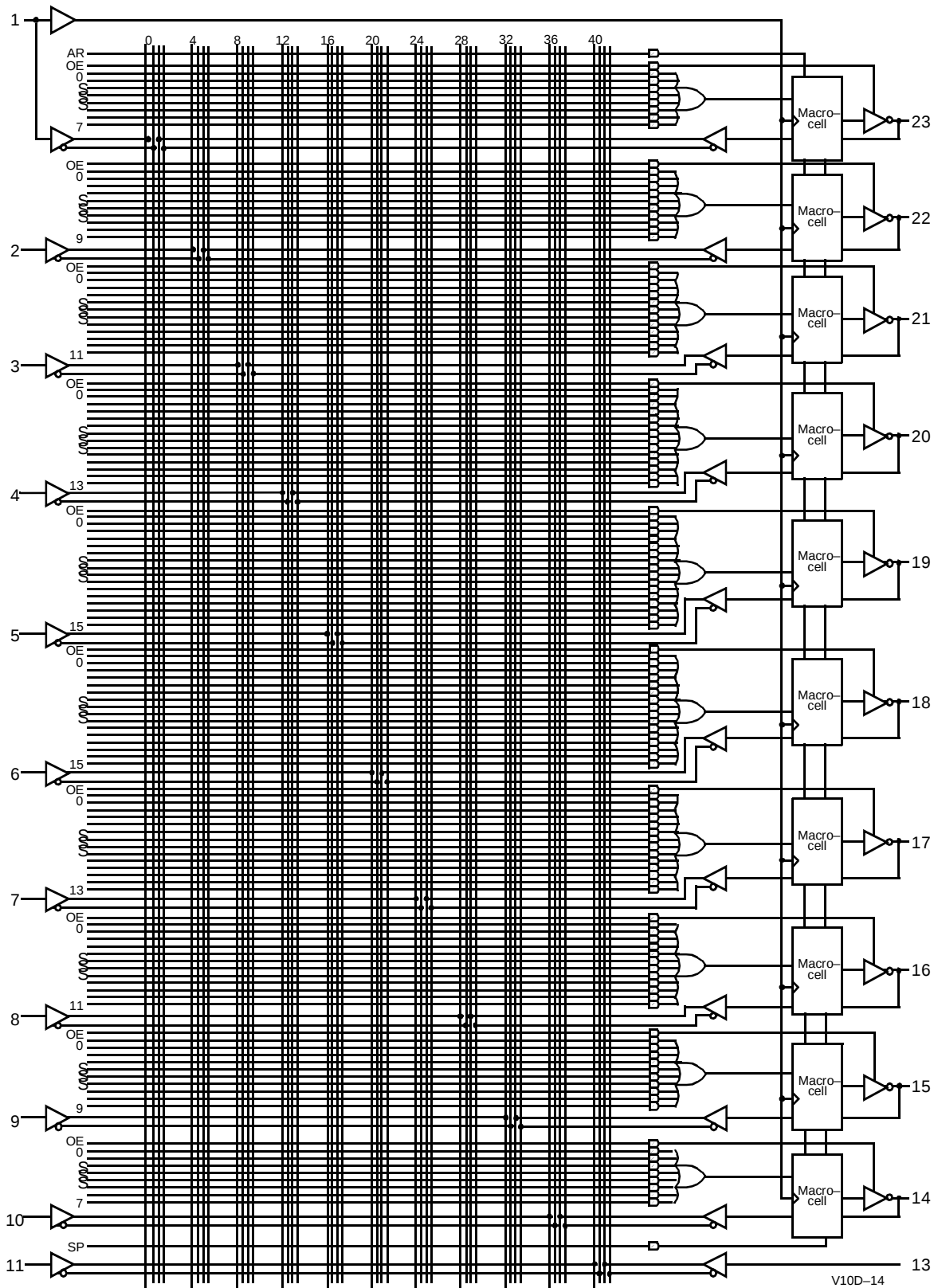
## Switching Waveform



## Power-Up Reset Waveform<sup>[16]</sup>



# Functional Logic Diagram for PALC22V10D



**Ordering Information**

| $I_{CC}$<br>(mA) | $t_{PD}$<br>(ns) | $t_S$<br>(ns) | $t_{CO}$<br>(ns) | Ordering Code    | Package Name | Package Type                        | Operating Range |
|------------------|------------------|---------------|------------------|------------------|--------------|-------------------------------------|-----------------|
| 130              | 7.5              | 5             | 5                | PALC22V10D-7JC   | J64          | 28-Lead Plastic Leaded Chip Carrier | Commercial      |
|                  |                  |               |                  | PALC22V10D-7PC   | P13          | 24-Lead (300-Mil) Molded DIP        |                 |
| 90               | 10               | 6             | 7                | PALC22V10D-10JC  | J64          | 28-Lead Plastic Leaded Chip Carrier | Commercial      |
|                  |                  |               |                  | PALC22V10D-10PC  | P13          | 24-Lead (300-Mil) Molded DIP        |                 |
| 150              | 10               | 6             | 7                | PALC22V10D-10JI  | J64          | 28-Lead Plastic Leaded Chip Carrier | Industrial      |
|                  |                  |               |                  | PALC22V10D-10PI  | P13          | 24-Lead (300-Mil) Molded DIP        |                 |
| 150              | 10               | 6             | 7                | PALC22V10D-10DMB | D14          | 24-Lead (300-Mil) CerDIP            | Military        |
|                  |                  |               |                  | PALC22V10D-10KMB | K73          | 24-Lead Rectangular Cerpack         |                 |
|                  |                  |               |                  | PALC22V10D-10LMB | L64          | 28-Square Leadless Chip Carrier     |                 |
| 90               | 15               | 7.5           | 10               | PALC22V10D-15JC  | J64          | 28-Lead Plastic Leaded Chip Carrier | Commercial      |
|                  |                  |               |                  | PALC22V10D-15PC  | P13          | 24-Lead (300-Mil) Molded DIP        |                 |
| 120              | 15               | 7.5           | 10               | PALC22V10D-15JI  | J64          | 28-Lead Plastic Leaded Chip Carrier | Industrial      |
|                  |                  |               |                  | PALC22V10D-15PI  | P13          | 24-Lead (300-Mil) Molded DIP        |                 |
| 120              | 15               | 7.5           | 10               | PALC22V10D-15DMB | D14          | 24-Lead (300-Mil) CerDIP            | Military        |
|                  |                  |               |                  | PALC22V10D-15KMB | K73          | 24-Lead Rectangular Cerpack         |                 |
|                  |                  |               |                  | PALC22V10D-15LMB | L64          | 28-Square Leadless Chip Carrier     |                 |
| 90               | 25               | 15            | 15               | PALC22V10D-25JC  | J64          | 28-Lead Plastic Leaded Chip Carrier | Commercial      |
|                  |                  |               |                  | PALC22V10D-25PC  | P13          | 24-Lead (300-Mil) Molded DIP        |                 |
| 120              | 25               | 15            | 15               | PALC22V10D-25JI  | J64          | 28-Lead Plastic Leaded Chip Carrier | Industrial      |
|                  |                  |               |                  | PALC22V10D-25PI  | P13          | 24-Lead (300-Mil) Molded DIP        |                 |
| 120              | 25               | 15            | 15               | PALC22V10D-25DMB | D14          | 24-Lead (300-Mil) CerDIP            | Military        |
|                  |                  |               |                  | PALC22V10D-25KMB | K73          | 24-Lead Rectangular Cerpack         |                 |
|                  |                  |               |                  | PALC22V10D-25LMB | L64          | 28-Square Leadless Chip Carrier     |                 |

**MILITARY SPECIFICATIONS**
**Group A Subgroup Testing**
**DC Characteristics**

| Parameter | Subgroups |
|-----------|-----------|
| $V_{OH}$  | 1, 2, 3   |
| $V_{OL}$  | 1, 2, 3   |
| $V_{IH}$  | 1, 2, 3   |
| $V_{IL}$  | 1, 2, 3   |
| $I_{IX}$  | 1, 2, 3   |
| $I_{OZ}$  | 1, 2, 3   |
| $I_{CC}$  | 1, 2, 3   |

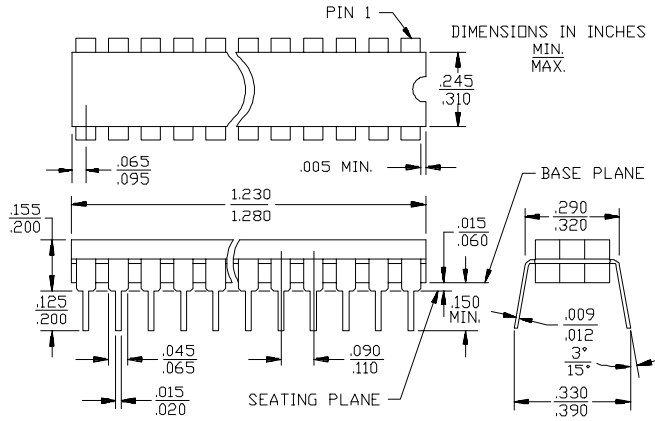
**Switching Characteristics**

| Parameter | Subgroups |
|-----------|-----------|
| $t_{PD}$  | 9, 10, 11 |
| $t_{CO}$  | 9, 10, 11 |
| $t_S$     | 9, 10, 11 |
| $t_H$     | 9, 10, 11 |

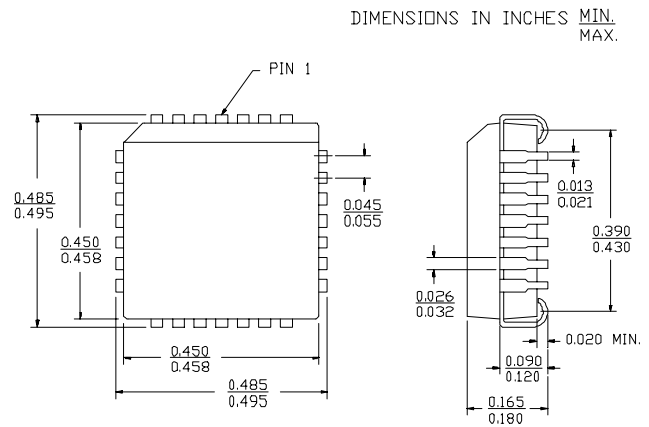
Document #: 38-00185-H

## Package Diagrams

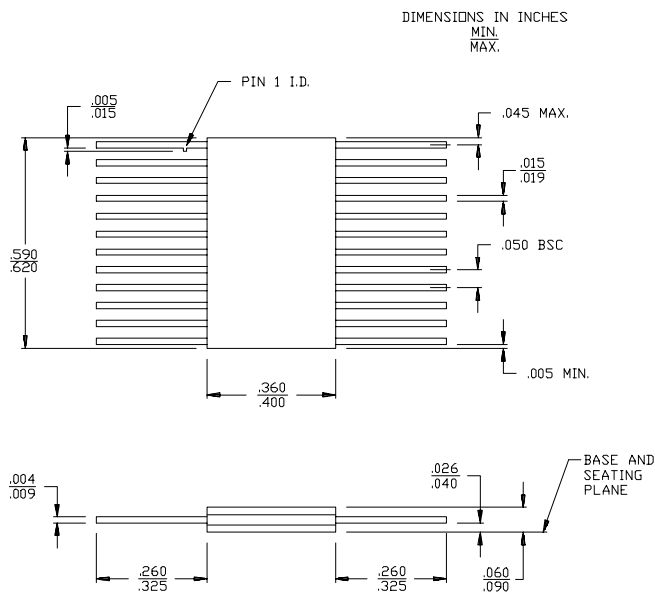
**24-Lead (300-Mil) CerDIP D14**  
MIL-STD-1835 D-9 Config. A



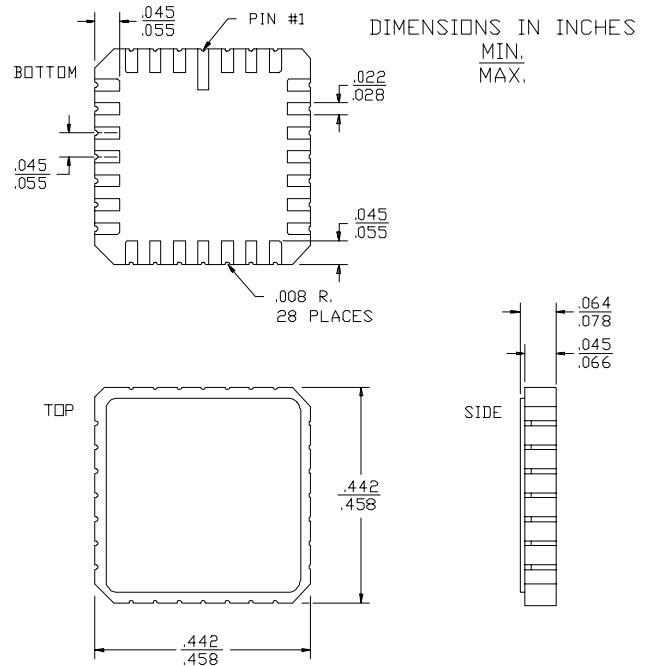
**28-Lead Plastic Leaded Chip Carrier J64**



**24-Lead Rectangular Cerpack K73**  
MIL-STD-1835 F-6 Config. A



**28-Square Leadless Chip Carrier L64**  
MIL-STD-1835 C-4



**Package Diagrams (continued)**
**24-Lead (300-Mil) Molded DIP P13/P13A**
