32-BIT ARM926EJ-S RISC PROCESSOR

- 103, 155, 177 MHz
- 5-stage pipeline
- Harvard architecture
- 8 kB I-cache and 4 kB D-cache
- 32-bit ARM and 16-bit Thumb instruction sets, can be mixed for performance/code density tradeoffs
- MMU to support virtual memory based OS's such as Linux, WinCE/Pocket PC, VxWorks, etc.
- DSP instruction extensions: improved divide, single cycle multiply accumulate
- ARM Jazelle, 1060 CM (Caffeine Marks) Java Accelerator
- Embedded ICE-RT debug unit
- JTAG boundary scan support
- Clock-gated processor for decreased power dissipation

EXTERNAL SYSTEM BUS INTERFACE

- 32-bit data bus, 28-bit external address bus
- Glueless interface to SDRAM, SRAM, EEPROM, buffered DIMM, Flash
- Up to 256 MB SDRAM, up to 2 GB DIMM
- 4 static and 4 dynamic chip selects
- 0-63 wait states per chip select
- Self-refresh during system sleep
- Automatic dynamic bus sizing to 8-bits, 16-bits, 32-bits
- Burst-mode support with automatic data width adjustment
- 2 external DMA channels for external peripheral support

SYSTEM BOOT

- High-speed boot from 8-bit, 16-bit, or 32-bit ROM or Flash
- Hardware-supported low cost boot from serial EEPROM through SPI port (patent pending)

OPTIMIZED 10/100 ETHERNET MAC

- MII or RMII PHY interfaces
- Full or half duplex
- Station, broadcast, multicast address filtering
- 2 kB Rx FIFO
- 256 B Tx FIFO with on-chip buffer descriptor ring (eliminates underruns and decreases bus traffic)
- Separate Tx and Rx DMA channels
- Intelligent receive-side buffer size selection
- Support for full statistics gathering
- Support for external CAM filtering

FLEXIBLE LCD CONTROLLER

- Supports commercially available displays up to SVGA
- Active-matrix color TFT displays
- Up to 18 bpp; 256K colors
- Single and dual-panel color passive-matrix displays
  - Up to 16 bpp 4:4:4 RGB; 3375 colors
- Single and dual-panel monochrome STN displays
- 1, 2, 4 bpp palletized grayscale
- Formats image data and generates timing control signals
- Internal programmable palette-LUT and grayscaler support different color techniques
- Programmable panel-clock frequency

USB PORTS

- USB v.2.0 Full Speed (12 Mbps) and low speed (1.5 Mbps)
- OHCI host and 11 end points device
- Single PHY can be used with either host or device
- Interface to external PHY for simultaneous host and device operation
- USB host is a bus master
- Each USB device endpoint is supported by a dedicated DMA channel, 13 total
- 20 B Rx FIFO and 20 B Tx FIFO

SERIAL PORTS

- 4 serial modules, each independently configurable to UART mode, SPI master mode, or SPI slave mode
- Bit rates from 75 bps to 1.8 Mbps: asynchronous x8 mode
- Max bit rates for synchronous mode are:
  - 1/16 CPU speed for SPI master
  - 1/32 CPU speed for SPI slave
- UART provides:
  - High-performance hardware and software flow control
  - Odd, even, or no parity
  - 5, 6, 7 or 8 bits
  - 1 or 2 stop bits
  - Receive-side character and buffer gap timers
- Internal or external clock support for synchronous mode
- 4 receive-side data match detectors
- 2 dedicated DMA channels per module, 8 total
- 32 B Tx FIFO and 32 B Rx FIFO per module

I²C PORT

- I²C v.1.0, configurable to master or slave mode
- Bit rates: fast (400 kHz) or normal (100 kHz) with clock stretching
- 7-bit and 10-bit address modes

1284 PARALLEL PERIPHERAL-TO-HOST PORT

- All standard modes:
  - ECP, Byte, Nibble, Compatibility
- RLE (Run Length Encoding) decoding of compressed data in ECP mode
- Operating clock from 100 kHz to 2 MHz
- 4 dedicated DMA channels
  - 2 for data and 2 for control
- Microsoft Plug-and-Play, no Windows driver needed

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Hardware Specifications

SYSTEM BUS DMA

- Every system bus peripheral is a bus master with dedicated DMA engine
- Deterministic bus bandwidth allocation (patent pending)

EXTERNAL PERIPHERAL DMA

- 2-channel DMA engine
- Supports memory-to-memory transfers

POWER MANAGEMENT

- Power save during normal operation
- Disables unused modules
- Power save during sleep mode
  - Sets SDRAM to self-refresh mode
  - Individually disables every module except selected wakeup modules
  - Wakeup on valid packets or characters
- Patent pending technology

VECTORED INTERRUPT CONTROLLER

- Holds pointers to all interrupt service routines for rapid service
- Services all peripherals
- Hardware interrupt prioritization

GENERAL PURPOSE TIMERS/CONTROLLERS/PWM

- 8 independent 16- or 32-bit programmable timers, counters, or 4 PWM functions
- Each has an I/O pin
- Mode selectable into:
  - Internal timer mode®
  - External gated timer mode
  - External event counter
  - PWM
- Timers/counters can be concatenated
- Minute-range events measurable
- Source clock selectable
- Internal clock or external pulse event
- Individually enabled/disabled

SYSTEM TIMERS

- Watchdog timer
- System bus monitor timer
- Peripheral bus monitor timer

GENERAL PURPOSE I/O

- 73 programmable GPIO pins (muxed with other functions)
  - Includes 7 high-current (8 mA) GPIO pins
- Software-readable power-up status registers for customer-defined bootstrapping

EXTERNAL INTERRUPTS

- 4 external programmable interrupts
  - Rising- or falling-edge sensitive
  - Low- or high-level sensitive

REAL TIME CLOCK

- Time of day clock
- Alarm
- 100 year calendar
- Programmable periodic interrupt
- 10 ms resolution
- Dedicated time domain in the system PLL
  - RTC-only mode available
- Initial time from network through SNTP routine
  - No battery backup
- Additional benefits
  - Frees CPU from math calculations
  - Decreased response time for queries

MICROSOFT® WINDOWS® CE SUPPORT

- Complete Windows CE 5.0 Board Support Package (BSP)
- Custom-developed drivers to support peripherals, modules and Development Kits
- Exclusive software to provide debugging channel via Ethernet connection

CLOCK GENERATOR

- Low cost external crystal
- Internal Phase-Locked Loop (PLL)
- Software programmable PLL parameters
- Optional external oscillator
- Separate oscillator for USB

OPERATING VOLTAGE

- Core: 1.5V ± 0.1V
- I/O ring: 3.3V ± 10%

OPERATING FREQUENCY

- 103 MHz: 0° C to 70° C
- 155 MHz: -40° C to 85° C
- 177 MHz: 0° C to 70° C

POWER CONSUMPTION

- 177 MHz: 0.64 W
- 155 MHz: 0.59 W
- 103 MHz: 0.52 W

PACKAGE

- 272-pin BGA including 16 thermal balls
- 1.27 mm ball pitch
- 27 mm x 27 mm
- Lead-free, RoHS compliant

LINUX SUPPORT (LXNETES)

- Based on Linux 2.6.x kernel
- Complete GNU ToolSuite of compilers and debuggers
- Bootloader for managing and installing software updates

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NET+Works Integrated Development Package

NET+ARM network-attached processors are the core of the NET+Works family of solutions that add intelligence and connectivity to electronic devices. We offer extensive networking software to support industrial automation, building automation, point-of-sale, office automation and other enterprise applications.

DEVELOPMENT TOOLS

- Green Hills® MULTI® IDE or Microcross GNU X-Tools™

RTOS

- ThreadX® picokernel

BOARD SUPPORT PACKAGE

- 10/100Base-T Ethernet
- UART
- SPI
- HDLC
- I^2C
- Flash
- USB host & device
- LCD
- 1284 peripheral
- Power save

NETWORKING PROTOCOLS

- TCP/IP stack
- TCP and UDP Sockets API
- ICMP
- IGMP
- PPP for serial communications
- Address Configuration Executive (ACE):
  - ARP
  - RARP
  - Ping ARP
  - AutoIP
  - DHCP client
  - BootP
- Fast IP
- Fast sockets
- SSL, TLS

NETWORKING SERVICES

- FTP server/client; TFTP
- LDAPv3 agent, for access to network information services
- HTTP APIs for serving basic and advanced web pages
- HTTPS for security
- Email (POP3 and SMTP)
- SNMP v1/MIBII for remote management
- SNTP
- DNS
- Telnet
- Multi-homing

UTILITIES

- HTML compilation
- MIB compilation
- Download of Flash images
- Bootloader
- Code builds
- Integrated flash file system
- Code Profiler
- Boundary Scan Description Language (BSDL)

TECHNICAL SUPPORT

- One year of software maintenance and technical support

DEVELOPMENT BOARD

- NS9360 development board and JTAG debugger

MODEL.....PART NUMBERS

Model	Worldwide
103 MHz, 0° C to 70° C operation	NS9360B-0-C103
155 MHz, -40° C to 85° C operation	NS9360B-0-I155
177 MHz, 0° C to 70° C operation	NS9360B-0-C177

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