Table of Contents

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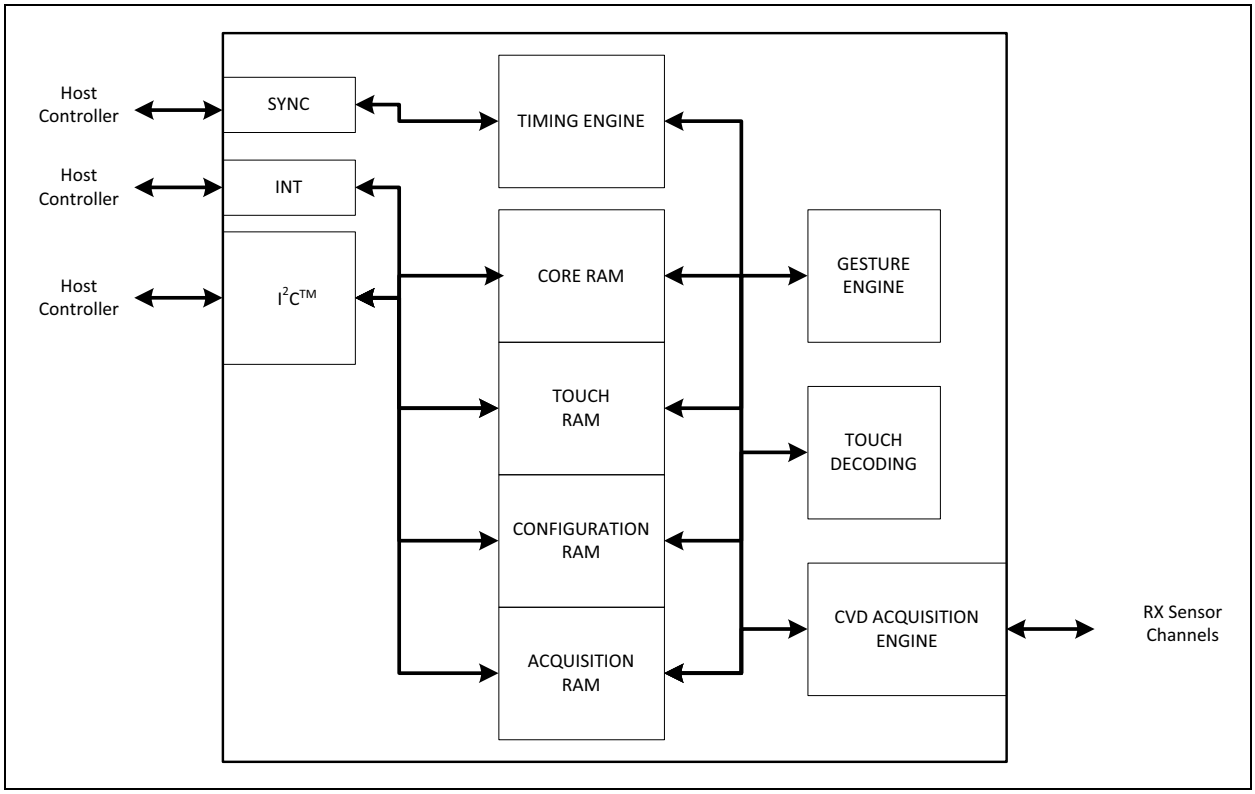
1.0 MTCH6102 BLOCK DIAGRAM

FIGURE 1-1: MTCH6102 BLOCK DIAGRAM



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2.0 PIN DIAGRAMS

FIGURE 2-1: 28-PIN UQFN (4X4)

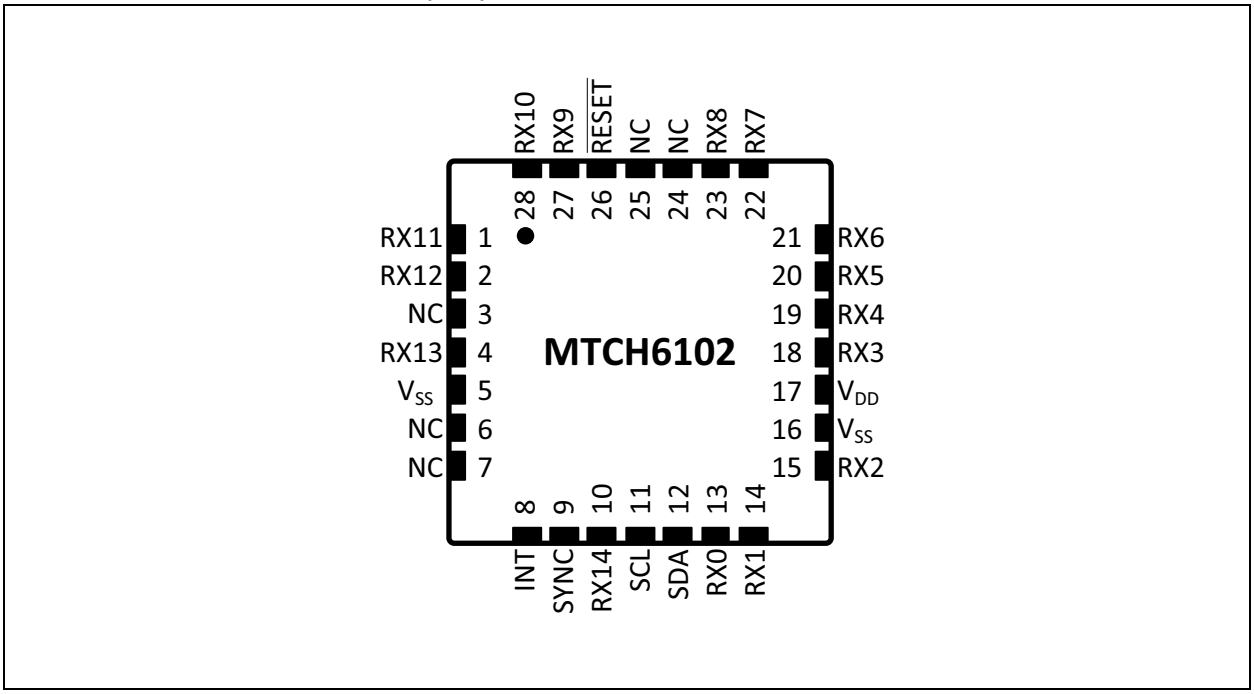
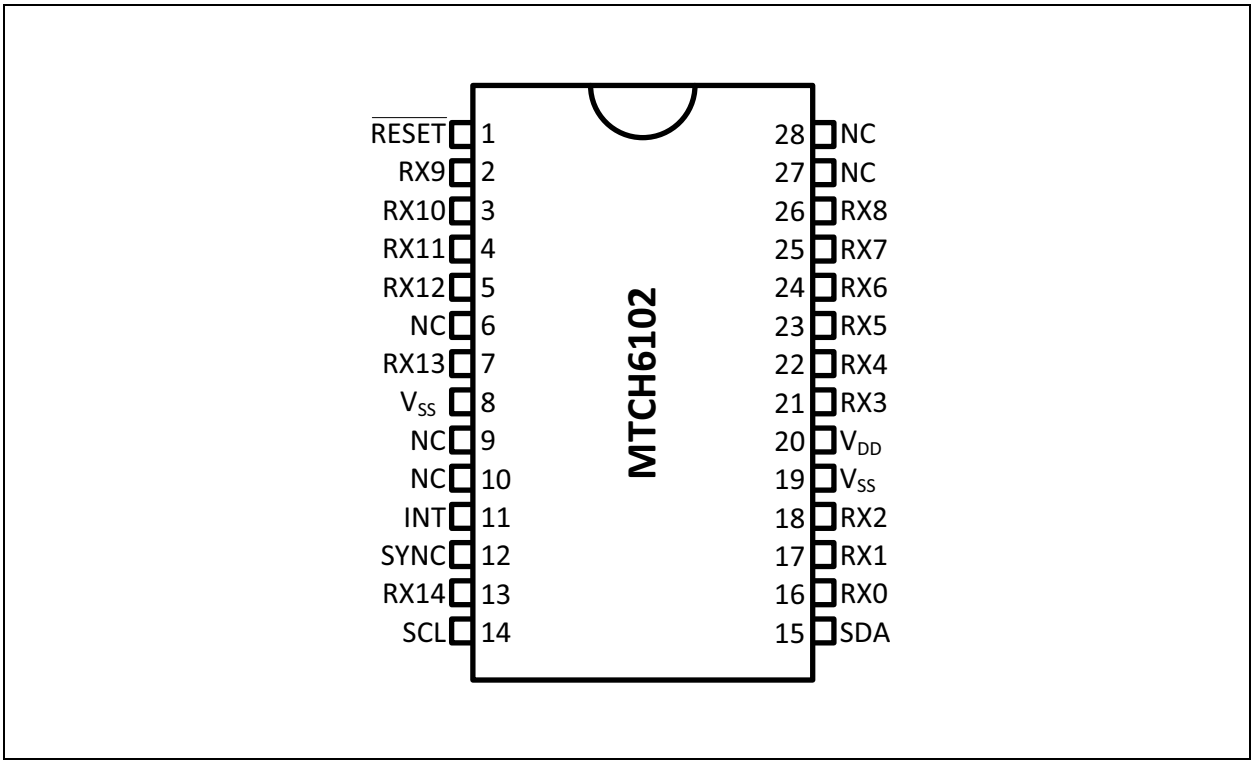


FIGURE 2-2: 28-PIN SSOP



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3.0 MTCH6102 PINOUT DESCRIPTION

TABLE 3-1: MTCH6102 PINOUT DESCRIPTION

Pin Name	UQFN Pin	SSOP Pin	Pin Type	Description
$\overline{\text{RESET}}$	26	1	I	Master Reset with Internal Pull-up
SCL	11	14	I/O	I^2C™ Clock
SDA	12	15	I/O	I^2C Data Input/Output
INT	8	11	O	Interrupt Request Output
SYNC	9	12	O	Synchronous Frame Output
RX0	13	16	I/O	Touch Sensor Channel Input
RX1	14	17	I/O	
RX2	15	18	I/O	
RX3	18	21	I/O	
RX4	19	22	I/O	
RX5	20	23	I/O	
RX6	21	24	I/O	
RX7	22	25	I/O	
RX8	23	26	I/O	
RX9	27	2	I/O	
RX10	28	3	I/O	
RX11	1	4	I/O	
RX12	2	5	I/O	
RX13	4	7	I/O	
RX14	10	13	I/O	
V_{DD}	17	20	Power	Positive Supply
V_{SS}	5,16	8,19	Power	Ground Reference
N/C	3, 6, 7, 24, 25	6, 9, 10, 27, 28	N/C	No Connect

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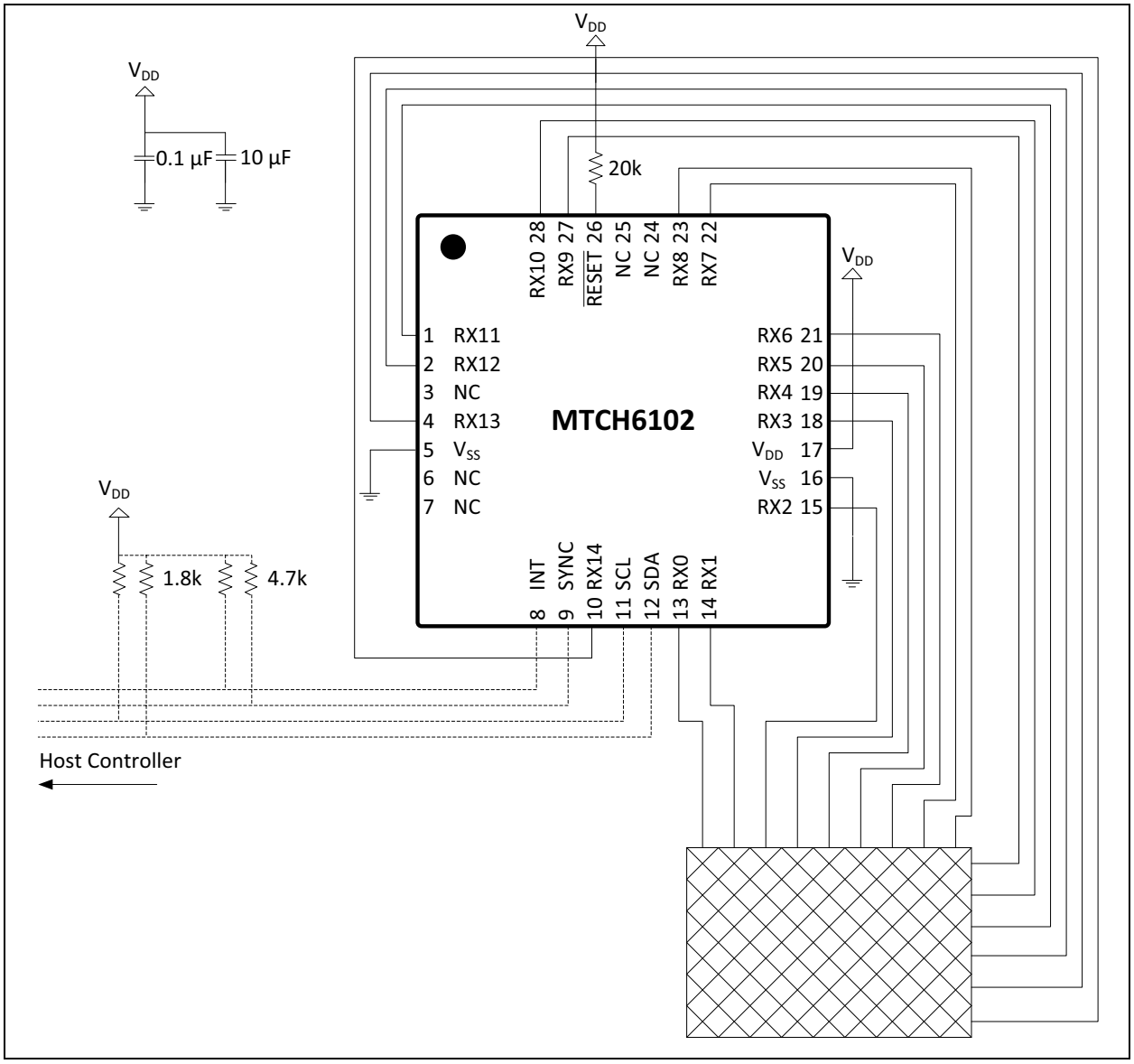
4.0 LAYOUT

FIGURE 4-1: TYPICAL APPLICATION CIRCUIT



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4.1 Decoupling Capacitors

The use of decoupling capacitors on power-supply pins, such as VDD and VSS, is required. Consider the following criteria when using decoupling capacitors:

1. Value and type of capacitor:

A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.

2. Placement on the Printed Circuit Board:

The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.

3. Handling high-frequency noise:

If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above-described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible (for example, 0.1 µF in parallel with 0.001 µF).

4. Maximizing performance:

On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. It is equally important to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

4.2 Bulk Capacitors

The use of a bulk capacitor is recommended to improve power-supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

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5.0 COMMUNICATION

5.1 I²C Pin Specification

5.1.1 DESCRIPTION

The MTCH6102 low-power projected capacitive touch controller uses a standard register-based read/write I²C protocol based upon the memory map. This protocol is similar to many other devices such as temperature sensors and serial EEPROMs. Although data can be read at any time (polling), an interrupt pin (INT) is provided for flexible integration options.

5.1.2 READING/WRITING REGISTERS

To access memory (both to read or write), the I²C transaction must start by addressing the chip with the Write bit set, then writing out a single byte of data representing the memory address to be operated on. After that, the host can choose to do either of the following (see Figure 5-1):

1. To write memory, continue writing [n] data bytes (see Figure 5-2).
2. To read memory, restart the I²C transaction (via either a Stop-Start or Restart), then address the chip with the Read bit set. Continue to read in [n] data bytes (see Figure 5-3).

During either of these transactions, multiple bytes within the same block may be read or written due to the device's address auto-increment feature. See **Section 17.0 "Memory Map"** for block separation.

FIGURE 5-1: I²C™ TRANSACTION DIAGRAM

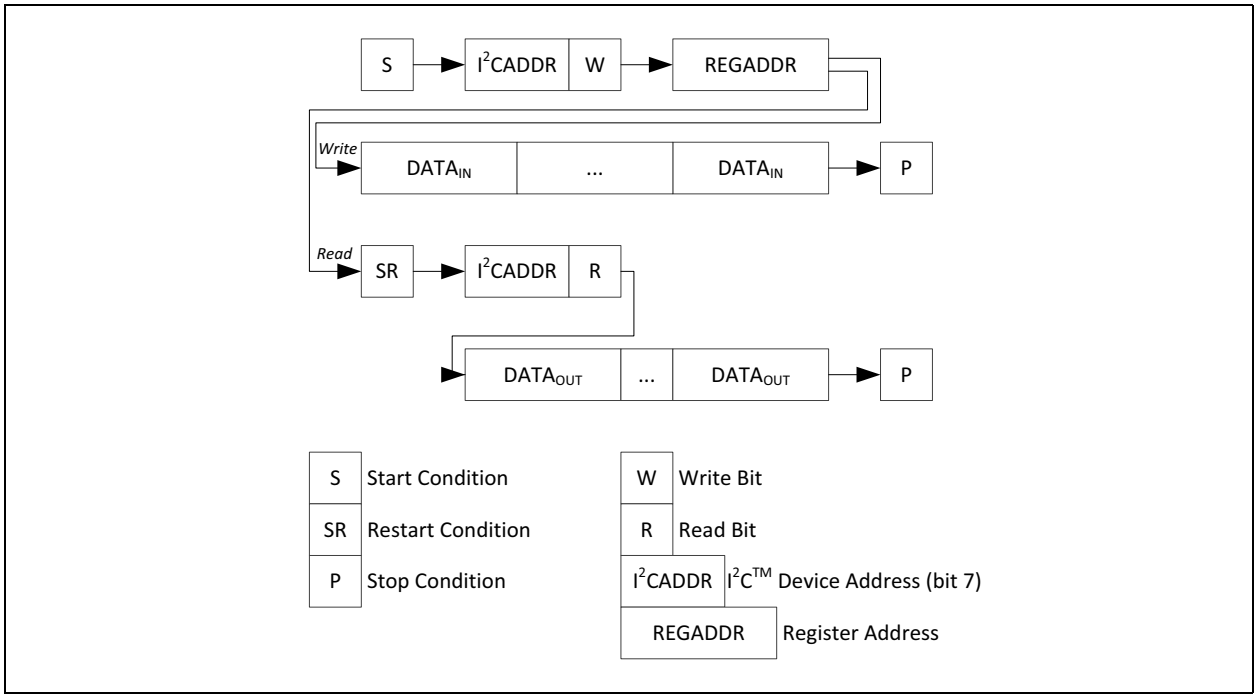


FIGURE 5-2: EXAMPLE I²C™ WRITE TRANSACTION

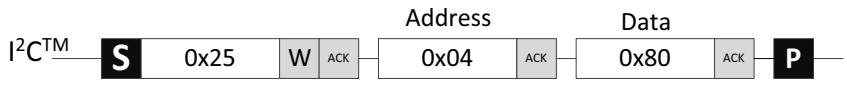
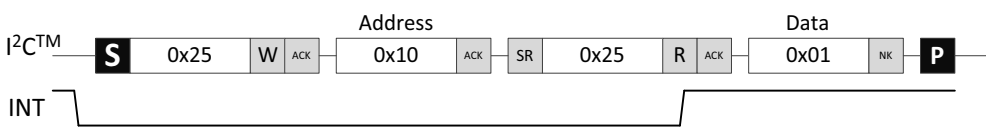


FIGURE 5-3: EXAMPLE I²C™ READ TRANSACTION



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5.1.3 DEVICE ADDRESSING

The MTCH6102 default 7-bit base address is 0x25. Every transmission must be prefixed with this address, as well as a bit signifying whether the transmission is a master write ('0') or master read ('1'). After appending this Read/Write bit to the base address, this first byte becomes either 0x4A (write) or 0x4B (read).

This address can be modified (see I²CADDR), but this requires initially communicating with the device under the default address. If this is not feasible in the user's application, contact Microchip support for additional options.

5.2 Interrupt Pin

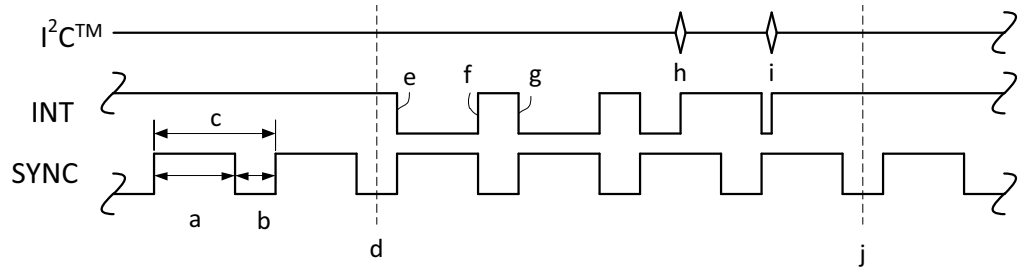
MTCH6102 provides an open-collector active-low Interrupt pin (INT) that will be asserted any time new data is available. INT is automatically released under two conditions:

1. A read is performed of *any* register within the device.
2. The next frame of decoding has started.

5.3 SYNC Output Pin

MTCH6102 provides an active-high sync signal that correlates with the current touch frame status. The SYNC pin is low while the device is sleeping (between frames) and high while touch sensing/decoding is occurring. A common use of this pin includes a host that makes use of data on every frame (such as raw-acquisition data), for host-side decoding (see Figure 5-4).

FIGURE 5-4: EXAMPLE INT/SYNC LOGIC



a	Controller sleeping
b	Controller decoding
c	Touch frame
d	Finger is present
e	INT asserted due to (d)

f	INT is released as controller goes to Sleep
g	INT is asserted due to (d)
h	INT is released due to I²C™ read
i	INT is released due to I²C™ read
j	Finger is not present

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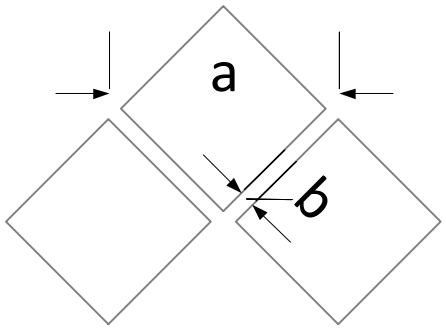
6.0 SENSOR DESIGN CONSIDERATIONS

6.1 General Guidelines

FIGURE 6-1: DIAMOND DIMENSION GUIDELINES



Dim.	Typ.	Min.	Max.
a	6 mm	4 mm	10 mm
b	0.2 mm	—	0.5 mm

6.1.1 PROTOTYPING DESIGNS

Touch sensor designs typically require a thorough debugging phase to ensure a reliable product. If possible, it is suggested that flexible prototyping hardware be created with this in mind. A common example is providing external access to the communication lines for quick test and tuning while in-circuit.

6.1.2 SENSOR OVERLAY MATERIAL

To prevent saturation of sensor levels, a minimum overlay of 0.5 mm plastic or glass is required for proper operation of the device, even during a prototyping phase, even if this value is different than the final design.

Note:	At no time should the device be expected to respond correctly to a user touching a bare PCB sensor.

6.1.3 OPERATION WITH AN LCD

MTCH6102 has integrated algorithms to detect and minimize the effects of noise, but proper care should always be taken in selecting an LCD and support components with a focus on reducing noise as much as possible. Since the interaction between the touch sensor and display is highly dependent upon the physical arrangement of the components, proper testing should always be executed with a fully integrated device. Please reference the appropriate projected capacitive touch screen manufacturer's integration guide for additional design considerations.

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6.2 Sensor Layout Configuration

TABLE 6-1: REGISTERS ASSOCIATED WITH SENSOR LAYOUT CONFIGURATION

Address	Name	Description
0x20	NUMBEROFXCHANNELS	Number of channels used for X axis
0x21	NUMBEROFYCHANNELS	Number of channels used for Y axis

MTCH6102 is designed to work with sensors with a minimum of 3x3 sensor channels, and a total maximum of 15 channels. The number of channels on each axis is governed by the registers in Table 6-1. For all sensor configurations, the following conditions must be met:

1. Channel layout must start at RX0.
2. Each axis must have the associated channels in either ascending or descending order.
3. No unconnected channel pins are allowed in the middle of a layout.

Table 6-2 shows an example of each rule being broken by a 6x5 sensor layout, followed by the correct layout in the last column.

TABLE 6-2: EXAMPLE OF INCORRECT 6X5 SENSOR CONNECTIONS

	(1)	(2)	(3)	Correct
RX0		X0	X0	X0
RX1		X1	X1	X1
RX2		X2	X2	X2
RX3		X4	X3	X3
RX4	X0	X3	X4	X4
RX5	X1	X5	X5	X5
RX6	X2	Y0		Y0
RX7	X3	Y2		Y1
RX8	X4	Y1	Y0	Y2
RX9	X5	Y3	Y1	Y3
RX10	Y0	Y4	Y2	Y4
RX11	Y1		Y3	
RX12	Y2			
RX13	Y3		Y4	
RX14	Y4			

6.3 Sensor Output Resolution

MTCH6102 interpolates 64 discrete points between each channel and 32 points past the centerline of each edge. As a result, the maximum value in the TOUCHX and TOUCHY registers will be (64xNUMBEROFCHANNELS) on each axis. For the default 9x6 sensor, this results in a maximum resolution of 576x384.

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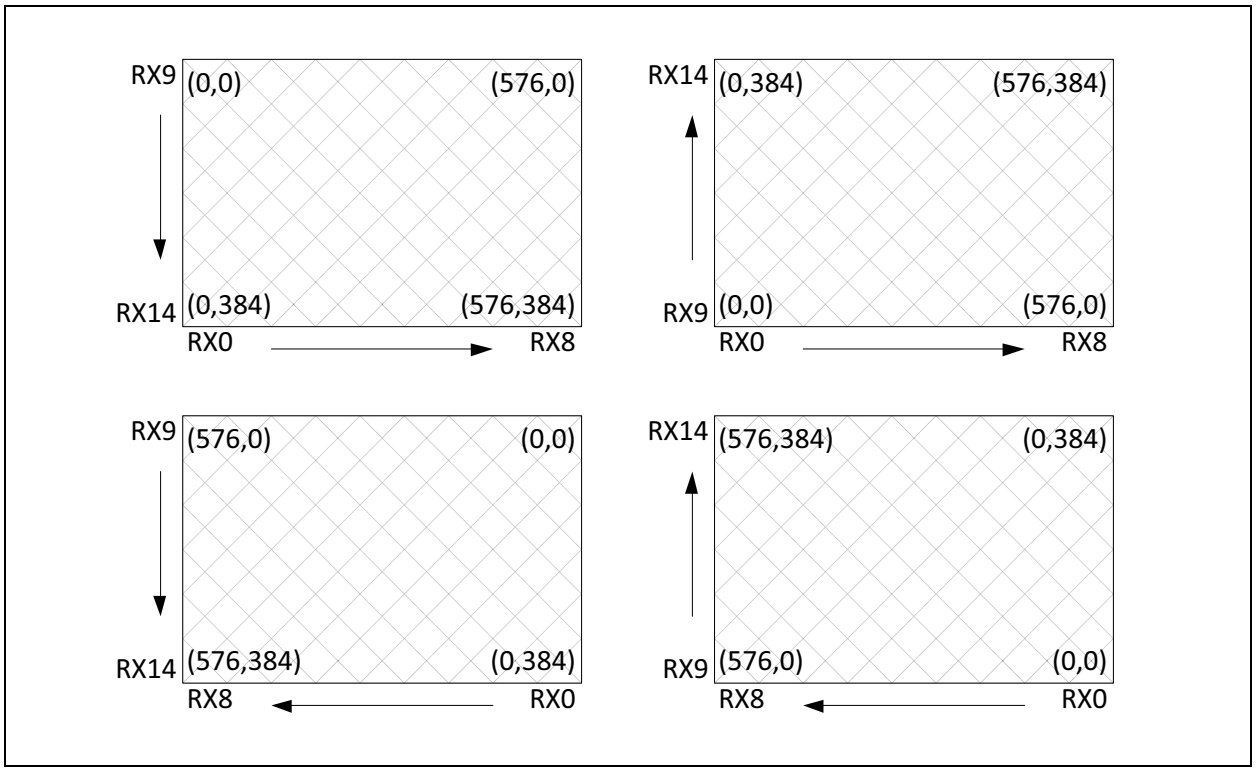
6.4 Sensor Orientation

To aid in PCB layout, the sensor can be oriented in any direction, have either axis reversed, or even have the axes swapped. The host controller must take into account the X/Y output and gesture orientation based on Figure 6-2.

FIGURE 6-2: SENSOR ORIENTATION EXAMPLES



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7.0 OPERATING MODES

MTCH6102 operates in multiple modes (see Table 7-1) governed by the MODE register (see Register 7-1).

TABLE 7-1: OPERATING MODE DESCRIPTIONS

Mode Name	Description	INT Behavior
Full	Full X/Y and gesture decoding occurs (Default mode)	Asserted if touch is present or if a change in touch status or a gesture have occurred
Touch	Full X/Y decoding only	Asserted if touch is present or if a change in touch status occurs
Gesture	Full X/Y and gesture decoding occurs, but INT is no longer asserted for touch data	Asserted for gestures only(1)
Raw	Raw-capacitance signals are stored in RAWADC registers, no decoding done. Channel selection and type of measurement is governed by the MODECON register	None
Standby	Device is no longer sensing or performing baseline tasks	None

Note 1: Data in TOUCH registers is still valid.

REGISTER 7-1: MODE: TOUCH DECODE MODE REGISTER

U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-1	R/W-1
—	—	—	—	MODE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	x = Bit is unknown	-n = Value after initialization (default)
W = Writable bit	'0' = Bit is cleared	U = Unimplemented bit	q = Conditional

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **MODE<3:0>:** Touch Decoding mode bits

0000 = Standby
0001 = Gesture
0010 = Touch only
0011 = Full (touch and gesture)
01XX = Raw ADC

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REGISTER 7-2: MODECON: RAWADC MODE CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TYPE<3:0>				CH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	x = Bit is unknown	-n = Value after initialization (default)
W = Writable bit	'0' = Bit is cleared	U = Unimplemented bit	q = Conditional

bit 7-4 **TYPE<3:0>:** CVD Result Arithmetic bits

0000 = (1023 – Result1) + Result 2
0001 = Result 1 only
0010 = Result 2 only

bit 3-0 **CH<3:0>:** RX Sense Channel bits

0000 = RX0
..
..
1110 = RX14
1111 = Reserved, do not use

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8.0 CONTROLLER COMMANDS

Various controller commands can be initiated by writing a '1' to the appropriate bit in the CMD register (Register 8-1). This bit will automatically be cleared after the command has been completed.

REGISTER 8-1: CMD: COMMAND REGISTER

R/W-0	R/W-0	R/W-0	U-x	R/W-0	U-x	U-x	R/W-0
NV	DEF	CFG	—	MFG	—	—	BS
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	x = Bit is unknown	-n = Value after initialization (default)
W = Writable bit	'0' = Bit is cleared	U = Unimplemented bit	q = Conditional

bit 7 **NV:** Nonvolatile Storage Write bit

bit 6 **DEF:** Restore Controller to Default Configuration Values bit

bit 5 **CFG:** Configure Controller bit (after parameters have been changed)

bit 4 **Unimplemented:** Read as '0'

bit 3 **MFG:** Execute Manufacturing Test bit

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **BS:** Force Baseline bit (recalibration) to occur

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9.0 TOUCH FRAME CONTROL

Touch decoding is based around the concept of a touch *frame* that begins with acquisition, followed by decoding of the acquired values, and lastly a Sleep phase for power savings. The duration of the touch frame is governed by the current touch state, as well as the timing registers outlined in this section (see Table 9-1). Figure 9-1 shows the interaction between these registers during a typical touch cycle.

TABLE 9-1: REGISTERS ASSOCIATED WITH TOUCH FRAME CONTROL

Address	Name	Description
0x25	ACTIVEPERIODL	Active Period
0x26	ACTIVEPERIODH	
0x27	IDLEPERIODL	Idle Period
0x28	IDLEPERIODH	
0x29	IDLETIMEOUT	Idle Timeout
0x2B	DEBOUNCEUP	Liftoff Debounce
0x2C	DEBOUNCEDOWN	Touch Down Debounce

Both active and idle period calculations are as shown in Equation 9-1.

EQUATION 9-1:

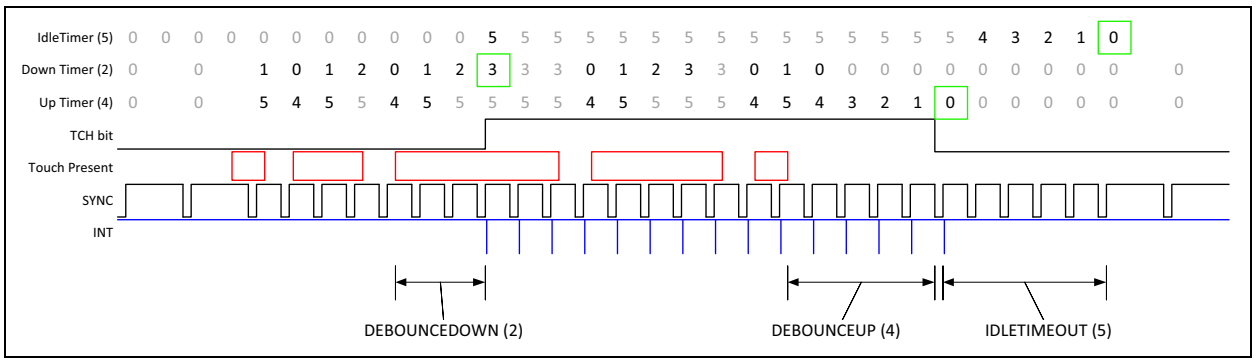
$$\left(\frac{Duration(ms) \times 1000}{31}\right) + 1 = PERIOD$$

Typical frame rates have been computed for the user's convenience and are shown in Table 9-2.

TABLE 9-2: EXAMPLE FRAME RATE PERIOD CALCULATIONS

Desired Rate (ms)	Period
10	0x0142
20	0x0284
50	0x064C
100	0x0C99

FIGURE 9-1: TOUCH FRAME TIMING



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10.0 TOUCH DATA REGISTERS

REGISTER 10-1: TOUCHSTATE: CURRENT TOUCH STATE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-x	R/W-0	R/W-0	R/W-0
FRAME<3:0>				—	LRG	GES	TCH
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	x = Bit is unknown	-n = Value after initialization (default)
W = Writable bit	'0' = Bit is cleared	U = Unimplemented bit	q = Conditional

bit 7-4 **FRAME<3:0>:** Increments on Every Touch Frame
bit 3 **Unimplemented:** Read as '0'
bit 2 **LRG:** Large Activation is Present
bit 1 **GES:** Gesture is Present
bit 0 **TCH:** Touch is Present

REGISTER 10-2: TOUCHLSB REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TOUCHX<3:0>				TOUCHY<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	x = Bit is unknown	-n = Value after initialization (default)
W = Writable bit	'0' = Bit is cleared	U = Unimplemented bit	q = Conditional

bit 7-4 **TOUCHX<3:0>:** Current X Position (Least Significant bits)
bit 3-0 **TOUCHY<3:0>:** Current Y Position (Least Significant bits)

TABLE 10-1: SUMMARY OF REGISTERS ASSOCIATED WITH TOUCH DATA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	TOUCHSTATE	FRAME<3:0>				—	LRG	GES	TCH
0x11	TOUCHX	TOUCHX<11:4>							
0x12	TOUCHY	TOUCHY<11:4>							
0x13	TOUCHLSB	TOUCHX<3:0>				TOUCHY<3:0>			

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11.0 ACQUISITION AND TOUCH PARAMETERS

TABLE 11-1: REGISTERS ASSOCIATED WITH ACQUISITION AND TOUCH PARAMETERS

Address	Name	Default
0x22	SCANCOUNT	6
0x23	TOUCHTHRESHX	55
0x24	TOUCHTHRESHY	40
0x2A	HYSTERESIS	4
0x31	FILTERTYPE	2
0x32	FILTERSTRENGTH	1
0x35	LARGEACTIVATIONTHRESHL	0
0x36	LARGEACTIVATIONTHRESHH	0

11.1 SCANCOUNT

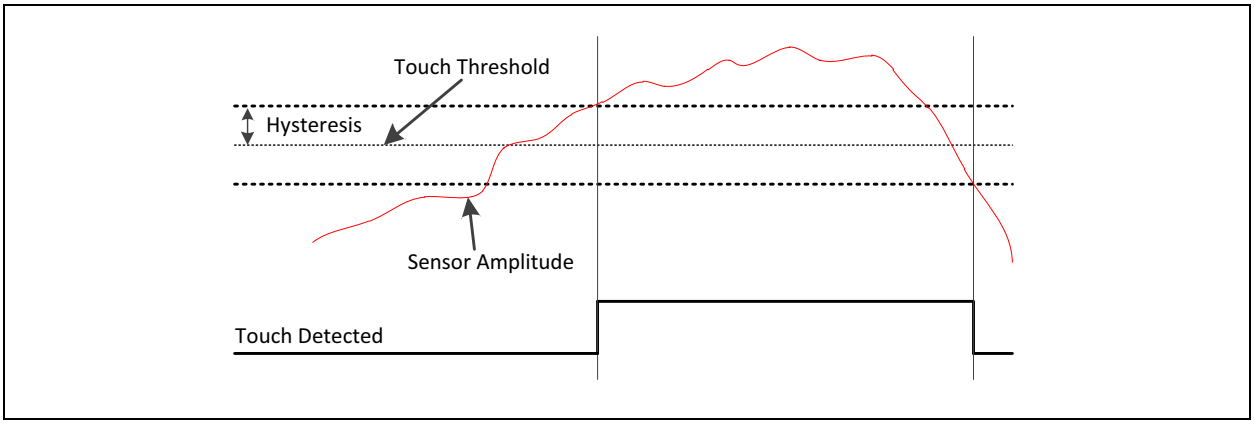
Every time a channel is scanned, it is scanned multiple times (SCANCOUNT) and summed. Increasing this number will give an inherent averaging effect, but at the cost of time and subsequently increased power consumption.

11.2 TOUCHTHRESHX/ TOUCHTHRESHY and HYSTERESIS

The presence of a touch is determined by the sensor channel's current value compared to the touch thresholds set by TOUCHTHRESHX (or TOUCHTHRESHY if the channel is on the Y axis).

The HYSTERESIS register contains a threshold modifier that acts as a dynamic threshold modifier depending on the state of the touch (higher without a touch). A single channel of touch is shown in Figure 11-1.

FIGURE 11-1: TOUCH THRESHOLD AND HYSTERESIS FUNCTIONALITY



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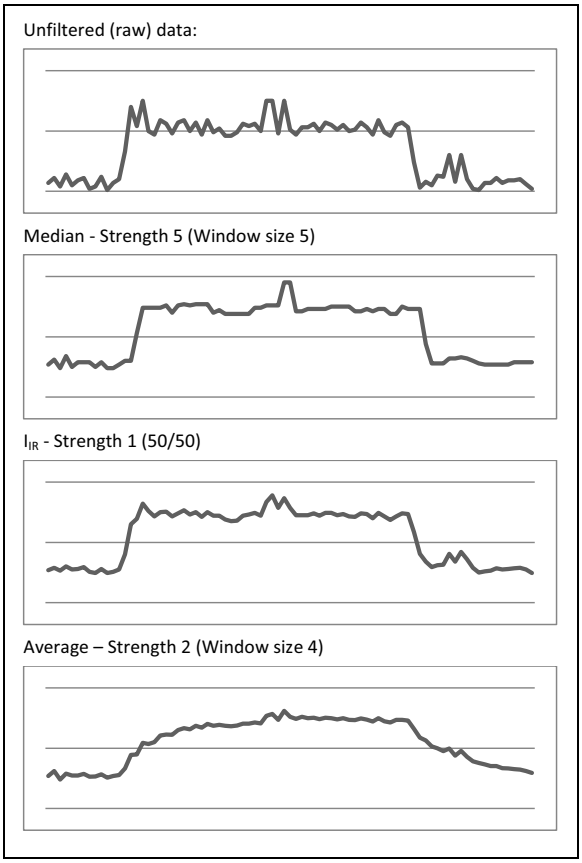
11.3 FILTERTYPE/FILTERSTRENGTH

As new sensor values are acquired, they are filtered based on the settings of the FILTERTYPE/ FILTERSTRENGTH registers (see Table 11-2). Examples of the effects of each filter type are shown in Figure 11-2.

TABLE 11-2: FILTERTYPE AND FILTERSTRENGTH DEFINITIONS

FILTERTYPE	FILTERSTRENGTH	Valid Values
0 – No Filter	N/A	—
1 – Median	Size of median window	3, 5, 7, 9
2 – IIR	Weighting of previous to current value	1, 2, 3 (1/2, 1/4 and 1/8 weighting accordingly)
3 – Average	Size of average window	1, 2, 3 (2, 4 and 8 accordingly)

FIGURE 11-2: FILTER EXAMPLES



Choosing the correct filtering option for the user's application depends on the environment and sensor. Note that while the median filter has good characteristics, it is not the most efficient and will consume more power than other filters.

11.4 Large Activation

The LARGEACTIVATIONTHRESH registers provide a way to do simple rejection of signals that are too large to interpret. The amplitude of all sensor channels are added together and compared to this threshold. If greater, the LRG bit of the TOUCHSTATE register (Register 10-1) will be set.

Note that this does not affect touch decoding. In other words, even if the large activation threshold is breached, the controller will still decode the touch position as normal. The LRG bit merely serves to inform the host that the large activation threshold has been reached.

If this functionality is not intended to be used, this register should be set to zero, which will disable the large activation routines from running.

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12.0 COMPENSATION RAM

It is very common for a typical touch sensor to have non-uniform capacitive properties. To equalize the sensor, a series of coefficients can be written to the compensation RAM block. These coefficients represent a ratio that is applied to the individual channel in post-acquisition, before touch decoding occurs.

EQUATION 12-1: COMPENSATION RAM CALCULATION

$$\frac{[RAW\ VALUE] \times SENSORCOMP}{64} = [FINAL\ VALUE]$$

To obtain the correct compensation RAM values, the following procedure should be used:

1. Set all SENSORVALUES registers to zero (if necessary).
2. Record the peak values that occur in the SENSORVALUES registers when using the sensor under normal conditions (column A of Table 12-1).
3. Pick a commonly occurring value to represent the median of the set (‘125’).
4. Calculate the ratio of the peak value by dividing the median value by the peak (column B).
5. Multiply this value by 64 and truncate (column C). These are the compensation values that should be written to the SENSORCOMP registers. Please note that, if no compensation is required (value of ‘64’, ratio of ‘1’), the register should be set to ‘0’, to save time running compensation routines for that channel.
6. To see the expected output from the compensation values, follow Equation 12-1 (result in column D).

TABLE 12-1: COMPENSATION RAM EXAMPLE CALCULATION

CH	A	B	C	D
0	102	1.225	78	124
1	113	1.106	71	125
2	118	1.059	68	125
3	125	1	64 (0)	125
4	125	1	64 (0)	125
5	128	0.977	63	126
6	132	0.947	61	126
7	160	0.781	50	125

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13.0 BASELINE

Capacitive touch principles rely on analyzing a change in capacitance from a previously-stored baseline value (sometimes referred to as a calibration value). Baseline routines and behavior can be tweaked using the registers listed in Table 13-1.

TABLE 13-1: REGISTERS ASSOCIATED WITH BASELINE

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x04	NV	DEF	CFG	-	MFG	-	-	BS	0
0x2D	BASEINTERVALL								10
0x2E	BASEINTERVALH								0
0x2F	BASEPOSFILTER								20
0x30	BASENEGFILTER								20
0x33	BASEFILTERTYPE								2
0x34	BASEFILTERSTRENGTH								1

13.1 BS Bit (CMD Register)

The BS bit forces the current sensor values to be stored as the baseline values, disregarding the constraints of BASEPOSFILTER and BASENEGFILTER.

13.2 BASEINTERVAL

It represents the number of touch frames between baseline sampling. Data that is sampled will be applied at the next baseline interval, provided that a touch has not occurred between the two.

If at any point, the touch threshold is breached, the baseline counter is reset, and a full interval without a touch must occur before baselining resumes.

Note that this value is specified in terms of the number of touch frames, so any changes in frame rate should take this into consideration by raising or lowering this interval accordingly.

13.3 BASEPOSFILTER/BASENEGFILTER

The positive and negative filters act as slew-rate limiters for a new baseline being applied. For example, if the new baseline value is larger than the previous by a value of 35, and the BASEPOSFILTER is set to 20 (default), the new baseline will only be increased by 20.

Use of these registers helps prevent unwanted spikes in the baseline value.

13.4 BASEFILTERTYPE/ BASEFILTERSTRENGTH

Baseline acquisition frames follow the same filter type and strength parameters as normal acquisition filters, defined in **Section 11.3 "FILTERTYPE/FILTER-STRENGTH"**.

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14.0 GESTURE FEATURES AND PARAMETERS

Gesture detection and reporting is governed by the registers outlined in Table 14-1.

TABLE 14-1: SUMMARY OF REGISTERS ASSOCIATED WITH GESTURES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x10	TOUCHSTATE	FRAME<3:0>				-	LRG	GES	TCH	N/A
0x14	GESTURESTATE	GESTURESTATE								0
0x15	GESTUREDIAG	GESTUREDIAG								0
0x37	HORIZONTALSWIPEDISTANCE	HORIZONTALSWIPEDISTANCE								64
0x38	VERTICALSWIPEDISTANCE	VERTICALSWIPEDISTANCE								64
0x39	SWIPEHOLDBOUNDARY	SWIPEHOLDBOUNDARY								25
0x3A	TAPDISTANCE	TAPDISTANCE								25
0x3B	DISTANCEBETWEENTAPS	DISTANCEBETWEENTAPS								64
0x3C	TAPHOLDTIME	TAPHOLDTIMEL								50
0x3D		TAPHOLDTIMEH								0
0x3E	GESTURECLICKTIME	GESTURECLICKTIME								12
0x3F	SWIPEHOLDTHRESH	SWIPEHOLDTHRESH								32
0x40	MINSWIPEVELOCITY	MINSWIPEVELOCITY								4
0x41	HORIZONTALGESTUREANGLE	HORIZONTALGESTUREANGLE								45
0x42	VERTICALGESTUREANGLE	VERTICALGESTUREANGLE								45

When a gesture is performed, the gesture ID will be placed in GESTURESTATE, and the GES bit of the TOUCHSTATE register will be set. Both of these items are cleared after reading the GESTURESTATE register. The GESTUREDIAG register contains a code explaining the logic behind the last operation of the gesture engine, primarily to help with debugging of the gesture parameters. These diagnostic codes are shown in Register 14-2.

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REGISTER 14-1: GESTURESTATE: CURRENT GESTURE STATE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GESTURESTATE<7:0>							
bit 7							bit 0

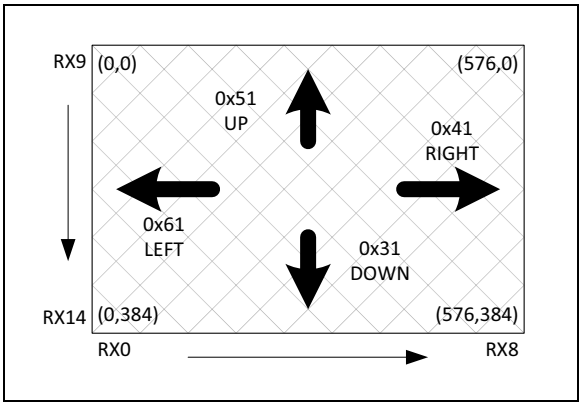
Legend:			
R = Readable bit	'1' = Bit is set	x = Bit is unknown	-n = Value after initialization (default)
W = Writable bit	'0' = Bit is cleared	U = Unimplemented bit	q = Conditional

bit 7-0 **GESTURESTATE<7:0>:**

0x00	No Gesture Present
0x10	Single Click
0x11	Click and Hold
0x20	Double Click
0x31	Down Swipe
0x32	Down Swipe and Hold
0x41	Right Swipe
0x42	Right Swipe and Hold
0x51	Up Swipe
0x52	Up Swipe and Hold
0x61	Left Swipe
0x62	Left Swipe and Hold

Please note that the gesture orientations listed in Register 14-1 are correct for a default layout, with *right* moving on increasing X-axis channels, and *down* moving on increasing Y-axis channels. These default orientations are shown in Figure 14-1. Depending on the application, the host may need to associate the gesture IDs differently.

FIGURE 14-1: GESTURE ORIENTATION



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REGISTER 14-2: GESTUREDIAG: GESTURE DIAGNOSTICS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GESTUREDIAG<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	'1' = Bit is set	x = Bit is unknown	-n = Value after initialization (default)
W = Writable bit	'0' = Bit is cleared	U = Unimplemented bit	q = Conditional

bit 7-0 **GESTUREDIAG<7:0>:**

0x01	Click Timeout
0x02	Swipe Timeout
0x03	General Timeout
0x04	Click Threshold Exceeded
0x05	Swipe Threshold Exceeded
0x06	Swipe and Hold Threshold Exceeded
0x07	Swipe Opposite Direction Threshold Exceeded
0x08	Reserved
0x09	Swipe and Hold Value Exceeded
0x0A	Outside Swipe Angle

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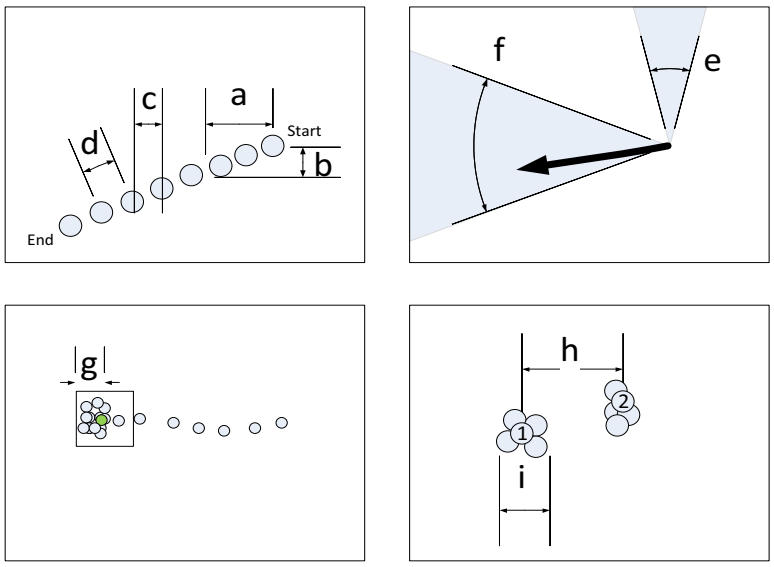
14.1 Gesture Tuning

FIGURE 14-2: GESTURE PARAMETER VISUALIZATION



Legend:

1. HORIZONTALSWIPEDISTANCE/VERTICALSWIPEDISTANCE (**a/b**): Distance that a touch must move from the initial touchdown to be considered a *swipe*.
2. SWIPEHOLDTHRESH (**c**): Allowed movement in the opposite direction before a swipe is canceled.
3. MINSWIPEVELOCITY (**d**): Once a movement is classified as a *swipe*, this distance must be kept frame to frame before the swipe is classified as a *hold* (direction of travel is not important).
4. HORITZONTALGESTUREANGLE/VERTICALGESTUREANGLE (**f/e**): Angle in degrees allowed on horizontal (X-axis) and vertical (Y-axis) swipe movements. Swipes outside this parameter are detected, but not reported.
5. SWIPEHOLDBOUNDARY (**g**): Once a swipe is classified as a *hold*, movement must not exceed this parameter in any direction.
6. DISTANCEBETWEENTAPS (**h**): Distance allowed between two taps to be considered a *double click*.
7. TAPDISTANCE (**i**): Even when a sensor is pressed for a very short time (click), multiple frames of touch data occur. This parameter governs how close those individual touch points must be for a *click*.
8. TAPHOLDTIME (not shown): Duration of time a click must be held for to be considered a *click and hold.*
9. GESTURECLICKTIME (not shown): Maximum time between two clicks to be considered a *double click.*

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15.0 CONFIGURING A NON-DEFAULT APPLICATION

When modifying sensor configuration parameters, the CFG bit of the CMD register must be set for the configuration to take effect. Setting this bit analyzes the following registers for validity and coerces them if necessary:

1. IDLEPERIOD/ACTIVEPERIOD
2. FILTERTYPE/FILTERSTRENGTH
3. BASELINEFILTERTYPE/FILTERSTRENGTH
4. NUMBEROFXCHANNELS/NUMBEROFYCHANNELS

Afterwards, the values take effect, and the sensor is base-lined and ready for use.

Note:	If the controller is not in Standby mode when changing configuration parameters, unreliable touch data may be generated until the CFG is set.

Most applications will require custom parameters to be stored in the configuration RAM. The following methods are recommended for achieving this:

1. For permanent configuration: Either during manufacturing test or on first start-up, the host controller writes all configuration values to the controller, sets the CFG bit and stores them to NVRAM by using the NV bit.
2. For configuration on every power-up: The host writes all configuration data to the controller and sets the CFG bit on start-up.

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16.0 MANUFACTURING TESTING

16.1 Automated Manufacturing Test

To start the automated manufacturing test, set the MFG bit of the CMD register. This test re-purposes the same RAM used for RAWADC commands to store the results. When the test is complete, the MFG bit will be cleared. The results of the manufacturing test are stored in the registers shown in Table 16-1.

TABLE 16-1: MFG TEST RX LOOK-UP TABLE(1,2)

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0XD0	—	—	RX13H	—	RX12H	RX11H	RX10H	RX9H
0XD1	—	—	RX13L	—	RX12L	RX11L	RX10L	RX9L
0XD2	—	—	RX8H	RX7H	RX6H	RX5H	RX4H	RX3H
0XD3	—	—	RX8L	RX7L	RX6L	RX5L	RX4L	RX3L
0XD4	RX2H	RX1H	RX0H	—	—	RX14H	—	—
0XD5	RX2L	RX1L	RX0L	—	—	RX14L	—	—

Note 1: RXnH: Pin was unable to set high and is likely shorted to VDD.

2: RXnL: Pin was unable to set low and is likely shorted to GND.

16.2 Sensor Integrity Testing

To test the integrity of both the touch sensor and the overlay for defects, the following test outline is advised:

1. For this test, a way to retrieve data from the MTCH6102 will be required. This can be either through a host controller, or the host controller can conduct the test itself with pre-set test values.
2. Collect the raw-capacitance values by reading the RAWVALUES registers under normal conditions on a set of at least 30 completely assembled sensors.
3. Use the information collected in step 2 to determine the variance and average value for each sensor channel. These values will be used as the standard by which manufactured sensors will need to fall within.
4. For each new sensor produced, compare the RAWVALUES to the range described in step 3. If the sensor falls out of this range, inspect the sensor assembly for defects.
5. To test for touch acquisition ability, repeat steps 1-4 with a known touch stimulus applied (e.g., simulated metal finger).

The above outline is intentionally generic, as manufacturing test setup will need to be modified for every application.

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17.0 MEMORY MAP

TABLE 17-1: CORE RAM MEMORY MAP

Addr.	Name	Core RAM								
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x00	FWMAJOR	FW MAJOR								0x02
0x01	FWMINOR	FW MINOR								0x00
0x02	APPID	APPIDH <15:8>								0x00
0x03		APPIDL <7:0>								0x12
0x04	CMD	NV	DEF	CFG	—	MFG	—	—	BS	0x00
0x05	MODE	—	—	—	—	MODE<3:0>				0x03
0x06	MODECON	TYPE<3:0>				CH<3:0>				0x00

TABLE 17-2: TOUCH RAM MEMORY MAP

Addr.	Name	Touch RAM								
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x10	TOUCHSTATE	FRAME<3:0>				—	LRG	GES	TCH	0x00
0x11	TOUCHX	TOUCHX<11:4>								0x00
0x12	TOUCHY	TOUCHY<11:4>								0x00
0x13	TOUCHLSB	TOUCHX<3:0>				TOUCHY<3:0>				0x00
0x14	GESTURESTATE	GESTURESTATE								0x00
0x15	GESTUREDIAG	GESTUREDIAGNOSTIC								0x00

TABLE 17-3: COMPENSATION RAM MEMORY MAP

Addr.	Compensation RAM							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x50	SENSORCOMP<RX0>							
...	...							
0x5F	SENSORCOMP<RX14>							

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TABLE 17-4: ACQUISITION RAM MEMORY MAP

Addr.	Acquisition RAM							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x80	SENSORVALUES<RX0>							
...	...							
0x8E	SENSORVALUES<RX14>							
—								
0x90	RAWVALUES<RX0>							
...	...							
0xAC	RAWVALUES<RX14>							
—								
0xB0	BASEVALUES<RX0>							
...	...							
0xCC	BASEVALUES<RX15>							
—								
0xD0	RAWADC<0>							
...	...							
0xEF	SENSORVALUES<31>							

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TABLE 17-5: CONFIGURATION RAM MEMORY MAP

Addr.	Configuration RAM								
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x20	NUMBEROFXCHANNELS								0x09
0x21	NUMBEROFYCHANNELS								0x06
0x22	SCANCOUNT								0x06
0x23	TOUCHTHRESHX								0x37
0x24	TOUCHTHRESHY								0x28
0x25	ACTIVEPERIODL								0x85
0x26	ACTIVEPERIODH								0x02
0x27	IDLEPERIODL								0x4C
0x28	IDLEPERIODH								0x06
0x29	IDLETIMEOUT								0x10
0x2A	HYSTERESIS								0x04
0x2B	DEBOUNCEUP								0x01
0x2C	DEBOUNCEDOWN								0x01
0x2D	BASEINTERVALL								0x0A
0x2E	BASEINTERVALH								0x00
0x2F	BASEPOSFILTER								0x14
0x30	BASENEGFILTER								0x14
0x31	FILTERTYPE								0x02
0x32	FILTERSTRENGTH								0x01
0x33	BASEFILTERTYPE								0x01
0x34	BASEFILTERSTRENGTH								0x05
0x35	LARGEACTIVATIONTHRESHL								0x00
0x36	LARGEACTIVATIONTHRESHH								0x00
0x37	HORIZONTALSWIPEDISTANCE								0x40
0x38	VERTICALSWIPEDISTANCE								0x40
0x39	SWIPEHOLDBOUNDARY								0x19
0x3A	TAPDISTANCE								0x19
0x3B	DISTANCEBETWEENTAPS								0x40
0x3C	TAPHOLDTIMEL								0x32
0x3D	TAPHOLDTIMEH								0x00
0x3E	GESTURECLICKTIME								0x0C
0x3F	SWIPEHOLDTHRESH								0x20
0x40	MINSWIPEVELOCITY								0x04
0x41	HORIZONTALGESTUREANGLE								0x2D
0x42	VERTICALGESTUREANGLE								0x2D
0x43	I^2CADDR								0x25

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18.0 ELECTRICAL CHARACTERISTICS

18.1 Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +85°C
Storage temperature ..... -65°C to +150°C
Voltage on pins with respect to VSS
- on VDD pin ..... -0.3V to +4.0V
- on all other pins ..... 0.3V to (VDD + 0.3V)

Maximum current
- out of VSS pin ..... 340 mA
- into VDD pin ..... 255 mA

Maximum output current
- sunk by any I/O pin ..... 25 mA
- sourced by any I/O pin ..... 25 mA

Note: This device is sensitive to ESD damage and must be handled appropriately. Failure to properly handle and protect the device in an application may cause partial to complete failure of the device.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

18.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \le V_{DD} \le V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \le T_A \le T_{A\_MAX}$

VDD — Operating Supply Voltage

MTCH6102
- VDDMIN 1.8V
- VDDMAX 3.6V

TA — Operating Ambient Temperature Range

Industrial Temperature
- TA_MIN ..... –40°C
- TA_MAX ..... +85°C

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18.3 DC Characteristics

TABLE 18-1: OPERATING CONDITIONS

Rating	Min.	Typ.	Max.	Units
Supply Voltage	1.8	—	3.6	V
Supply Current (Full Active, No Frame Rate)	0.7	—	1.17	mA
Supply Current (Sleep)	<1			uA

TABLE 18-2: I/O PORTS

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param. No.	Sym.	Characteristic	Min.	Typ.†	Max.	Units	Conditions
	VIL	**Input Low Voltage**					
		I/O PORT:					
D030		with TTL buffer	—	—	0.15 VDD	V	1.8V ≤ VDD ≤ 4.5V
D031		with Schmitt Trigger buffer	—	—	0.2 VDD	V	2.0V ≤ VDD ≤ 5.5V
		with I2C™ levels	—	—	0.3 VDD	V	
		with SMBus levels	—	—	0.8	V	2.7V ≤ VDD ≤ 5.5V
D032		$\overline{\text{RESET}}$, OSC1 (RC mode)	—	—	0.2 VDD	V	
D033		OSC1 (HS mode)	—	—	0.3 VDD	V	
	VIH	**Input High Voltage**					
		I/O ports:					
D040		with TTL buffer	0.25 VDD + 0.8	—	—	V	1.8V ≤ VDD ≤ 4.5V
D041		with Schmitt Trigger buffer	0.8 VDD	—	—	V	2.0V ≤ VDD ≤ 5.5V
		with I2C levels	0.7 VDD	—	—	V	
		with SMBus levels	2.1	—	—	V	2.7V ≤ VDD ≤ 5.5V
D042		$\overline{\text{RESET}}$	0.8 VDD	—	—	V	
D043A		OSC1 (HS mode)	0.7 VDD	—	—	V	
D043B		OSC1 (RC mode)	0.9 VDD	—	—	V	**Note 1**
	IIL	**Input Leakage Current(2)**					
D060		I/O ports	—	± 5	± 125	nA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance at 85°C
D061		$\overline{\text{RESET}}$(2)	—	± 50	± 200	nA	VSS ≤ VPIN ≤ VDD at 85°C

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

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TABLE 18-2: I/O PORTS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
	IPUR	**Weak Pull-up Current**					
D070*			25	100	200	µA	VDD = 3.3V, VPIN = VSS
	VOL	**Output Low Voltage**					
D080		I/O ports	—	—	0.6	V	IOL = 6 mA, VDD = 3.3V IOL = 1.8 mA, VDD = 1.8V
	VOH	**Output High Voltage**					
D090		I/O ports	VDD - 0.7	—	—	V	IOH = 3 mA, VDD = 3.3V IOH = 1 mA, VDD = 1.8V
	CIO	**Capacitive Loading Specs on Output Pins**					
D101*		All I/O pins	—	—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ." column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Negative current is defined as current sourced by the pin.

2: The leakage current on the $\overline{\text{RESET}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

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18.4 AC Characteristics and Timing Parameters

FIGURE 18-1: I²C™ BUS DATA TIMING

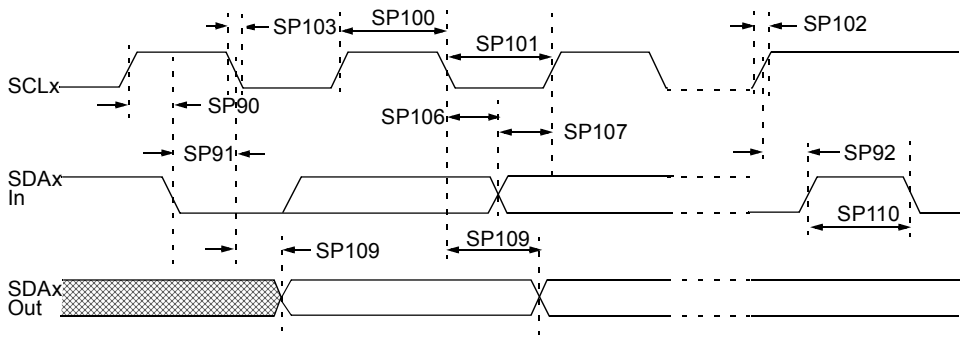

TABLE 18-3: I²C™ BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
SP100*	THIGH	Clock high time	400 kHz mode	0.6	—	µs	
			SSP module	1.5TCY	—	—	
SP101*	TLOW	Clock low time	400 kHz mode	1.3	—	µs	
			SSP module	1.5TCY	—	—	
SP102*	TR	SDAx and SCLx rise time	400 kHz mode	20 + 0.1CB	300	ns	
SP103*	TF	SDAx and SCLx fall time	400 kHz mode	20 + 0.1CB	250	ns	
SP106*	THD:DAT	Data input hold time	400 kHz mode	0	0.9	µs	
SP107*	TSU:DAT	Data input setup time	400 kHz mode	100	—	ns	
SP109*	TAA	Output valid from clock	400 kHz mode	—	—	ns	
SP110*	TBUF	Bus free time	400 kHz mode	1.3	—	µs	
SP111	CB	Bus capacitive loading		—	400	pF	

* These parameters are characterized but not tested.

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19.0 ORDERING INFORMATION

TABLE 19-1: ORDERING INFORMATION

Part Number	Pin Package	Packing
MTCH6102-I/SS	28-Lead SSOP (5.30 mm)	Tube
MTCH6102-I/MV	28-Lead UQFN (4x4x0.5 mm)	Tube
MTCH6102T-I/SS	28-Lead SSOP (5.30 mm)	T/R
MTCH6102T-I/MV	28-Lead UQFN (4x4x0.5 mm)	T/R

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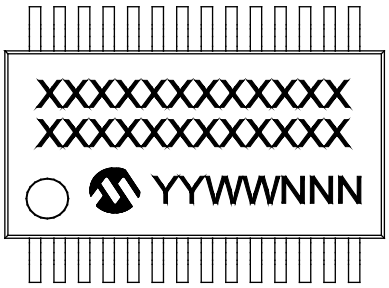
20.0 PACKAGING INFORMATION

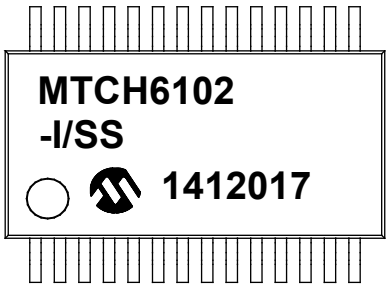
20.1 Package Marking Information

28-Lead Plastic Shrink Small Outline – 5.30 mm Body [SSOP]

28-Lead SSOP (5.30 mm)

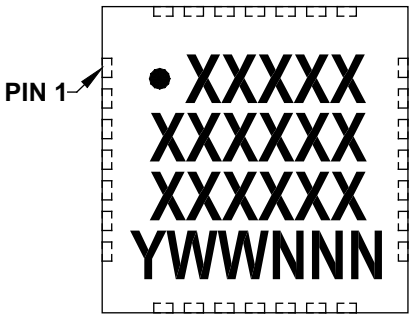


Example

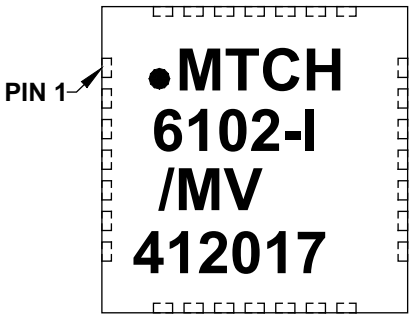


28-Lead Plastic Ultra Thin Quad Flat, No Lead Package – 4x4x0.5 mm Body [UQFN]

28-Lead UQFN (4x4x0.5 mm)



Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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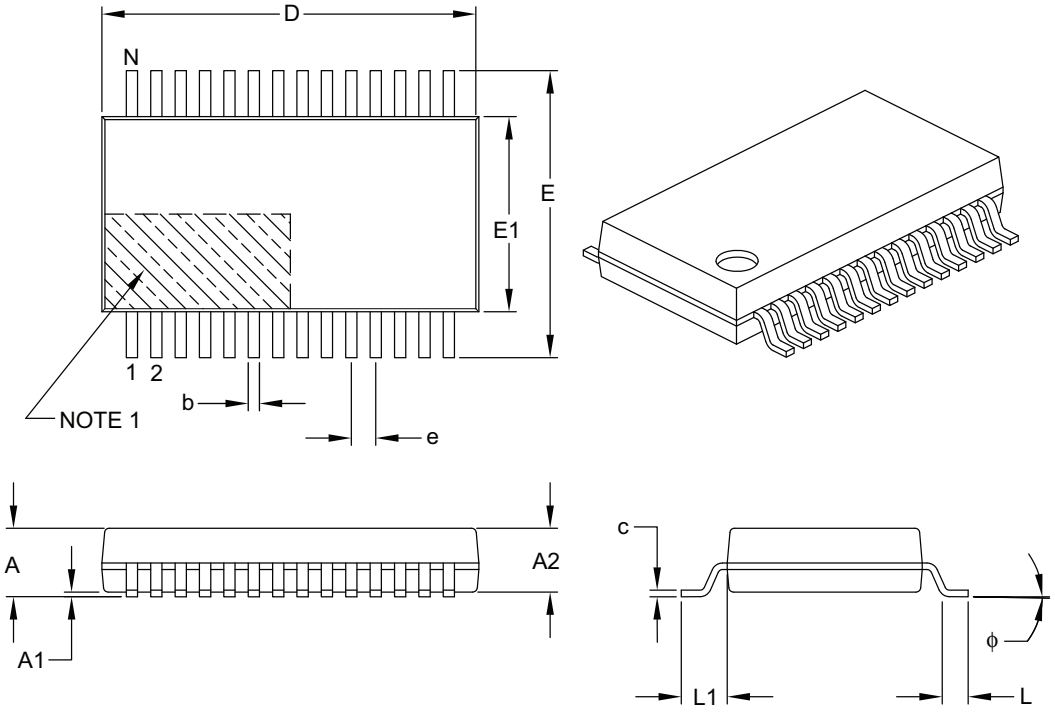
20.2 Package Details

The following sections give the technical details of the packages.

28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

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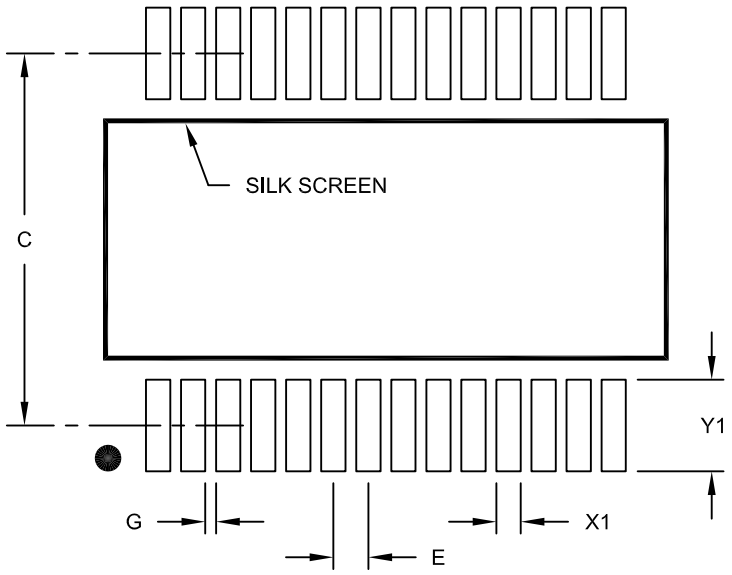
28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A

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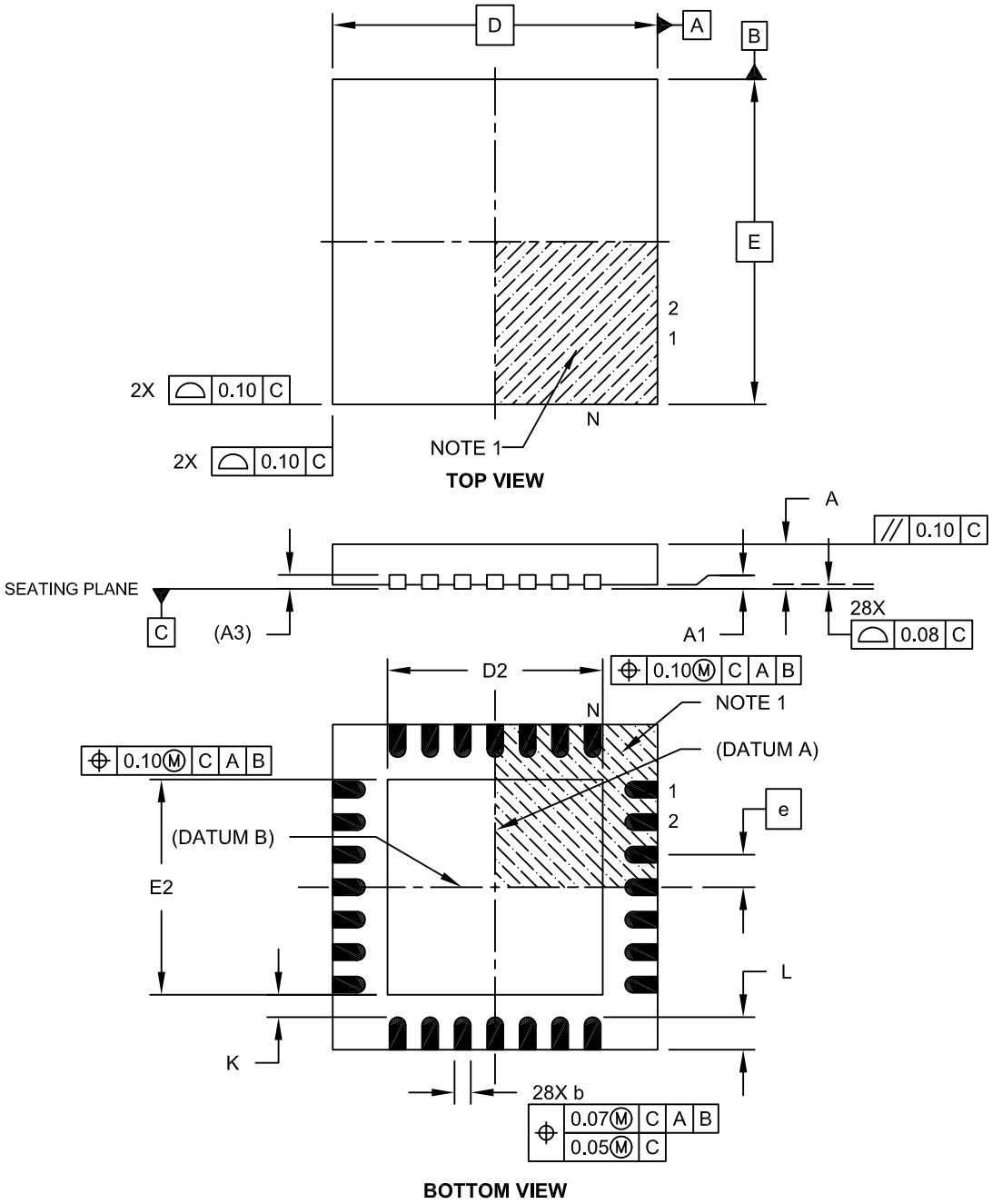
28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-152A Sheet 1 of 2

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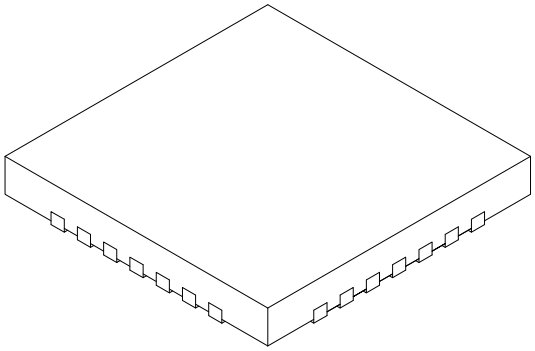
28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.55	2.65	2.75
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.55	2.65	2.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-152A Sheet 2 of 2

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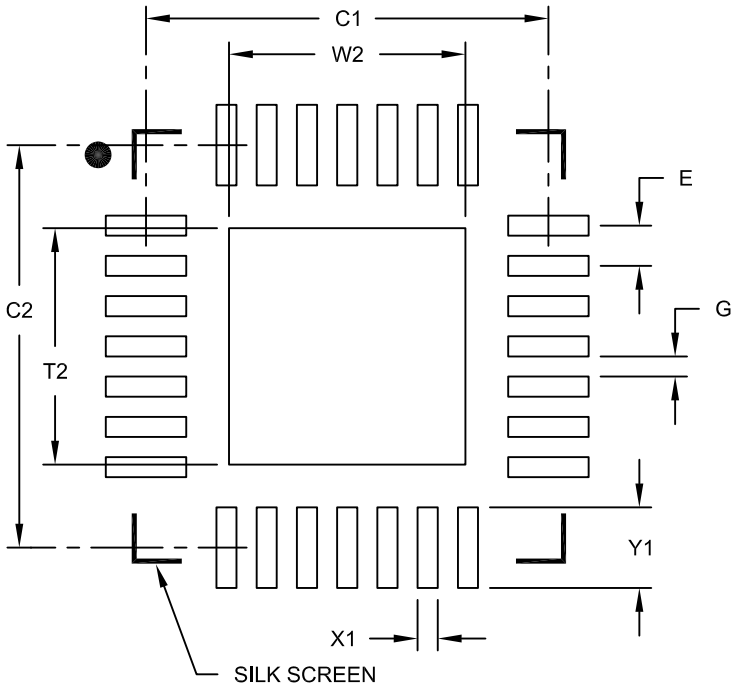
28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 4x4 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			2.35
Optional Center Pad Length	T2			2.35
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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APPENDIX A: DATA SHEET REVISION HISTORY

Revision A (03/2014)

Initial release of the document.

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