

MGSF1N02LT1

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 10\text{ }\mu\text{Adc}$)	$V_{(BR)DSS}$	20	–	–	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 20\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = 20\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	–	–	± 100	nAdc

ON CHARACTERISTICS (Note 1)

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1.0	1.7	2.4	Vdc
Static Drain-to-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.2\text{ Adc}$) ($V_{GS} = 4.5\text{ Vdc}$, $I_D = 1.0\text{ Adc}$)	$r_{DS(on)}$	– –	0.075 0.115	0.090 0.130	Ω

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 5.0\text{ Vdc}$)	C_{iss}	–	125	–	pF
Output Capacitance	($V_{DS} = 5.0\text{ Vdc}$)	C_{oss}	–	120	–	
Transfer Capacitance	($V_{DG} = 5.0\text{ Vdc}$)	C_{rss}	–	45	–	

SWITCHING CHARACTERISTICS (Note 2)

Turn-On Delay Time	(V _{DD} = 15 Vdc, I _D = 1.0 Adc, R _L = 50 Ω)	$t_{d(on)}$	–	2.5	–	ns
Rise Time		t_r	–	1.0	–	
Turn-Off Delay Time		$t_{d(off)}$	–	16	–	
Fall Time		t_f	–	8.0	–	
Gate Charge (See Figure 6)		Q_T	–	6000	–	pC

SOURCE-DRAIN DIODE CHARACTERISTICS

Continuous Current	I_S	–	–	0.6	A
Pulsed Current	I_{SM}	–	–	0.75	–
Forward Voltage (Note 2)	V_{SD}	–	0.8	–	V

1. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.
2. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

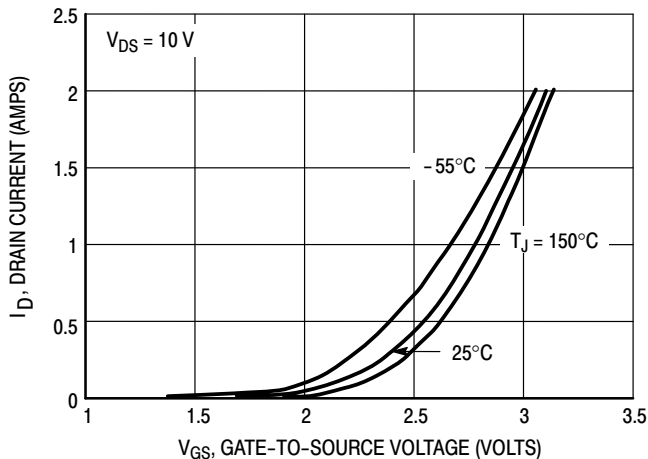


Figure 1. Transfer Characteristics

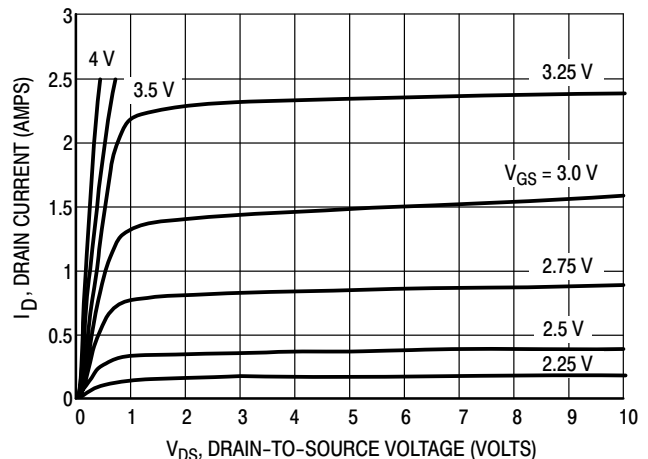


Figure 2. On-Region Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

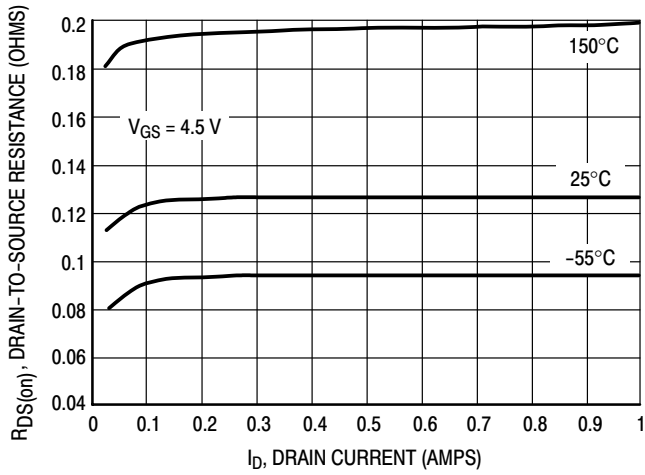


Figure 3. On-Resistance versus Drain Current

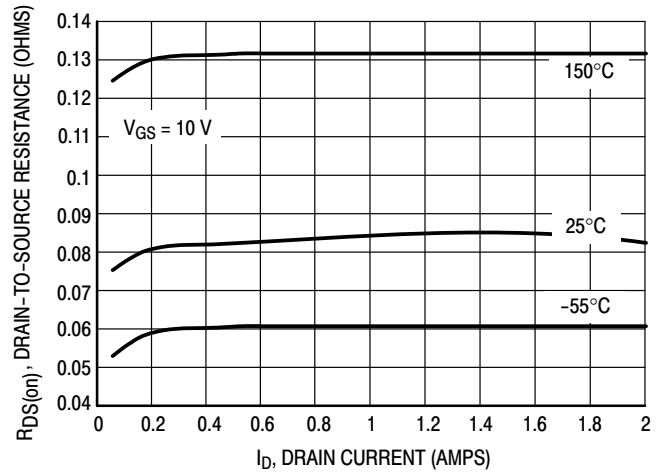


Figure 4. On-Resistance versus Drain Current

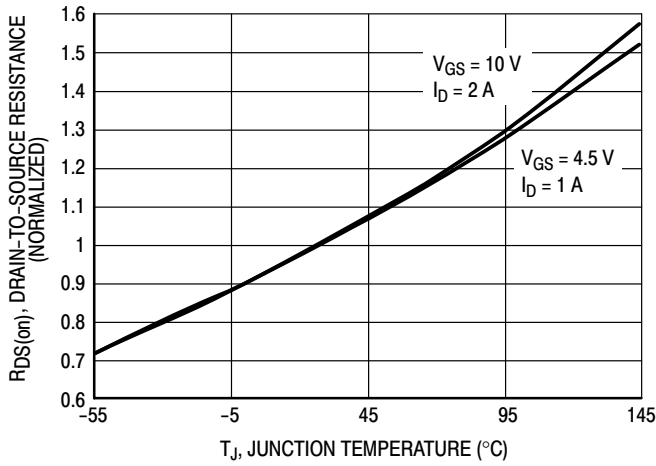


Figure 5. On-Resistance Variation with Temperature

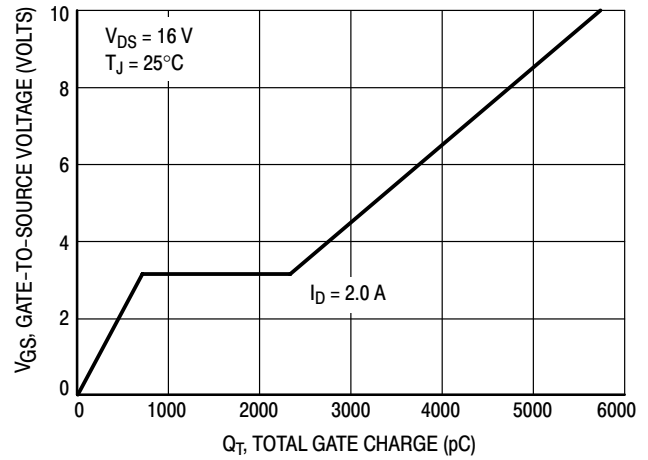


Figure 6. Gate Charge

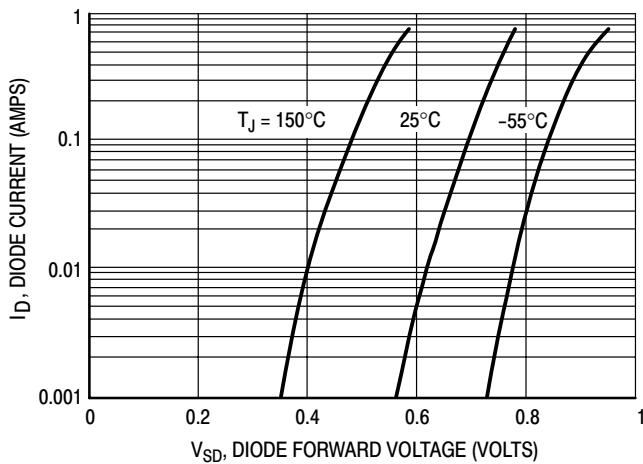


Figure 7. Body Diode Forward Voltage

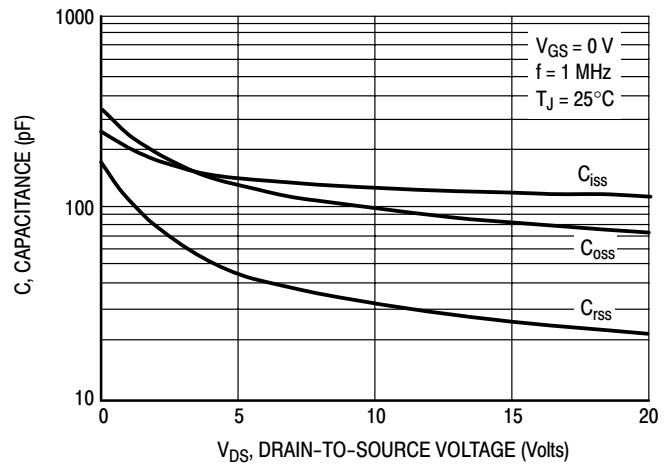
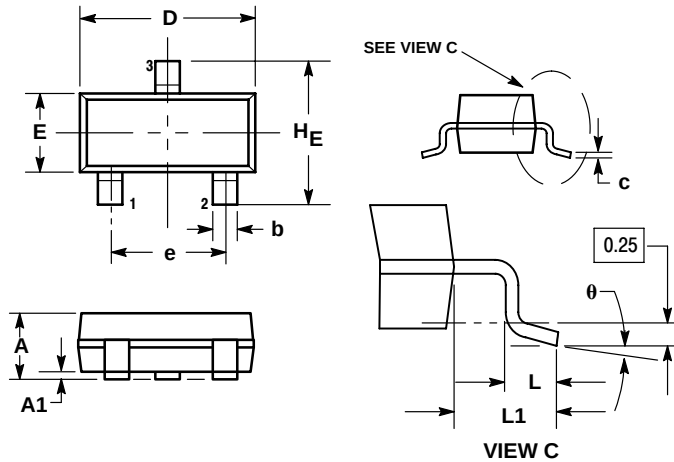


Figure 8. Capacitance

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PACKAGE DIMENSIONS

SOT-23 (TO-236) CASE 318-08 ISSUE AN



NOTES:

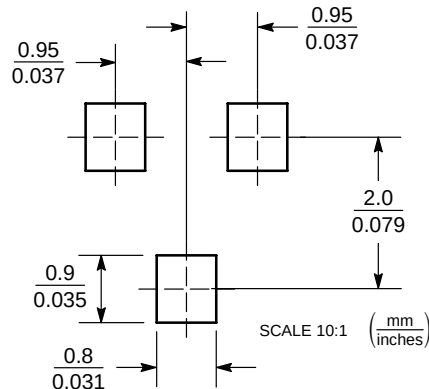
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104

STYLE 21:

- PIN 1. GATE
- SOURCE
- DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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