NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} – V_{SS}$ 7.0V
Current at Analog Input Pins (V_{IN+} and $V_{IN–}$).....±2 mA
Analog Inputs (V_{IN}+ and V_{IN}–) †† .. V_{SS} – 0.3V to V_{DD} + 0.3V
All other Inputs and Outputs ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Difference Input Voltage ..... $|V_{DD} – V_{SS}|$
Output Short Circuit Current .....Continuous
Current at Output and Supply Pins .....±30 mA
Storage Temperature .....–65°C to +150°C
Maximum Junction Temperature (T_J).....+150°C
ESD Protection On All Pins (HBM; MM) ..... ≥ 4 kV; 400V

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 "Input Voltage and Current Limits"**.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2 and R_L = 100 kΩ to V_{DD}/2.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-150	—	+150	µV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	±2.5	—	µV/°C	T_A = -40°C to +85°C
Power Supply Rejection	PSRR	86	105	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	-35	-15	-5	nA	
At Temperature	I_B	-70	-21	—	nA	T_A = -40°C
At Temperature	I_B	—	-12	—	nA	T_A = +85°C
Input Offset Current	I_{OS}	—	±0.15	—	nA	
Common-mode Input Impedance	Z_{CM}	—	600||4	—	MΩ||pF	
Differential Input Impedance	Z_{DIFF}	—	3||2	—	MΩ||pF	
Common-mode						
Common-mode Input Voltage Range	V_{CMR}	V_{SS}		V_{DD} – 0.9	V	
Common-mode Rejection Ratio	CMRR	80	100	—	dB	V_{DD} = 5.0V, V_{CM} = 0.0V to 4.1V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	100	120	—	dB	R_L = 25 kΩ to V_{DD}/2, V_{OUT} = 0.05V to V_{DD} – 0.05V
DC Open-Loop Gain (large signal)	A_{OL}	95	115	—	dB	R_L = 5 kΩ to V_{DD}/2, V_{OUT} = 0.1V to V_{DD} – 0.1V
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} - 20	mV	R_L = 25 kΩ to V_{DD}/2, 0.5V input overdrive
	V_{OL}, V_{OH}	V_{SS} + 45	—	V_{DD} - 60	mV	R_L = 5 kΩ to V_{DD}/2, 0.5V input overdrive
Linear Output Voltage Range	V_{OUT}	V_{SS} + 50	—	V_{DD} - 50	mV	R_L = 25 kΩ to V_{DD}/2, A_{OL} ≥ 100 dB
	V_{OUT}	V_{SS} + 100	—	V_{DD} - 100	mV	R_L = 5 kΩ to V_{DD}/2, A_{OL} ≥ 95 dB
Output Short Circuit Current	I_{SC}	—	±7	—	mA	V_{DD} = 2.3V
	I_{SC}	—	±17	—	mA	V_{DD} = 5.5V
Power Supply						
Supply Voltage	V_{DD}	2.3	—	5.5	V	
Quiescent Current per Amplifier	I_Q	12	19	25	µA	I_O = 0

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	190	—	kHz	
Phase Margin	PM	—	57	—	°	G = +1V/V
Slew Rate	SR	—	0.08	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	2.2	—	μV_{P-P}	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	32	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	70	—	fA/√Hz	f = 1 kHz

MCP618 CHIP SELECT ($\overline{CS}$) ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{CS}$ Low Specifications						
$\overline{CS}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{CS}$ Input Current, Low	I_{CSL}	-1.0	0.01	—	µA	$\overline{CS}$ = V_{SS}
$\overline{CS}$ High Specifications						
$\overline{CS}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{CS}$ Input Current, High	I_{CSH}	—	0.01	2	µA	$\overline{CS}$ = V_{DD}
GND Current	I_{SS}	-2	-0.05	—	µA	$\overline{CS}$ = V_{DD}
Amplifier Output Leakage	$I_{O(LEAK)}$	—	10	—	nA	$\overline{CS}$ = V_{DD}
$\overline{CS}$ Dynamic Specifications						
$\overline{CS}$ Low to Amplifier Output Turn-on Time	t_{ON}	—	9	100	µs	$\overline{CS}$ = 0.2V_{DD} to V_{OUT} = 0.9V_{DD}/2, G = +1 V/V, R_L = 1 kΩ to V_{SS}
$\overline{CS}$ High to Amplifier Output High-Z	t_{OFF}	—	0.1	—	µs	$\overline{CS}$ = 0.8V_{DD} to V_{OUT} = 0.1V_{DD}/2, G = +1 V/V, R_L = 1 kΩ to V_{SS}
$\overline{CS}$ Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5.0V

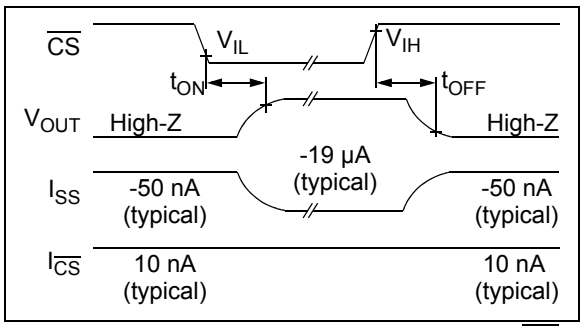


FIGURE 1-1: *Timing Diagram for the $\overline{CS}$ Pin on the MCP618.*

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V and V_{SS} = GND.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	**Note 1**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP616/7/8/9 operate over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

1.1 Test Circuits

The test circuits used for the DC and AC tests are shown in Figure 1-2 and Figure 1-3. The bypass capacitors are laid out according to the rules discussed in **Section 4.6 "Supply Bypass"**.

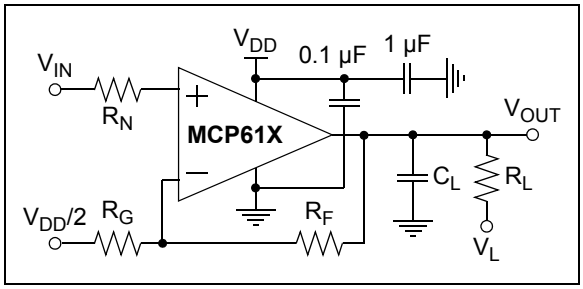


FIGURE 1-2: *AC and DC Test Circuit for Most Non-Inverting Gain Conditions.*

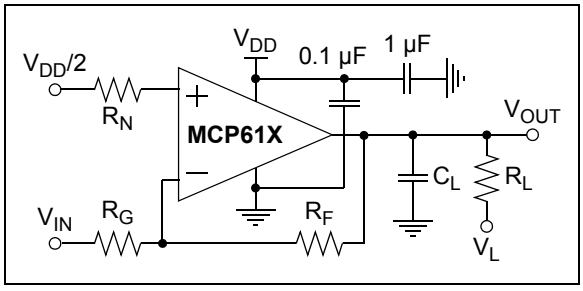


FIGURE 1-3: *AC and DC Test Circuit for Most Inverting Gain Conditions.*

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

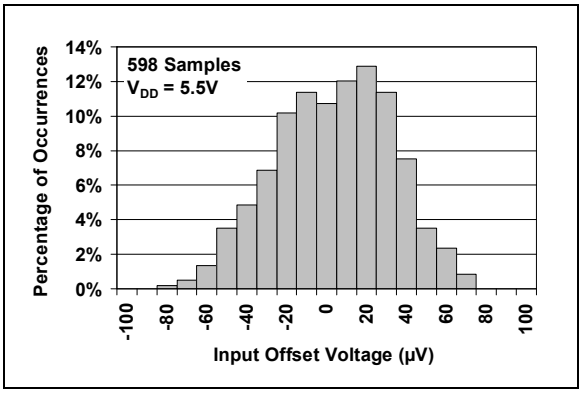


FIGURE 2-1: *Input Offset Voltage at V_{DD} = 5.5V.*

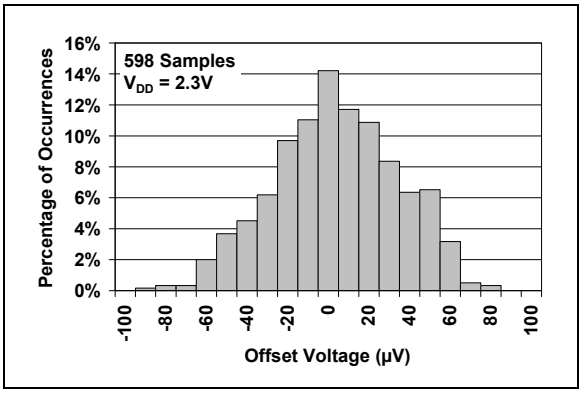


FIGURE 2-2: *Input Offset Voltage at V_{DD} = 2.3V.*

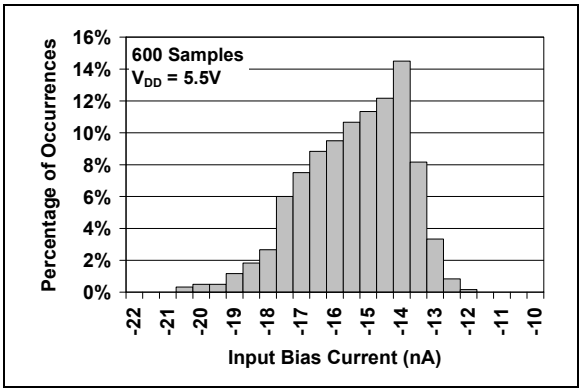


FIGURE 2-3: *Input Bias Current at V_{DD} = 5.5V.*

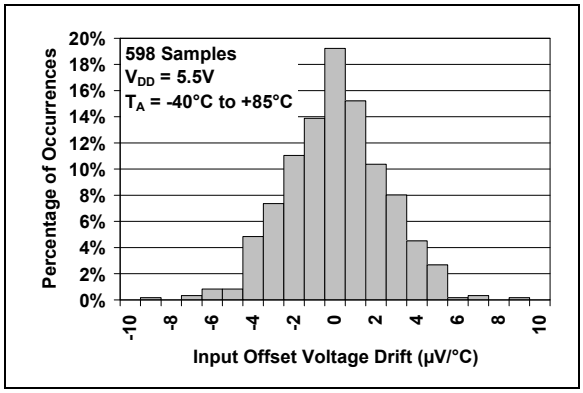


FIGURE 2-4: *Input Offset Voltage Drift at V_{DD} = 5.5V.*

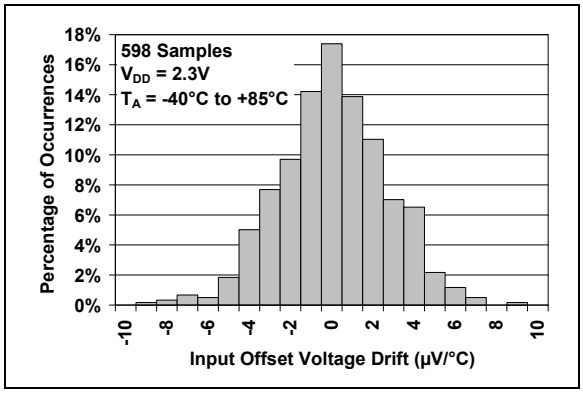


FIGURE 2-5: *Input Offset Voltage Drift at V_{DD} = 2.3V.*

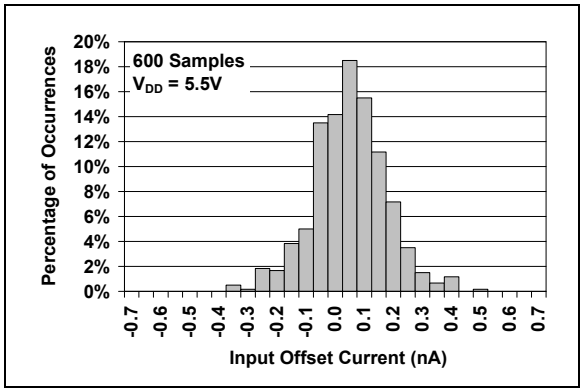


FIGURE 2-6: *Input Offset Current at V_{DD} = 5.5V.*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

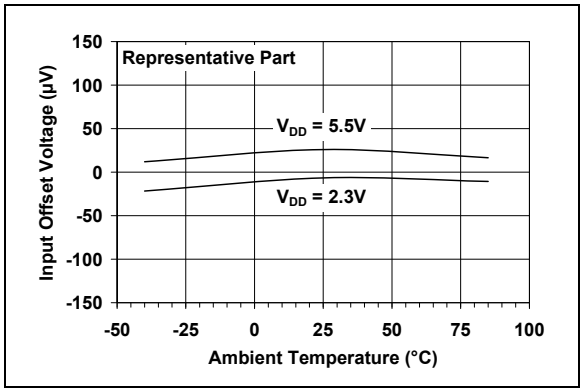


FIGURE 2-7: *Input Offset Voltage vs. Ambient Temperature.*

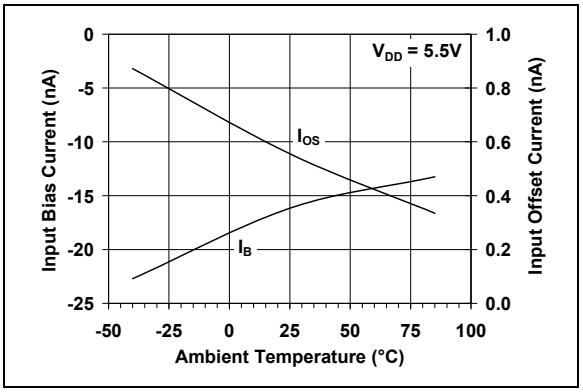


FIGURE 2-10: *Input Bias, Offset Currents vs. Ambient Temperature.*

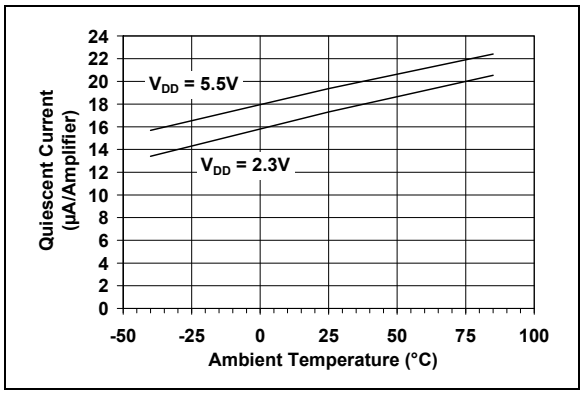


FIGURE 2-8: *Quiescent Current vs. Ambient Temperature.*

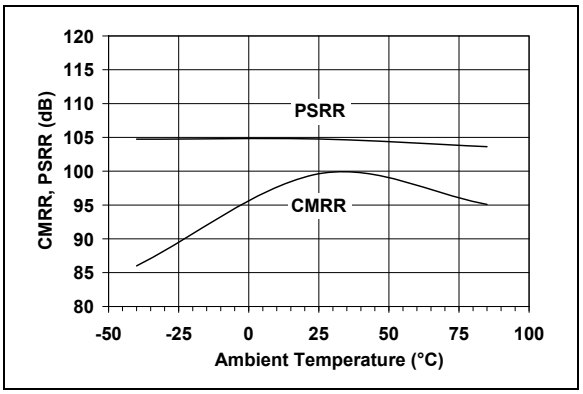


FIGURE 2-11: *CMRR, PSRR vs. Ambient Temperature.*

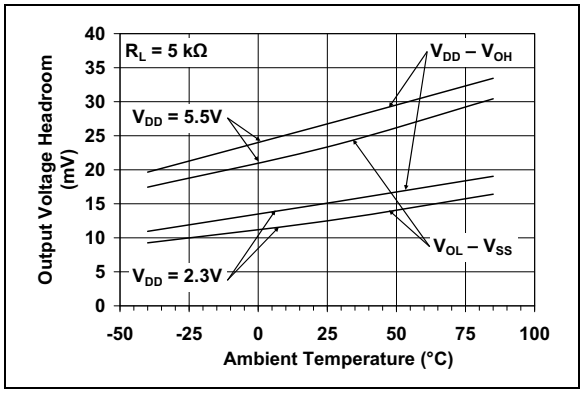


FIGURE 2-9: *Maximum Output Voltage Swing vs. Ambient Temperature at R_L = 5 kΩ.*

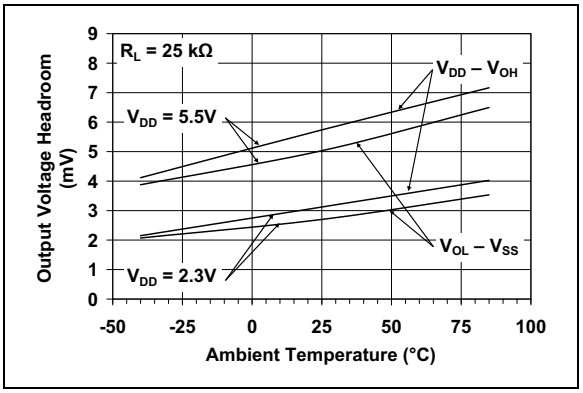


FIGURE 2-12: *Maximum Output Voltage Swing vs. Ambient Temperature at R_L = 25 kΩ.*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

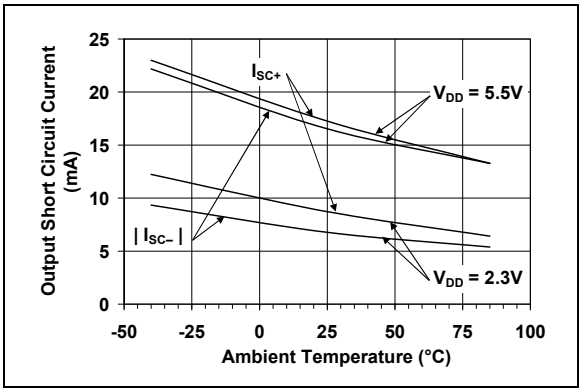


FIGURE 2-13: *Output Short Circuit Current vs. Ambient Temperature.*

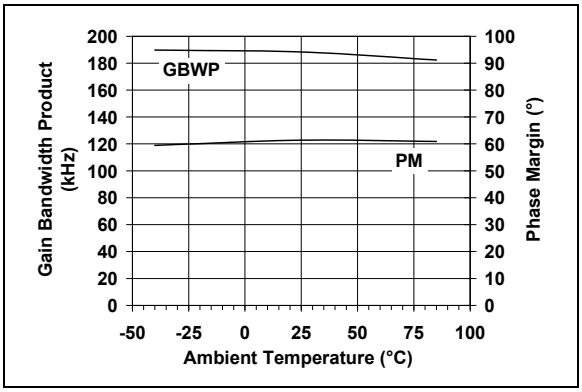


FIGURE 2-16: *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

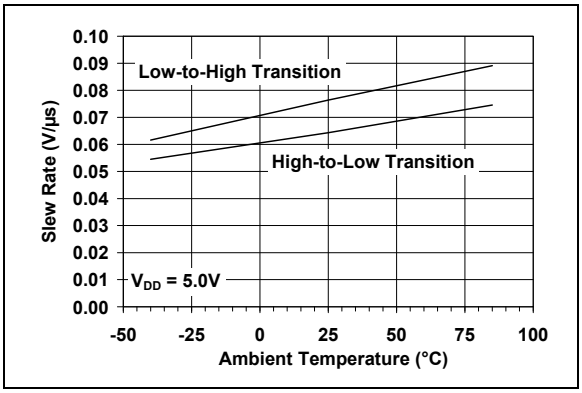


FIGURE 2-14: *Slew Rate vs. Ambient Temperature.*

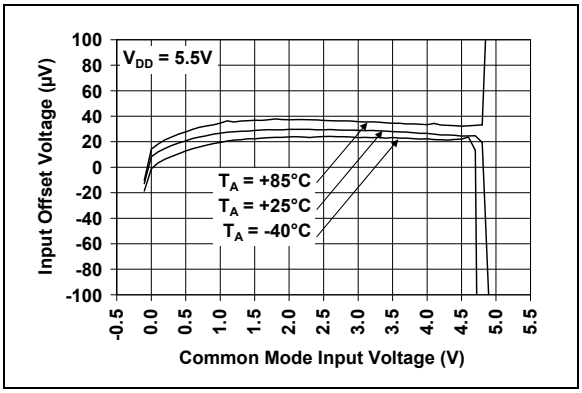


FIGURE 2-17: *Input Offset Voltage vs. Common-mode Input Voltage.*

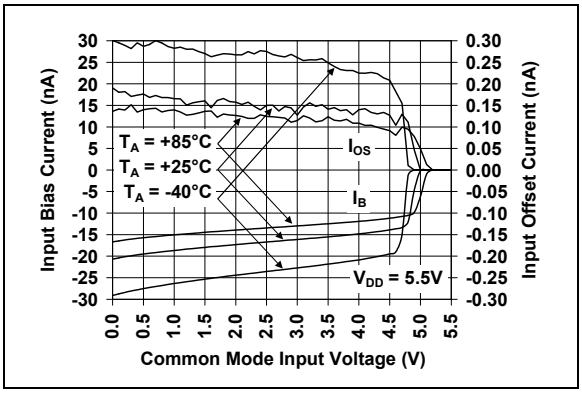


FIGURE 2-15: *Input Bias, Offset Currents vs. Common-mode Input Voltage.*

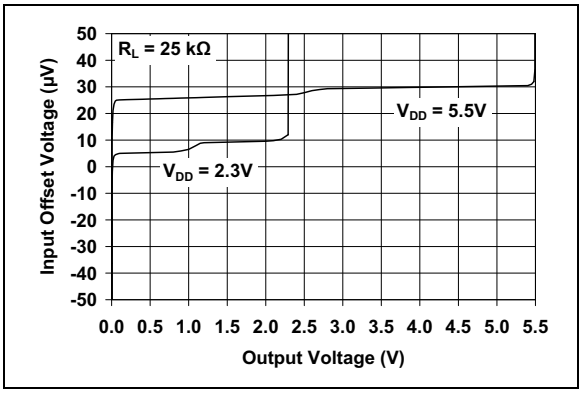


FIGURE 2-18: *Input Offset Voltage vs. Output Voltage.*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

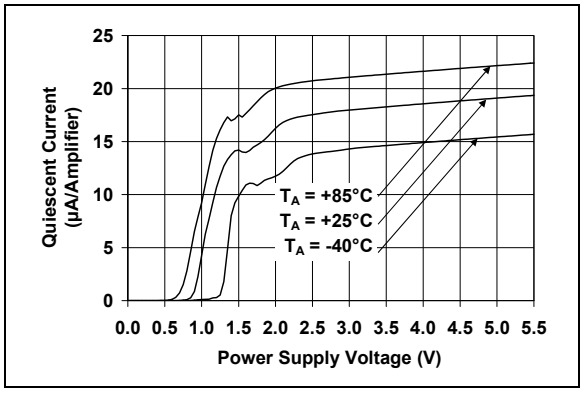


FIGURE 2-19: *Quiescent Current vs. Power Supply Voltage.*

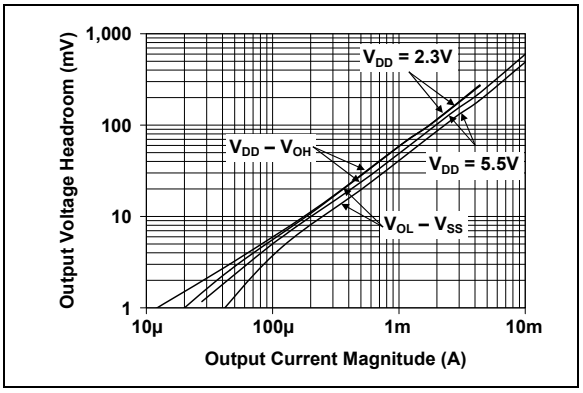


FIGURE 2-22: *Output Voltage Headroom vs. Output Current Magnitude.*

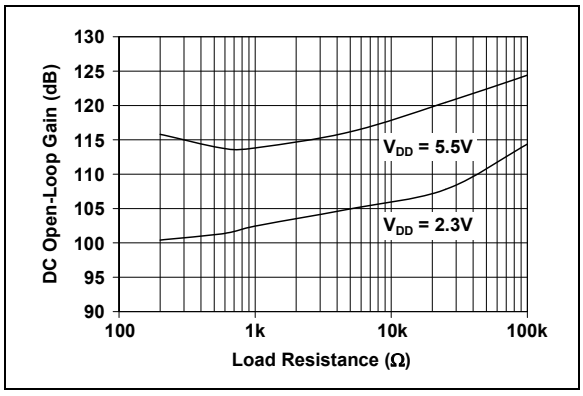


FIGURE 2-20: *DC Open-Loop Gain vs. Load Resistance.*

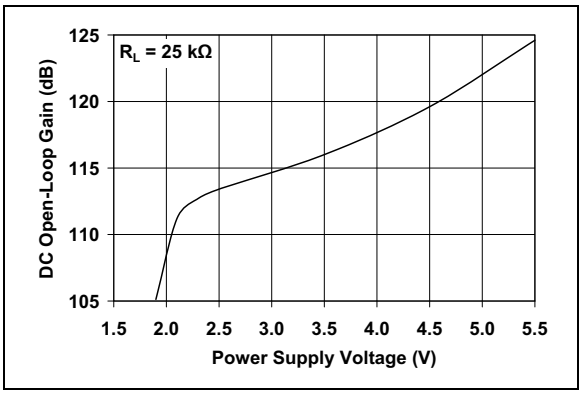


FIGURE 2-23: *DC Open-Loop Gain vs. Power Supply Voltage.*

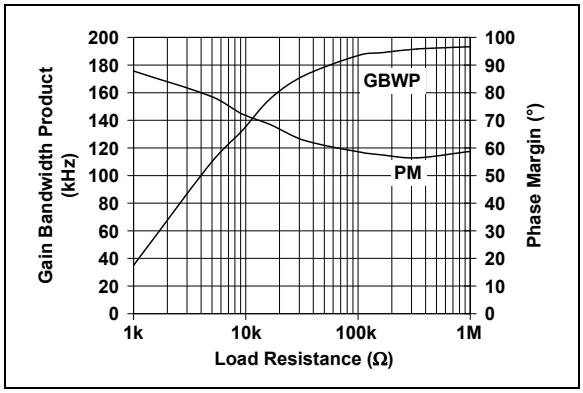


FIGURE 2-21: *Gain-Bandwidth Product, Phase Margin vs. Load Resistance.*

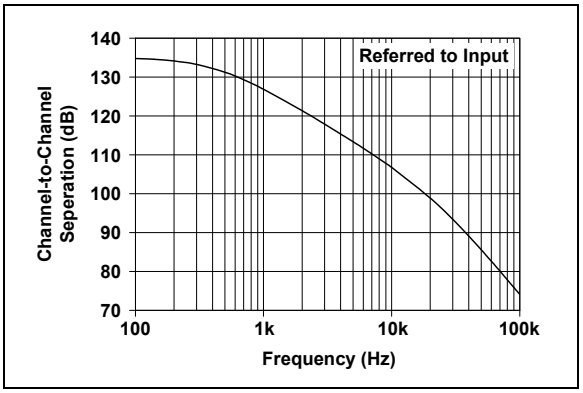


FIGURE 2-24: *Channel-to-Channel Separation vs. Frequency (MCP617 and MCP619 only).*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 100 kΩ to V_{DD}/2 and C_L = 60 pF.

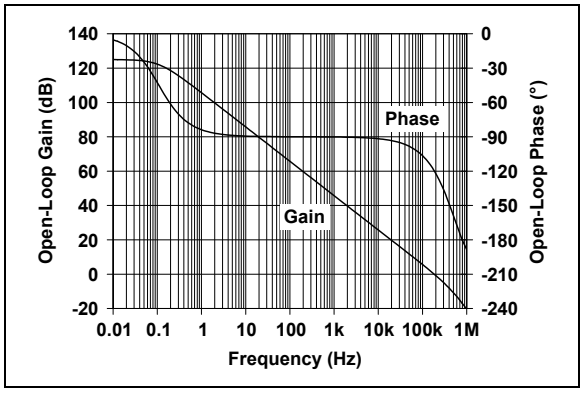


FIGURE 2-25: *Open-Loop Gain, Phase vs. Frequency.*

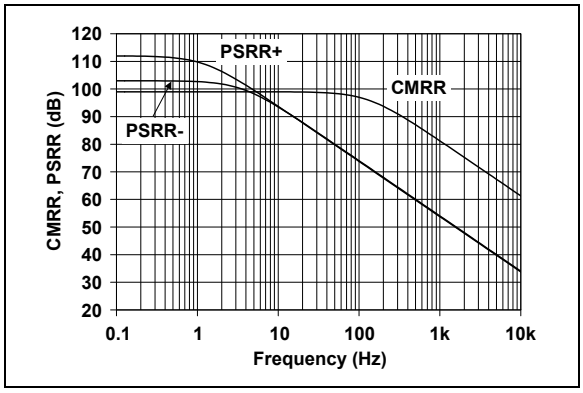


FIGURE 2-28: *CMRR, PSRR vs. Frequency.*

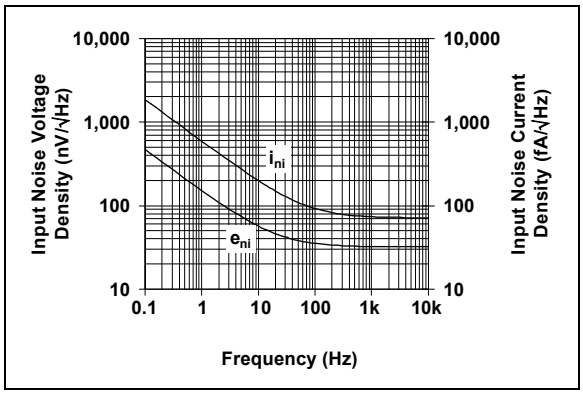


FIGURE 2-26: *Input Noise Voltage, Current Densities vs. Frequency.*

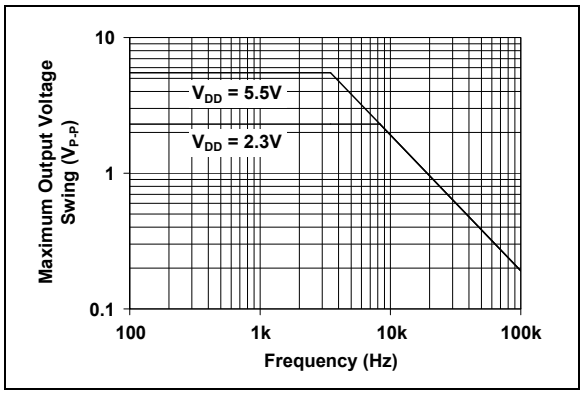


FIGURE 2-29: *Maximum Output Voltage Swing vs. Frequency.*

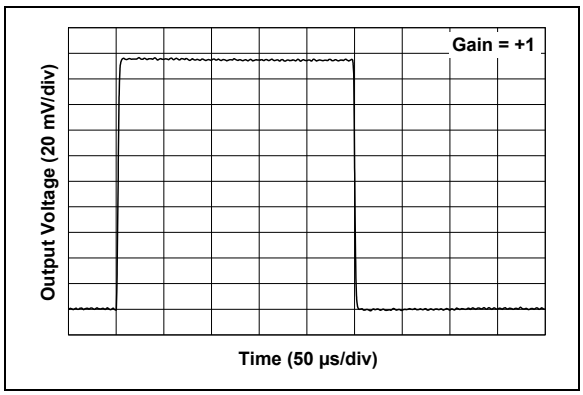


FIGURE 2-27: *Small-Signal, Non-Inverting Pulse Response.*

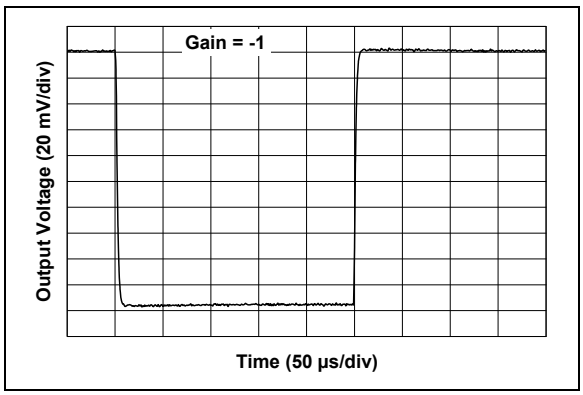


FIGURE 2-30: *Small-Signal, Inverting Pulse Response.*

Note: Unless otherwise indicated, V_{DD} = +2.3V to +5.5V, V_{SS} = GND, T_A = 25°C, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 100 kΩ to $V_{DD}/2$ and C_L = 60 pF.

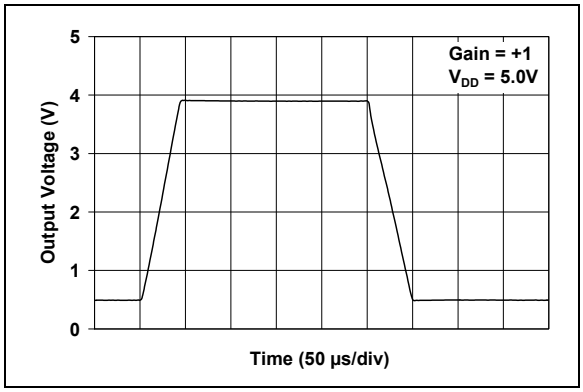


FIGURE 2-31: *Large-Signal, Non-Inverting Pulse Response.*

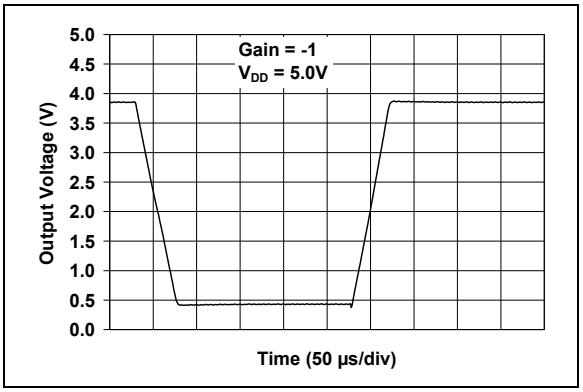


FIGURE 2-34: *Large-Signal, Inverting Pulse Response.*

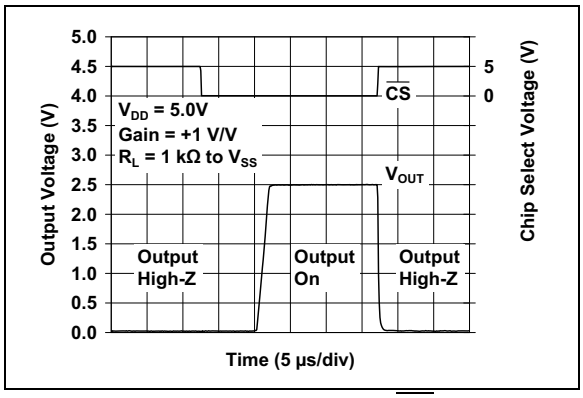


FIGURE 2-32: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time (MCP618 only).*

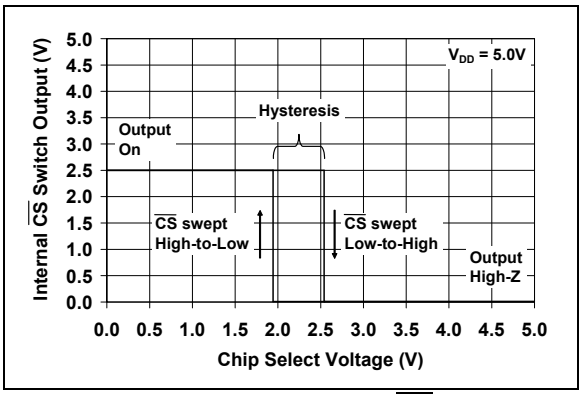


FIGURE 2-35: *Chip Select ($\overline{CS}$) Internal Hysteresis (MCP618 only).*

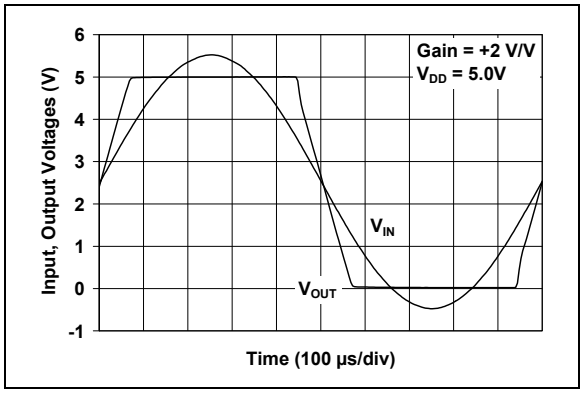


FIGURE 2-33: *The MCP616/7/8/9 Show No Phase Reversal.*

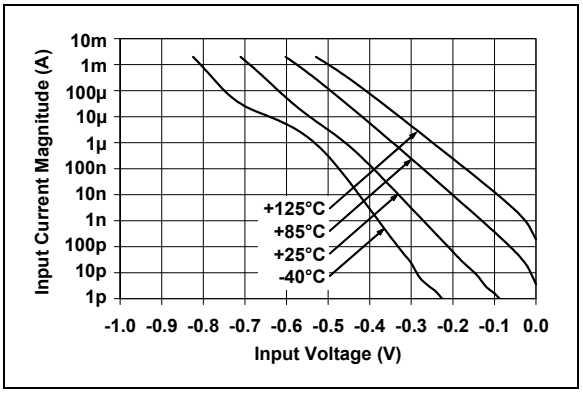


FIGURE 2-36: *Measured Input Current vs. Input Voltage (below V_{SS}).*

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP616	MCP617	MCP618	MCP619	Symbol	Description
MSOP, PDIP, SOIC	MSOP, PDIP, SOIC	MSOP, PDIP, SOIC	PDIP, SOIC, TSSOP		
6	1	6	1	V_{OUT}, V_{OUTA}	Output (op amp A)
2	2	2	2	V_{IN}–, V_{INA}–	Inverting Input (op amp A)
3	3	3	3	V_{IN}+, V_{INA}+	Non-inverting Input (op amp A)
7	8	7	4	V_{DD}	Positive Power Supply
—	5	—	5	V_{INB}+	Non-inverting Input (op amp B)
—	6	—	6	V_{INB}–	Inverting Input (op amp B)
—	7	—	7	V_{OUTB}	Output (op amp B)
—	—	—	8	V_{OUTC}	Output (op amp B)
—	—	—	9	V_{INC}–	Inverting Input (op amp C)
—	—	—	10	V_{INC}+	Non-inverting Input (op amp C)
4	4	4	11	V_{SS}	Negative Power Supply
—	—	—	12	V_{IND}+	Non-inverting Input (op amp D)
—	—	—	13	V_{IND}–	Inverting Input (op amp D)
—	—	—	14	V_{OUTD}	Output (op amp D)
—	—	8	—	$\overline{CS}$	Chip Select
1, 5, 8	—	1, 5	—	NC	No Internal Connection

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance PNP inputs with low bias currents.

3.3 Chip Select Digital Input ($\overline{CS}$)

This is a CMOS, Schmitt-triggered input that places the MCP618 op amp into a low-power mode of operation.

3.4 Power Supply Pins (V_{DD}, V_{SS})

The positive power supply (V_{DD}) is 2.3V to 5.5V higher than the negative power supply (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single-supply (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need bypass capacitors.

NOTES:

4.0 APPLICATIONS INFORMATION

The MCP616/7/8/9 family of op amps is manufactured using Microchip's state-of-the-art CMOS process, which includes PNP transistors. These op amps are unity-gain stable and suitable for a wide range of general purpose applications.

4.1 Rail-to-Rail Inputs

4.1.1 PHASE REVERSAL

The MCP616/7/8/9 op amp is designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-36 shows the input voltage exceeding the supply voltage without any phase reversal.

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-1. This structure was chosen to protect the input transistors and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation and low enough to bypass quick ESD events within the specified limits.

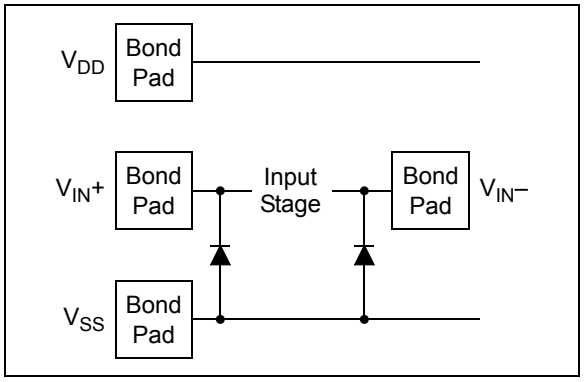


FIGURE 4-1: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these op amps, the circuit they are in must limit the currents and voltages at the V_{IN}+ and V_{IN}– pins (see **"Absolute Maximum Ratings †"** at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-2 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}–) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pins. Diodes D_1 and D_2 prevent the input pins (V_{IN}+ and V_{IN}–) from going too far above V_{DD}, and dump any currents onto V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

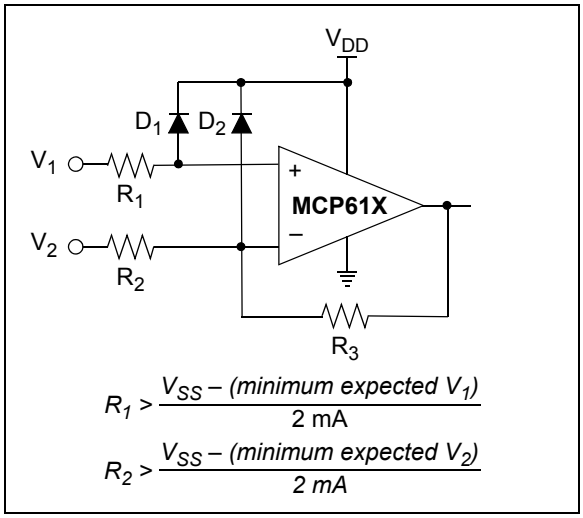


FIGURE 4-2: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of resistors R_1 and R_2. In this case, current through the diodes D_1 and D_2 needs to be limited by some other mechanism. The resistors then serve as in-rush current limiters; the DC current into the input pins (V_{IN}+ and V_{IN}–) should be very small.

A significant amount of current can flow out of the inputs when the Common-mode voltage (V_{CM}) is below ground (V_{SS}) (see Figure 2-36). Applications that are high impedance may need to limit the usable voltage range.

4.1.3 NORMAL OPERATION

The inputs of the MCP616/7/8/9 op amps connect to a differential PNP input stage. The Common-mode input voltage range (V_{CMR}) includes ground in single-supply systems (V_{SS}), but does not include V_{DD}. This means that the amplifier input behaves linearly as long as the Common-mode input voltage (V_{CM}) is kept within the specified V_{CMR} limits (V_{SS} to V_{DD}–0.9V at +25°C).

4.2 DC Offsets

The MCP616/7/8/9 family of op amps have a PNP input differential pair that gives good DC performance. They have very low input offset voltage (±150 µV, maximum) at T_A = +25°C, with a typical bias current of -15 nA (sourced out of the inputs).

There must be a DC path to ground (or power supply) from both inputs, or the op amp will not bias properly. The DC resistances seen by the op amp inputs ($R_1||R_2$ and $R_4||R_5$ in Figure 4-3) need to be equal and less than 100 kΩ, to minimize the total DC offset.

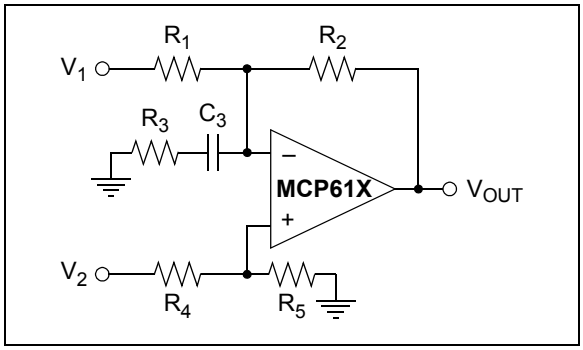


FIGURE 4-3: *Example Circuit for Calculating DC Offset.*

To calculate the DC bias point and DC offset, convert the circuit to its DC equivalent:

- Replace capacitors with open circuits
- Replace inductors with short circuits
- Replace AC voltage sources with short circuits
- Replace AC current sources with open circuits
- Convert DC sources and resistances into their Thevenin equivalent form

The DC equivalent circuit for Figure 4-3 is shown in Figure 4-4.

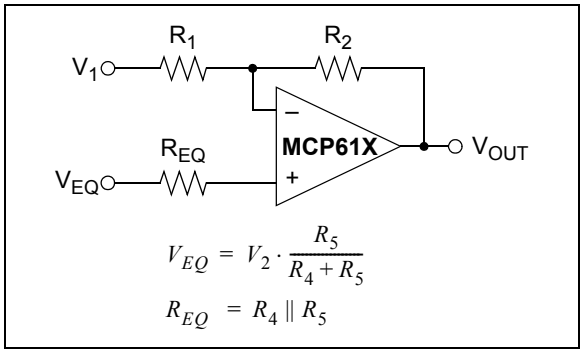


FIGURE 4-4: *Equivalent DC Circuit.*

Now calculate the nominal DC bias point with offset:

EQUATION 4-1:

$$G_N = 1 + R_2/R_1$$

$$V_{OOS} = G_N [V_{OS} + I_B ((R_1 \,||R_2) - R_{EQ}) - I_{OS} ((R_1 \,||R_2) + R_{EQ}) / 2]$$

$$V_{CM} = V_{EQ} - (I_B + I_{OS}/2)\, R_{EQ}$$

$$V_{OUT} = V_{EQ}\,(G_N) - V_1\,(G_N - 1) + V_{OOS}$$

Where:

G_N	=	op amp's noise gain (from the non-inverting input to the output)
V_{OOS}	=	circuit's output offset voltage
V_{OS}	=	op amp's input offset voltage
I_B	=	op amp's input bias current
I_{OS}	=	op amp's input offset current
V_{CM}	=	op amp's Common-mode input voltage

Use the worst-case specs and source values to determine the worst-case output voltage range and offset for your design. Make sure the Common-mode input voltage range and output voltage range are not exceeded.

4.3 Rail-to-Rail Output

There are two specifications that describe the output swing capability of the MCP616/7/8/9 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load conditions. For instance, the output voltage swings to within 15 mV of the negative rail with a 25 kΩ load tied to $V_{DD}/2$. Figure 2-33 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output swing capability of these amplifiers is the Linear Output Voltage Range. This specification defines the maximum output swing that can be achieved while the amplifier still operates in its linear region. To verify linear operation in this range, the large-signal DC Open-Loop Gain (A_{OL}) is measured at points inside the supply rails. The measurement must meet the specified A_{OL} conditions in the specification table.

4.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 4-5) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

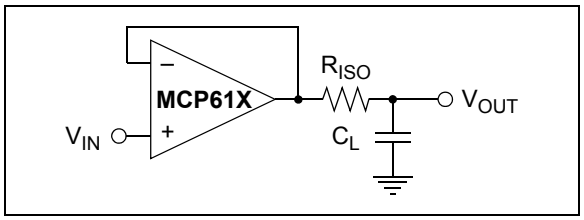


FIGURE 4-5: *Output Resistor, R_{ISO} stabilizes large capacitive loads.*

Figure 4-6 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is 1+|Signal Gain| (e.g., -1 V/V gives G_N = +2 V/V).

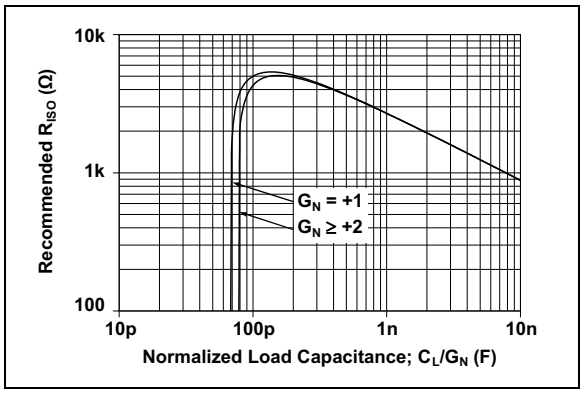


FIGURE 4-6: *Recommended R_{ISO} Values for Capacitive Loads.*

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO}'s value until the response is reasonable. Bench evaluation and simulations with the MCP616/7/8/9 SPICE macro model are helpful.

4.5 MCP618 Chip Select ($\overline{CS}$)

The MCP618 is a single op amp with Chip Select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 50 nA (typical) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. The $\overline{CS}$ pin has an internal 5 MΩ (typical) pull-down resistor connected to V_{SS}, so it will go low if the $\overline{CS}$ pins is left floating. Figure 1-1 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

4.6 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good high-frequency performance. It may use a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor is not required and can be shared with other analog parts.

4.7 Unused Op Amps

An unused op amp in a quad package (MCP619) should be configured as shown in Figure 4-7. These circuits prevent the output from toggling and causing crosstalk. Circuits A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.

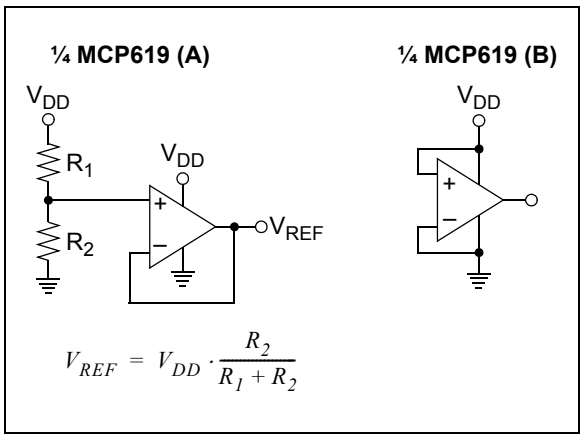


FIGURE 4-7: *Unused Op Amps.*

4.8 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP616/7/8/9 family's bias current at 25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example is shown below in Figure 4-8.

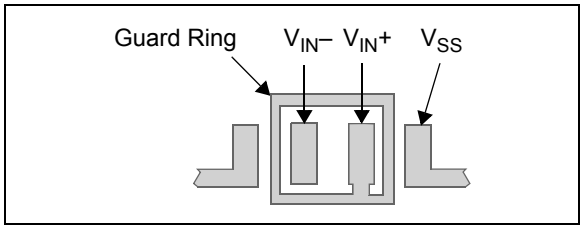


FIGURE 4-8: *Example Guard Ring Layout for Inverting Gain.*

1. Non-inverting Gain and Unity Gain Buffer:
   a) Connect the non-inverting pin (V_{IN}+) to the input with a wire that does not touch the PCB surface.
   b) Connect the guard ring to the inverting input pin (V_{IN}–). This biases the guard ring to the Common-mode input voltage.
2. Inverting Gain and Transimpedance gain (convert current to voltage, such as photo detectors) amplifiers:
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the op amp (e.g., V_{DD}/2 or ground).
   b) Connect the inverting pin (V_{IN}–) to the input with a wire that does not touch the PCB surface.

4.9 Application Circuits

4.9.1 HIGH GAIN PRE-AMPLIFIER

The MCP616/7/8/9 op amps are well suited to amplifying small signals produced by low-impedance sources/sensors. The low offset voltage, low offset current and low noise fit well in this role. Figure 4-9 shows a typical pre-amplifier connected to a low-impedance source (V_S and R_S).

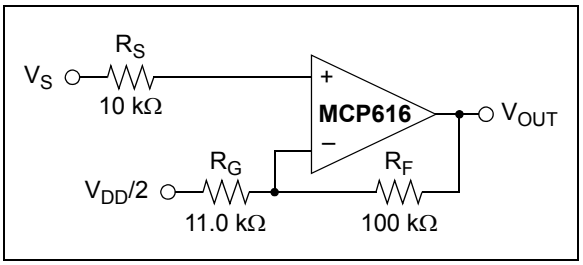


FIGURE 4-9: *High Gain Pre-amplifier.*

For the best noise and offset performance, the source resistance R_S needs to be less than 15 kΩ. The DC resistances at the inputs are equal to minimize the offset voltage caused by the input bias currents (**Section 4.2 "DC Offsets"**). In this circuit, the DC gain is 10 V/V, which will give a typical bandwidth of 19 kHz.

4.9.2 TWO OP AMP INSTRUMENTATION AMPLIFIER

The two-op amp instrumentation amplifier shown in Figure 4-10 serves the function of taking the difference of two input voltages, level-shifting it and gaining it to the output. This configuration is best suited for higher gains (i.e., gain > 3 V/V). The reference voltage (V_{REF}) is typically at mid-supply (V_{DD}/2) in a single-supply environment.

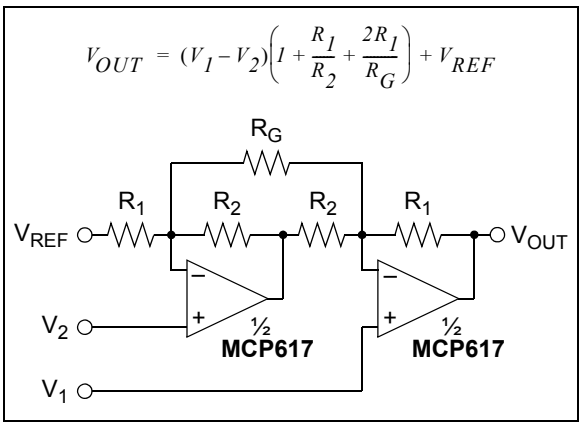


FIGURE 4-10: *Two-Op Amp Instrumentation Amplifier.*

The key specifications that make the MCP616/7/8/9 family appropriate for this application circuit are low input bias current, low offset voltage and high Common-mode rejection.

4.9.3 THREE OP AMP INSTRUMENTATION AMPLIFIER

A classic, three-op amp instrumentation amplifier is illustrated in Figure 4-11. The two-input op amps provide differential signal gain and a Common-mode gain of +1. The output op amp is a difference amplifier, which converts its input signal from differential to a single-ended output; it rejects Common-mode signals at its input. The gain of this circuit is simply adjusted with one resistor (R_G). The reference voltage (V_{REF}) is typically referenced to mid-supply ($V_{DD}/2$) in single-supply applications.

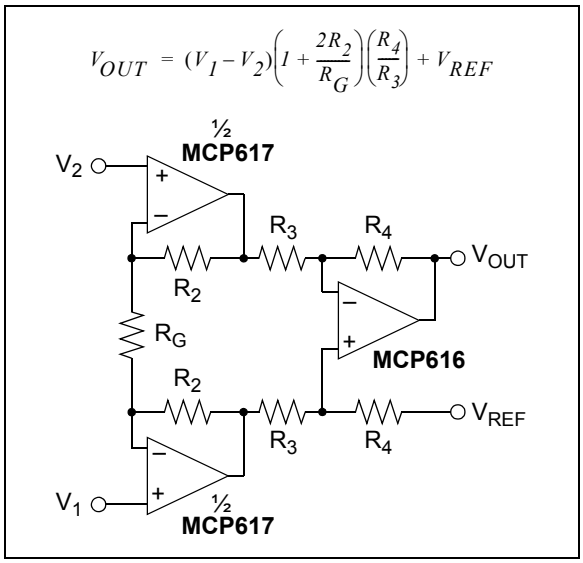


FIGURE 4-11: *Three-Op Amp Instrumentation Amplifier.*

4.9.4 PRECISION GAIN WITH GOOD LOAD ISOLATION

In Figure 4-12, the MCP616 op amp, R_1 and R_2 provide a high gain to the input signal (V_{IN}). The MCP616's low offset voltage makes this an accurate circuit.

The MCP606 is configured as a unity-gain buffer. It isolates the MCP616's output from the load, increasing the high gain stage's precision. Since the MCP606 has a higher output current, and the two amplifiers are housed in separate packages, there is minimal change in the MCP616's offset voltage due to loading effect.

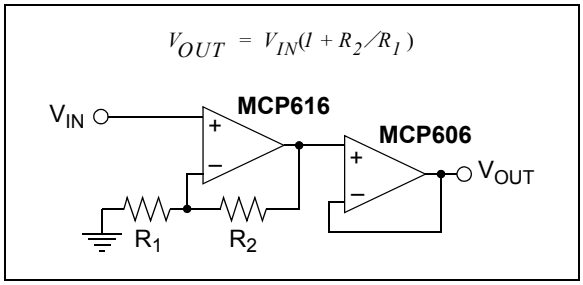


FIGURE 4-12: *Precision Gain with Good Load Isolation.*

NOTES:

5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP616/7/8/9 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP616/7/8/9 op amps is available on the Microchip website at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation over the temperature range. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 Mindi™ Circuit Designer & Simulator

Microchip's Mindi™ Circuit Designer & Simulator aids in the design of various circuits useful for active filter, amplifier and power-management applications. It is a free online circuit designer & simulator available from the Microchip website at www.microchip.com/mindi. This interactive circuit designer & simulator enables designers to quickly generate circuit diagrams, simulate circuits. Circuits developed using the Mindi Circuit Designer & Simulator can be downloaded to a personal computer or workstation.

5.3 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Datasheets, Purchase, and Sampling of Microchip parts.

5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip website at www.microchip.com/analogtools.

Two of our boards that are especially useful are:

- **P/N SOIC8EV:** *8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board*
- **P/N SOIC14EV:** *14-Pin SOIC/TSSOP/DIP Evaluation Board*

5.5 Application Notes

The following Microchip Application Notes are available on the Microchip website at www.microchip.com/appnotes and are recommended as supplemental reference resources.

ADN003: *"Select the Right Operational Amplifier for your Filtering Circuits,"* DS21821

AN722: *"Operational Amplifier Topologies and DC Specifications,"* DS00722

AN723: *"Operational Amplifier AC Specifications and Applications,"* DS00723

AN884: *"Driving Capacitive Loads With Op Amps,"* DS00884

AN990: *"Analog Sensor Conditioning Circuits – An Overview,"* DS00990

These application notes and others are listed in the design guide:

"Signal Chain Design Guide," DS21825

NOTES:

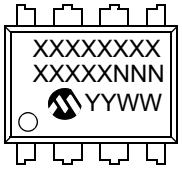
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

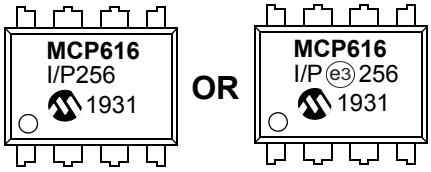
8-Lead MSOP

Example:

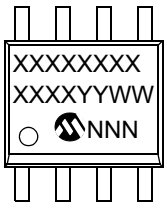
8-Lead PDIP (300 mil)



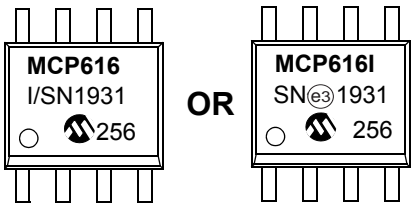
Examples:



8-Lead SOIC (150 mil)



Examples:

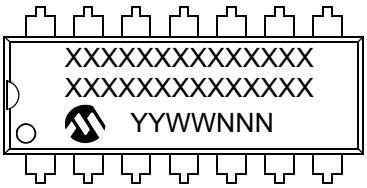


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

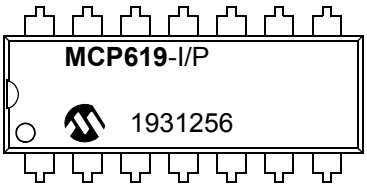
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

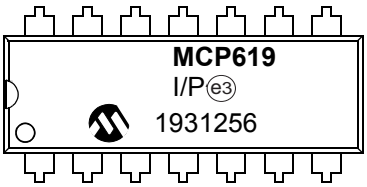
14-Lead PDIP (300 mil) (**MCP619**)



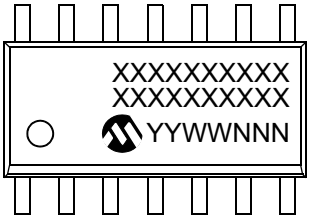
Examples:



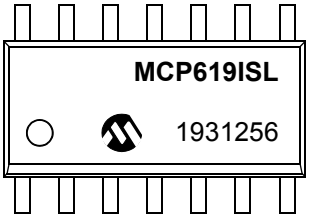
OR



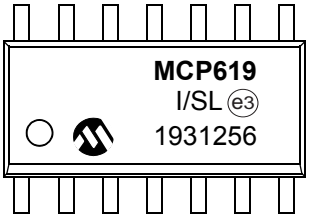
14-Lead SOIC (150 mil) (**MCP619**)



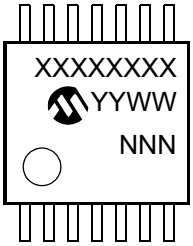
Examples:



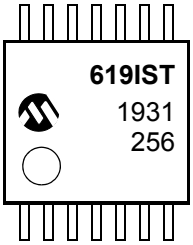
OR



14-Lead TSSOP (**MCP619**)

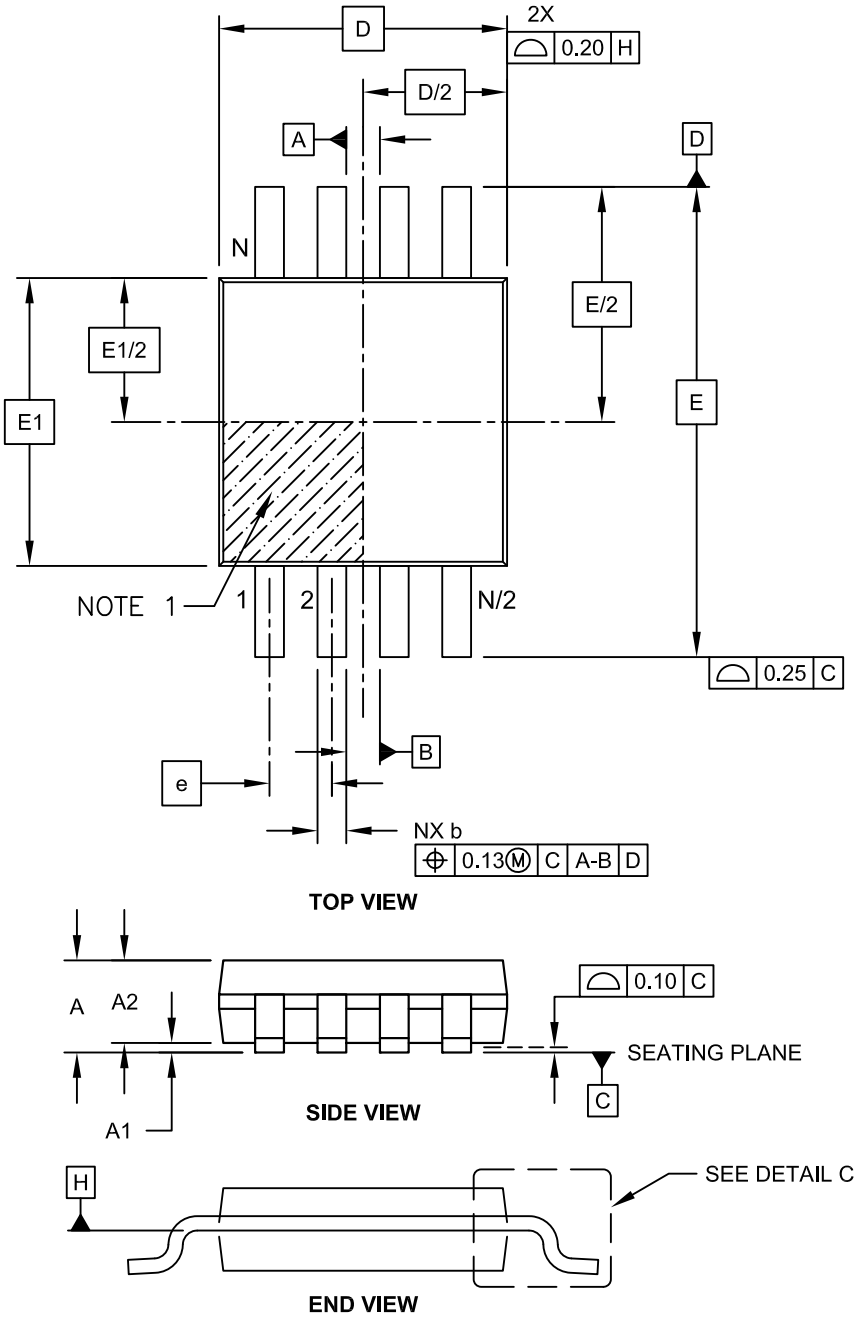


Example:



8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

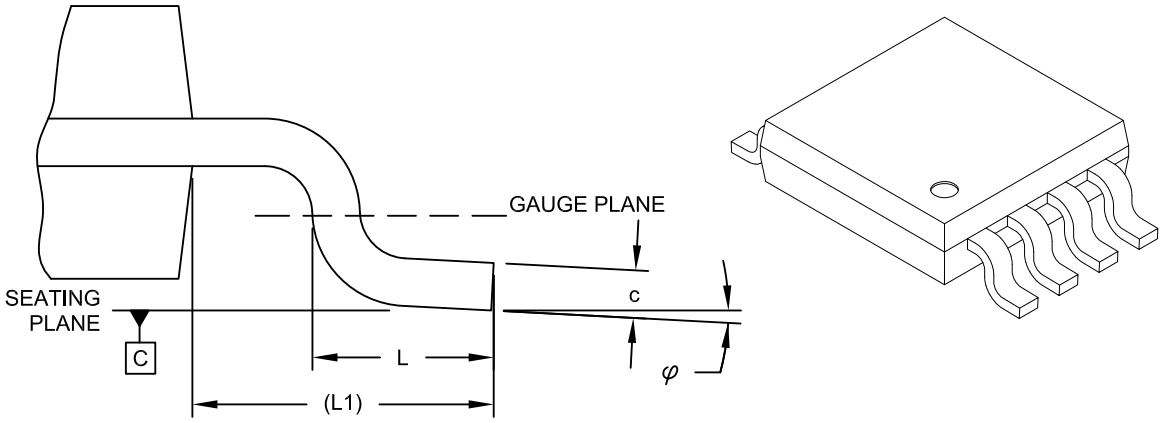
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

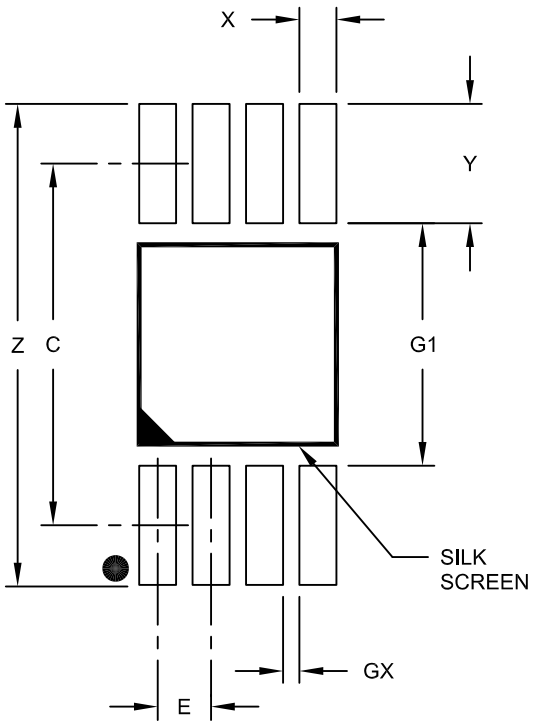
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

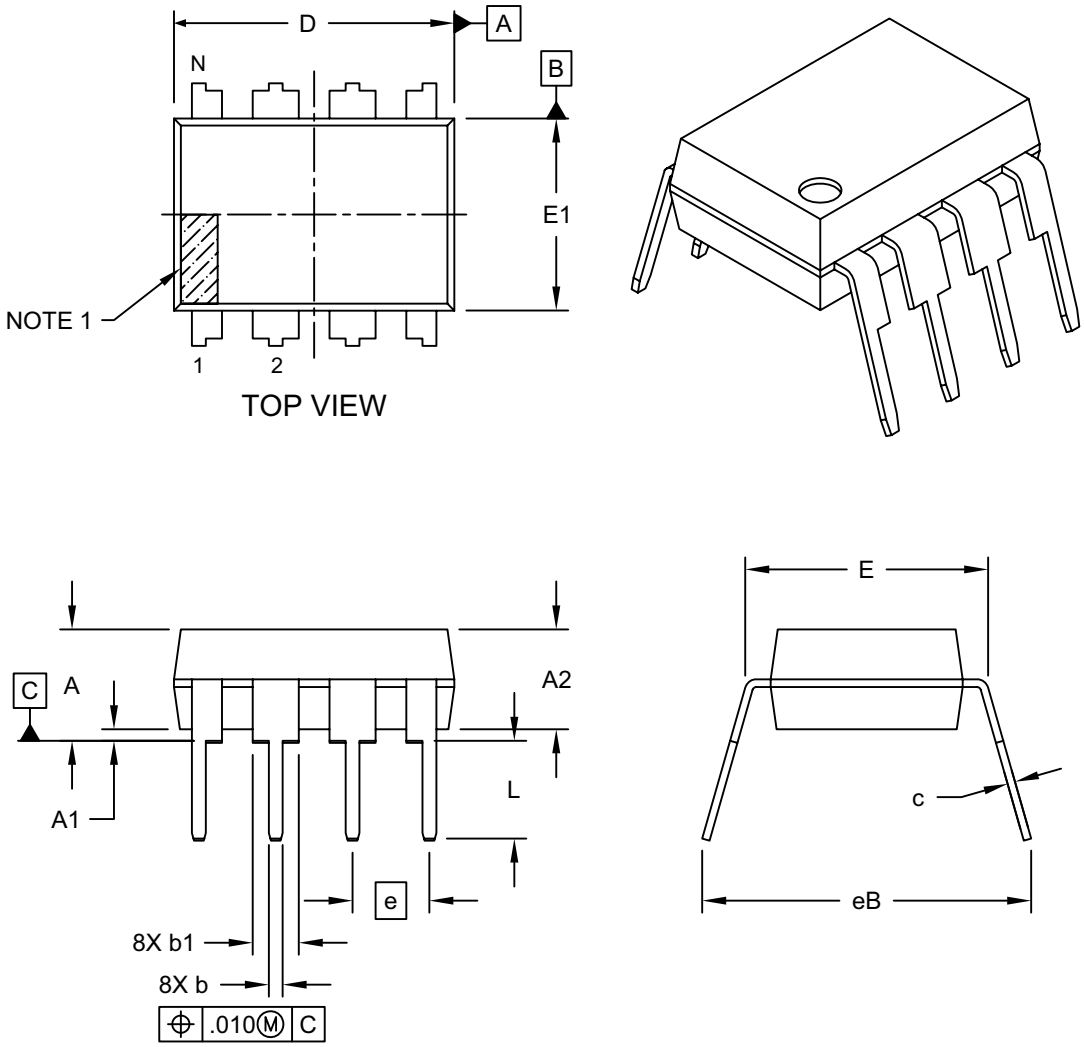
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

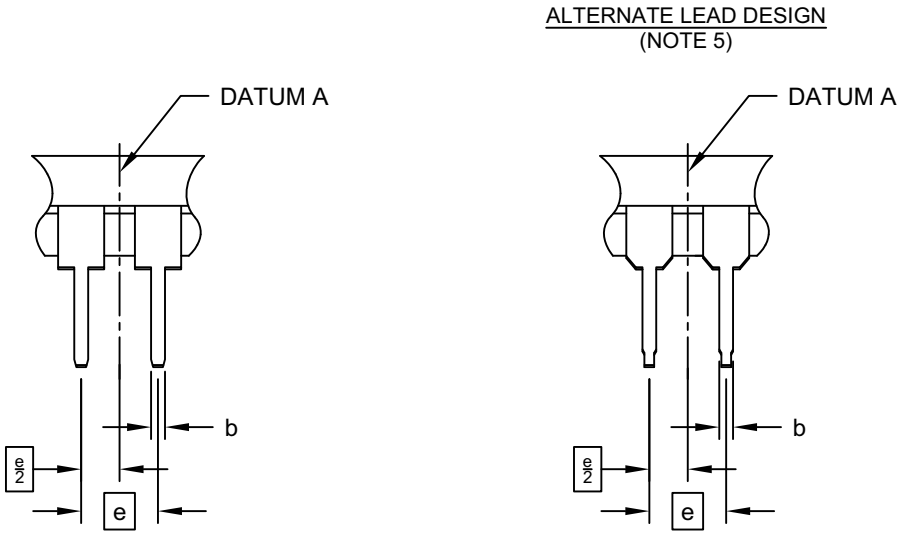
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

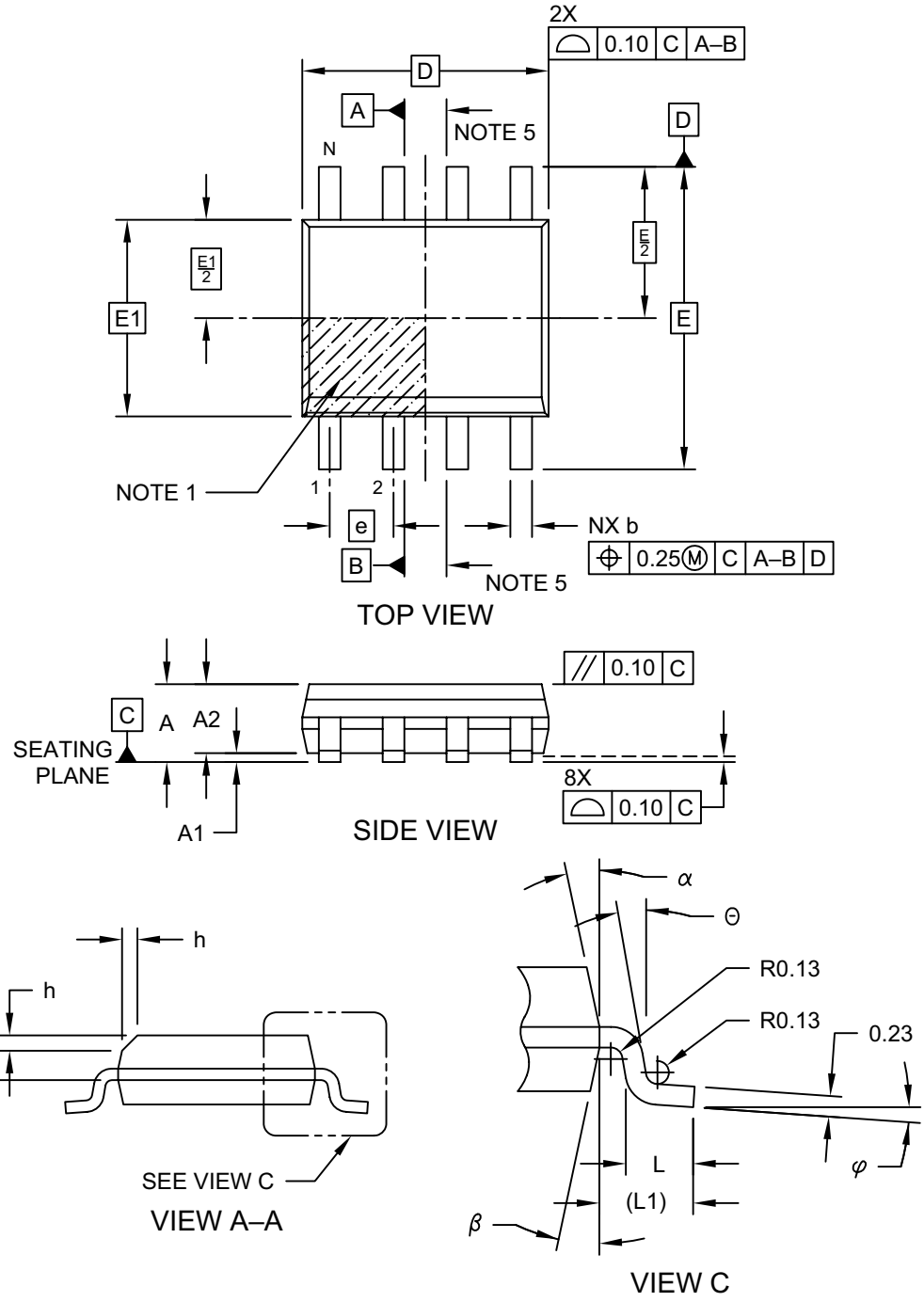
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

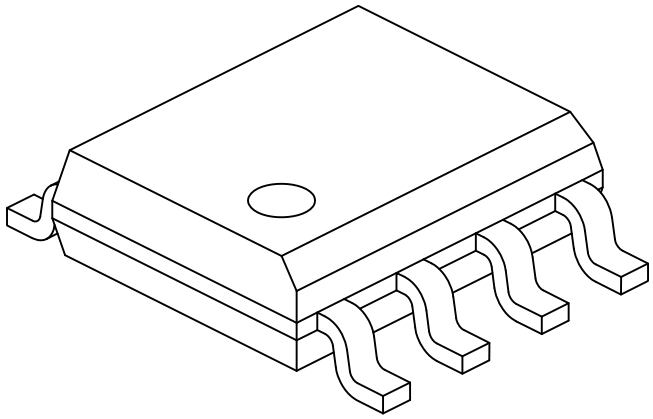
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev E Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

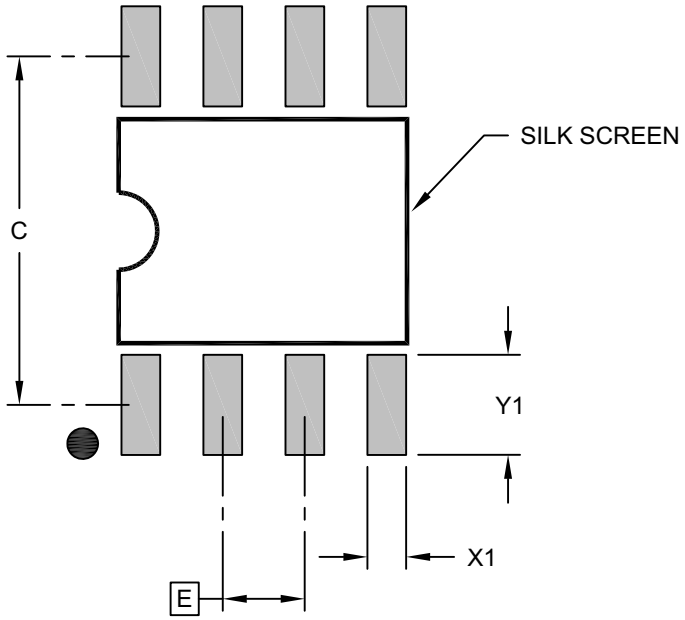
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

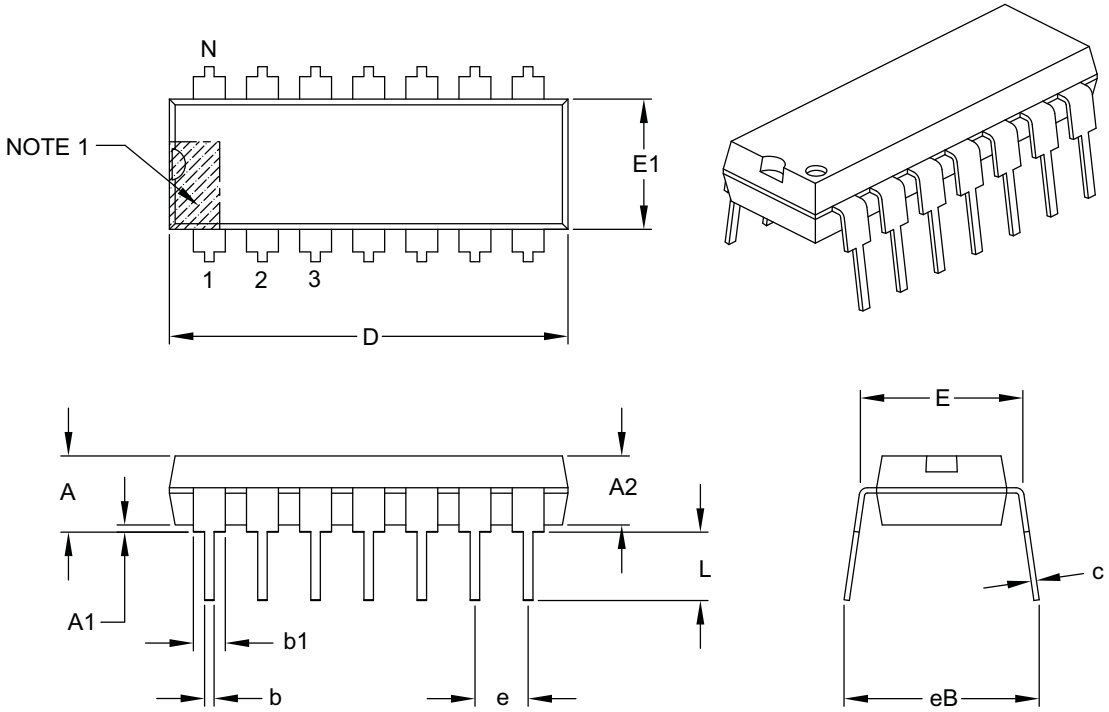
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev E

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

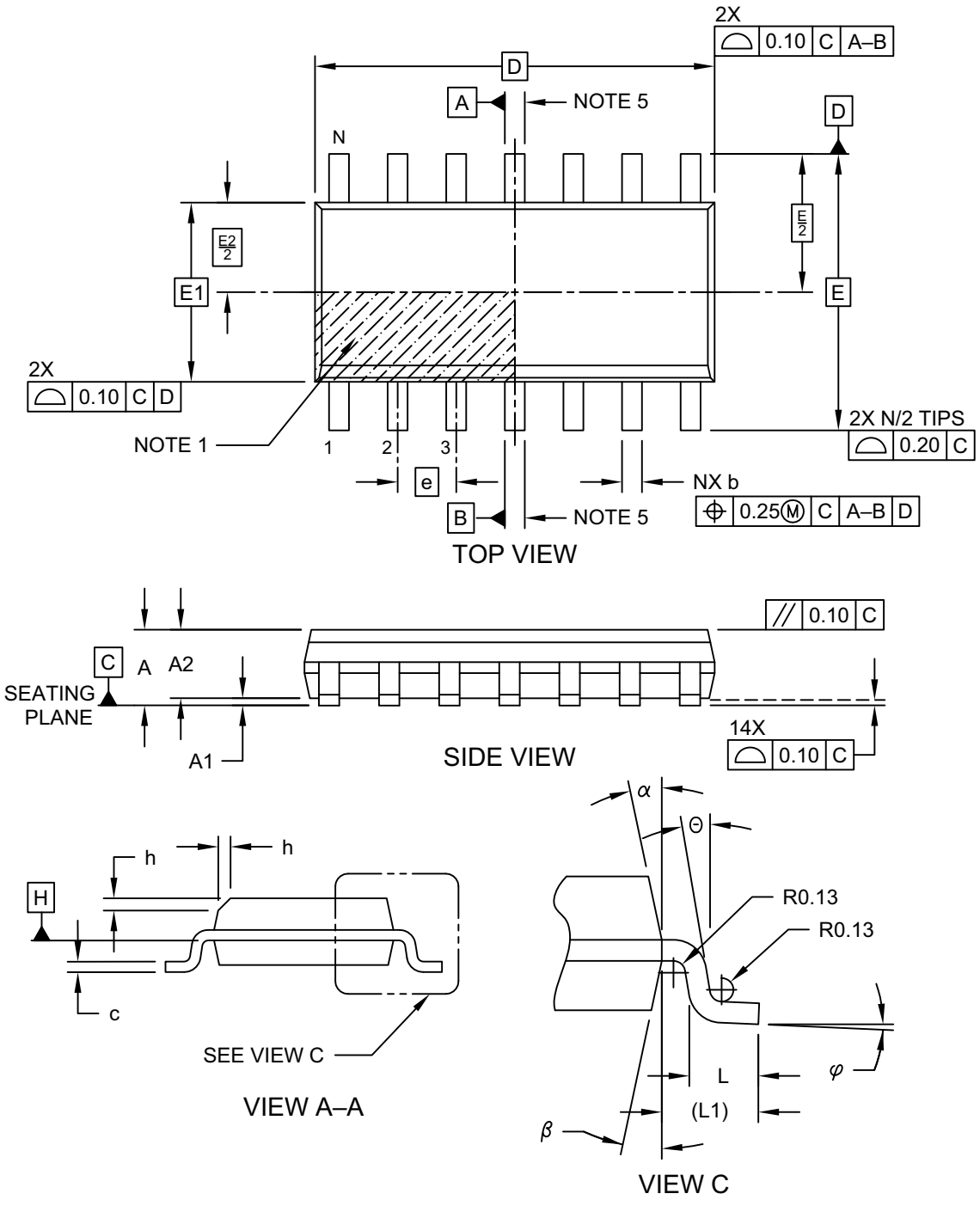
1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

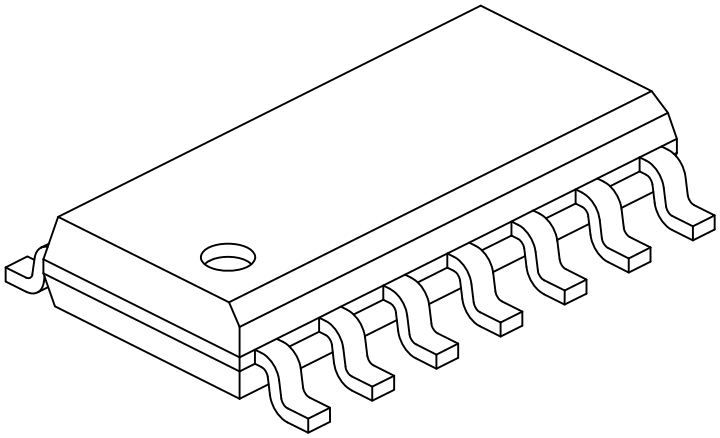
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

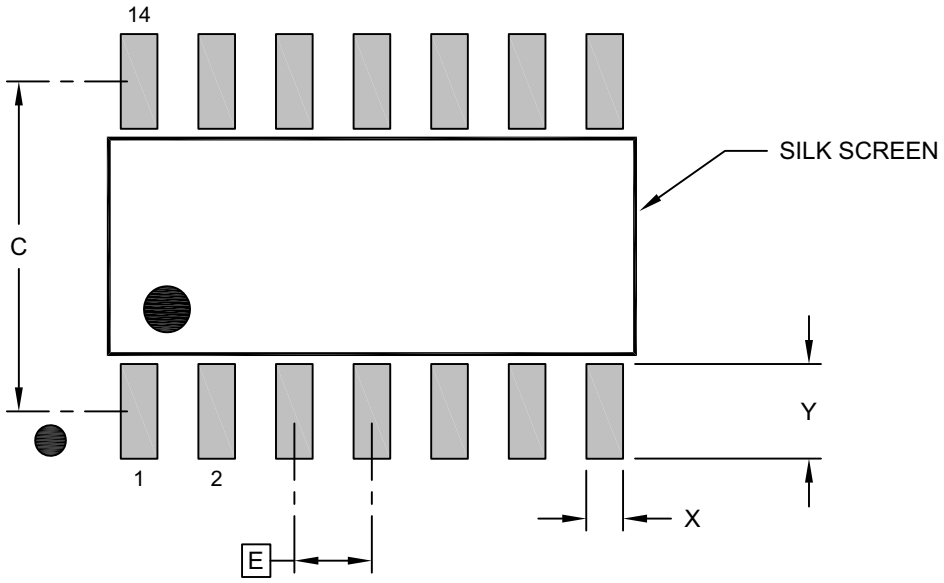
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

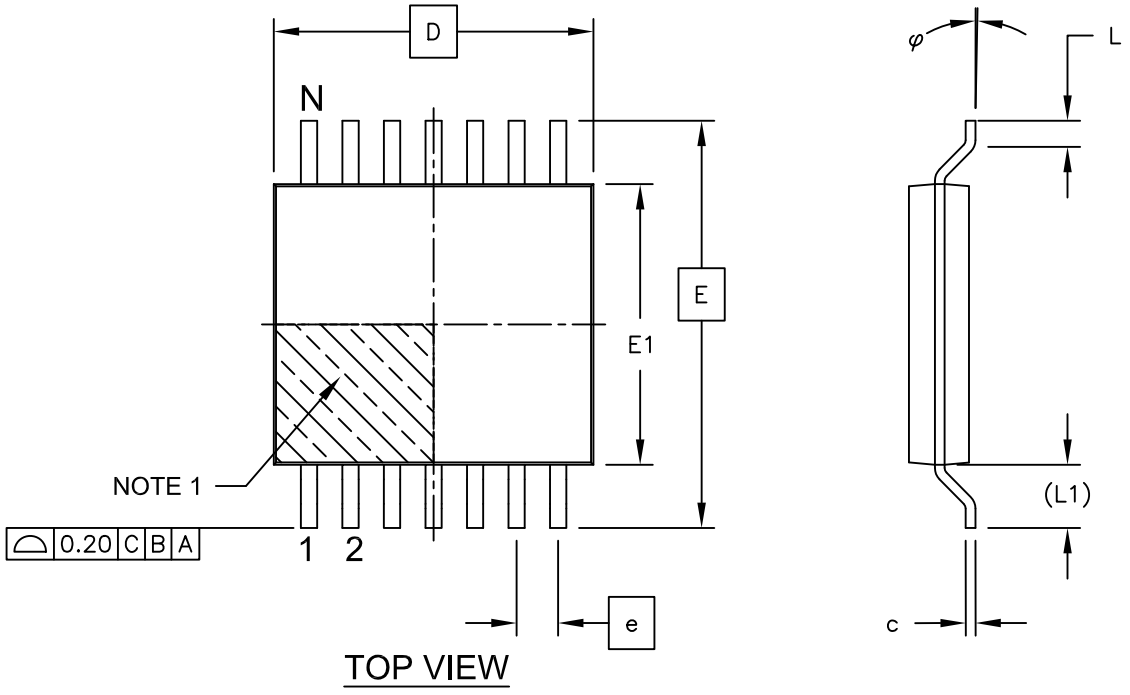
1. Dimensioning and tolerancing per ASME Y14.5M

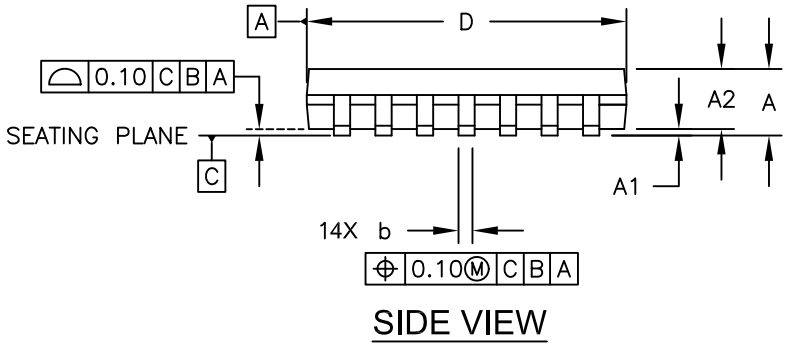
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

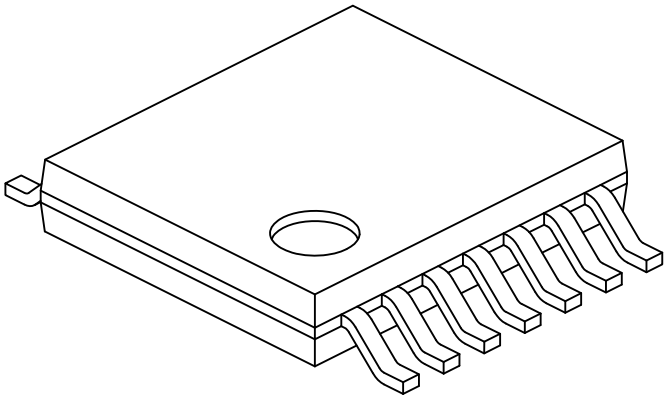




Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

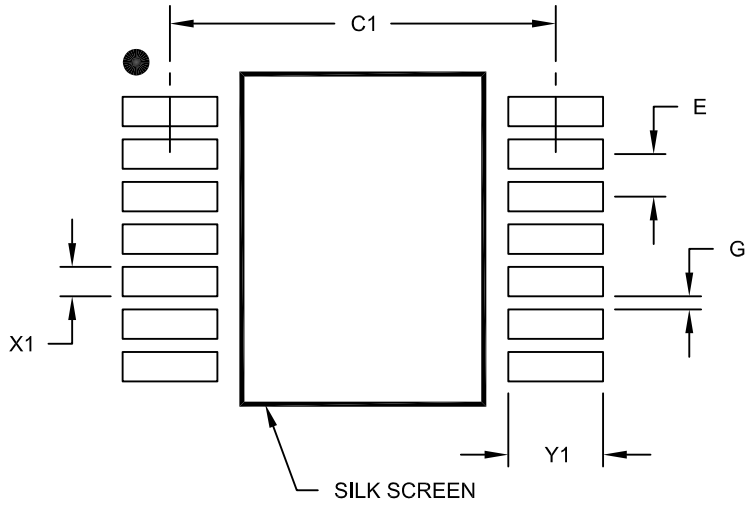
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

NOTES:

APPENDIX A: REVISION HISTORY

Revision D (November 2019)

The following is the list of modifications:

1. Updated **Section 6.0 "Packaging Information"**.

Revision C (October 2008)

The following is the list of modifications:

1. Added **Section 1.1 "Test Circuits"**.
2. Added Figure 2-36.
3. Added **Section 4.1.1 "Phase Reversal"**, **Section 4.1.2 "Input Voltage and Current Limits"**, and **Section 4.1.3 "Normal Operation"**.
4. Updated Figure 4-7.
5. Updated **Section 5.0 "Design Aids"**.
6. Updated **Section 6.0 "Packaging Information"**

Revision B (April 2005)

The following is the list of modifications:

1. Clarified specifications found in **Section 1.0 "Electrical Characteristics"**.
2. Updated **Section 2.0 "Typical Performance Curves"** and added input noise current density plot.
3. Added **Section 3.0 "Pin Descriptions"**.
4. Updated **Section 4.0 "Applications Information"**.
5. Updated the SPICE macro model and added information on the FilterLab software, in **Section 5.0 "Design Aids"**.
6. Corrected package marking information (**Section 6.0 "Packaging Information"**).
7. Added **Appendix A: "Revision History"**.

Revision A (April 2001)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	MCP616:	Single Operational Amplifier
	MCP616T:	Single Operational Amplifier (Tape and Reel for SOIC, MSOP)
	MCP617:	Dual Operational Amplifier
	MCP617T:	Dual Operational Amplifier (Tape and Reel for SOIC and MSOP)
	MCP618:	Single Operational Amplifier w/Chip Select ($\overline{CS}$)
	MCP618T:	Single Operational Amplifier w/Chip Select ($\overline{CS}$) (Tape and Reel for SOIC and MSOP)
	MCP619:	Quad Operational Amplifier
	MCP619T:	Quad Operational Amplifier (Tape and Reel for SOIC and TSSOP)
Temperature Range:	I =	-40°C to +85°C
Package:	MS =	Plastic MSOP, 8-lead
	P =	Plastic DIP (300 mil Body), 8-lead, 14-lead
	SN =	Plastic SOIC (3.90 mm body), 8-lead
	SL =	Plastic SOIC (3.90 mm Body), 14-lead (MCP619)
	ST =	Plastic TSSOP (4.4mm Body), 14-lead (MCP619)

Examples:

a)	MCP616-I/P:	Industrial Temperature, 8 lead PDIP.
b)	MCP616-I/SN:	Industrial Temperature, 8 lead SOIC.
c)	MCP616T-I/MS:	Tape and Reel, Industrial Temperature, 8 lead MSOP.
a)	MCP617-I/MS:	Industrial Temperature, 8 lead MSOP.
b)	MCP617T-I/MS:	Tape and Reel, Industrial Temperature, 8 lead MSOP.
c)	MCP617-I/P:	Industrial Temperature, 8 lead PDIP.
a)	MCP618-I/SN:	Industrial Temperature, 8 lead SOIC.
b)	MCP618T-I/SN:	Tape and Reel, Industrial Temperature, 8 lead SOIC.
c)	MCP618-I/P:	Industrial Temperature, 8 lead PDIP.
a)	MCP619T-I/SL:	Tape and Reel, Industrial Temperature, 14 lead SOIC.
b)	MCP619T-I/ST:	Tape and Reel, Industrial Temperature, 14 lead TSSOP.
c)	MCP619-I/P:	Industrial Temperature, 14 lead PDIP.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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