**NOTES:**

## 1.0 DEVICE OVERVIEW

The MCP201 provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus speeds up to 20 Kbaud.

The MCP201 provides a half-duplex, bidirectional communications interface between a microcontroller and the serial network bus. This device will translate the CMOS/TTL logic levels to LIN level logic, and vice versa.

The LIN specification 1.3 requires that the transceiver of all nodes in the system be connected via the LIN pin, referenced to ground and with a maximum external termination resistance of 510Ω from LIN bus to battery supply. The 510Ω corresponds to 1 Master and 16 Slave nodes.

The MCP201 provides a +5V 50 mA regulated power output. The regulator uses a LDO design, is short-circuit-protected and will turn the regulator output off if it falls below 3.5V. The MCP201 also includes thermal shutdown protection. The regulator has been specifically designed to operate in the automotive environment and will survive reverse battery connections, +40V load dump transients and double-battery jumps (see **Section 1.6 "Internal Voltage Regulator"**).

## 1.1 Optional External Protection

### 1.1.1 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 27V transient suppressor (TVS) diode, between $V_{BAT}$ and ground, with a 50Ω resistor in series with the battery supply and the $V_{BAT}$ pin, serves to protect the device from power transients (see Figure 1-2) and ESD events. While this protection is optional, it should be considered as good engineering practice.

### 1.1.2 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode can be used to provide polarity protection (see Figure 1-2). This protection is optional, but should be considered as good engineering practice.

## 1.2 Internal Protection

### 1.2.1 ESD PROTECTION

For component-level ESD ratings, please refer to the maximum operation specifications.

### 1.2.2 GROUND LOSS PROTECTION

The LIN bus specification states that the LIN pin must transition to the recessive state when ground is disconnected. Therefore, a loss of ground effectively forces the LIN line to a hi-impedance level.

### 1.2.3 THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator. Refer to Table 1-1 for details.

There are three causes for a thermal overload. A thermal shut down can be triggered by any one, or a combination of, the following thermal overload conditions.

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environment temperature

Driving the TXD and checking the RXD pin makes it possible to determine whether there is a bus contention (Rx = low, Tx = high) or a thermal overload condition (Rx = high, Tx = low).

| | |
|---|---|
| **Note:** | After recovering from a thermal, bus or voltage regulator overload condition, the device will be in the Ready1 mode. In order to go into Operational mode, the CS/WAKE pin has to be toggled. |

**TABLE 1-1: SOURCES OF THERMAL OVERLOAD(1,2)**

| TXD | RXD | Comments |
|---|---|---|
| L | H | LIN transmitter shutdown, receiver and voltage regulator active, thermal overload condition. |
| H | L | Regulator shutdown, receiver active, bus contention. |

**Legend:** x = Don't care, L = Low, H = High

**Note 1:** LIN transceiver overload current on the LIN pin is 200 mA.

**2:** Voltage regulator overload current on voltage regulator greater than 50 mA.

## 1.3 Modes of Operation

For an overview of all operational modes, please refer to Table 1-2.

### 1.3.1 POWER-DOWN MODE

In the Power-down mode, the transmitter and the voltage regulator are both off. Only the receiver section and the CS/WAKE pin wake-up circuits are in operation. This is the lowest power mode.

If any bus activity (e.g., a BREAK character) should occur during Power-down mode, the device will immediately enable the voltage regulator. Once the output has stabilized, the device will enter Ready mode.

The part will enter the Operation mode, if the CS/WAKE pin should become active-high ('1').

### 1.3.2 READY AND READY1 MODES

There are two states for the Ready mode. The only difference between these states is the transition during start-up. The state Ready1 mode ensures that the transition from Ready to Operation mode (once a rising edge of CS/WAKE) occurs without disrupting bus traffic.

Immediately upon entering either Ready1 or Ready mode, the voltage regulator will turn on and provide power. The transmitter portion of the circuit is off, with all other circuits (including the receiver) of the MCP201 being fully operational. The LIN pin is kept in a recessive state.

If a microcontroller is being driven by the voltage regulator output, it will go through a power-on reset and initialization sequence. All other circuits, other than the transmitter, are fully operational. The LIN pin is held in the recessive state.

The device will stay in Ready mode until the CS/WAKE pin transitions high ('1'). After CS/WAKE is active, the transmitter is enabled and the device enters Operation mode.

The device may only enter Power-down mode after going through the Operation mode step.

At power-on of the VBAT supply pin, the component is in either Ready or Ready1 mode, waiting for a CS/WAKE rising edge.

The MCP201 will stay in either mode for 600 µs as the regulator powers its internal circuitry and waits until the CS/WAKE pin transitions high. During the 600 µs delay, the MCP201 will not recognize a CS/WAKE event. The CS/WAKE transition from low to high should not occur until after this delay.

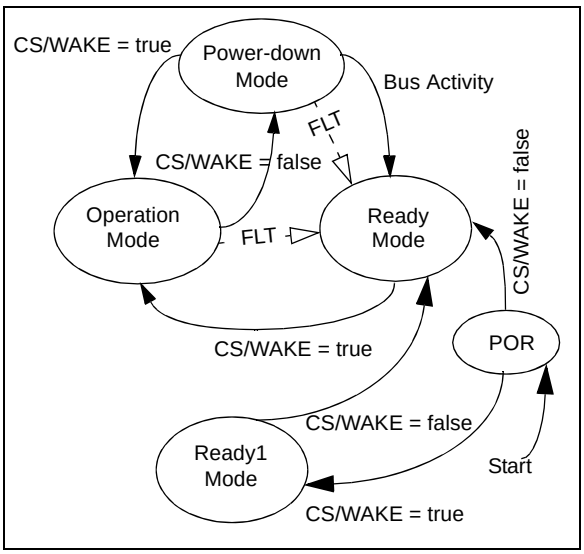
- The CS input is edge, not level, sensitive.
- The CS pin is not monitored until approximately 600 µs after VREG has stabized.
- The transistion from Ready1 to Ready is made on the falling edge of CS.
- The transition from Ready mode to Operational mode is on the rising edge of CS.

### 1.3.3 OPERATION MODE

In this mode, all internal modules are operational.

The MCP201 will go into Power-down mode on the falling edge of CS/WAKE.

**FIGURE 1-1: OPERATIONAL MODES STATE DIAGRAMS**




| | |
|---|---|
| **Note:** | After power-on, CS will not be sampled until VREG has stabized and an additional 600 µs has elapsed. The microcontroller should toggle CS approximately 1mS after RESET to ensure that CS will be recognized. |

| | |
|---|---|
| **Note:** | While the MCP201 is in shutdown, TXD should not be actively driven high. If TXD is driven high actively, it may power internal logic. |

### 1.3.4 DESCRIPTION OF BROWNOUT CONDITIONS

As VBAT decreases VREG is regulated to 5.0 VDC (see VREG in **Section 2.2 "DC Specifications"**) while VBAT is greater than 5.5 - 6.0 VDC.

As VBAT decreases further VREG tracks VBAT (VREG = VBAT - (0.5 to 1.0) VDC.

The MCP201 monitors VREG and as long as VREG does not fall below VSD (see VSD in **Section 2.2 "DC Specifications"**), VREG will remain powered.

As VBAT increases VREG will continue to track VBAT until VREG reaches 5.0 VDC.

If VREG falls below VSD, VREG is turned off and the MCP201 powers itself down.

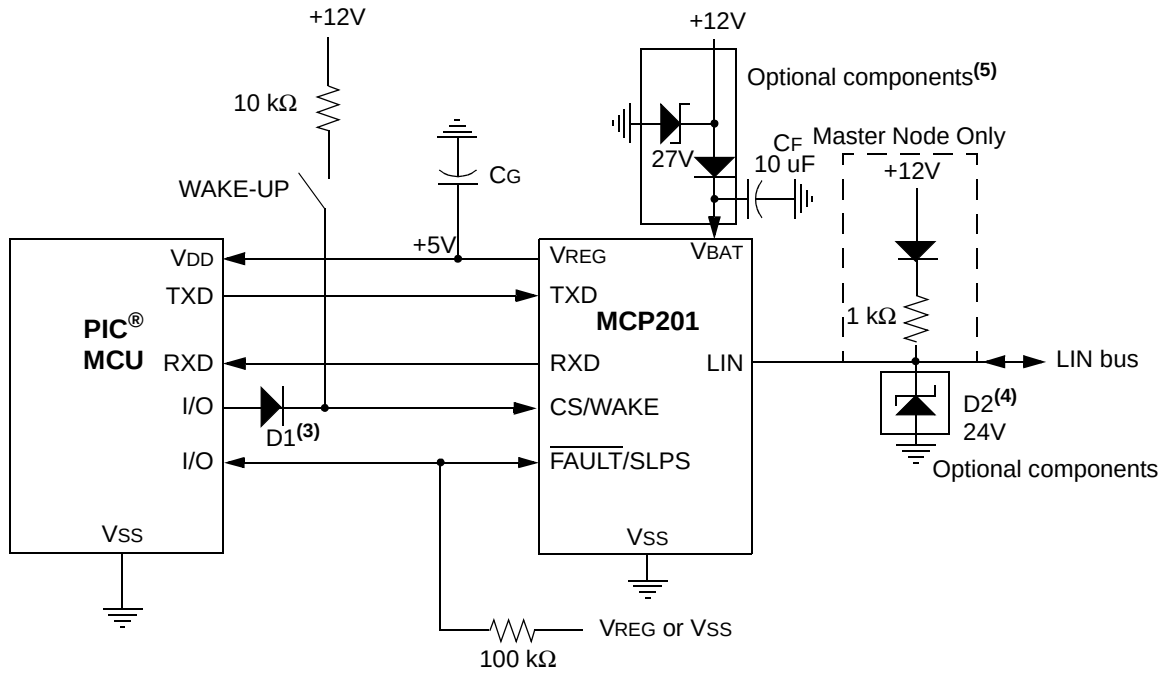
The MCP201 will remain powered down until VBAT increases above VON (see VON in **Section 2.2 "DC Specifications"**.

**TABLE 1-2: OVERVIEW OF OPERATIONAL MODES**

| State | Transmitter | Voltage Regulator | Operation | Comments |
|---|---|---|---|---|
| POR | OFF | OFF | Read CS/WAKE.<br>If low, then READY.<br>If high, READY1 mode. | Sample FAULT/SLPS and select slope |
| Ready | OFF | ON | If CS/WAKE rising edge, then Operation mode. | Bus Off state |
| Ready1 | OFF | ON | If CS/WAKE falling edge, then READY mode. | Bus Off state |
| Operation | ON | ON | If CS/WAKE falling edge, then Power down. | Normal Operation mode |
| Power-down | OFF | OFF | On LIN bus falling, go to READY mode.<br>On CS/WAKE rising edge, go to Operational mode | Low-Power mode |
| **Note:** After power-on, CS will not be sampled until $V_{REG}$ has stabized and an additional 600 µs has elapsed. The microcontroller should toggle CS approximately 1mS after RESET to ensure that CS will be recognized. | | | | |

## 1.4 Typical Applications

**FIGURE 1-2: TYPICAL MCP201 APPLICATION(1,2)**




**Note 1:** The load capacitor, CG, should be a ceramic or tantalum rated for extended temperatures and be in the range of 1.0 - 22 µF with an ESR 0.4Ω - 5Ω.

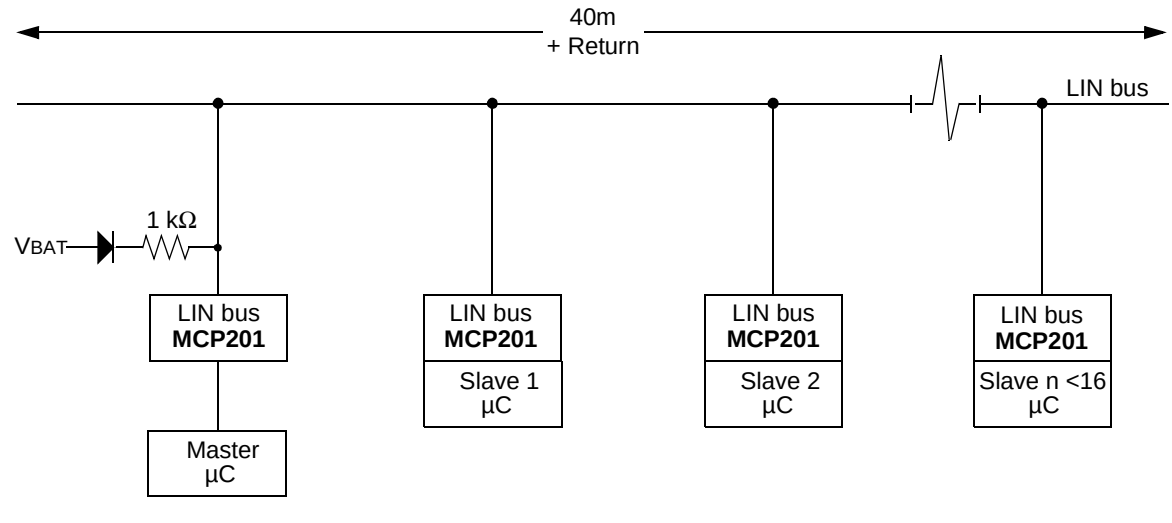
**2:** CF if the filter capacitor for the external voltage supply.

**3:** This diode is only needed if CS/WAKE is connected to 12V supply.

**4:** Transient suppressor diode. Vclamp L = 40V.

**5:** These components are for load dump protection.

**FIGURE 1-3: TYPICAL LIN NETWORK CONFIGURATION**



## 1.5 Pin Descriptions

**TABLE 1-3: MCP201 PINOUT OVERVIEW**

| Devices | Bond Pad Name | Function |
|---|---|---|
| 8-Pin PDIP/ SOIC/DFN | | Normal Operation |
| 1 | RXD | Receive Data Output (CMOS output) |
| 2 | CS/WAKE | Chip Select (TTL-HV input) |
| 3 | VREG | Power Output |
| 4 | TXD | Transmit Data Input (TTL) |
| 5 | VSS | Ground |
| 6 | LIN | LIN bus (bidirectional-HV) |
| 7 | VBAT | Battery |
| 8 | $\overline{\text{FAULT}}$/SLPS | Fault Detect Output, Slope Select Input |

**Legend:** TTL = TTL input buffer,
HV = High Voltage (VBAT)

### 1.5.1 RECEIVE DATA OUTPUT (RXD)

The Receive Data Output pin is a standard CMOS output and follows the state of the LIN pin.

The LIN receiver monitors the state of the LIN pin and generates the output signal RXD.

### 1.5.2 CS/WAKE

Chip Select Input pin. This pin controls whether the part goes into READY1 or READY mode at power-up. The internal pull-down resistor will keep the CS/WAKE pin low. This is done to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-on Reset and I/O initialization sequence. The pin must see a low-to-high transition to activate the transmitter.

After CS/WAKE transitions to '1', the transmitter is enabled. If CS/WAKE = '0', the device is in Ready1 mode on power-up or in Low-Power mode. In Low-Power mode, the voltage regulator is shut down, the transmitter driver is disabled and the receiver logic is enabled.

An external switch (see Figure 1-2) can then wake up both the transceiver and the microcontroller. An external-blocking diode and current-limiting resistor are necessary to protect the microcontroller I/O pin.

| | |
|---|---|
| **Note:** | On POR, the MCP201 enters Ready or Ready1 mode (see Figure 1-1). In order to enter Operational mode, the MCP201 has to see one rising edge on CS/WAKE 600 µs after the voltage regulator reaches 5V. |

### 1.5.3 POWER OUTPUT (VREG)

Positive Supply Voltage Regulator Output pin.

### 1.5.4 TRANSMIT DATA INPUT (TXD)

The Transmit Data Input pin has an internal pull-up to VREG. The LIN pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

In case the thermal protection detects an over-temperature condition while the signal TXD is low, the transmitter is shutdown. The recovery from the thermal shutdown is equal to adequate cooling time.

### 1.5.5 GROUND (VSS)

Ground pin.

### 1.5.6 LIN

The bidirectional LIN bus Interface pin is the driver unit for the LIN pin and is controlled by the signal TXD. LIN has an open collector output with a current limitation. To reduce EMI, the edges during the signal changes are slope-controlled.

### 1.5.7 BATTERY (VBAT)

Battery Positive Supply Voltage pin. This pin is also the input for the internal voltage regulator.

### 1.5.8 $\overline{\text{FAULT}}$/SLPS

FAULT Detect Output, Slope Select Input.

This pin is usually in Output mode. Its state is defined as shown in Table 1-5.

The state of this pin is internally sampled during power-on of VBAT. Once VBAT has reached a stable level, (approximately 6 VDC) and VREG is stable at 4.75 to 5.25 VDC, the state of this pin selects which slew rate profile to apply to the LIN output. It is only during this time that the pin is used as an input (the output driver is off during this time). The slope will stay selected until the next VBAT power-off/power-on sequence, regardless of any power-down, wake-up or SLEEP events. Only a VBAT rising state will cause a sampling of the $\overline{\text{FAULT}}$/SLPS pin. The Slope selection will be made irrespective of the state of any other pin.

The $\overline{\text{FAULT}}$/SLPS pin is connected to either VREG or VSS through a resistor (approximately 100 kΩ) to make the slope selection. This large resistance allows the FAULT indication function to overdrive the resistor in normal operation mode.

If the $\overline{\text{FAULT}}$/SLPS is high ('1'), the normal slope shaping is selected (dv/dt = 2 V/µs). If $\overline{\text{FAULT}}$/SLPS is low ('0') during this time, the alternate slope-shaping is selected (dv/dt = 4 V/µs). This mode can be used if a user desires to run at a faster slope. This mode is not LIN compliant.

**TABLE 1-4: $\overline{\text{FAULT}}$ / SLPS SLOPE SELECTION DURING POR**

| $\overline{\text{FAULT}}$/SLPS | Slope Shaping |
|---|---|
| H | Normal |
| L | Alternate(1) |

**Note 1:** This mode does not conform to LIN bus specification version 1.3, but might be used for K-line applications.

**Note:** This pin is '0' whenever the internal circuits have detected a short or thermal excursion and have disabled the LIN output driver.

**Note:** Every time TX is toggled, a Fault condition will occur for the length of time, depending on the bus load. The Fault time is equal to the propagation delay.

**TABLE 1-5: $\overline{\text{FAULT}}$ / SLPS TRUTH TABLE**

| TXD In | RXD Out | LIN Bus I/O | Thermal Override | $\overline{\text{FAULT}}$ / SLPS Out | Comments |
|---|---|---|---|---|---|
| L | H | $V_{BAT}$ | OFF | L | Bus shorted to battery |
| H | H | $V_{BAT}$ | OFF | H | Bus recessive |
| L | L | GND | OFF | H | Bus dominant |
| H | L | GND | OFF | L | Bus shorted to ground |
| x | x | $V_{BAT}$ | ON | L | Thermal excursion |

**Legend:** x = don't care

## 1.6 Internal Voltage Regulator

The MCP201 has a low drop-out voltage, positive regulator capable of supplying 5.00 VDC ±5% at up to 50 mA of load current over the entire operating temperature range. With a load current of 50 mA, the minimum input-to-output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 1.0 mA, with a full 50 mA load current, when the input-to-output voltage differential is greater than +2V.

The regulator requires an external output bypass capacitor for stability. The capacitor should be either a ceramic or tantalum for stable operation over the extended temperature range. The compensation capacitor should range from 1.0 µf – 22 µf and have a ESR or CSR of 0.4Ω – 5.0Ω. The input capacitor, $C_F$, in Figure 1.4 should be on the order of 8 to 10 times larger than the output capacitor, $C_G$.

Designed for automotive applications, the regulator will protect itself from reverse battery connections, double-battery jumps and up to +40V load dump transients. The voltage regulator has both short-circuit and thermal shutdown protection built-in.

Regarding the correlation between $V_{BAT}$, $V_{REG}$ and $I_{DD}$, please refer to Figure 1-4 through 1-6. When the input voltage ($V_{BAT}$) drops below the differential needed to provide stable regulation, the output $V_{REG}$ will track the input down to approximately 3.5V, at which point the regulator will turn off. This will allow microcontrollers with internal POR circuits to generate a clean arming of the Power-on Reset trip point. The MCP201 will then monitor $V_{BAT}$ and turn on the regulator when $V_{BAT}$ is 6.0V. The device will come up in either READY1 or READY mode and will have to be transitioned to Operational mode to re-enable data transmission.

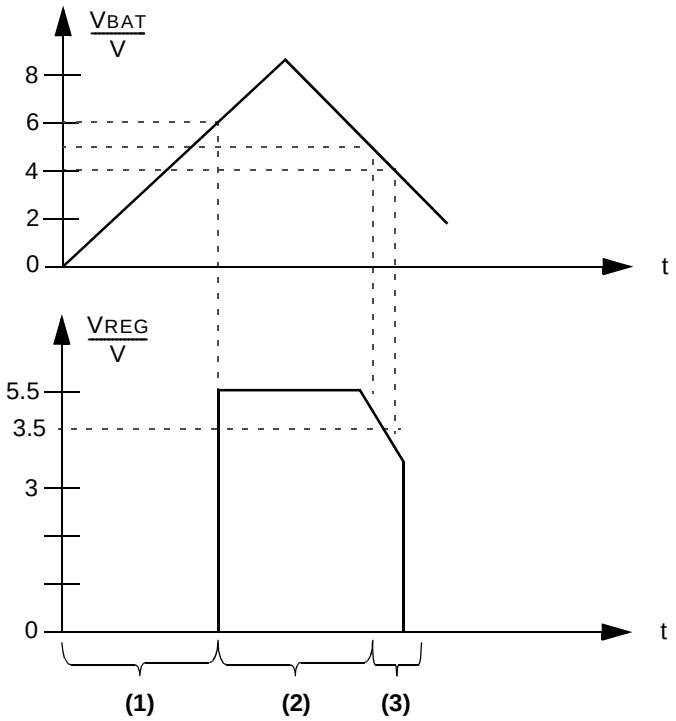
In the start phase, $V_{BAT}$ must be at least 6.0V (Figure 1-4) to initiate operation during power-up. In Power-down mode, the $V_{BAT}$ monitor will be turned off.

The regulator has a thermal shutdown. If the thermal protection circuit detects an overtemperature condition caused by an overcurrent condition (Figure 1-6) of the regulator, it will shut down.

The regulator has an overload current limiting. During a short-circuit, $V_{REG}$ is monitored. If $V_{REG}$ is lower than 3.5V, the regulator will turn off. After a thermal recovery time, the $V_{REG}$ will be checked again. If there is no short-circuit ($V_{REG}$ > 3.5V), the regulator will be switched back on. The MCP201 will come up in either READY1 or READY mode and will have to be transitioned to Operational mode to re-enable data transmission.

The accuracy of the voltage regulator, when using a pass transistor, will degrade due to the extra external components needed. All performance characteristics should be evaluated on every design.

**FIGURE 1-4: VOLTAGE REGULATOR OUTPUT ON POWER-ON RESET**

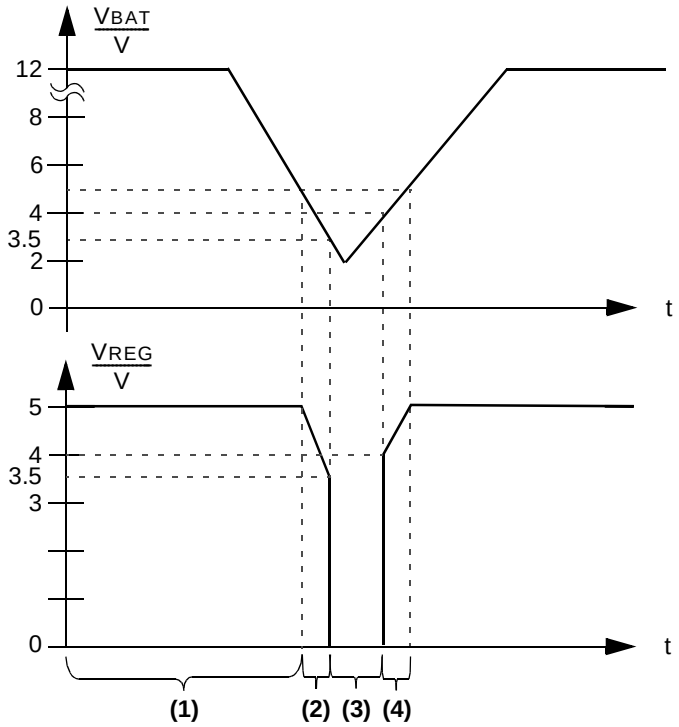



**Note 1:** Start-up, $V_{BAT}$ < 6.0V, regulator off.

**2:** $V_{BAT}$ > 6.0V, regulator on.

**3:** $V_{BAT} \leq$ 5.5V, regulator tracks $V_{BAT}$, regulator will turn off when $V_{REG}$ < 3.5V.

**FIGURE 1-5: VOLTAGE REGULATOR OUTPUT ON POWER DIP**



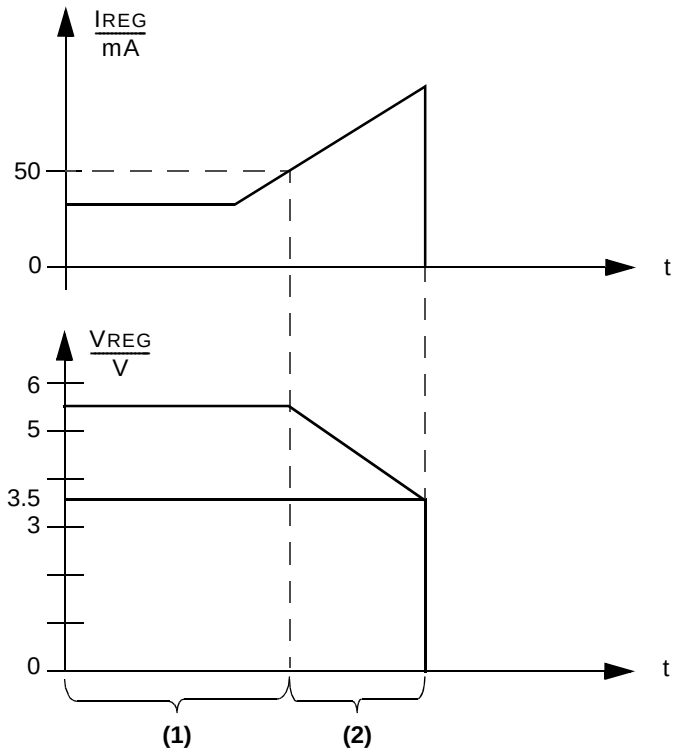

**Note 1:** Voltage regulator on.

**2:** $V_{REG} \leq 5.5V$, regulator tracks $V_{BAT}$ until $V_{REG} < 3.5V$.

**3:** $V_{REG} < 3.5V$, regulator is off. If the voltage regulator should shut off due to $V_{REG}$ falling below 3.5V, the $V_{BAT}$ must rise to 6.0V to turn $V_{REG}$ back on.

**4:** $V_{REG} > 4.0V$, voltage regulator tracks $V_{DD}$, when $V_{REG} > 4.0V$.

**FIGURE 1-6: VOLTAGE REGULATOR OUTPUT ON OVERCURRENT SITUATION**




**Note 1:** IREG less than 50 mA, regulator on.

**2:** After IREG exceeds IREGmax, voltage regulator output will be reduced until VREGoff is reached.

## 1.7 ICSP™ Considerations

The following should be considered when the MCP201 is connected to pins supporting in-circuit programming:

- Power used for programming the microcontroller should be supplied from the programmer, not from the MCP201
- The MCP201 should be left unpowered
- The voltage on VREG should not exceed the maximum output voltage of VREG
- The TXD pin should not be brought high during programming

**NOTES:**

# 2.0 ELECTRICAL CHARACTERISTICS

## 2.1 Absolute Maximum Ratings†

$V_{IN}$ DC Voltage on Logic pins except CS/WAKE ..... -0.3 to $V_{REG}$+0.3V

$V_{IN}$ DC Voltage on CS/WAKE ..... -0.3 to $V_{BAT}$+0.3V

$V_{BAT}$ Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) ..... -0.3 to +40V

$V_{BAT}$ Battery Voltage, transient (**Note 1**) ..... -0.3 to +40V

$V_{BAT}$ Battery Voltage, continuous ..... -0.3 to +30V

$V_{LBUS}$ Bus Voltage, continuous ..... -18 to +30V

$V_{LBUS}$ Bus Voltage, transient (**Note 1**) ..... -27 to +40V

$I_{LBUS}$ Bus Short Circuit Current Limit ..... 200 mA

ESD protection on LIN, $V_{BAT}$ (Human Body Model) (**Note 2**) ..... >4 kV

ESD protection on all other pins (Human Body Model) (**Note 2**) ..... >2 kV

Maximum Junction Temperature ..... 150°C

Storage Temperature ..... -55 to +150°C

**Note 1:** ISO 7637/1 load dump compliant (t < 500 ms).

**2:** According to JESD22-A114-B.

† **NOTICE**: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## 2.2 DC Specifications

| DC Specifications | | Electrical Characteristics: Unless otherwise indicated, all limits are specified for: $V_{BAT}$ = 6.0V to 18.0V, $T_{AMB}$ = -40°C to +125°C, $C_{LOADREG}$ = 10 µF | | | | |
|---|---|---|---|---|---|---|
| **Sym.** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| | **Power** | | | | | |
| $I_{BATQ}$ | $V_{BAT}$ Quiescent Operating Current (voltage regulator without load and transceiver) | — | 0.45 | 1.0 | mA | $I_{VREG}$ = 0 mA, LIN bus pin recessive, **(Note 3)** |
| $I_{BAT}$ | $V_{BAT}$ Power-down Current transceiver only | — | 23 | 50 | µA | CS/WAKE = High, voltage regulator disabled |
| $I_{DDQ}$ | $V_{REG}$ Quiescent Operating Current | — | 500 | — | µA | **(Note 2)** |
| $I_{VREG}$ | $V_{REG}$ maximum output current | — | — | 50 | mA | **(Note 4)** |
| | **Microcontroller Interface** | | | | | |
| $V_{IH}$ | High-level Input Voltage (TXD, FAULT/SLPS) | 2.0 | — | $V_{REG}$ + 0.3 | V | |
| $V_{IL}$ | Low-level Input Voltage (TXD, FAULT/SLPS) | -0.3 | — | 0.15 x $V_{REG}$ | V | |
| $I_{IHTXD}$ | High-level Output Current (TXD) | -90 | — | +30 | µA | Input voltage = 4V |
| $I_{ILTXD}$ | Low-level Output Current (TXD) | -150 | — | -10 | µA | Input voltage = 1V (though > 50 kΩ internal pull-up) |
| $V_{IHCS/WAKE}$ | High-level Input Voltage (CS/WAKE) | 3.0 | — | $V_{BAT}$ | V | Through an external current-limiting resistor (10 kΩ) |
| $V_{ILCS/WAKE}$ | Low-level Input Voltage (CS/WAKE) | -0.3 | — | 1.0 | V | |
| $I_{IHCS/WAKE}$ | High-level Input Current (CS/WAKE) | -10 | — | +80 | µA | Input voltage = 4V (though >100 kΩ internal pull-down) |
| $I_{ILCS/WAKE}$ | Low-level Input Current (CS/WAKE) | 5 | — | 30 | µA | Input voltage = 1V |
| $V_{OHRXD}$ | High-level Output Voltage (RXD) | 0.8 $V_{REG}$ | — | — | | $I_{OH}$ = -4 mA |
| $V_{OLRXD}$ | Low-level Output Voltage (RXD) | — | — | 0.2 $V_{REG}$ | | $I_{OL}$ = 4 mA |

**Note 1:** Internal current limited. 2.0 ms typical recovery time ($R_{LBUS}$ = 0Ω, TX = 0.4 $V_{REG}$, $V_{LBUS}$ = $V_{BAT}$, $T_{AMB}$ = 25C. Recovery time highly dependent on ambient temperature, package and thermal resistance).

**2:** For design guidance only, not tested.

**3:** This current is at the $V_{BAT}$ pin.

**4:** The maximum power dissipation is a function of $T_{JMAX}$, $\Theta_{JA}$ and ambient temperature $T_A$. The maximum allowable power dissipation at an ambient temperature is $P_D$ = ($T_{JMAX}$ - $T_A$)$\Theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the MCP201 will go into thermal shutdown.

## 2.2 DC Specifications (Continued)

| DC Specifications | | Electrical Characteristics: Unless otherwise indicated, all limits are specified for: $V_{BAT}$ = 6.0V to 18.0V, $T_{AMB}$ = -40°C to +125°C, $C_{LOADREG}$ = 10 µF | | | | |
|---|---|---|---|---|---|---|
| **Sym.** | **Parameter** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| | **Bus Interface** | | | | | |
| $V_{IHLBUS}$ | High-level Input Voltage ($L_{BUS}$) | 0.6 $V_{BAT}$ | — | 18 | V | Recessive state |
| $V_{ILLBUS}$ | Low-level Input Voltage ($L_{BUS}$) | -8 | — | 0.4 $V_{BAT}$ | V | Dominant state |
| $V_{HYS}$ | Input Hysteresis | 0.05 $V_{BAT}$ | — | 0.1 $V_{BAT}$ | V | $V_{IH}$ - $V_{IL}$ |
| $I_{OL}$ | Low-level Output Current ($L_{BUS}$) | 40 | — | 200 | mA | Output voltage = 0.1 $V_{BAT}$, $V_{BAT}$ = 12V |
| $I_O$ | High-level Output Current ($L_{BUS}$) | -20 | — | 20 | µA | $V_{BUS} \geq V_{BAT}$, $V_{LBUS}$ < 40V |
| $I_P$ | Pull-up Current on Input ($L_{BUS}$) | -180 | — | -60 | µA | Approx. 30 kΩ internal pull-up @ $V_{IH}$ = 0.7 $V_{BAT}$ |
| $I_{SC}$ | Short-circuit Current-Limit | 50 | — | 200 | mA | **(Note 1)** |
| $V_{OH}$ | High-level Output Voltage ($L_{BUS}$) | 0.8 $V_{BAT}$ | — | — | V | |
| $V_{OL}$ | Low-level Output Voltage ($L_{BUS}$) | — | — | 0.2 $V_{BAT}$ | V | |
| | **Voltage Regulator** | | | | | |
| $V_{REG}$ | Output Voltage | 4.75 | — | 5.25 | V | 0 mA > $I_{OUT}$ > 50 mA, 7.0V < $V_{BAT}$ < 18V |
| $V_{REG1}$ | Output Voltage | 4.4 | — | 5.25 | V | 0 mA > $I_{OUT}$ > 50 mA, 6.0V < $V_{BAT}$ < 7.0V |
| $\Delta V_{REG1}$ | Line Regulation | — | 10 | 50 | mV | $I_{OUT}$ = 1 mA, 7.0V < $V_{BAT}$ < 18V |
| $\Delta V_{REG2}$ | Load Regulation | — | 10 | 50 | mV | 5 mA < $I_{OUT}$ < 50 mA, $V_{BAT}$ = Constant |
| $V_N$ | Output Noise Voltage | — | — | 400 | µ$V_{RMS}$ | 1 $V_{RMS}$ @ 10 Hz - 100 kHz |
| $V_{SD}$ | Shutdown Voltage (monitoring $V_{REG}$) | 3.5 | — | 4.0 | V | See **Figure 1-4** |
| $V_{ON}$ | Input Voltage to Turn On Output (monitoring $V_{BAT}$) | 5.5 | — | 6.0 | V | |

**Note 1:** Internal current limited. 2.0 ms typical recovery time ($R_{LBUS}$ = 0Ω, TX = 0.4 $V_{REG}$, $V_{LBUS}$ = $V_{BAT}$, $T_{AMB}$ = 25C. Recovery time highly dependent on ambient temperature, package and thermal resistance).

**2:** For design guidance only, not tested.

**3:** This current is at the $V_{BAT}$ pin.

**4:** The maximum power dissipation is a function of $T_{JMAX}$, $\Theta_{JA}$ and ambient temperature $T_A$. The maximum allowable power dissipation at an ambient temperature is $P_D$ = ($T_{JMAX}$ - $T_A$)$\Theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the MCP201 will go into thermal shutdown.

## 2.3 AC Specifications

| AC Specifications | | Electrical Characteristics: Unless otherwise indicated, all limits are specified for: $V_{BAT}$ = 6.0V to 18.0V $T_{AMB}$ = -40°C to +125°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Typical** | **Max** | **Units** | **Conditions** |
| | **Bus Interface** | | | | | |
| \|dV/dt\| | Slope Rising and Falling Edges | 1.0 | 2.0 | 3.0 | V/µs | (40% to 60%), No Load |
| \|dV/dt\| | Slope Rising and Falling edges ALTERNATE | 2.0 | 4.0 | 6.0 | V/µs | (**Note 1**), No Load |
| $t_{TRANSPD}$ | Propagation Delay of Transmitter | — | — | 6.0 | µs | $t_{RECPD}$ = max |
| $t_{RECPD}$ | Propagation Delay of Receiver | — | — | 6.0 | µs | ($t_{RECPDR}$ or $t_{RECPDF}$) |
| $t_{RECSYM}$ | Symmetry of Propagation Delay of Receiver Rising Edge with Respect to Falling Edge | -2.0 | — | 2.0 | µs | $t_{RECSYM}$ = max |
| $t_{TRANSSYM}$ | Symmetry of Propagation Delay of Transmitter Rising Edge with Respect to Falling Edge | -2.0 | — | 2.0 | µs | $t_{TRANSSYM}$ = max ($t_{TRANSPDF}$ - $t_{RANSPDR}$) |
| | **Voltage Regulator** | | | | | |
| $t_{BACTVE}$ | Bus Activity to Voltage Regulator Enabled | 10 | — | 40 | µs | Bus debounce time |
| $t_{VEVR}$ | Voltage Regulator Enabled to Ready | — | 50 | 200 | µs | **(Note 2)** |
| $t_{VREGPOR}$ | Voltage Regulator Enabled to Ready after POR | — | — | 2.5 | ms | **(Note 2)** $C_{LOAD}$ = 25 nF |
| $t_{CSOR}$ | Chip Select to Operation Ready | 0 | 50 | 200 | µs | **(Note 2)** |
| $t_{CSPD}$ | Chip Select to Power-down | 0 | — | 40 | µs | **(Note 2)** No $C_{LOAD}$ |
| $t_{SHUTDOWN}$ | Short-Circuit to Shutdown | — | 450 | — | µs | Characterized but not tested |
| tSCREC | Short-Circuit Recovery Time | — | 2.0 | — | ms | Characterized but not tested **(Note 3)** |

**Note 1:** The mode does not conform to LIN Bus specification version 1.3.

**2:** Time depends on external capacitance and load.

**3:** Internal current limited. 2.0 ms typical recovery time ($R_{LBUS}$ = 0Ω, TX = 0.4 $V_{REG}$, $V_{LBUS}$ = $V_{BAT}$, $T_{AMB}$ = 25C. Recovery time highly dependent on ambient temperature, package, and thermal resistance).

**TABLE 2-1: MCP201 THERMAL SPECIFICATIONS**

| Sym | Parameter | Min | Typical | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $\theta_{RECOVERY}$ | Recovery Temperature (junction temperature) | — | +135 | — | °C | Characterized but not tested |
| $\theta_{SHUTDOWN}$ | Shutdown Temperature (junction temperature) | — | +155 | — | °C | Characterized but not tested |
| $t_{THERM}$ | Thermal Recovery Time (after Fault condition removed) | — | 2.0 | — | ms | Characterized but not tested **(Note 1)** |

**Note 1:** Internal current limited. 2.0 ms typical recovery time ($R_{LBUS}$ = 0Ω, TX = 0.4 $V_{REG}$, $V_{LBUS}$ = $V_{BAT}$, $T_{AMB}$ = 25C. Recovery time highly dependent on ambient temperature, package, and thermal resistance).

## 2.4 Timing Diagrams and Specifications

**FIGURE 2-1: BUS TIMING DIAGRAM**

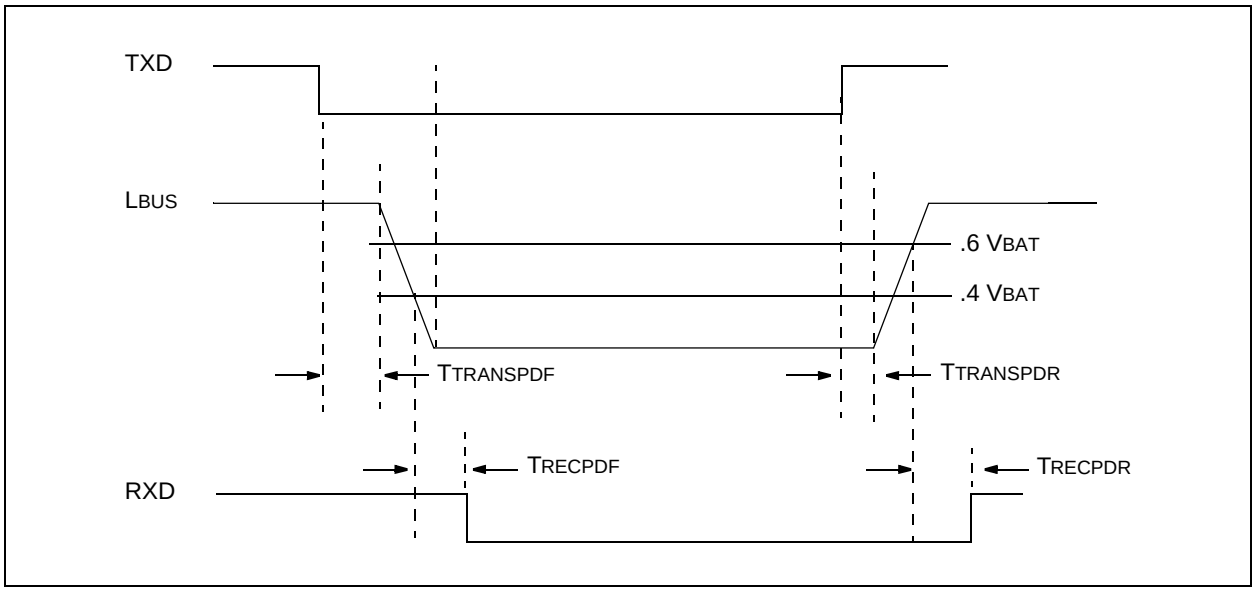



**FIGURE 2-2: REGULATOR TIMING DIAGRAM ON CS/WAKE SIGNAL**

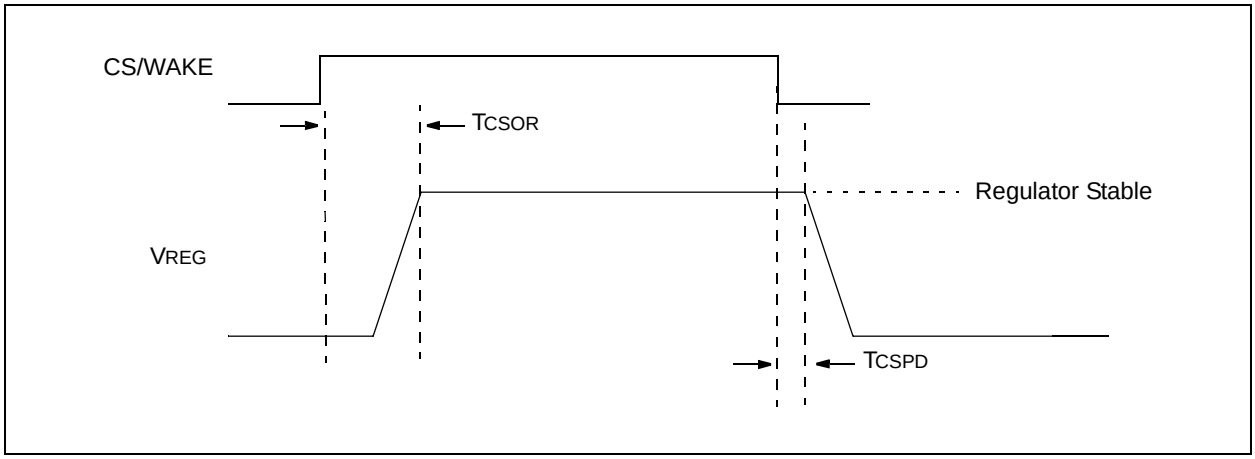


**FIGURE 2-3: REGULATOR TIMING DIAGRAM ON BUS ACTIVITY**

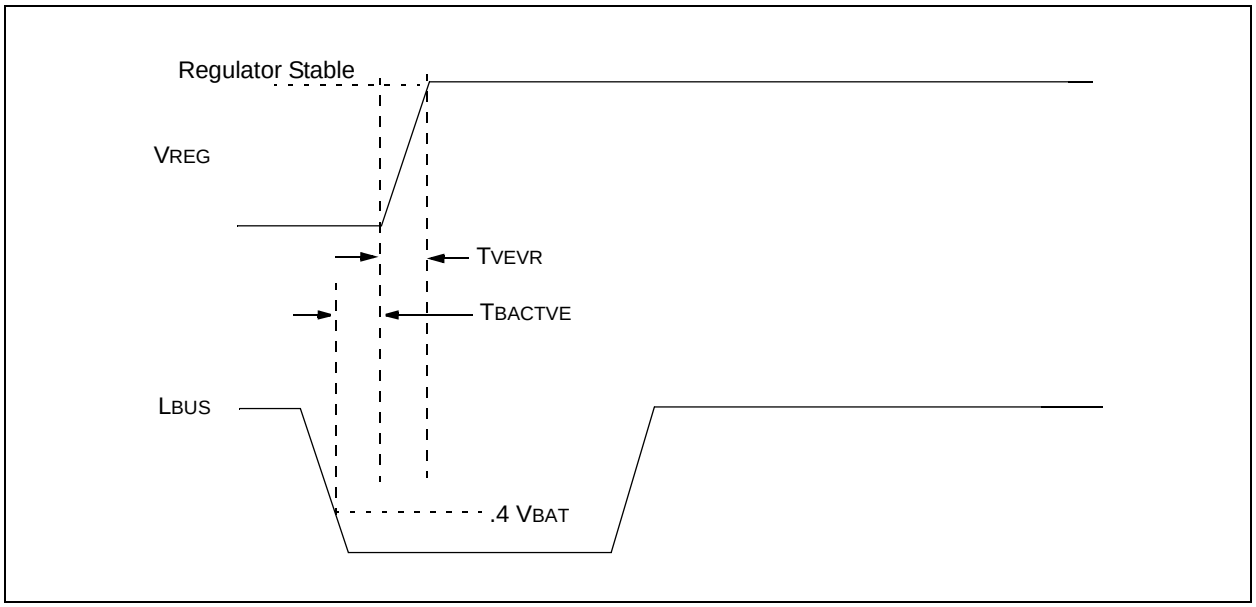
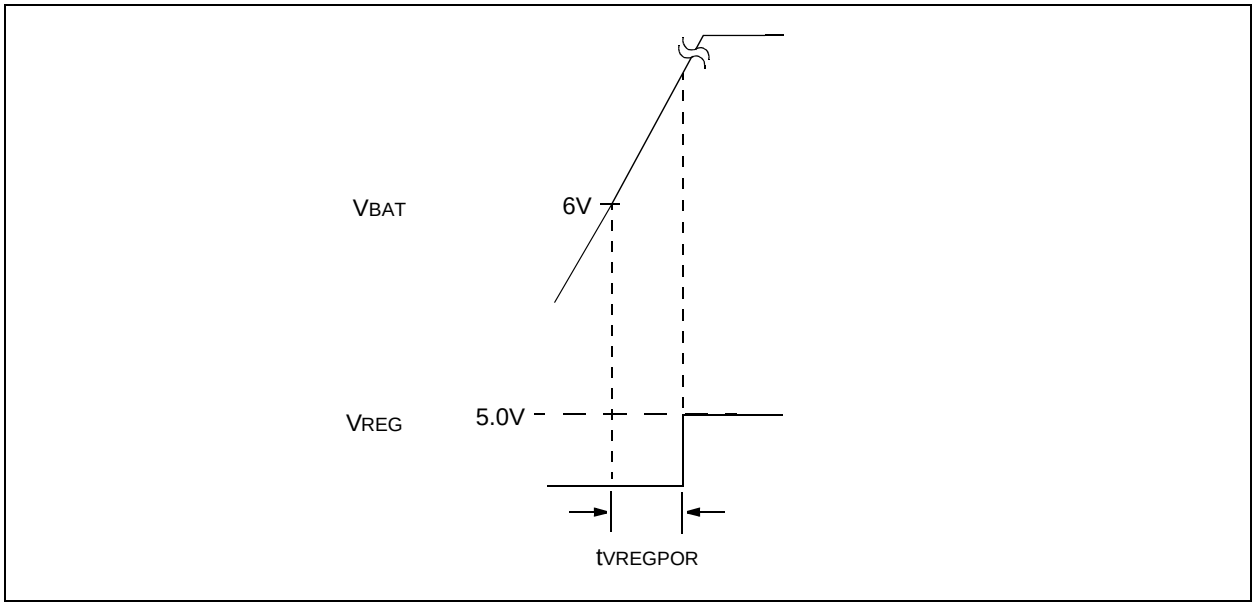



**FIGURE 2-4: POR DIAGRAM**



## 3.0 CHARACTERIZATION GRAPHS

**FIGURE 3-1: IDD(mA) vs. VBAT**

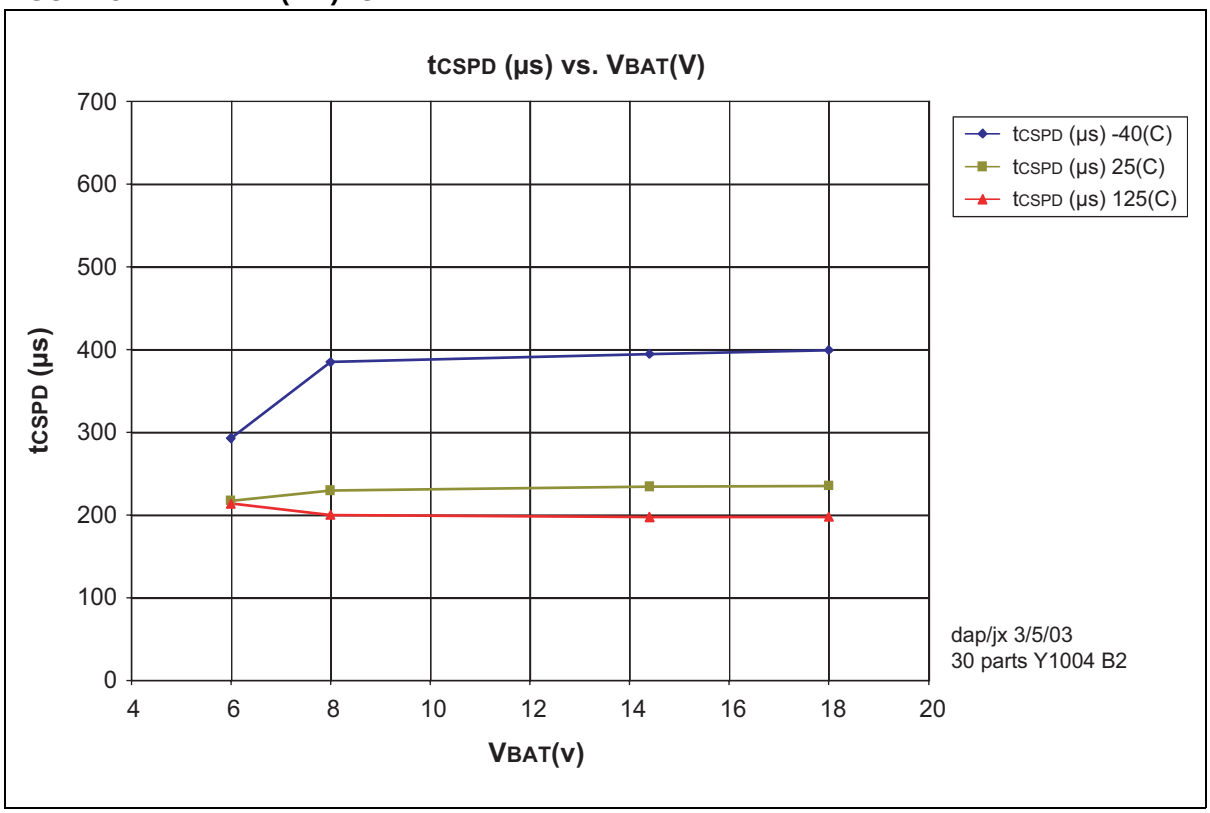


**FIGURE 3-2: REGULATOR VOLTAGE (V) VS. REGULATOR CURRENT**

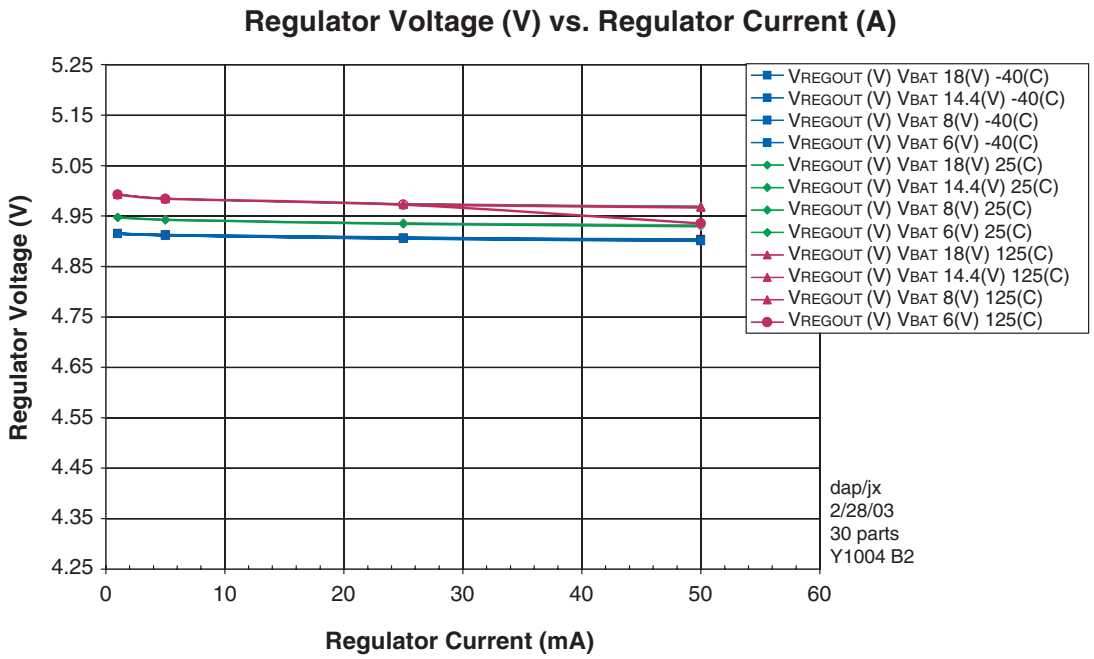


**FIGURE 3-3: REGULATOR CHANGE (V) VS. LINE VOLTAGE CHANGE**

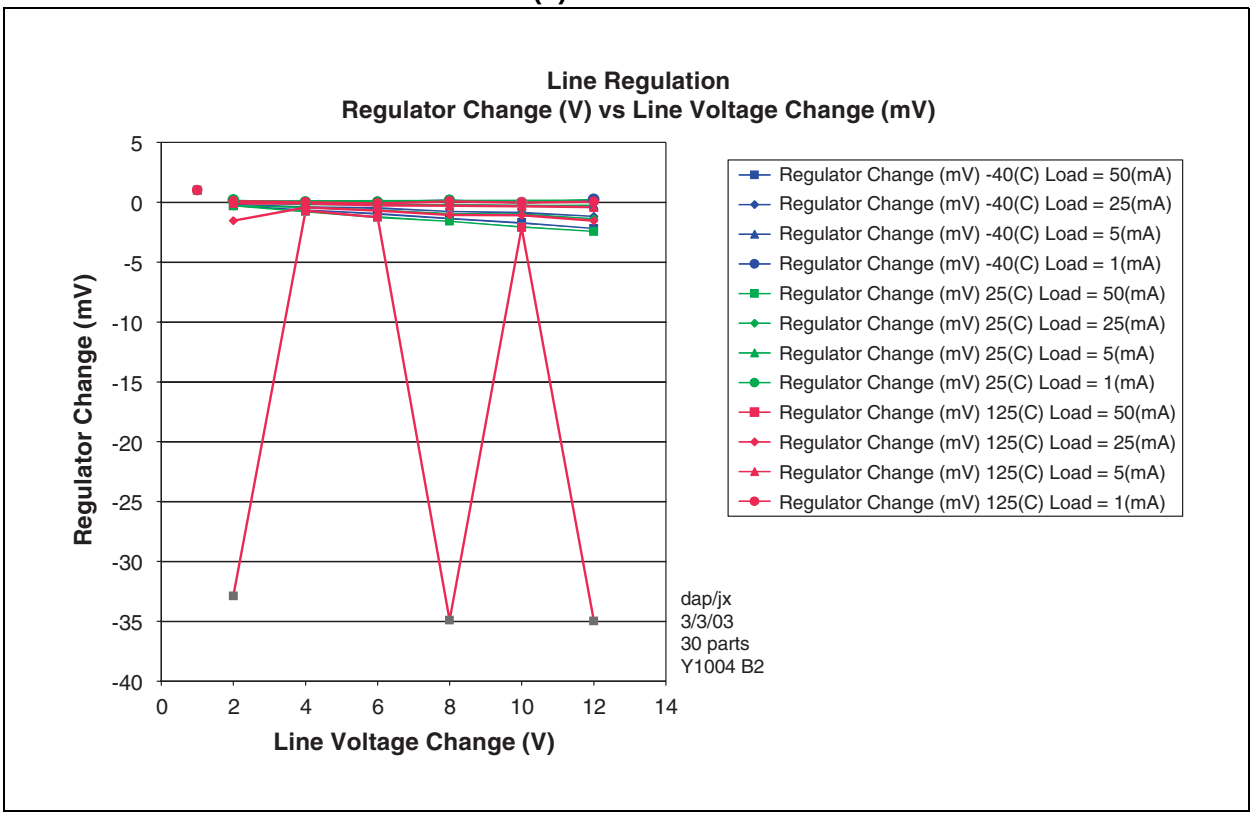


**FIGURE 3-4: LOAD REGULATION REGULATOR CHANGE VS. REGULATOR LOAD CHANGE**

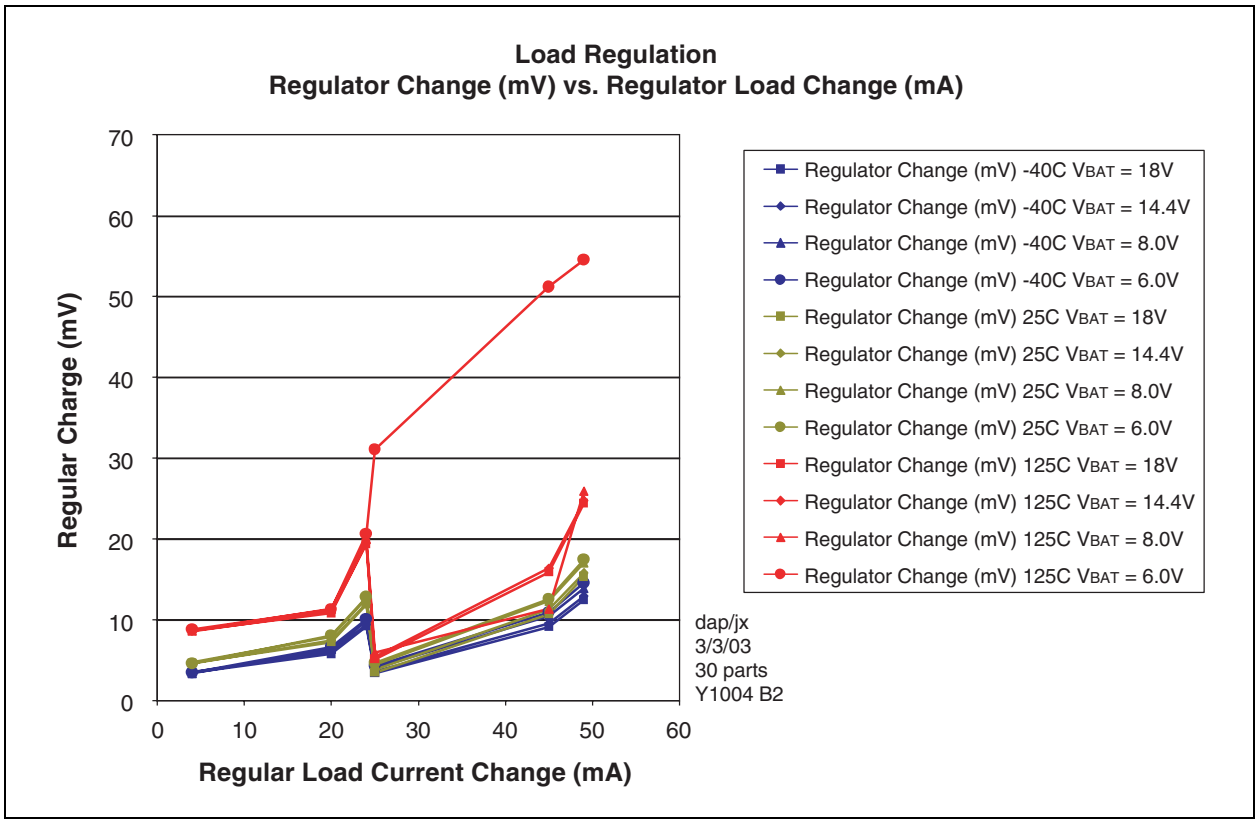


**FIGURE 3-5: FALLING EDGE NORMAL DV/DT VS. VBAT**

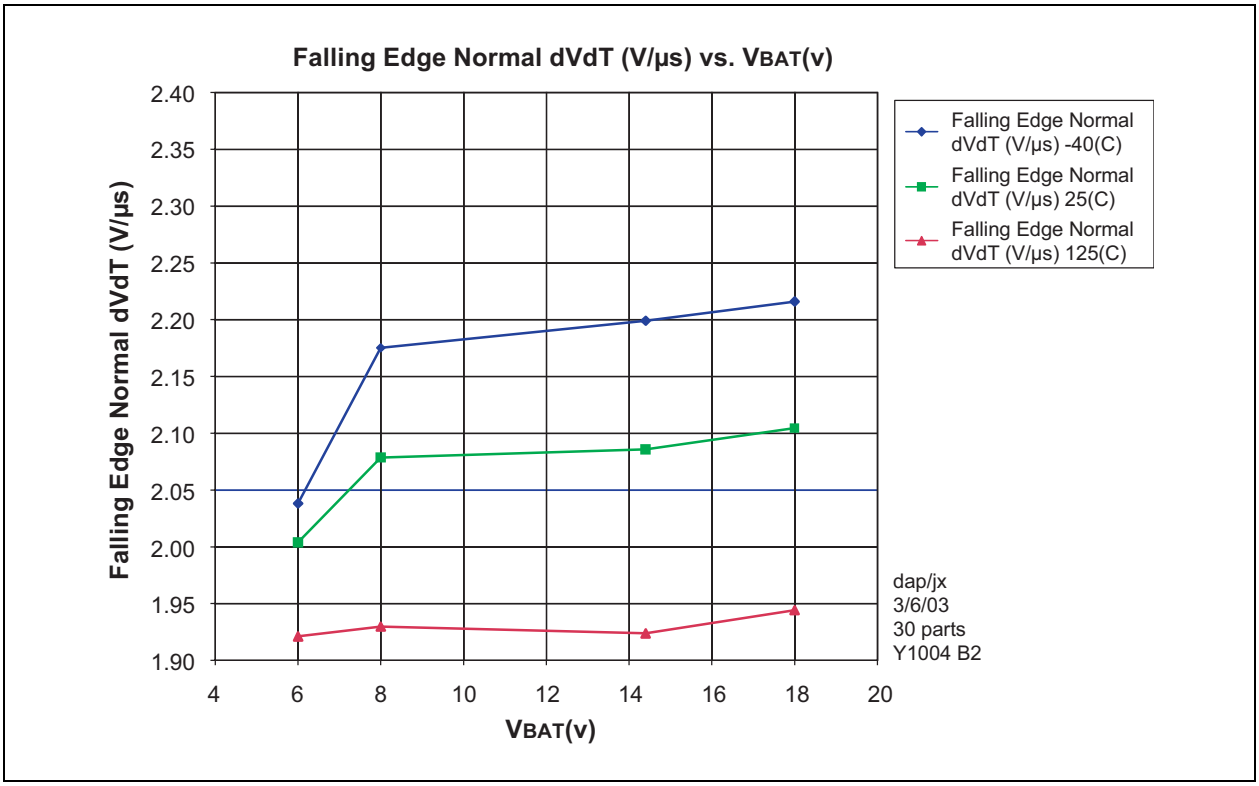


**FIGURE 3-6: RISING EDGE NORMAL DV/DT VS. VBAT**

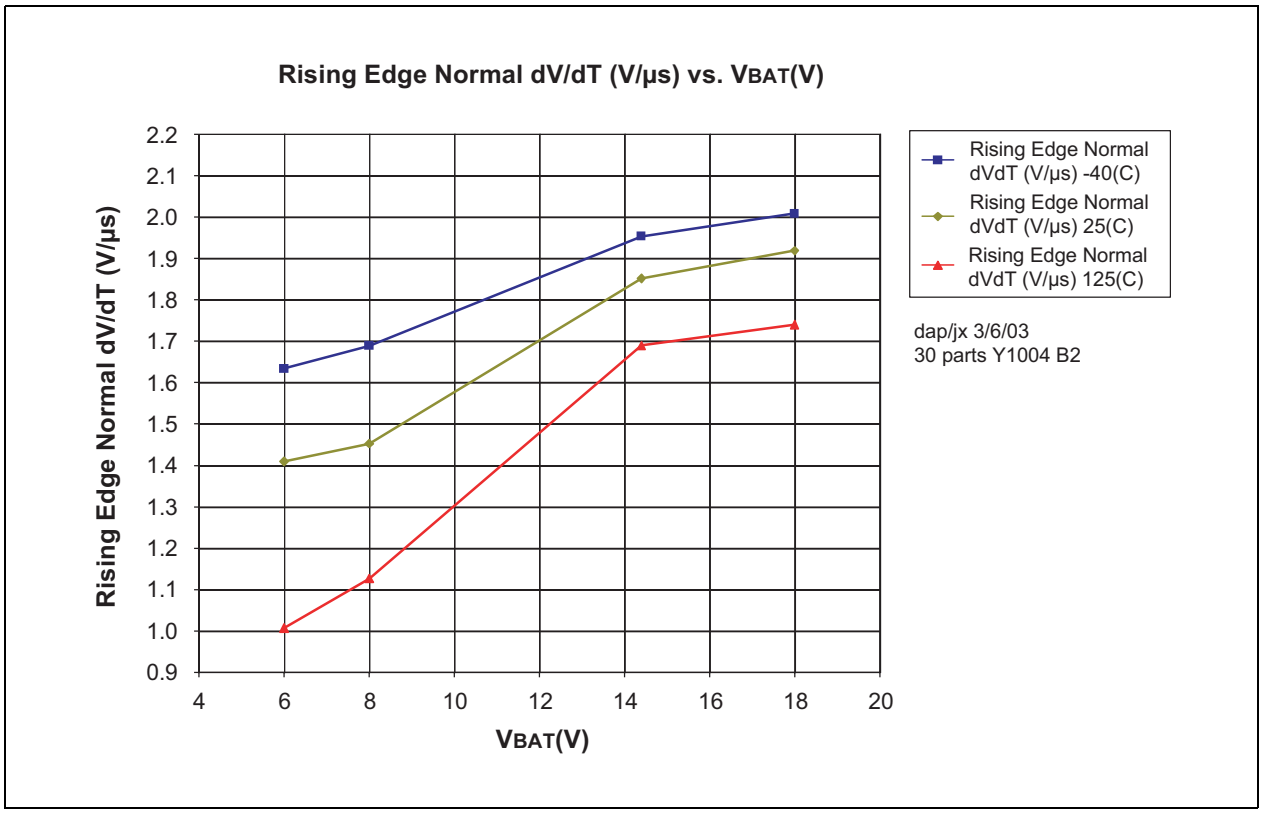


**FIGURE 3-7: BUS ACTIVE VS. VBAT**

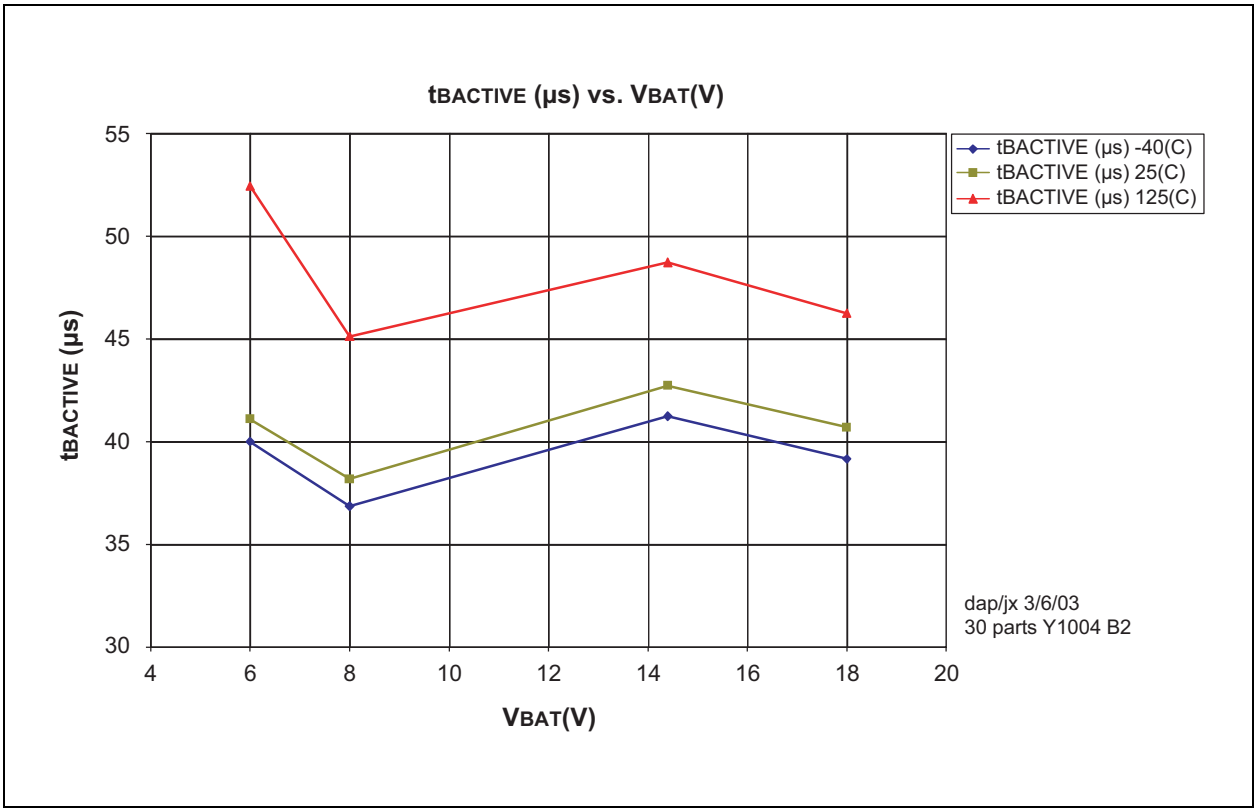


**FIGURE 3-8: VOLTAGE REGULATOR ACTIVE TIME VS. VBAT**

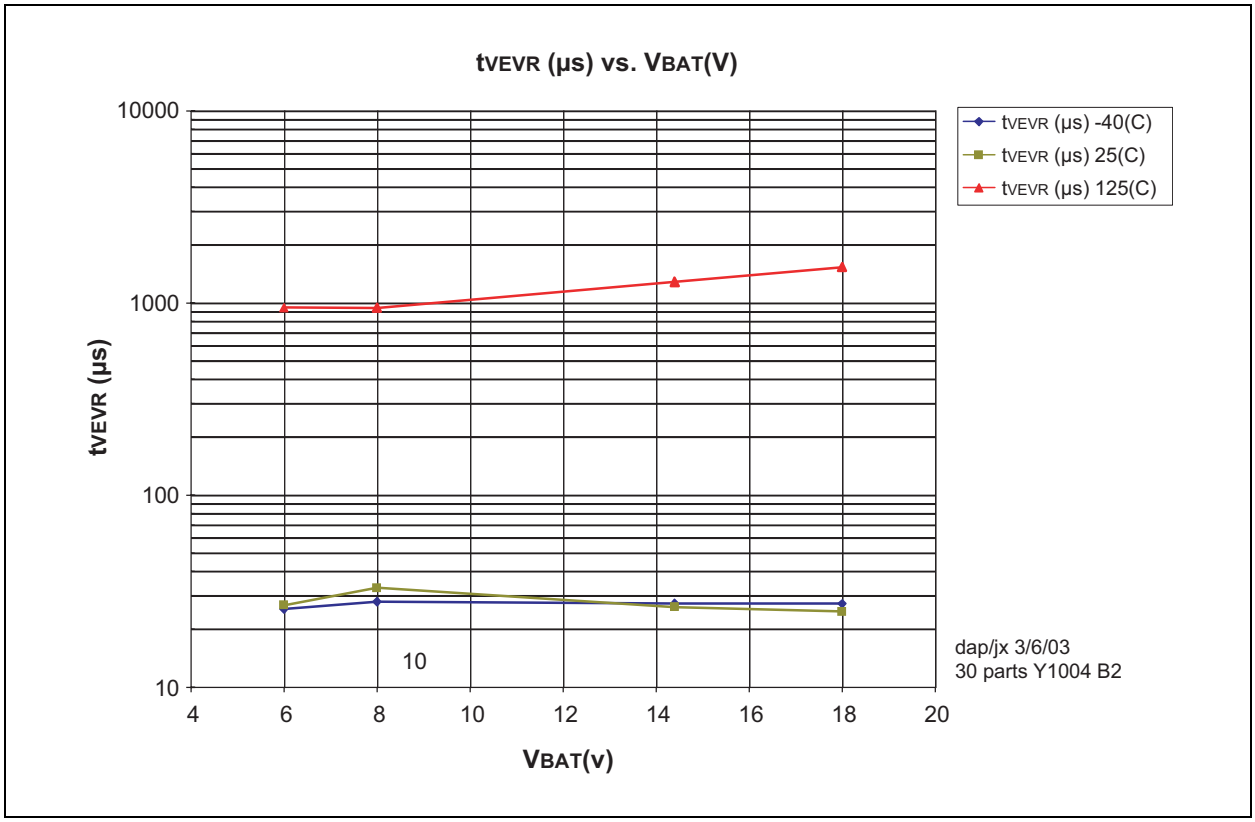


**FIGURE 3-9: CHIP SELECT TO OPERATION READY**

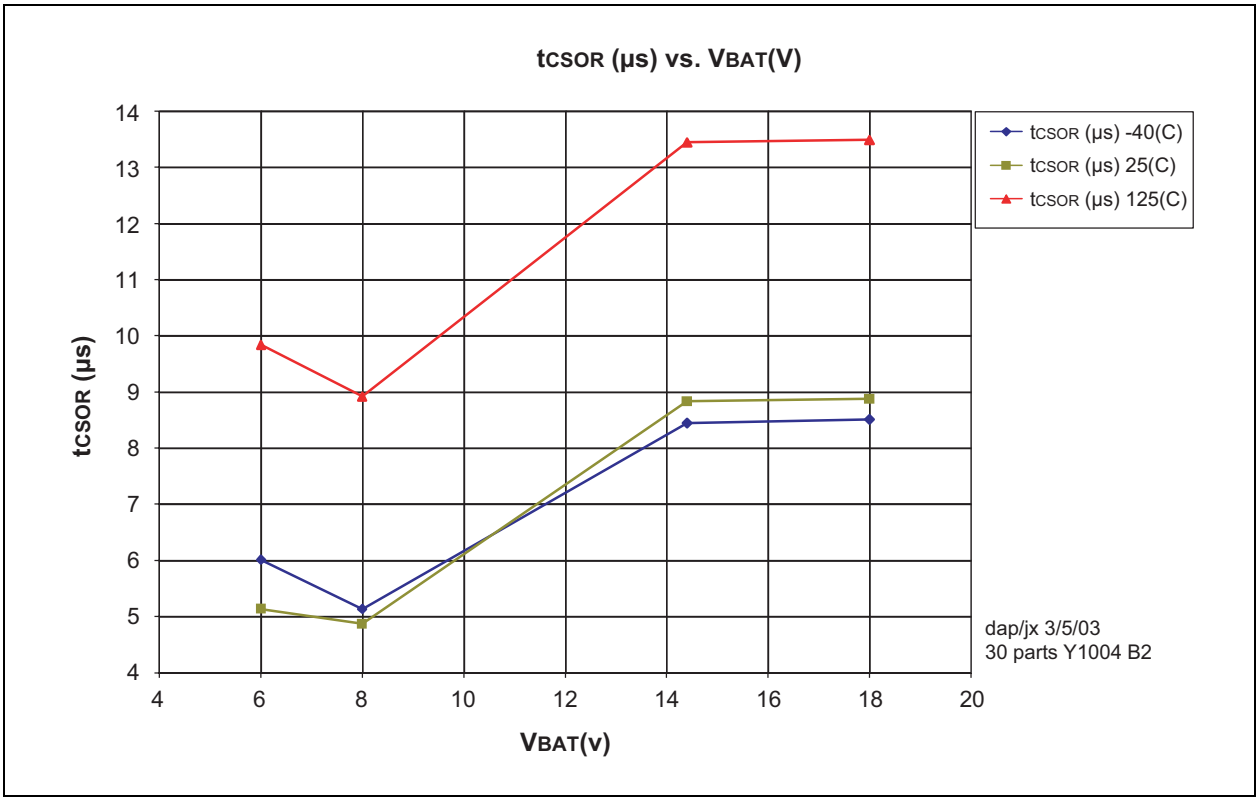


**FIGURE 3-10: CHIP SELECT TO POWER DOWN**

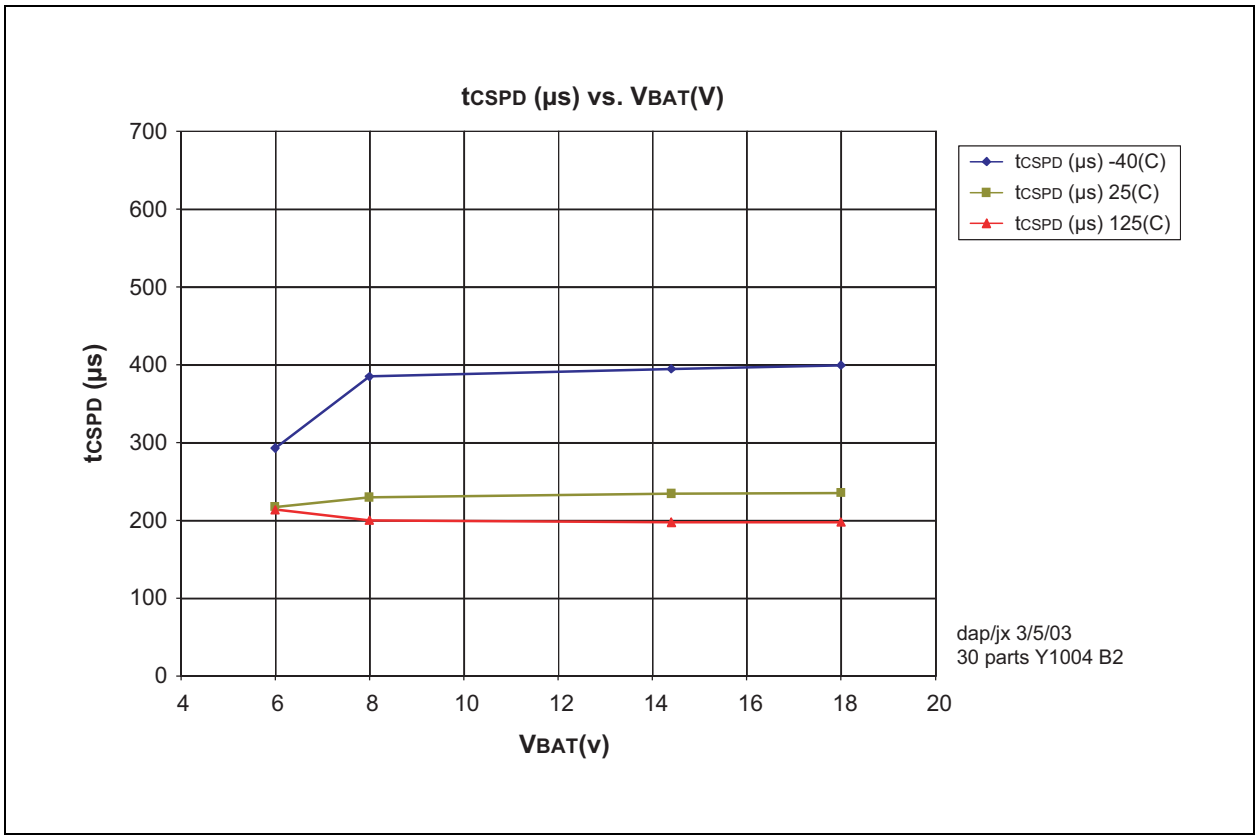


**FIGURE 3-11: PROPAGATION DELAY OF TRANSMITTER**

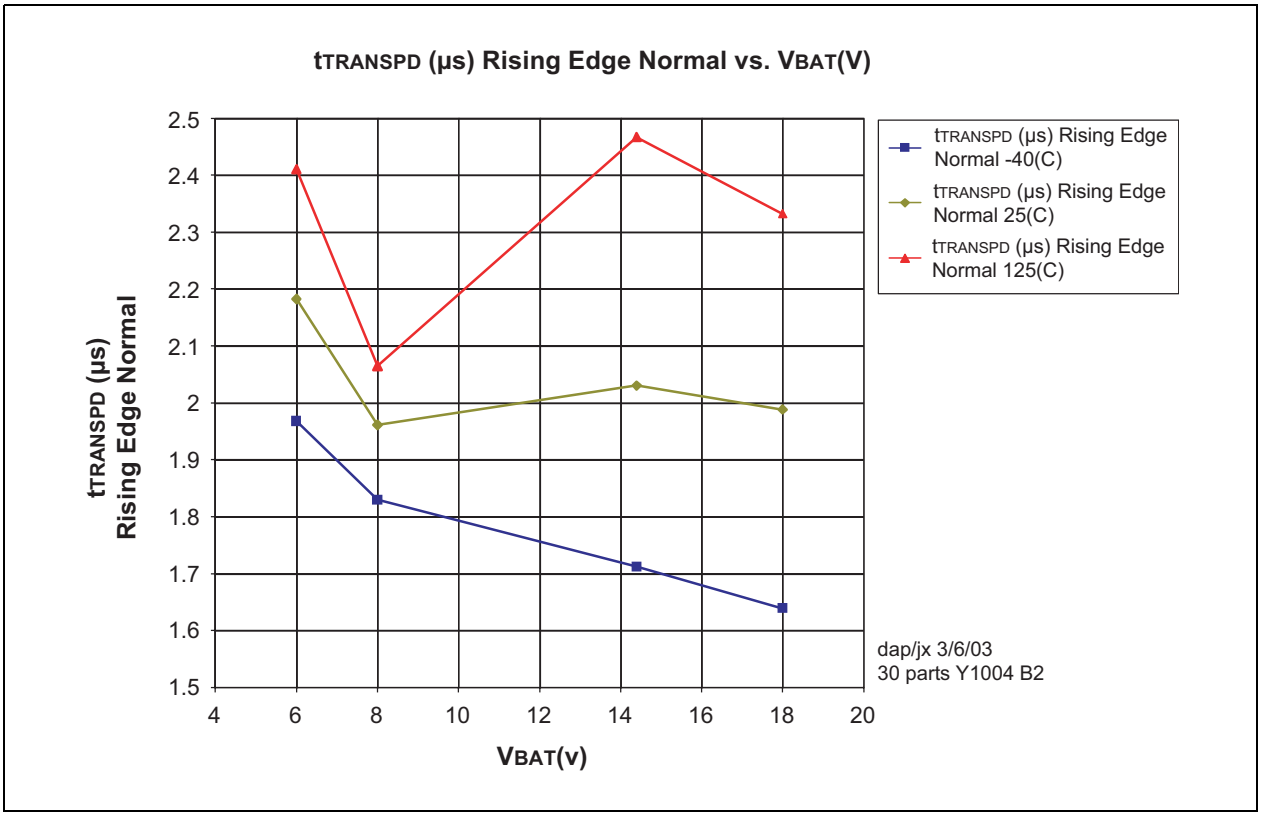
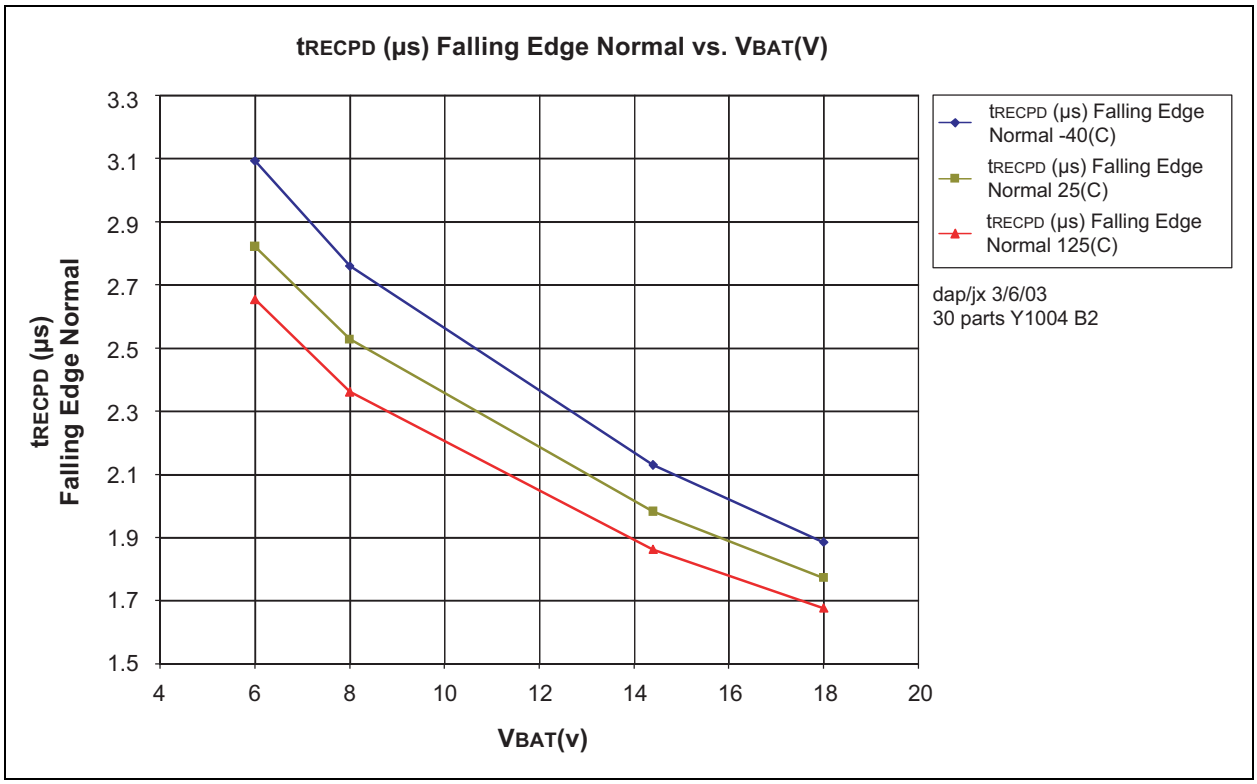


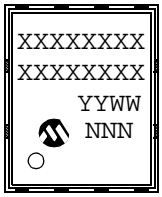
**FIGURE 3-12: PROPAGATION DELAY OF RECEIVER**



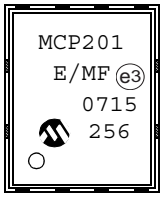
## 4.0 PACKAGING INFORMATION

### 4.1 Package Marking Information

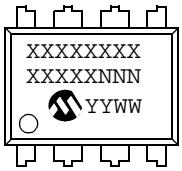
8-Lead DFN-S



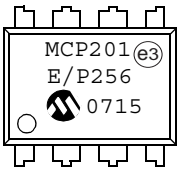

Example:



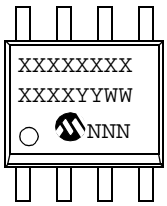

8-Lead PDIP (300 mil)



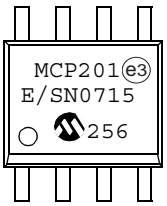

Example:




8-Lead SOIC (150 mil)




Example:

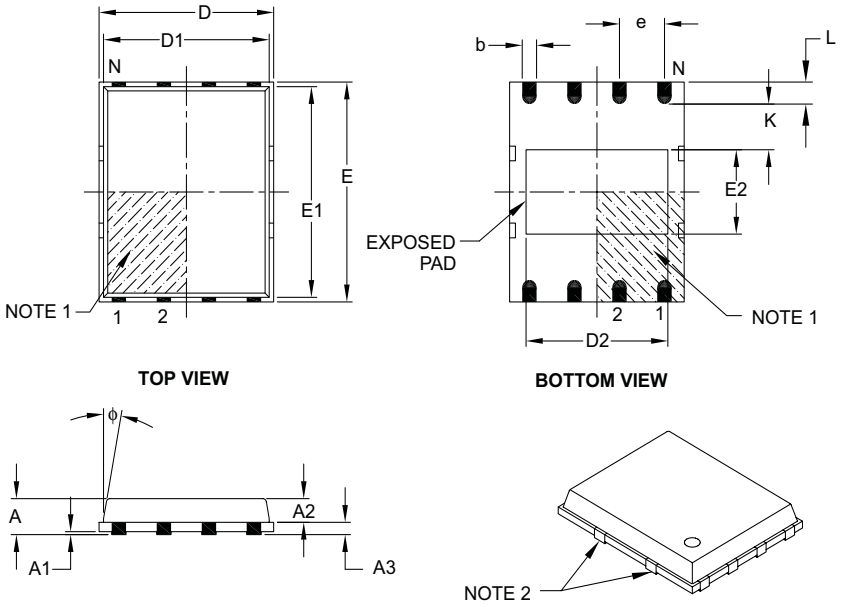



| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## 8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S] PUNCH SINGULATED

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | 0.85 | 1.00 |
| Molded Package Thickness | A2 | – | 0.65 | 0.80 |
| Standoff | A1 | 0.00 | 0.01 | 0.05 |
| Base Thickness | A3 | | 0.20 REF | |
| Overall Length | D | | 4.92 BSC | |
| Molded Package Length | D1 | | 4.67 BSC | |
| Exposed Pad Length | D2 | 3.85 | 4.00 | 4.15 |
| Overall Width | E | | 5.99 BSC | |
| Molded Package Width | E1 | | 5.74 BSC | |
| Exposed Pad Width | E2 | 2.16 | 2.31 | 2.46 |
| Contact Width | b | 0.35 | 0.40 | 0.47 |
| Contact Length | L | 0.50 | 0.60 | 0.75 |
| Contact-to-Exposed Pad | K | 0.20 | – | – |
| Model Draft Angle Top | ϕ | – | – | 12° |

**Notes:**

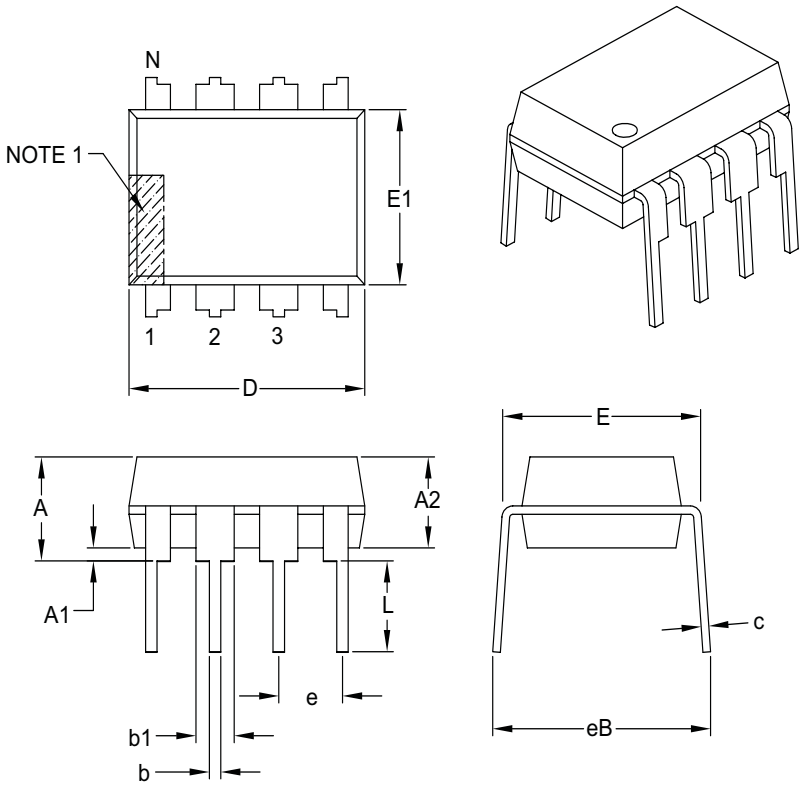
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-113B

## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

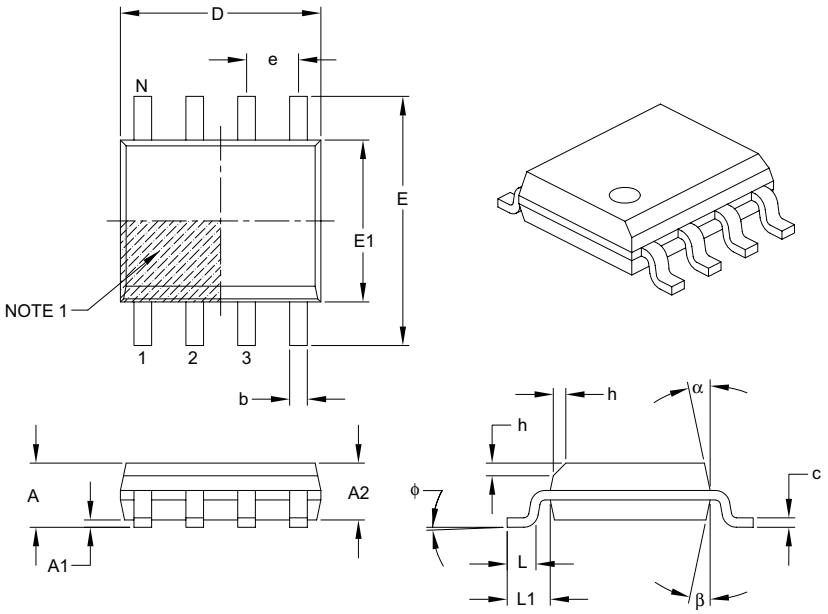
**Notes:**

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | – | – | 1.75 |
| Molded Package Thickness | A2 | 1.25 | – | – |
| Standoff § | A1 | 0.10 | – | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (optional) | h | 0.25 | – | 0.50 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | – | 8° |
| Lead Thickness | c | 0.17 | – | 0.25 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

## APPENDIX A: REVISION HISTORY

**Revision F (January 2007)**

This revision includes updates to the packaging diagrams.

**NOTES:**

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | /XX |
|---|---|---|
| Device | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP201: | LIN Transceiver with Voltage Regulator |
| | MCP201T: | LIN Transceiver with Voltage Regulator (Tape and Reel) |
| Temperature Range: | I = | -40°C to +85°C |
| | E = | -40°C to +125°C |
| Package: | MF = | Dual Flatpack, No-Lead (6x5 mm Body), 8-lead |
| | P = | Plastic DIP (300 mil Body), 8-lead |
| | SN = | Plastic SOIC (150 mil Body), 8-lead |

**Examples:**

a) MCP201-E/SN: Extended Temperature, SOIC package.

b) MCP201-E/P: Extended Temperature, PDIP package.

c) MCP201-I/SN: Industrial Temperature, SOIC package.

d) MCP201-I/P: Industrial Temperature, PDIP package.

e) MCP201T-I/SN: Tape and Reel, Industrial Temperature, SOIC package.

f) MCP201T-E/SN: Tape and Reel, Extended Temperature, SOIC package.

g) MCP201-E/MF: Extended Temperature, DFN package.

h) MCP201T-E/MF: Tape and Reel, Extended Temperature, DFN package.

**NOTES:**

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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ISO/TS 16949:2002

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