

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. LQFP-32 Pinout (Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
CLK0*, CLK0**	ECL/PECL/HSTL CLK Input
CLK1*, CLK1**	ECL/PECL/HSTL CLK Input
Q0:9, Q0:9	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
V _{BB}	Reference Voltage Output
V _{CC}	Positive Supply
V _{EE}	Negative Supply
EP	The exposed pad (EP) on the package
	bottom must be attached to a heat-sink-
	ing conduit. The exposed pad may only
	be electrically connected to $V_{\mbox{\footnotesize EE}}.$

^{*} Pins will default LOW when left open.

Table 2. FUNCTION TABLE

CLK_SEL	Active Input
I	CLK0, <u>CLK0</u> CLK1, <u>CLK1</u>

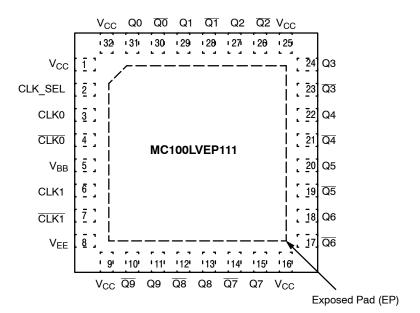


Figure 2. QFN-32 Pinout (Top View)

^{**} Pins will default to $2/3V_{CC}$ when left open.

Table 3. ATTRIBUTES

Characteris	tics	Value			
Internal Input Pulldown Resistor	75 kΩ				
Internal Input Pullup Resistor	37.5 kΩ				
ESD Protection	> 2 kV > 100 V > 2 kV				
Moisture Sensitivity (Note 1)		Pb Pkgs	Pb-Free Pkgs		
	LQFP QFN	Level 2 Level 1	Level 2 Level 1		
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in			
Transistor Count	602 Devices				
Meets or exceeds JEDEC Spec El	A/JESD78 IC Latchup Test				

^{1.} For additional information, refer to Application Note AND8003/D.

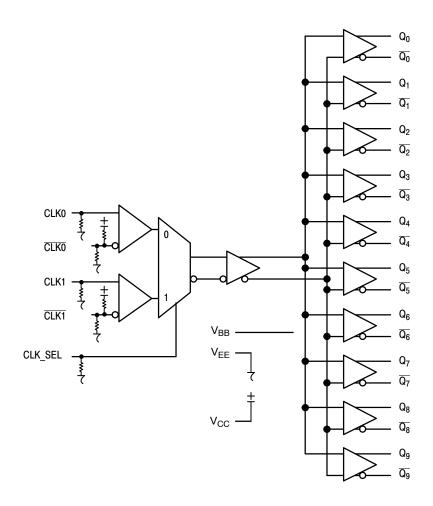


Figure 3. Logic Diagram

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		6	V
V _{EE}	NECL Mode Power Supply	V _{CC} = 0 V		-6	V
V _I	PECL Mode Input Voltage NECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	6 -6	V V
l _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θJA	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	LQFP-32 LQFP-32	80 55	°C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	LQFP-32	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	QFN-32 QFN-32	31 27	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	2S2P	QFN-32	12	°C/W
T _{sol}	Wave Solder Pb Pb-Free (QFN-32 Only)	< 3 sec @ 248°C < 3 sec @ 260°C		265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. PECL DC CHARACTERISTICS V_{CC} = 2.5 V; V_{FF} = 0 V (Note 2)

			-40°C			25°C		85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current	60	90	120	60	90	120	60	90	120	mA
V _{OH}	Output HIGH Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V _{OL}	Output LOW Voltage (Note 3)	555	730	900	555	730	900	555	730	900	mV
V _{IH}	Input HIGH Voltage (Single-Ended) (Note 4)	1335		1620	1335		1620	1275		1620	mV
V _{IL}	Input LOW Voltage (Single-Ended) (Note 4)	555		875	555		875	555		875	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 5)	1.2		2.5	1.2		2.5	1.2		2.5	V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current CLK CLK	0.5 -150			0.5 -150			0.5 -150			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 2. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary + 0.125 V to -1.3 V.
- 3. All loading with 50 Ω to V_{EE}.
- 4. Do not use V_{BB} at V_{CC} < 3.0 V.
 5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 6. PECL DC CHARACTERISTICS $V_{CC} = 3.3 \text{ V}$; $V_{EE} = 0 \text{ V}$ (Note 6)

		-40°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current	60	90	120	60	90	120	60	90	120	mA
V _{OH}	Output HIGH Voltage (Note 7)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V _{OL}	Output LOW Voltage (Note 7)	1355	1530	1700	1355	1530	1700	1355	1530	1700	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Reference Voltage (Note 8)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 9)	1.2		3.3	1.2		3.3	1.2		3.3	V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current CLK	0.5 -150			0.5 -150			0.5 -150			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 6. Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary + 0.925 V to -0.5 V.
- All loading with 50 Ω to V_{CC} 2.0 V.
 Single ended input operation is limited V_{CC} ≥ 3.0 V in PECL mode.
- 9. VIHCMR min varies 1:1 with VEE, VIHCMR max varies 1:1 with VCC. The VIHCMR range is referenced to the most positive side of the differential input signal.

Table 7. NECL DC CHARACTERISTICS V_{CC} = 0 V, V_{EE} = -2.375 V to -3.8 V (Note 10)

		-40°C				25°C		85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
I _{EE}	Power Supply Current	60	90	120	60	90	120	60	90	120	mA
V _{OH}	Output HIGH Voltage (Note 11)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V _{OL}	Output LOW Voltage (Note 11)	-1945	-1770	-1600	-1945	-1770	-1600	-1945	-1770	-1600	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
V _{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V _{BB}	Output Reference Voltage (Note 12)	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V _{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	V _{EE}	+ 1.2	0.0	V _{EE}	+ 1.2	0.0	V _{EE}	+ 1.2	0.0	V
I _{IH}	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current CLK	0.5 -150			0.5 -150			0.5 -150			μΑ

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 10. Input and output parameters vary 1:1 with V_{CC} .
- 11. All loading with 50 Ω to V_{CC} 2.0 V. 12. Single ended input operation is limited V_{EE} \leq –3.0V in NECL mode.

Table 8. HSTL DC CHARACTERISTICS V_{CC} = 2.375 to 3.8 V, V_{EE} = 0 V

		-40°C		25°C			85°C				
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
V _{IH}	Input HIGH Voltage	1200			1200			1200			mV
V _{IL}	Input LOW Voltage			400			400			400	mV
Vx	Input Crossover Voltage	680		900	680		900	680		900	mV
I _{CC}	Power Supply Current	70	100	120	70	100	120	70	100	120	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

^{13.} V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential

Table 9. AC CHARACTERISTICS $V_{CC} = 0 \text{ V}$; $V_{EE} = -2.375 \text{ to } -3.8 \text{ V}$ or $V_{CC} = 2.375 \text{ to } 3.8 \text{ V}$; $V_{EE} = 0 \text{ V}$ (Note 14)

			-40°C			25°C		85°C			
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{maxPECL/HSTL}	Maximum Frequency (Figure 4)		3			3			3		GHz
t _{PLH} t _{PHL}	Propagation Delay (Differential Configuration)	325	400	475	350	430	500	375	510	590	ps
t _{skew}	Within-Device Skew (Note 15) Within-Device Skew @ 2.5 V (Note 15) Device-to-Device Skew (Note 16)		20 20 85	25 25 150		20 20 85	25 25 150		25 20 85	35 25 150	ps
t JITTER	CLOCK Random Jitter (RMS) @ ≤ 0.5 GHz @ ≤ 1.0 GHz @ ≤ 1.5 GHz @ ≤ 2.0 GHz @ ≤ 2.5 GHz @ ≤ 3.0 GHz		0.209 0.200 0.197 0.220 0.232 0.348	0.5 0.5 0.4 0.5 0.4 0.6		0.204 0.214 0.213 0.224 0.290 0.545	0.5 0.6 0.5 0.5 0.5 0.8		0.221 0.229 0.243 0.292 0.522 0.911	0.5 0.5 0.4 0.6 0.8 1.3	ps
t _{jit(φ)}	Additive RMS Integrated Phase Jitter (fc = 156.25 MHz, 12 kHz – 20 MHz)					149					fs
V _{PP}	Input Swing (Differential Interconnect Configuration) Measured Single-Ended	150	800	1200	150	800	1200	150	800	1200	mV
t _r /t _f	Output Rise/Fall Time (20%-80%)	105	200	255	125	200	275	150	230	320	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 14. Measured with 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} 2.0 V.
- 15. Skew is measured between outputs under identical transitions and conditions on any one device.
- 16. Device–to–Device skew for identical transitions at identical V_{CC} levels.

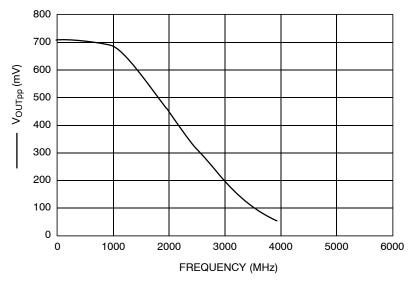


Figure 4. F_{max} Typical

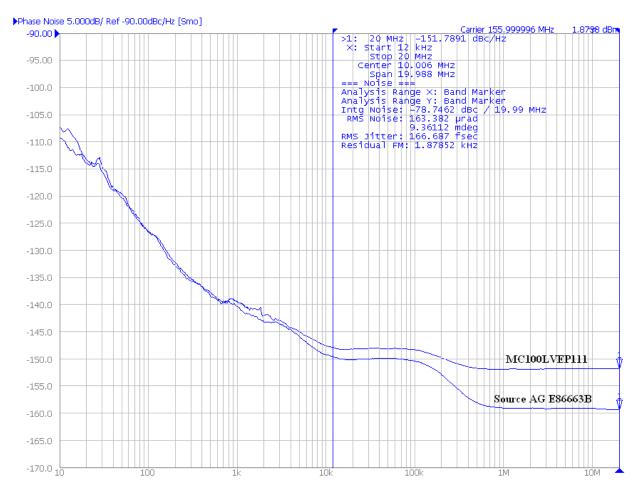


Figure 5. For a 155.52 MHz Carrier, the MC100LVEP111 Phase Noise (dBc/Hz) verses SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Upper Heavy Line) is 399.1 fs RMS. The VECTRON VCC Oscillator Source Generator Phase Noise (Lower Light Line) Phase Noise is 361.2 fs RMS. The Additive Phase Jitter is ((399.1^2)-(361.2^2))^0.5, or 169 fs

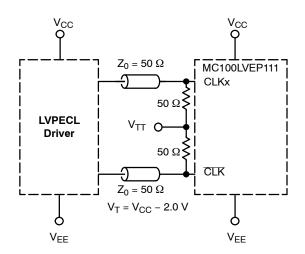


Figure 6. LVPECL in Interface

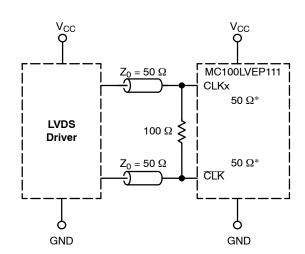
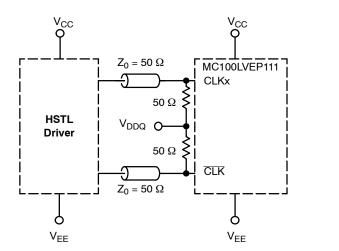


Figure 7. LVDS in Interface



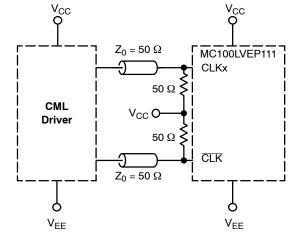


Figure 8. HSTL in Interface

Figure 9. Standard 50 Ω Load CML in Interface

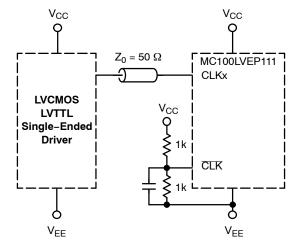


Figure 10. Single-Ended Interface LVCMOS/LVTTL in Interface Using an External Voltage Reference

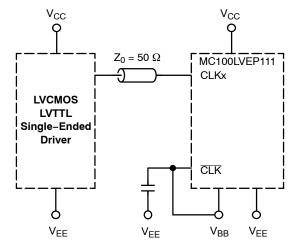


Figure 11. Single-Ended Interface LVCMOS/LVTTL in Interface Using V_{BB}

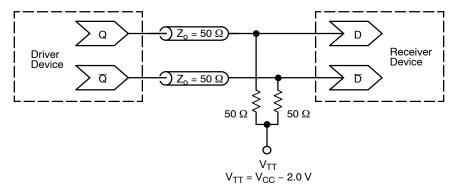
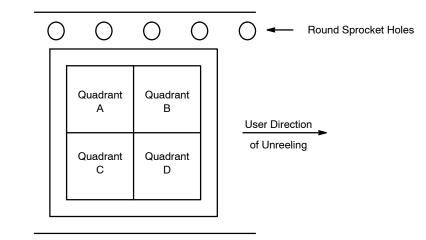


Figure 12. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices.)



Designations
Quadrant A = Upper Left
Quadrant B = Upper Right
Quadrant C = Lower Left
Quadrant D = Lower Right

Figure 13. Tape and Reel Pin 1 Quadrant Orientation

ORDERING INFORMATION

Device	Package	Shipping [†]
MC100LVEP111FA	LQFP-32	250 Units / Tray
MC100LVEP111FAG	LQFP-32 (Pb-Free)	250 Units / Tray
MC100LVEP111FAR2	LQFP-32	2000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 13)
MC100LVEP111FARG	LQFP-32 (Pb-Free)	2000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 13)
M100LVEP111FATWG	LQFP-32 (Pb-Free)	2000 / Tape & Reel (Pin 1 Orientation in Quadrant A, Figure 13)
MC100LVEP111MNG	QFN-32 (Pb-Free)	74 Units / Rail
MC100LVEP111MNRG	QFN-32 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AN1672/D - The ECL Translator Guide
AND8001/D - Odd Number Counters Design

AND8002/D - Marking and Date Codes

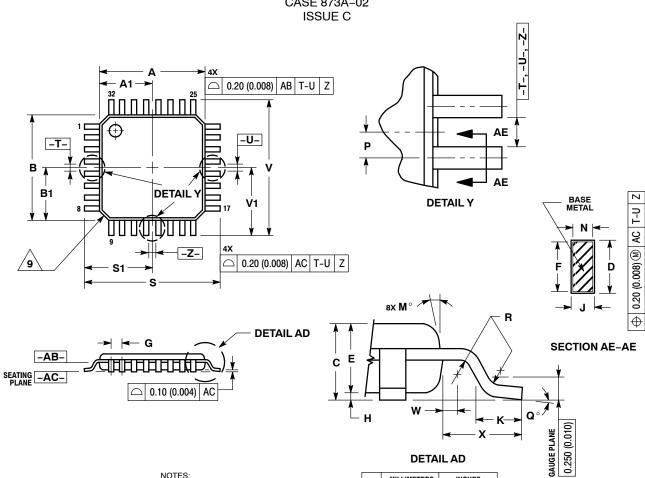
AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

32 LEAD LQFP CASE 873A-02



- NOTES:
 1. DIMENSIONING AND TOLERANCING
- PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION:
- MILLIMETER.

 3. DATUM PLANE -AB- IS LOCATED AT

- 3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.

 4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.

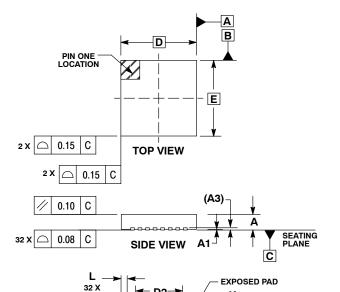
 5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.

 6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
- DETERMINED AT DATUM PLANE -AB-.
 7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR
 PROTRUSION SHALL NOT CAUSE THE
 D DIMENSION TO EXCEED 0.520 (0.020).
- MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
 EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIN	IETERS	INC	HES			
DIM	MIN	MAX	MIN	MAX			
Α	7.000	BSC	0.276	BSC			
A1	3.500	BSC	0.138 BSC				
В	7.000	BSC	0.276	BSC			
B1	3.500	BSC	0.138	BSC			
С	1.400	1.600	0.055	0.063			
D	0.300	0.450	0.012	0.018			
E	1.350	1.450	0.053	0.057			
F	0.300	0.400	0.012	0.016			
G	0.800	BSC	0.031	BSC			
Н	0.050	0.150	0.002	0.006			
J	0.090	0.200	0.004	0.008			
K	0.450	0.750	0.018	0.030			
M	12°	REF	12° REF				
N	0.090	0.160	0.004	0.006			
P	0.400	BSC	0.016	BSC			
Q	1°	5°	1°	5°			
R	0.150	0.250	0.006	0.010			
S	9.000	BSC	0.354	BSC			
S1	4.500	BSC	0.177	BSC			
٧	9.000	BSC	0.354	BSC			
V1	4.500	BSC	0.177 BSC				
W	0.200	REF	0.008	REF			
X	1.000	REF	0.039	REF			

PACKAGE DIMENSIONS

QFN32 5*5*1 0.5 P CASE 488AM-01 **ISSUE O**



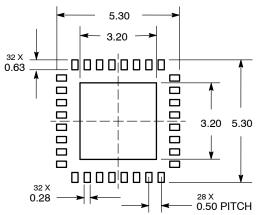
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NOTES:

- DIMENSIONS AND TOLERANCING PER
- ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
 DIMENSION 6 APPLIES TO PLATED
 TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL COPLANARITY APPLIES TO THE EXPOSED
- PAD AS WELL AS THE TERMINALS

	MILLIMETERS								
DIM	MIN	NOM	MAX						
Α	0.800	0.900	1.000						
A1	0.000	0.025	0.050						
A3	0.	0.200 REF							
b	0.180	0.250	0.300						
D		.00 BSC							
D2	2.950	3.100	3.250						
E	5	.00 BSC							
E2	2.950	3.100	3.250						
е	0.	500 BSC							
K	0.200	-							
L	0.300	0.400	0.500						

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ECLinPS is a trademark of Semiconductor Components Industries, LLC (SCILLC).

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BOTTOM VIEW

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0.05 С

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