ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to PGND.)

SVDD, SVDD2, and PVDD	-0.3V to +6V
PVSS and BIAS	-6V to +0.3V
SGND	-0.3V to +0.3V
INL-, INL+, INR-, and INR+ (A, B, and E)	$-V_{SVDD}/2$ to $+V_{SVDD}/2$
INL-, INL+, INR-, and INR+ (C and D)	$(-0.75 \times V_{SVDD})$ to $(+0.75 \times V_{SVDD})$
OUTL and OUTR	-4.5V to +4.5V
$\overline{SHDN}$	-0.3V to +6V
C1P	-0.3V to $(V_{PVDD} + 0.3V)$
C1N	$(V_{PVSS} - 0.3V)$ to +0.3V
OUT_ Short Circuit to PGND	Continuous
OUT_ Short Circuit to PVDD	Continuous
Short Circuit Between OUTL and OUTR	Continuous
Continuous Current Into/Out of All Pins	20mA
Continuous Power Dissipation (T_A = +70°C) (Multilayer Board) TQFN (derate 20.8mW/°C above +70°C)	1666.7mW
Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V$, $V_{PGND} = V_{SGND} = 0V$, $C_{BIAS} = 0.1µF$, C1 = C2 = 1µF, $R_{IN} = 20kΩ$, $R_F = 20kΩ$ (MAX97220A/MAX97220B/MAX97220E), typical values tested at T_A = +25°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Supply Voltage Range	PVDD, SVDD_	Guaranteed by PSRR test		2.5		5.5	V
Quiescent Supply Current	I_{PVDD}	No load, T_A = +25°C	A version		5.5	7	mA
		No load, T_A = +25°C	B/C/D/E versions		5	9	
		No load, $V_{PVDD} = V_{SVDD\_} = 3.3V$			5		
Undervoltage Lockout	UVLO	PVDD falling				2.35	V
Shutdown Supply Current	I_{PVDD_SD}	$\overline{SHDN}$ = 0, T_A = +25°C			1	10	µA
Turn-On Time	t_{ON}	Shutdown to full operation time	A/C/E versions	4.8	5.5	6.3	ms
			B/D versions	117	130	143	
AMPLIFIERS							
Input Resistance	R_{IN}	C/D versions only		7.4	10	12.7	kΩ
Output Signal Attenuation in Shutdown		$V_{\overline{SHDN}}$ = 0V, R_L = 10kΩ	A/B/E versions		76		dB
			C/D versions		71		
Gain	A_V	C/D versions only		5.5	6	6.5	dB
Output Offset Voltage	V_{OS}	Unity gain, T_A = +25°C				350	µV
Input Common-Mode Voltage Range	V_{CM}	Voltage at IN+ and IN-	A/B/E versions	$-0.5 \times V_{PVDD}$		$+0.5 \times V_{PVDD}$	V
			C/D versions	$-0.75 \times V_{PVDD}$		$+0.75 \times V_{PVDD}$	
Maximum Differential Input Signal	V_{DIFF}	(Note 4)				PVDD	V_P

ELECTRICAL CHARACTERISTICS (continued)

(V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V, V_{PGND} = V_{SGND} = 0V, C_{BIAS} = 0.1µF, C1 = C2 = 1µF, R_{IN} = 20kΩ, R_F = 20kΩ (MAX97220A/MAX97220B/MAX97220E), typical values tested at T_A = +25°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	V_{PVDD} = $V_{SVDD\_}$ = 2.5V to 5.5V	A/B/E versions	74	90		dB
		V_{PVDD} = $V_{SVDD\_}$ = 2.5V to 5.5V	C/D versions	73	90		
		f_{IN} = 217Hz, 200mV$_{P-P}$ ripple			78		
		f_{IN} = 10kHz, 200mV$_{P-P}$ ripple			63		
Common-Mode Rejection Ratio	CMRR	$-V_{PVDD}/2 \le V_{CM} \le +V_{PVDD}/2$	A/B/E versions	70	86		dB
		$-0.75 \times V_{PVDD} \le V_{CM} \le +0.75 \times V_{PVDD}$	C/D versions	45	60		
Output Voltage Swing	V_{OUT}	1kHz, 600Ω load, THD+N < 0.1%		3			V_{RMS}
		1kHz, R_L = 600Ω load, V_{PVDD} = $V_{SVDD\_}$ = 3.3V, THD+N < 0.1%			2.15		
		1kHz, R_L = 10kΩ load, THD+N < 0.1%			3.5		
Output Power	P_{OUT}	R_L = 16Ω, THD+N = 1%		40	110		mW
		R_L = 32Ω, THD+N = 1%			125		
Total Harmonic Distortion Plus Noise	THD+N	1kHz, 22Hz to 22kHz BW, V_{OUT} = 3V_{RMS}, R_L = 10kΩ			103		dB
		10kHz, 22Hz to 22kHz BW, V_{OUT} = 3V_{RMS}, R_L = 10kΩ			90		
		1kHz, 22Hz to 22kHz BW, V_{OUT} = 2V_{RMS}, R_L = 600Ω		80	105		
		10kHz, 22Hz to 30kHz BW, V_{OUT} = 2V_{RMS}, R_L = 600Ω			94		
		1kHz, 22Hz to 22kHz BW, P_{OUT} = 20mW, R_L = 32Ω			0.0035		%
Signal-to-Noise Ratio	SNR	A/B/E versions	V_{OUT} = 3V_{RMS}, THD+N = 0.1%, A-weighted, R_{IN} = R_F = 10kΩ, R_L = 1kΩ		112.5		dB
			V_{OUT} = 2V_{RMS}, V_{PVDD} = 3.3V, THD+N = 0.1%, A-weighted, R_{IN} = R_F = 10kΩ, R_L = 600Ω		109		
		C/D versions	V_{OUT} = 3V_{RMS}, THD+N = 0.1%, A-weighted, R_L = 1kΩ		106		
			V_{OUT} = 2V_{RMS}, V_{PVDD} = 3.3V, THD+N = 0.1%, A-weighted, R_L = 600Ω		103		

ELECTRICAL CHARACTERISTICS (continued)

($V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V$, $V_{PGND} = V_{SGND} = 0V$, $C_{BIAS} = 0.1\mu F$, $C1 = C2 = 1\mu F$, $R_{IN} = 20k\Omega$, $R_F = 20k\Omega$ (MAX97220A/MAX97220B/MAX97220E), typical values tested at $T_A = +25°C$, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise Voltage	V_N	A/B/E versions	A-weighted, $R_{IN} = R_F = 10k\Omega$		7		µV
		C/D versions	A-weighted		14		
Crosstalk	X_{TALK}	A/B/E versions	1kHz, $V_{OUT} = 3V_{RMS}$, $R_L = 10k\Omega$		-125		dB
			10kHz, $V_{OUT} = 3V_{RMS}$, $R_L = 10k\Omega$		-108		
			1kHz, $V_{OUT} = 2V_{RMS}$, $R_L = 600\Omega$, $V_{PVDD} = V_{SVDD\_} = 3.3V$		-123		
			10kHz, $V_{OUT} = 2V_{RMS}$, $R_L = 600\Omega$, $V_{PVDD} = V_{SVDD\_} = 3.3V$		-104		
			1kHz, $P_{OUT} = 20mW$, $R_L = 32\Omega$		-102		
			10kHz, $P_{OUT} = 20mW$, $R_L = 32\Omega$		-82		
		C/D versions	1kHz, $V_{OUT} = 2V_{RMS}$, $R_L = 10k\Omega$		100		
			10kHz, $V_{OUT} = 2V_{RMS}$, $R_L = 10k\Omega$		98		
			1kHz, $V_{OUT} = 2V_{RMS}$, $R_L = 600\Omega$		100		
			10kHz, $V_{OUT} = 2V_{RMS}$, $R_L = 600\Omega$		96		
			1kHz, $P_{OUT} = 20mW$, $R_L = 32\Omega$		95		
			1kHz, $P_{OUT} = 20mW$, $R_L = 16\Omega$		92		
Maximum Capacitive Load Drive	C_L				470		pF
External Feedback Resistor Range	R_F	A/B/E versions		4.7	20	100	kΩ
Oscillator Frequency	f_{OSC}			450	500	550	kHz

ELECTRICAL CHARACTERISTICS (continued)

($V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V$, $V_{PGND} = V_{SGND} = 0V$, $C_{BIAS} = 0.1\mu F$, $C1 = C2 = 1\mu F$, $R_{IN} = 20k\Omega$, $R_F = 20k\Omega$ (MAX97220A/ MAX97220B/MAX97220E), typical values tested at $T_A = +25°C$, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Click-and-Pop Level (Note 5)	KCP	32 samples per second, A-weighted, $R_L = 10k\Omega$, unity gain	Into shutdown		-70		dBV
			Out of shutdown		-70		
		32 samples per second, A-weighted, $R_L = 32\Omega$, unity gain	Into shutdown		-76		
			Out of shutdown		-76		
LOGIC INPUT ($\overline{\text{SHDN}}$)							
$\overline{\text{SHDN}}$ Input Logic-High	V_{IH}			1.4			V
$\overline{\text{SHDN}}$ Input Logic-Low	V_{IL}					0.4	V
$\overline{\text{SHDN}}$ Input Leakage Current High	I_{IH}	$T_A = +25°C$				1	µA
$\overline{\text{SHDN}}$ Input Leakage Current Low	I_{IL}	$T_A = +25°C$				1	µA

Note 2: 100% production tested at $T_A = +25°C$. Specifications over temperature limits are guaranteed by design.

Note 3: Dynamic specifications are taken over 2.5V to 5.5V supply range. Inputs AC-coupled to PGND.

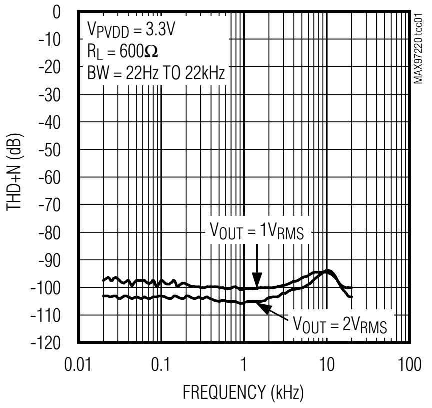
Note 4: The maximum differential input signal does not cause any excess distortion due to violation of the common-mode input range.

Note 5: Test performed with a resistive load connected to PGND. Mode transitions are controlled by $\overline{\text{SHDN}}$. KCP level is calculated as 20 x log (peak voltage during mode transition, no input signal).

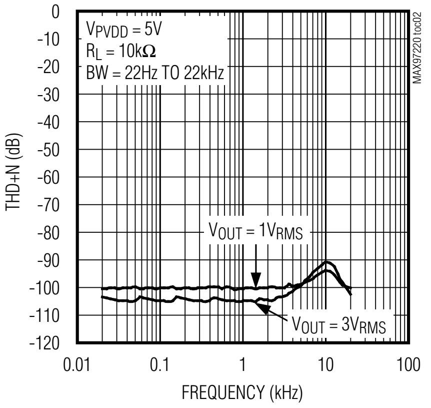
Typical Operating Characteristics

($V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V$, $V_{PGND} = V_{SGND} = 0V$, $C_{BIAS} = 0.1\mu F$, $C1 = C2 = 1\mu F$, $R_{IN} = 10k\Omega$, $R_F = 10k\Omega$, unless otherwise noted.)

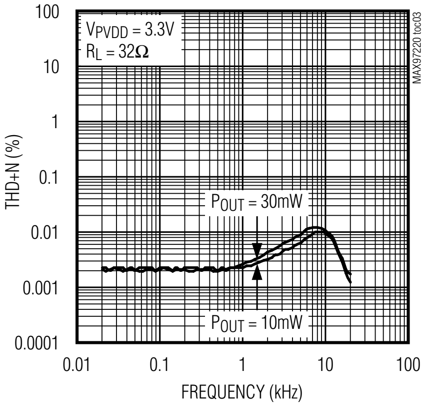
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



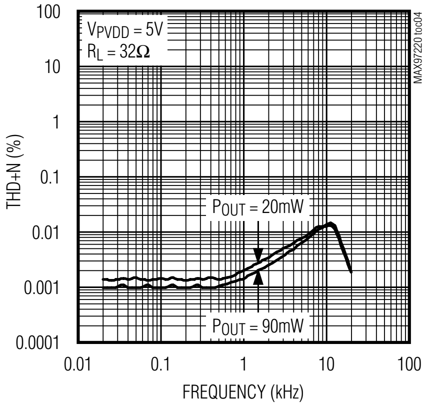
MAX97220A–MAX97220E

Differential Input DirectDrive Line Drivers/Headphone Amplifiers

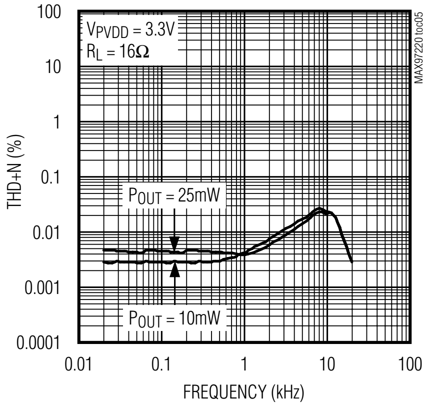
Typical Operating Characteristics (continued)

($V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V$, $V_{PGND} = V_{SGND} = 0V$, $C_{BIAS} = 0.1\mu F$, C1 = C2 = 1µF, $R_{IN} = 10k\Omega$, $R_F = 10k\Omega$, unless otherwise noted.)

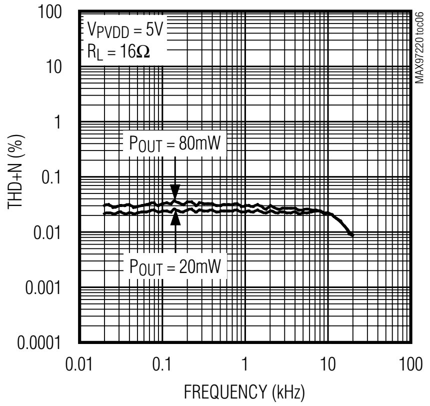
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



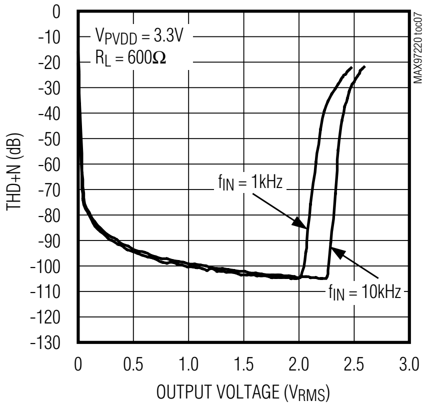
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



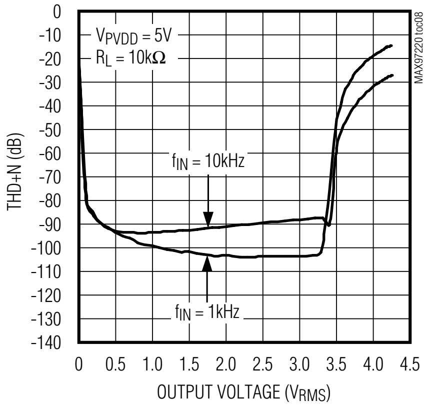
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



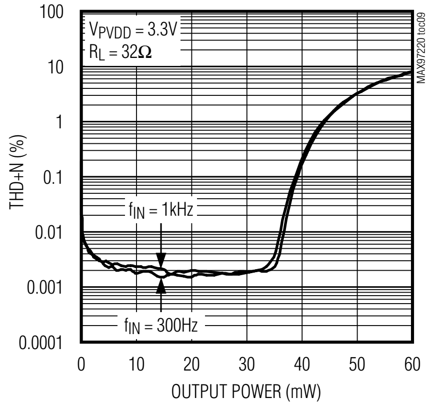
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE



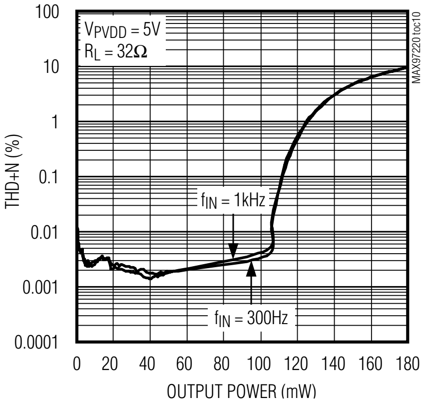
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE



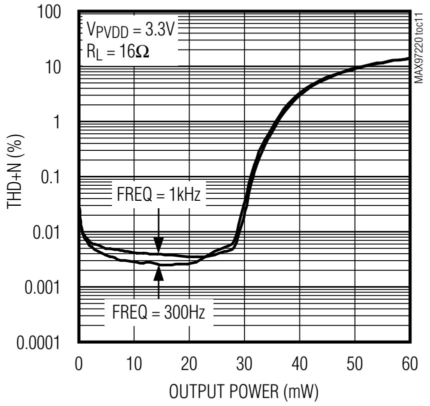
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



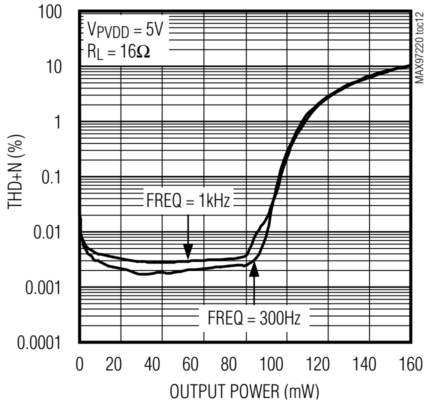
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER

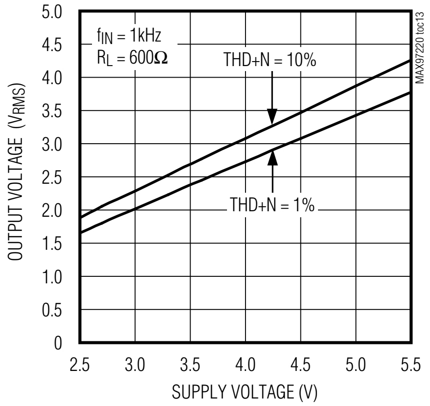


TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER

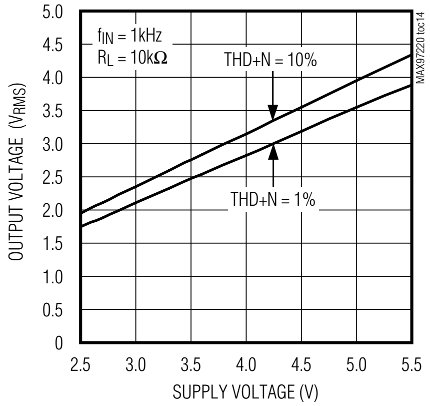


Typical Operating Characteristics (continued)

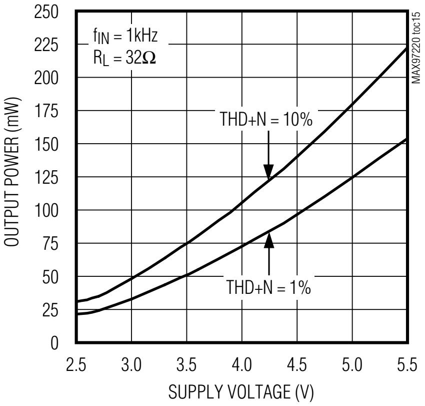
(V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V, V_{PGND} = V_{SGND} = 0V, C_{BIAS} = 0.1μF, C1 = C2 = 1μF, R_{IN} = 10kΩ, R_F = 10kΩ, unless otherwise noted.)



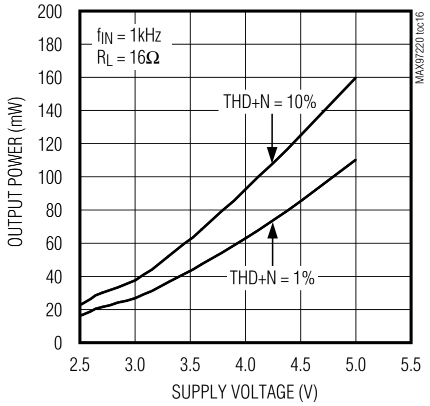
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



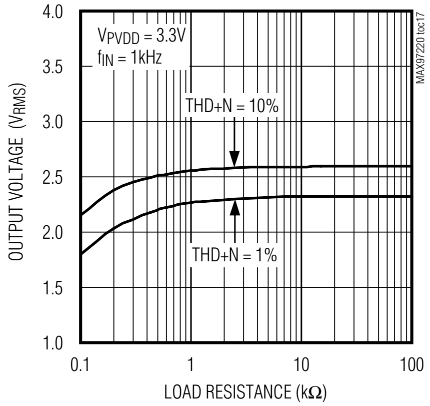
OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



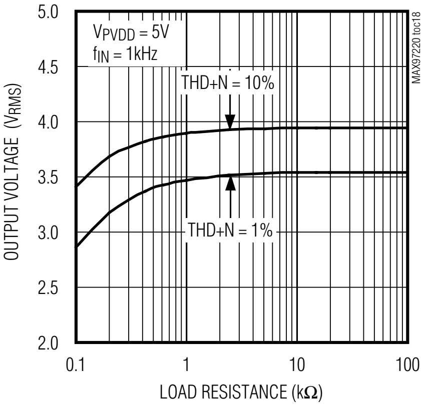
OUTPUT POWER vs. SUPPLY VOLTAGE



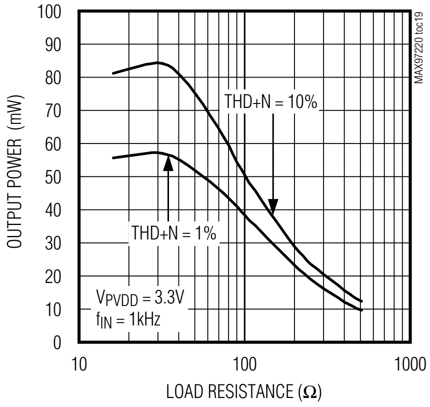
OUTPUT POWER vs. SUPPLY VOLTAGE



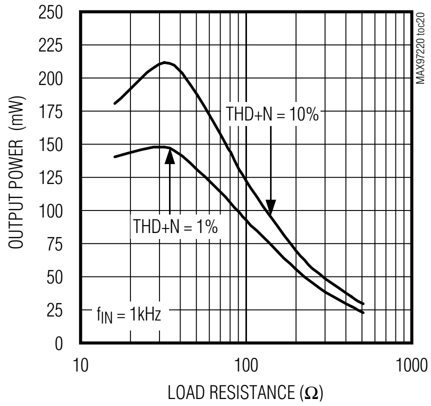
OUTPUT VOLTAGE vs. LOAD RESISTANCE



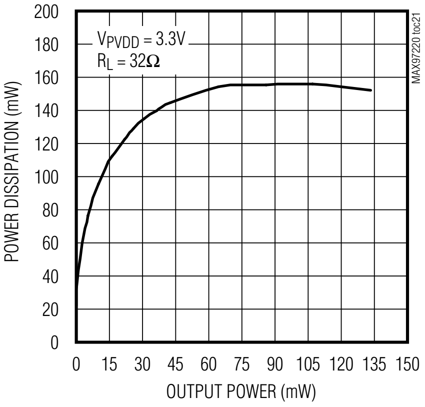
OUTPUT VOLTAGE vs. LOAD RESISTANCE



OUTPUT POWER vs. LOAD RESISTANCE



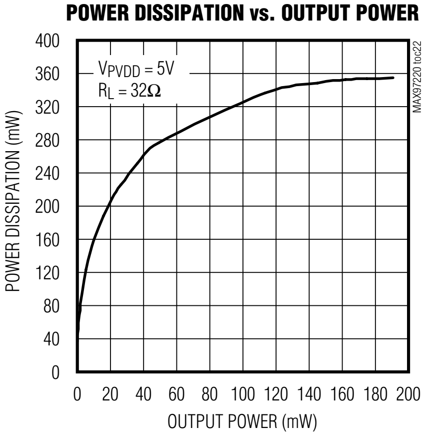
OUTPUT POWER vs. LOAD RESISTANCE

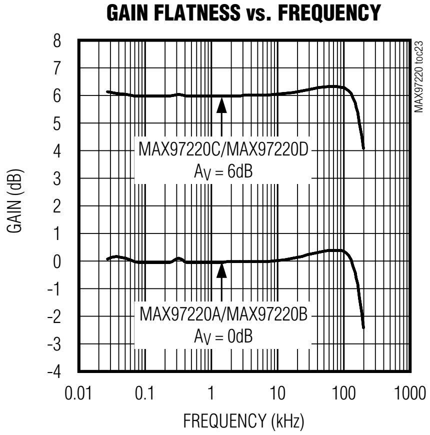


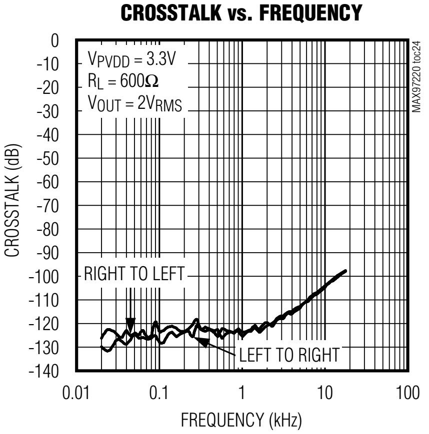
POWER DISSIPATION vs. OUTPUT POWER

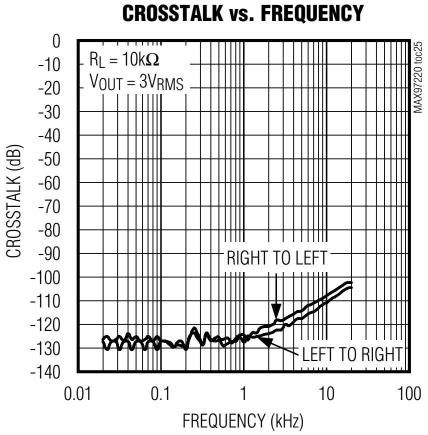
Typical Operating Characteristics (continued)

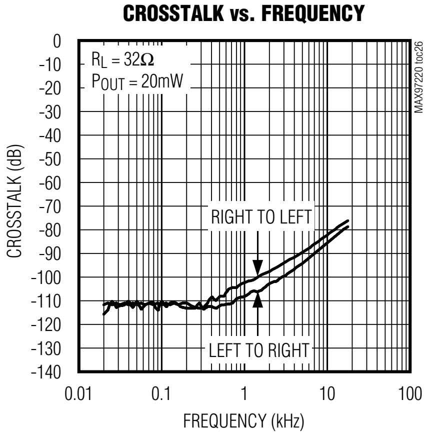
($V_{PVDD} = V_{SVDD} = V_{SVDD2}$ = 5V, $V_{PGND} = V_{SGND}$ = 0V, C_{BIAS} = 0.1µF, C1 = C2 = 1µF, R_{IN} = 10kΩ, R_F = 10kΩ, unless otherwise noted.)

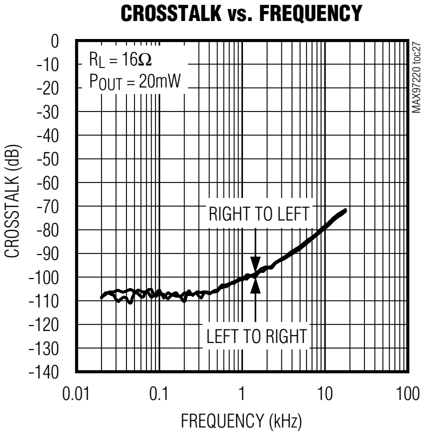

POWER DISSIPATION vs. OUTPUT POWER

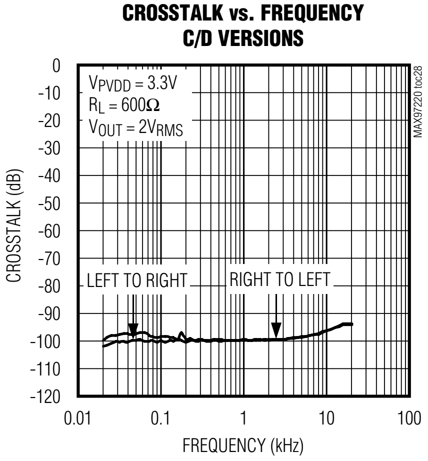

GAIN FLATNESS vs. FREQUENCY

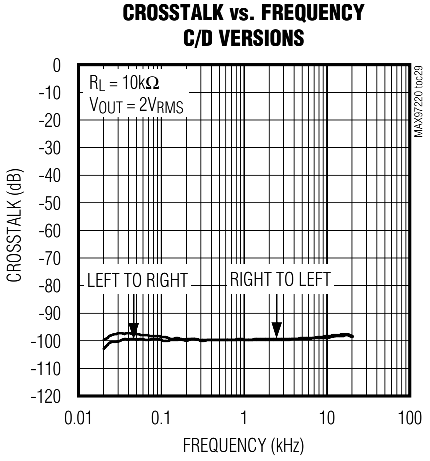

CROSSTALK vs. FREQUENCY

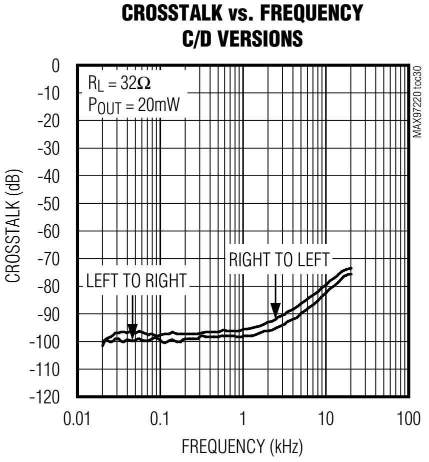

CROSSTALK vs. FREQUENCY


CROSSTALK vs. FREQUENCY


CROSSTALK vs. FREQUENCY

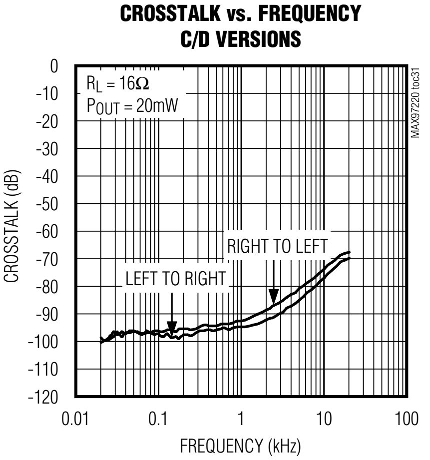

CROSSTALK vs. FREQUENCY
C/D VERSIONS

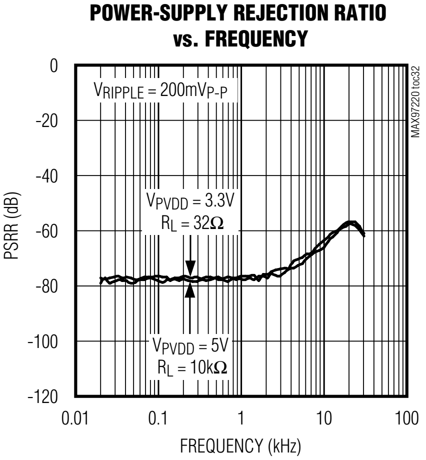

CROSSTALK vs. FREQUENCY
C/D VERSIONS

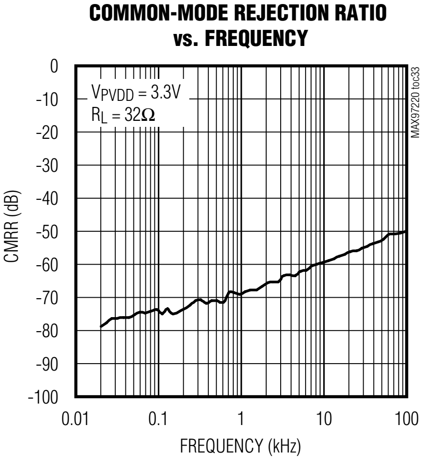

CROSSTALK vs. FREQUENCY
C/D VERSIONS

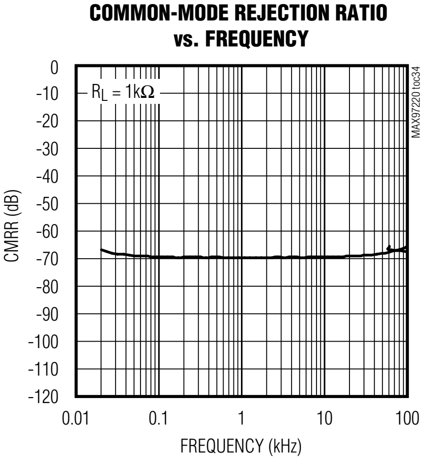
Typical Operating Characteristics (continued)

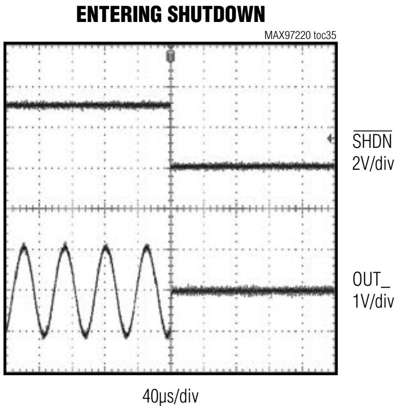
(V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V, V_{PGND} = V_{SGND} = 0V, C_{BIAS} = 0.1µF, C1 = C2 = 1µF, R_{IN} = 10kΩ, R_F = 10kΩ, unless otherwise noted.)

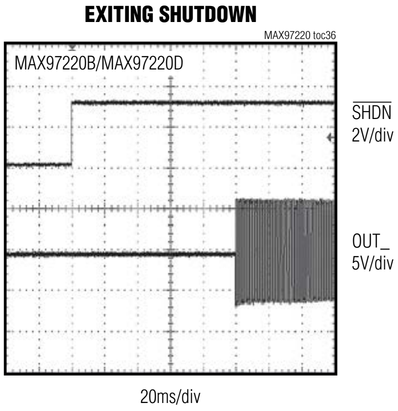






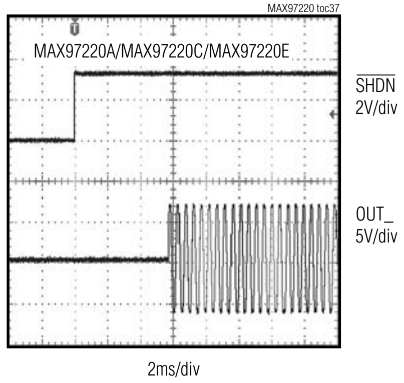




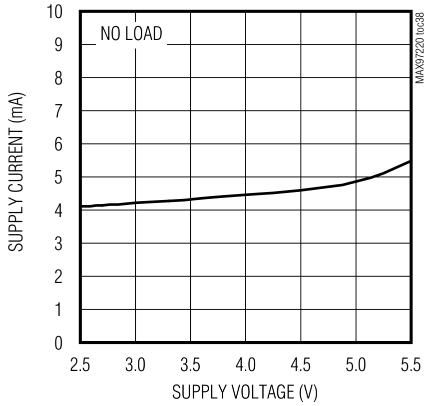


Typical Operating Characteristics (continued)

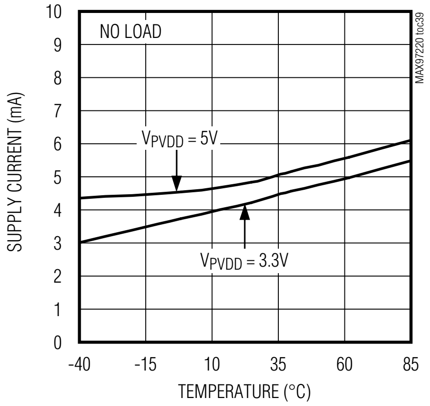
(V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V, V_{PGND} = V_{SGND} = 0V, C_{BIAS} = 0.1µF, C1 = C2 = 1µF, R_{IN} = 10kΩ, R_F = 10kΩ, unless otherwise noted.)



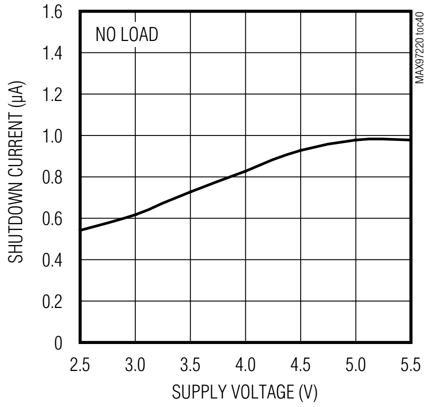
EXITING SHUTDOWN



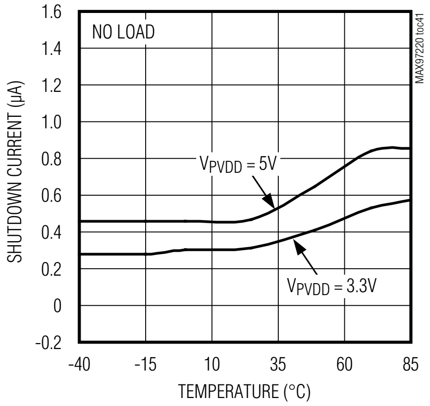
SUPPLY CURRENT vs. SUPPLY VOLTAGE



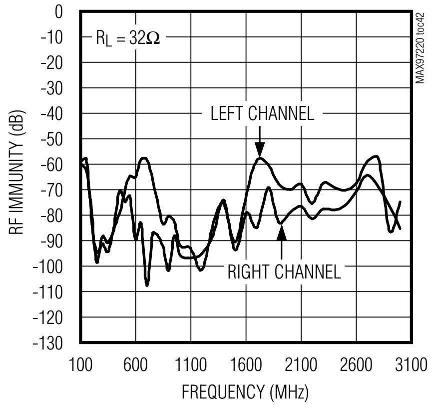
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE

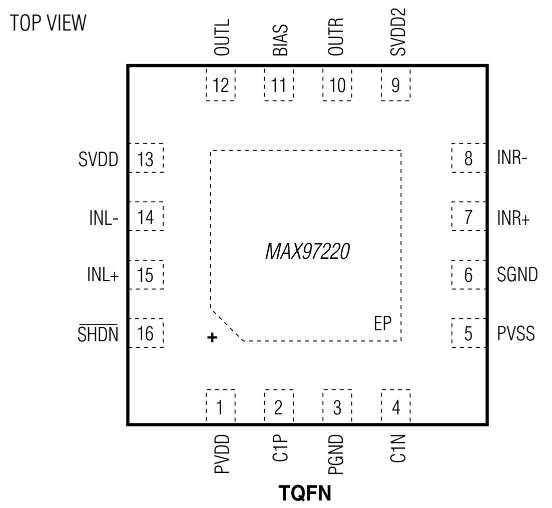


SHUTDOWN CURRENT vs. TEMPERATURE



RF IMMUNITY vs. FREQUENCY

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	PVDD	Charge-Pump Power-Supply Input. Bypass to PGND with 1µF.
2	C1P	Positive Flying Capacitor Connection. Connect a 1µF capacitor between C1P and C1N.
3	PGND	Power Ground. Connect PGND and SGND together at the system ground plane.
4	C1N	Negative Flying Capacitor Connection. Connect a 1µF capacitor between C1P and C1N.
5	PVSS	Negative Charge-Pump Output. Bypass to PGND with 1µF.
6	SGND	Signal Ground. Connect PGND and SGND together at the system ground plane.
7	INR+	Right Positive Polarity Input
8	INR-	Right Negative Polarity Input
9	SVDD2	Signal Path Power-Supply Input. Bypass to PGND with 1µF. Connect directly to PVDD.
10	OUTR	Right DirectDrive Output
11	BIAS	Internal Supply Node. Bypass to PGND with 0.1µF.
12	OUTL	Left DirectDrive Output
13	SVDD	Signal Path Power-Supply Input. Bypass to PGND with 1µF. Connect directly to PVDD.
14	INL-	Left Negative Polarity Input
15	INL+	Left Positive Polarity Input
16	$\overline{\text{SHDN}}$	Active-Low Shutdown. Drive $\overline{\text{SHDN}}$ high for normal operation.
—	EP	Exposed Pad. Electrically connect to PGND or leave unconnected.

Detailed Description

The MAX97220_ is a fully differential input line driver/headphone amplifier for set-top boxes, LCD TV, and home theater applications where audio fidelity is of primary importance. Power consumption of the amplifier is reduced while maintaining high SNR and THD+N performance. The MAX97220A/MAX97220B/MAX97220E require external input and feedback resistors to set amplifier gain. The MAX97220C/MAX97220D feature internal input and feedback resistors for a set gain of +6dB. Output swings of $3V_{RMS}$ with a 5V supply and $2V_{RMS}$ with a 3.3V supply are perfect for line driver applications.

High fidelity is maintained through the differential input connection. An output noise voltage of $7\mu V_{RMS}$ allows for 112dB SNR when powered from 5V and 109dB SNR when powered from 3.3V. The IC has better than 90dB THD+N across the entire audio bandwidth.

The MAX97220_ operates from a single supply ranging from 2.5V to 5.5V. An on-chip charge pump inverts the positive supply (PVDD), creating an equal magnitude negative supply (PVSS). The headphone amplifiers operate from bipolar supplies with their outputs biased about PGND (Figure 1). The benefit of this PGND bias is that the amplifier outputs do not have a DC component, typically PVDD/2. The large DC-blocking capacitors required with conventional headphone amplifiers are unnecessary, thus conserving board space, reducing system cost, and improving frequency response. Output power of 125mW into 32Ω is achievable from a 5V supply. The device features an undervoltage lockout that prevents operation from an insufficient power supply and click-and-pop suppression that eliminates audible transients on startup and shutdown.

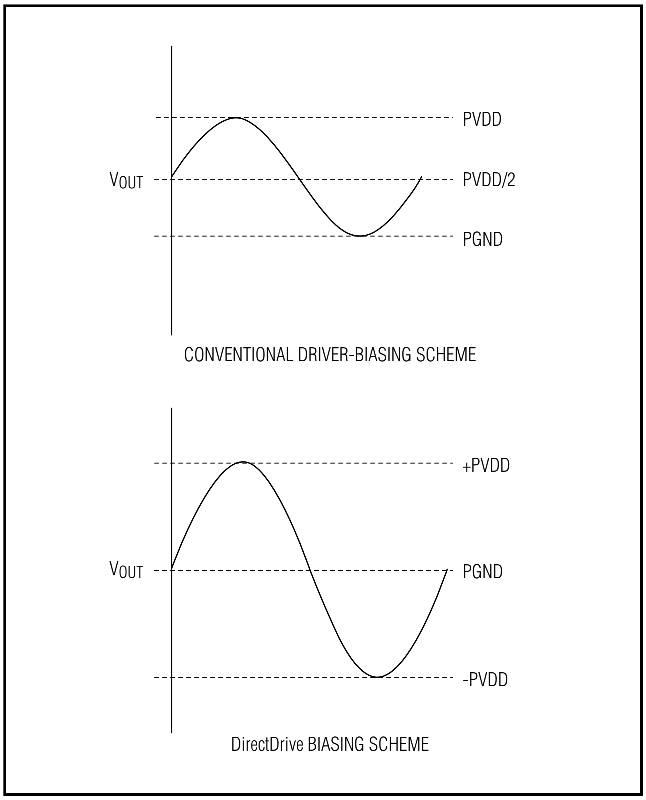


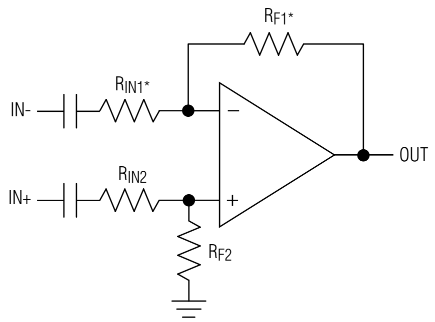
Figure 1. Conventional Driver Output Waveform vs. MAX97220_ Output Waveform

Differential Input

The IC can be configured as differential or pseudo-differential input amplifiers (Figures 2 and 3), making it compatible with all codecs. A differential input offers improved noise immunity over a single-ended input. In devices such as cellular phones, high-frequency signals from the RF transmitter can couple into the amplifier's input traces. The signals appear at the amplifier's inputs as common-mode noise. A differential input amplifier amplifies the difference of the two inputs while signals common to both inputs are cancelled. Configured differentially, the gain of the MAX97220A/MAX97220B/MAX97220E is set by:

$$A_V = R_F/R_{IN}$$

The common-mode rejection ratio (CMRR) is limited by the external resistor matching, and if used, input capacitor matching at low frequencies. For example, the worst-case variation of 1% tolerant resistors results in 40dB CMRR, while 0.1% resistors result in 60dB CMRR. For best matching, use resistor arrays.



$R_{IN1} = R_{IN2}$, $R_{F1} = R_{F2}$

*R_{IN1} AND R_{F1} ARE INTERNAL FOR MAX97220C/MAX97220D

Figure 2. Differential Input Configuration

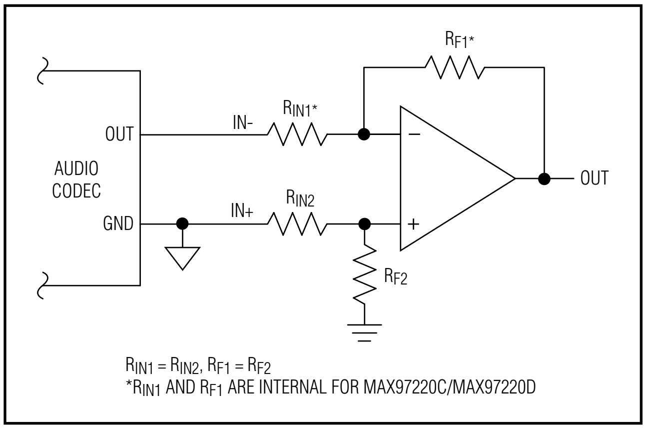


Figure 3. Pseudo-Differential Input Configuration

DirectDrive

Conventional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both the headphone and the headphone amplifier.

Maxim's patented DirectDrive architecture uses a charge pump to create an internal negative supply voltage, allowing the IC's outputs to be biased about PGND. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF, typ) tantalum capacitors, the IC charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier.

Input Filter

In addition to the cost and size disadvantages of DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal.

If input capacitors are used, input capacitor C_{IN}, in conjunction with internal input resistor R_{IN}, forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Setting f_{-3dB} too high affects the low-frequency response of the amplifier. Use capacitors with adequately low voltage coefficients, such as X7R ceramic capacitors with a high voltage rating. Capacitors with higher voltage coefficients result in increased distortion at low frequencies.

BIAS Capacitor

Bypass BIAS with a 0.1µF capacitor to PGND. Do not connect external loads to BIAS.

Charge Pump

The MAX97220_ features a low-noise charge pump. The 500kHz switching frequency is well beyond the audio range and, thus, does not interfere with the audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic bond wire and trace inductance is minimized. The IC requires a 1µF flying capacitor between C_{1P} and C_{1N} and a 1µF hold capacitor from PVSS to PGND.

Click-and-Pop Suppression

The IC features Maxim's industry-leading click-and-pop suppression circuitry. When entering shutdown, the amplifier outputs are high impedance to ground. This scheme minimizes the energy present in the audio band.

Shutdown

The IC features a 1µA low-power shutdown mode that reduces power consumption. When the active-low shutdown mode is entered, the device's internal bias circuitry is disabled, the amplifier outputs go high impedance, and BIAS is driven to PGND. The MAX97220A/MAX97220B/MAX97220E inputs are driven to PGND.

Applications Information

MAX9722 Compatibility

The MAX97220_ is compatible with the footprint of the MAX9722. BIAS on the MAX97220_ is in the same position as SVSS. On the MAX9722, SVSS is connected to PVSS. For the MAX97220_, there is only one charge-pump output that doubles as the amplifier's negative power-supply input. The connection of negative charge-pump output and amplifier negative power-supply input is internal on the MAX97220_ and external on the MAX9722.

To implement a PCB that is compatible with both the MAX9722 and MAX97220_, put a capacitor pad from BIAS/SVSS (MAX97220_/MAX9722 pin 11) to PGND. Also, place a 0Ω resistor pad from BIAS/SVSS (MAX97220_/MAX9722 pin 11) to PVSS (pin 5 on both parts). Install the 0Ω resistor when the MAX9722 is used and leave the resistor out of circuit when the MAX97220_ is used (Figure 4).

Power Dissipation

While driving a headphone load, the IC dissipates a significant amount of power. The maximum power dissipation is given in the Continuous Power Dissipation of the *Absolute Maximum Ratings* section or can be calculated by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section.

Since the IC is a stereo amplifier, the total maximum internal power dissipation for a given V_{DD} and load is given by the following equation:

$$P_{D(MAX)} = \frac{4V_{DD}^2}{\pi^2 R_L}$$

If the internal power dissipation for a given application exceeds the maximum allowed for a given package, reduce power dissipation by decreasing supply voltage, ambient temperature, input signal, or gain, or by increasing load impedance.

The TQFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal impedance by providing a direct heat conduction path from the die to the PCB. Connect the exposed thermal pad to PGND or an isolated plane.

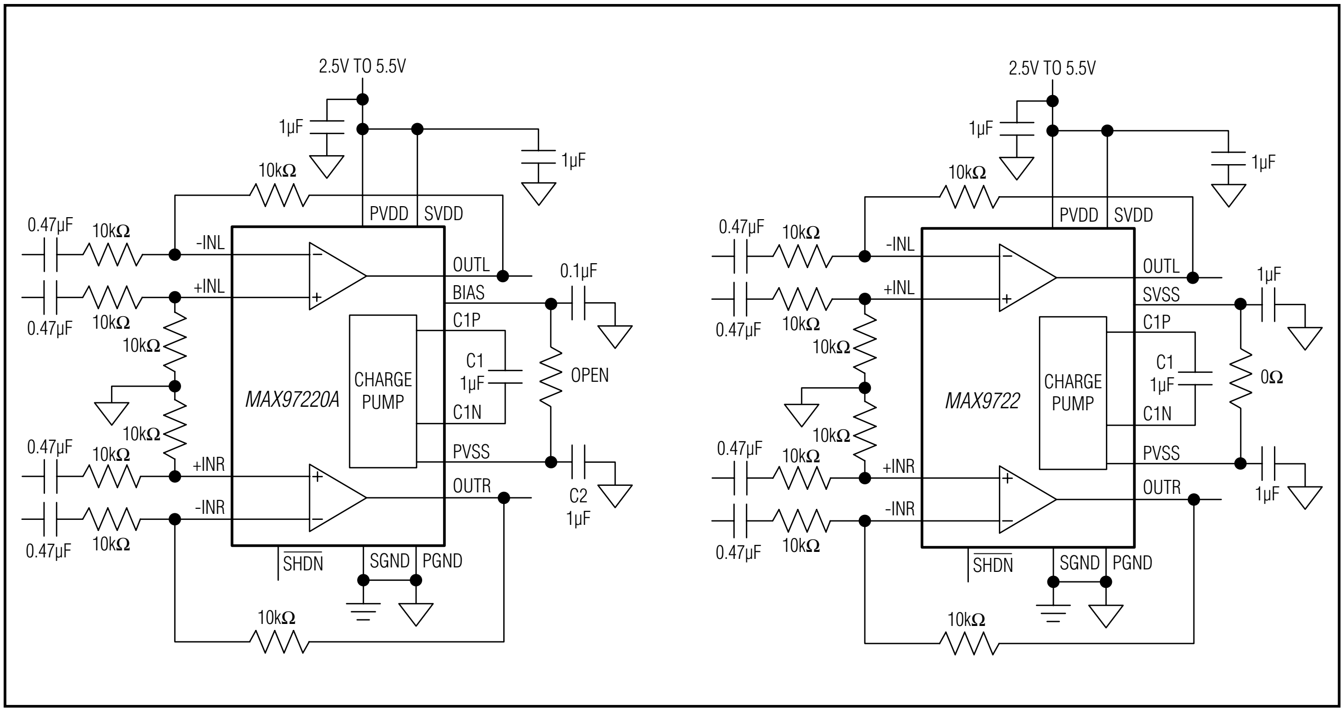


Figure 4. MAX97220A vs. MAX9722 PCB Layout

Thermal-overload protection limits total power dissipation in the IC. When the junction temperature exceeds +160°C, the thermal protection circuitry disables the amplifier. Operation returns to normal once the die cools by 15°C.

Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the charge pump's load regulation and output resistance. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. Above 1µF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Hold Capacitor (C2)

The hold capacitor value and ESR directly affect the ripple at PVSS. Use a low-ESR 1µF capacitor for C2.

Amplifier Gain

The gain of the MAX97220C/MAX97220D is internally set at 6dB where all gain-setting resistors are integrated into the device. The internally set gain, in combination with DirectDrive, results in a headphone amplifier that requires only tiny 1µF capacitors to complete the amplifier circuit.

The gain of the MAX97220A/MAX97220B/MAX97220E amplifier is set externally as shown in Figure 5. The gain is:

$$A_V = -R_F/R_{IN}$$

Choose feedback resistor values between the 4.7kΩ and 100kΩ range.

Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Connect a 1µF ceramic capacitor from PVDD to PGND and a 1µF ceramic capacitor from SVDD to PGND. Add additional bulk capacitance as required by the application. Locate the bypass capacitor as close as possible to the device.

PCB Layout and Grounding

Good PCB layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance and route heat away from the device. Good grounding improves audio performance, and prevents any digital switching noise from coupling into the audio.

Connect PGND and SGND together at a single point on the PCB. Connect all components associated with the charge pump (C1 and C2) to the PGND plane. Connect PVDD and SVDD together at the device. Place capacitors C1 and C2 as close as possible to the device. Ensure the PCB layout is partisioned so that the large switching currents in the ground plane do not return through SGND and the traces and components in the audio signal path. Refer to the MAX97220 Evaluation Kit for layout guidelines.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes. Also, ensure a solid ground plane is used in multilayer PCB designs.

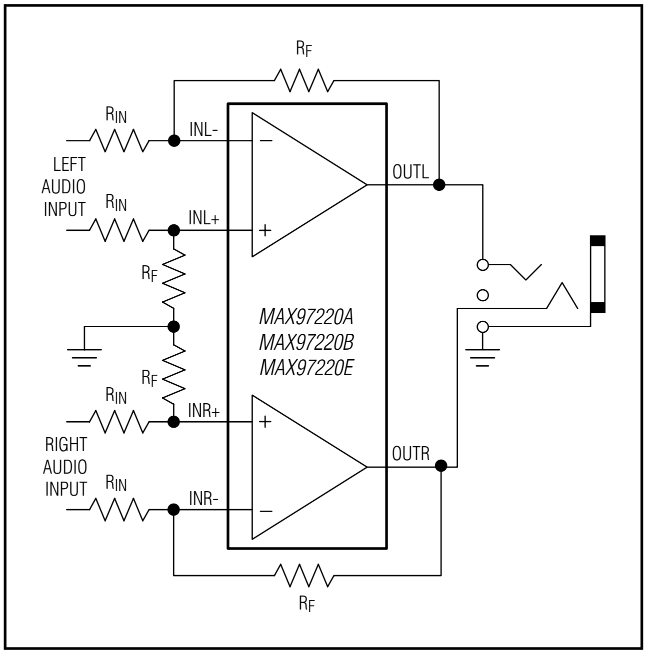
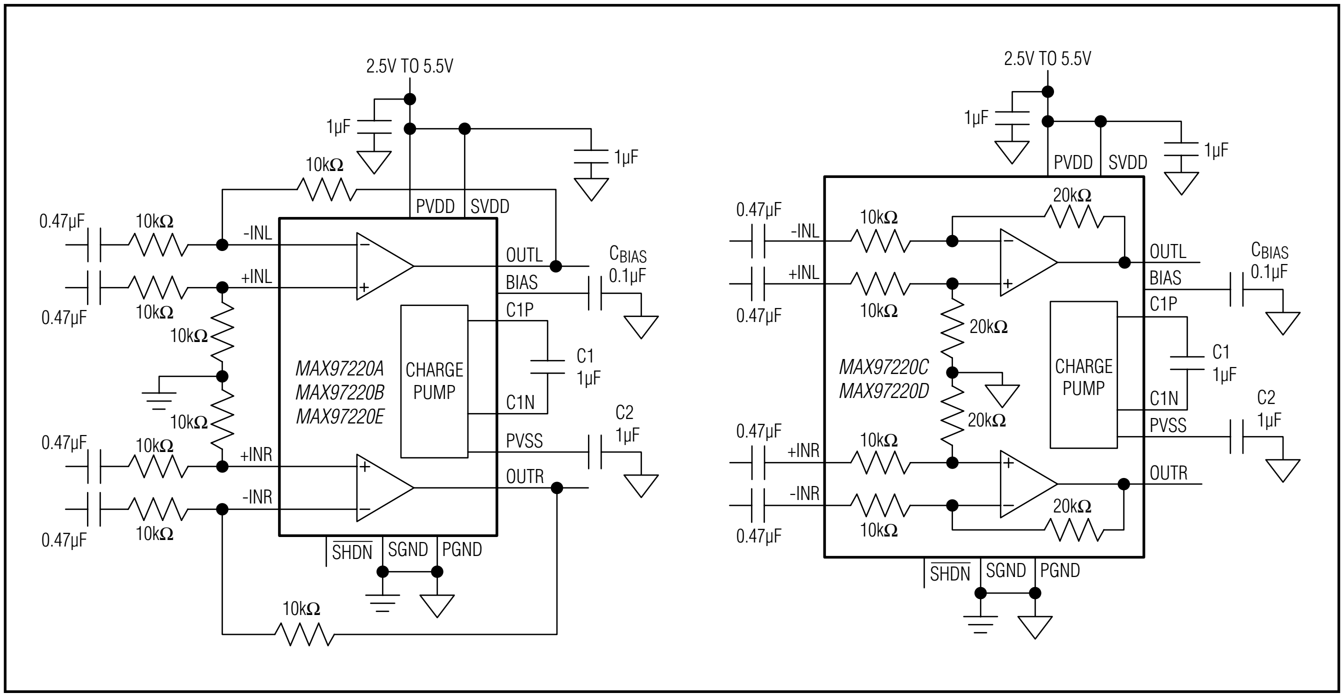


Figure 5. Setting the MAX97220A/MAX97220B/MAX97220E Gain

Functional Diagrams



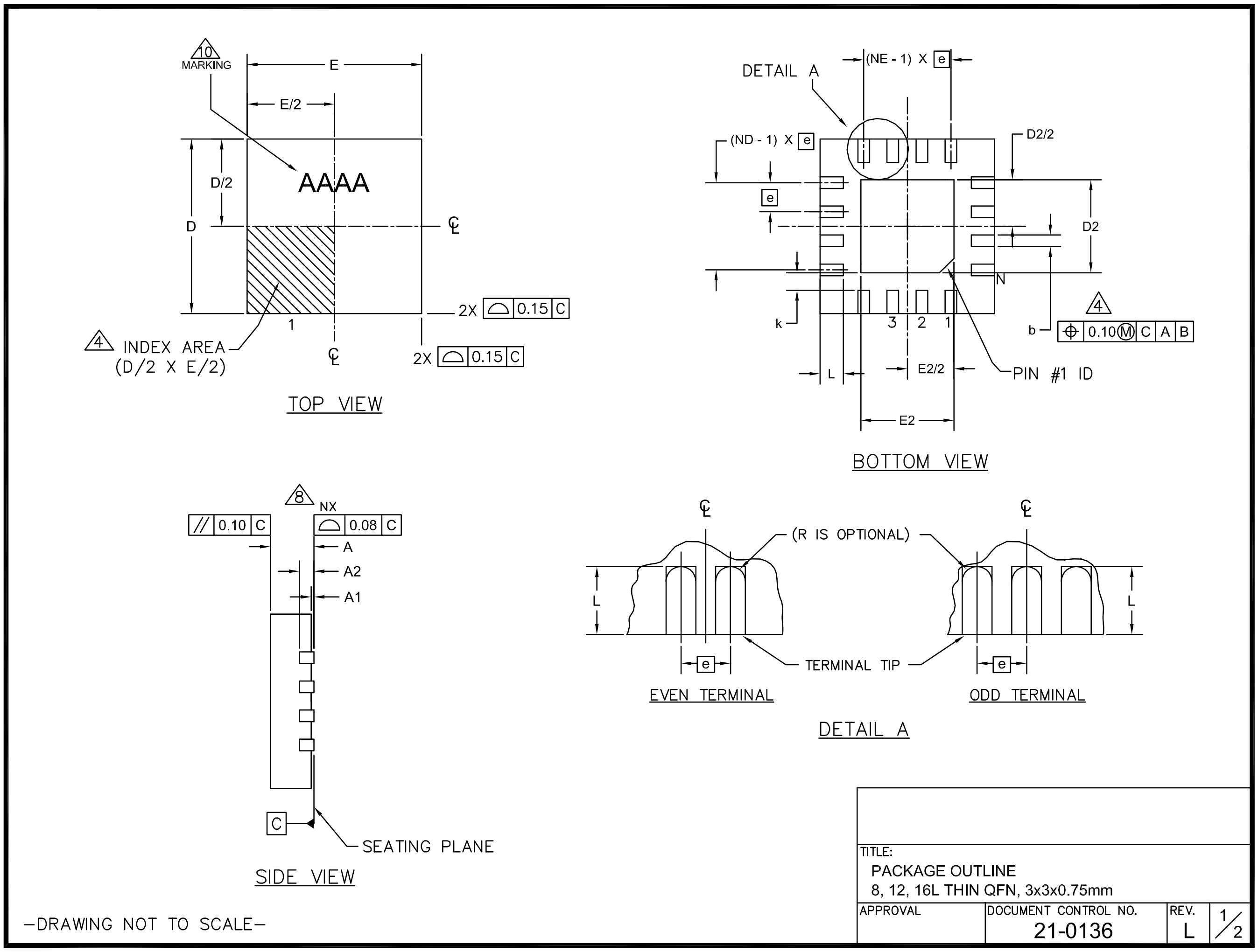
Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1633-4	21-0136	90-0031



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND Pb FREE (+) PARTS.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. J	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/11	Initial release	—
1	10/11	Added top marks to *Ordering Information*, added B/C/D versions to Quiescent Supply Current, Output Signal Attenuation in Shutdown, and Power-Supply Rejection Ratio in the *Electrical Characteristics* table	1, 2, 3
2	7/12	Added MAX97220E	1–19