+5V Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- V_{CC}, BATT ..... -0.3V to +6.0V
- All Other Pins (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} Peak 1A
- V_{CC} Continuous 250mA
- BATT Peak 250mA
- BATT Continuous 50mA
- GND 25mA

Output Current
- OUT 250mA
- All Other Outputs 25mA

OUT Short-Circuit Duration 10sec

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- µMAX (derate 4.10mW/°C above +70°C) 330mW

Operating Temperature Ranges
- MAX81_ _C_A ..... 0°C to +70°C
- MAX81_ _E_A ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The input voltage limits on PFI and WDI may be exceeded (up to 12V V_{IN}) if the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V for MAX81_L, V_{CC} = +4.5V to +5.5V for MAX81_M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, V_{BATT} (Note 2)				0		5.5	V
Supply Current (excluding I_{OUT})	I_{SUPPLY}	As applicable; $\overline{CE}$ IN = 0V, WDI and $\overline{MR}$ unconnected	MAX81_ _C		11	45	µA
			MAX81_ _E		11	60	
Supply Current in Battery-Backup Mode (excluding I_{OUT})		V_{CC} = 0V	T_A = +25°C		0.05	1.0	µA
			T_A = T_{MIN} to T_{MAX}			5.0	
BATT Standby Current (Note 3)		5.5V > V_{CC} > (V_{BATT} + 0.2V)	T_A = +25°C	-0.10		0.02	µA
			T_A = T_{MIN} to T_{MAX}	-1.00		0.02	
BATT Leakage Current, Freshness Seal Enabled		V_{CC} = 0V, V_{OUT} = 0V				1	µA
V_{OUT} Output		I_{OUT} = 5mA		V_{CC} - 0.05	V_{CC} - 0.025		V
		I_{OUT} = 50mA		V_{CC} - 0.5	V_{CC} - 0.25		
V_{CC} to OUT On-Resistance					5	10	Ω
BATT to OUT On-Resistance					100		Ω
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < (V_{BATT} - 0.2V)		V_{BATT} - 0.1	V_{BATT} - 0.02		V
Battery Switch Threshold (V_{CC} - V_{BATT})		V_{CC} < V_{RST}	Power-up		20		mV
			Power-down		-20		
Battery Switchover Hysteresis					40		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.5V for MAX81_L, V_{CC} = +4.5V to +5.5V for MAX81_M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET AND WATCHDOG TIMER						
Reset Threshold	V_{RST}	MAX81_L	4.50	4.65	4.75	V
		MAX81_M	4.25	4.40	4.50	
Reset Threshold Hysteresis				25		mV
Reset Timeout Period	t_{RP}		140	200	280	ms
$\overline{RESET}$ Output Voltage	V_{OH}	V_{CC} > $V_{RST(MAX)}$, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
	V_{OL}	V_{CC} < $V_{RST(MIN)}$, I_{SINK} = 3.2mA			0.4	
		MAX81_ _C, V_{CC} = 1V, V_{CC} falling, V_{BATT} = 0V, I_{SINK} = 50µA			0.3	
		MAX81_ _E, V_{CC} = 1.2V, V_{CC} falling, V_{BATT} = 0V, I_{SINK} = 100µA			0.3	
V_{CC} to $\overline{RESET}$ Delay		From V_{RST}, V_{CC} falling at 10V/ms		100		µs
Watchdog Timeout Period	t_{WD}		1.00	1.60	2.25	sec
WDI Pulse Width	t_{WDI}	V_{IL} = 0.4V, V_{IH} = 0.8V_{CC}	50			ns
WDI Input Threshold (Note 4)	V_{IL}	V_{CC} = 5V			0.8	V
	V_{IH}		3.5			
WDI Input Current (Note 5)		WDI = V_{CC}, time average		120	160	µA
		WDI = GND, time average	-20	-15		
POWER-FAIL COMPARATOR (MAX817/MAX819 only)						
PFI Input Threshold	V_{PFT}		1.20	1.25	1.30	V
PFI Input Hysteresis				4		mV
PFI Input Current	I_{PFI}		-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OL}	V_{PFI} < 1.20V, I_{SINK} = 3.2mA, V_{CC} > 4.50V			0.4	V
	V_{OH}	V_{PFI} > 1.30V, I_{SOURCE} = 40µA, V_{CC} > 4.5V	V_{CC} - 1.5			
$\overline{PFO}$ Short-Circuit Current		$V_{\overline{PFO}}$ = 0V		250	500	µA
MANUAL RESET INPUT (MAX819 only)						
$\overline{MR}$ Input Threshold	V_{IL}		0.8			V
	V_{IH}				2.0	
$\overline{MR}$ Pulse Width			1			µs
$\overline{MR}$ Pulse that Would Not Cause a Reset				100		ns
$\overline{MR}$ to Reset Delay				120		ns
$\overline{MR}$ Pull-Up Resistance			45	63	85	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.75V to +5.5V for MAX81_L, V_{CC} = +4.5V to +5.5V for MAX81_M, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

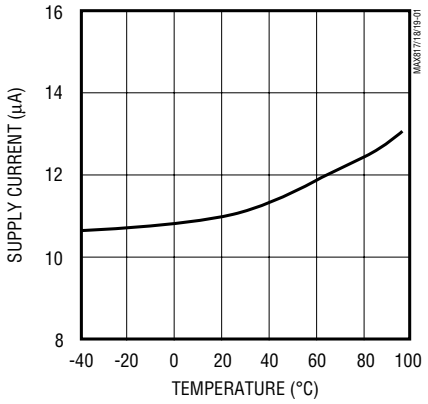
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHIP-ENABLE GATING (MAX818 only)						
$\overline{CE}$ IN Leakage Current		Disable mode		±0.005	±1	µA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance (Note 6)		Enable mode		40	150	Ω
$\overline{CE}$ OUT Short-Circuit Current (Reset Active)		Disable mode, $\overline{CE}$ OUT = 0V	0.1	0.75	2.0	mA
$\overline{CE}$ IN to $\overline{CE}$ OUT Propagation Delay (Note 7)		50Ω source impedance driver, C_{LOAD} = 50pF		3	8	ns
$\overline{CE}$ OUT Output	V_{OH}	I_{OUT} = -100µA, V_{CC} = 0V	V_{CC} - 1V			V
		I_{OUT} = -1µA, V_{CC} = 0V, V_{BATT} = 2.8V	2.7			
$\overline{CE}$ OUT Input Threshold	V_{IH}	V_{CC} = 5V			0.8	V
	V_{IL}		3.5			
$\overline{RESET}$ to $\overline{CE}$ OUT Delay		Power-down		15		µs

Note 2: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2.0V.
Note 3: "-" = battery-charging current, "+" = battery-discharging current.
Note 4: WDI is internally serviced within the watchdog timeout period if WDI is left unconnected.
Note 5: WDI input is designed to be driven by a three-stated output device. To float WDI, the "high-impedance mode" of the output device must have a maximum leakage current of 10µA and a maximum output capacitance of 200pF. The output device must also be able to source and sink at least 200µA when active.
Note 6: The chip-enable resistance is tested with V_{CC} = +4.75V for the MAX818L and V_{CC} = +4.5V for the MAX818M. $V_{\overline{CE}\ IN}$ = $V_{\overline{CE}\ OUT}$ = V_{CC}/2.
Note 7: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.

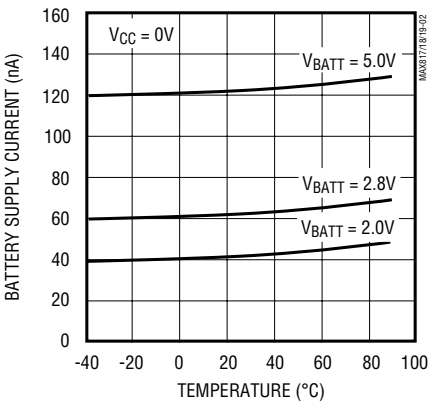
Typical Operating Characteristics

(V_{CC} = +5V, V_{BATT} = 3.0V, T_A = +25°C, unless otherwise noted.)

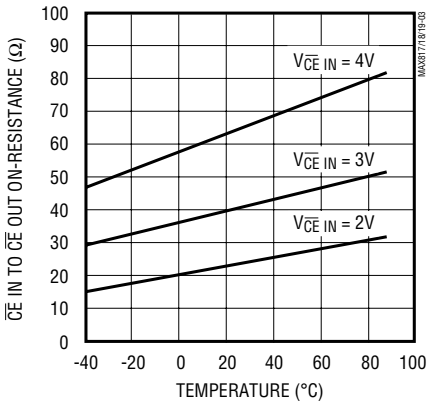
SUPPLY CURRENT vs. TEMPERATURE (NO LOAD)



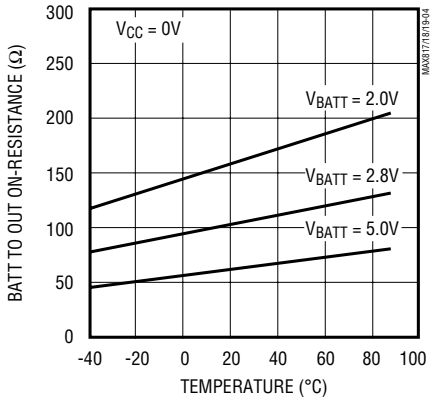
BATTERY SUPPLY CURRENT (BACKUP MODE) vs. TEMPERATURE



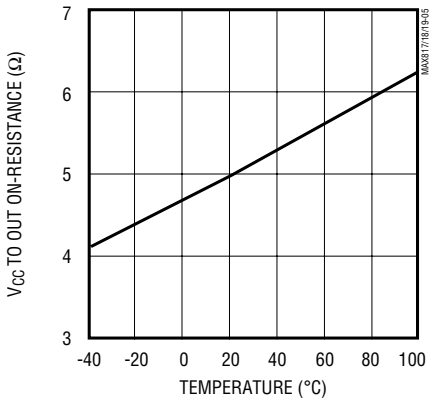
$\overline{CE}$ IN TO $\overline{CE}$ OUT ON-RESISTANCE vs. TEMPERATURE



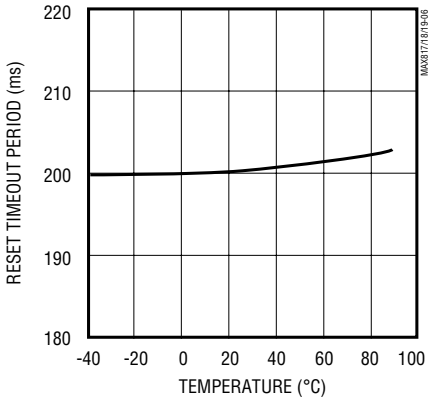
BATT TO OUT ON-RESISTANCE vs. TEMPERATURE



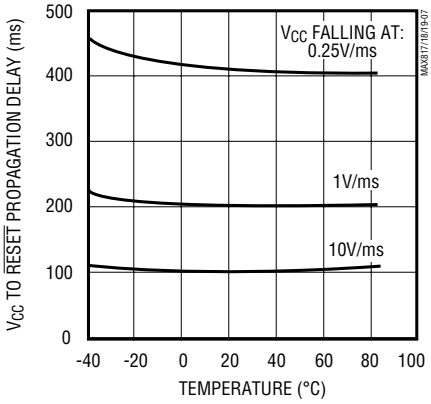
V_{CC} TO OUT ON-RESISTANCE vs. TEMPERATURE



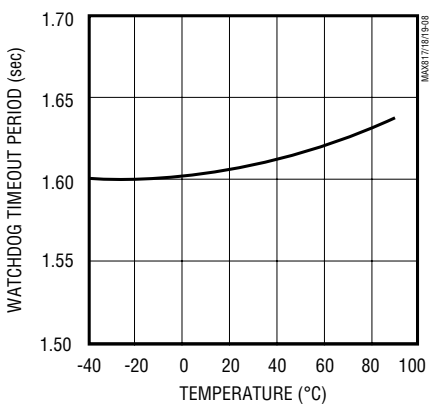
RESET TIMEOUT PERIOD vs. TEMPERATURE



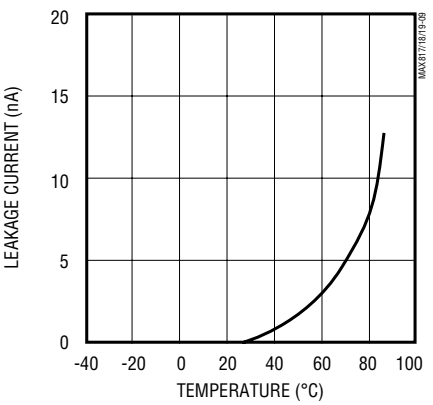
V_{CC} TO $\overline{RESET}$ PROPAGATION DELAY vs. TEMPERATURE



WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



BATTERY FRESHNESS SEAL LEAKAGE CURRENT vs. TEMPERATURE

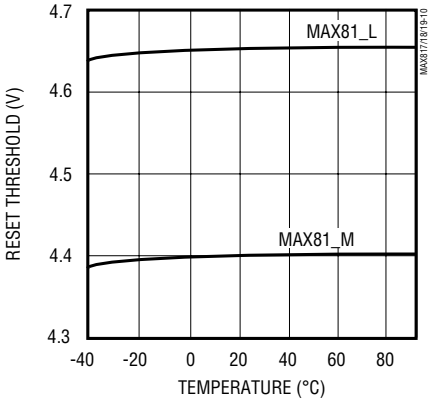


+5V Microprocessor Supervisory Circuits

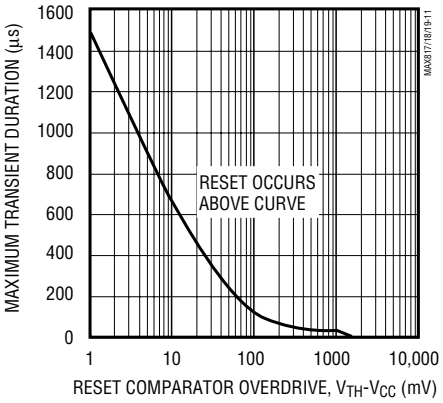
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{BATT} = 3.0V, T_A = +25°C, unless otherwise noted.)

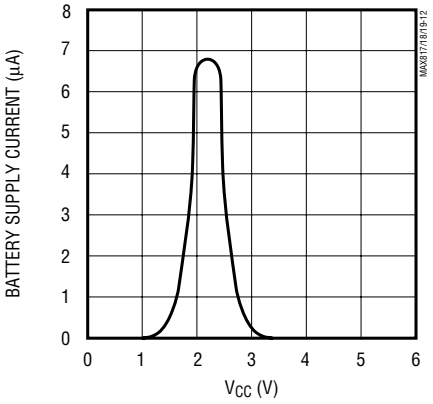
RESET THRESHOLD vs. TEMPERATURE



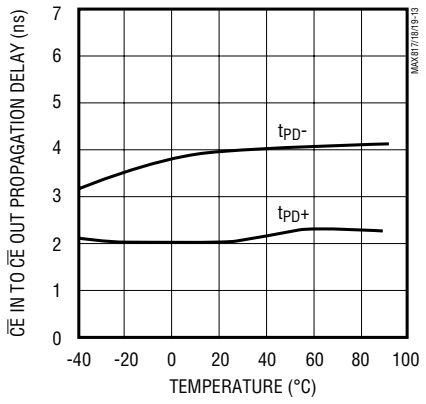
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



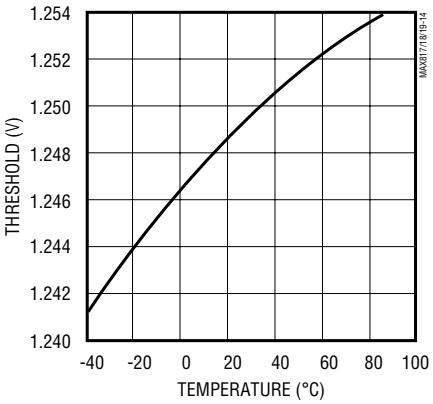
BATTERY SUPPLY CURRENT vs. SUPPLY VOLTAGE



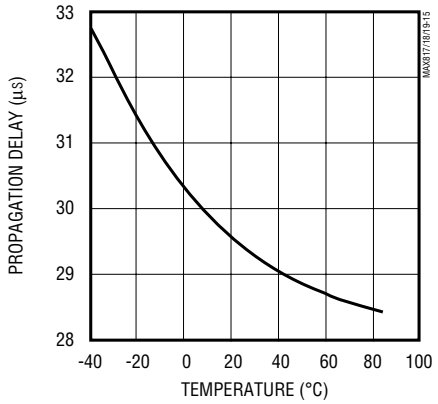
$\overline{CE}$ IN TO $\overline{CE}$ OUT PROPAGATION DELAY vs. TEMPERATURE



MAX817/MAX819 PFI THRESHOLD vs. TEMPERATURE



MAX817/MAX819 PFI TO $\overline{PFO}$ PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX817	MAX818	MAX819		
1	1	1	OUT	Supply Output for CMOS RAM. When V_{CC} rises above the reset threshold or above V_{BATT}, OUT is connected to V_{CC} through an internal P-channel MOSFET switch. When V_{CC} falls below V_{BATT}, BATT connects to OUT.
2	2	2	V_{CC}	Input Supply Voltage, +5V input.
3	3	3	GND	Ground. 0V reference for all signals.
4	—	4	PFI	Power-Fail Comparator Input. When V_{PFI} is below V_{PFT} or when V_{CC} is below V_{BATT}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high (see *Power-Fail Comparator* section). Connect to ground if unused.
—	4	—	$\overline{CE}$ IN	Chip-Enable Input. The input to the chip-enable gating circuit. Connect to ground if unused.
5	—	5	$\overline{PFO}$	Power-Fail Comparator Output. When PFI is less than V_{PFT} or when V_{CC} is below V_{BATT}, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. $\overline{PFO}$ is also used to enable the battery freshness seal (see *Battery Freshness Seal* and *Power-Fail Comparator* sections).
—	5	—	$\overline{CE}$ OUT	Chip-Enable Output. $\overline{CE}$ OUT goes low only if $\overline{CE}$ IN is low while reset is not asserted. If $\overline{CE}$ IN is low when reset is asserted, $\overline{CE}$ OUT will remain low for 15µs or until $\overline{CE}$ IN goes high, whichever occurs first. $\overline{CE}$ OUT is pulled up to OUT in battery-backup mode. $\overline{CE}$ OUT is also used to enable the battery freshness seal (see *Battery Freshness Seal* section).
6	6	—	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a reset is triggered. If WDI is left unconnected or is connected to a high-impedance three-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever reset is asserted, WDI is three-stated, or WDI sees a rising or falling edge. The WDI input is designed to be driven by a three-stated-output device with a maximum high-impedance leakage current of 10µA and a maximum output capacitance of 200pF. The output device must also be capable of sinking and sourcing 200µA when active.
—	—	6	$\overline{MR}$	Manual Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted for as long as $\overline{MR}$ is held low and for 200ms after $\overline{MR}$ returns high. The active-low input has an internal 63kΩ pull-up resistor. It can be driven from a TTL- or CMOS-logic line or shorted to ground with a switch. Leave open, or connect to V_{CC} if unused.
7	7	7	$\overline{RESET}$	Active-Low Reset Output. Pulses low for 200ms when triggered and remains low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for 200ms after V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes low to high.
8	8	8	BATT	Backup-Battery Input. When V_{CC} falls below V_{BATT}, OUT switches from V_{CC} to BATT. When V_{CC} rises above V_{BATT}, OUT reconnects to V_{CC}.

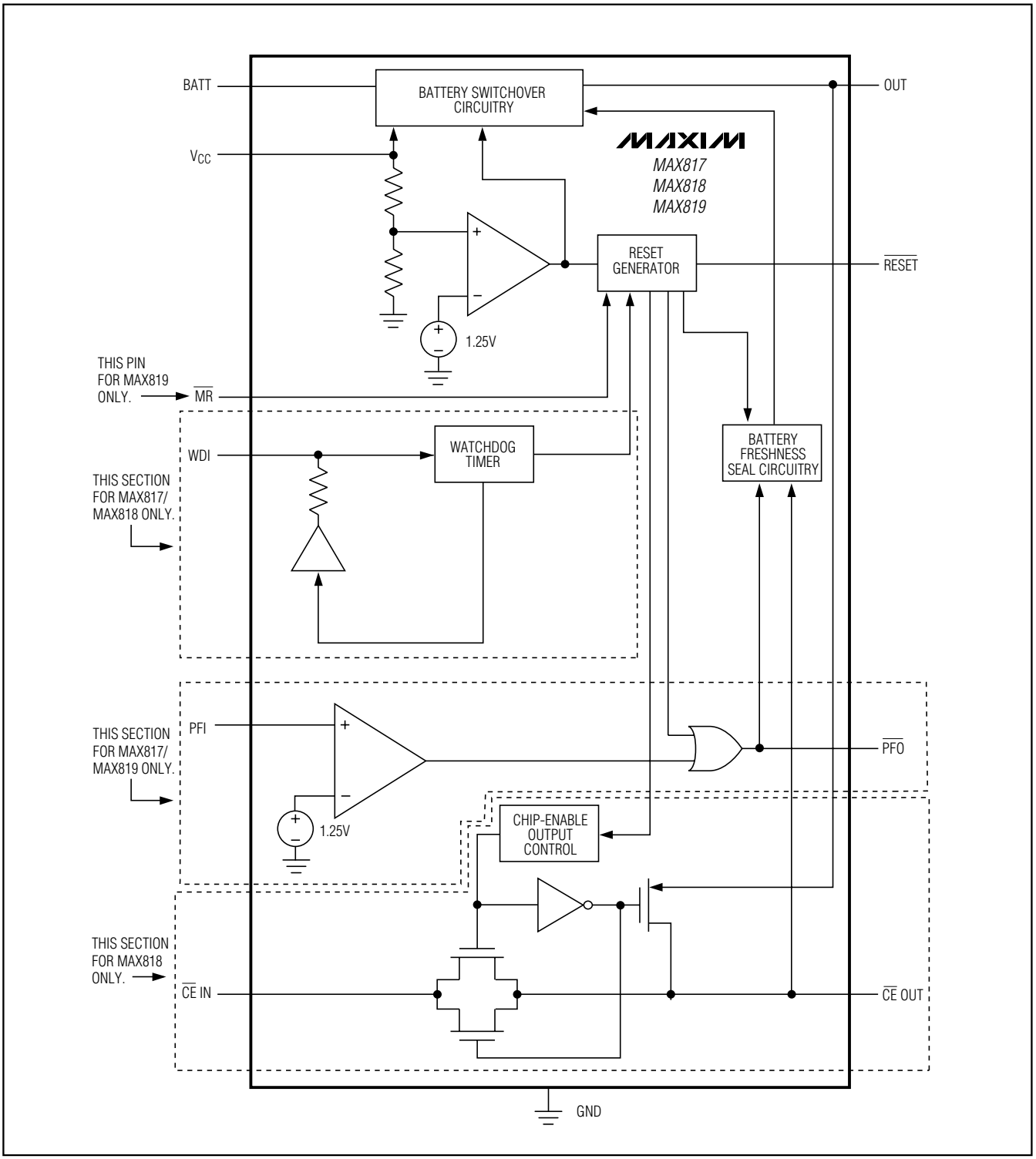


Figure 1. Functional Diagram

Detailed Description

General Timing Characteristics

Designed for 5V systems, the MAX817/MAX818/MAX819 provide a number of microprocessor (µP) supervisory functions (see the *Selector Guide* on the first page). Figure 2 shows the typical timing relationships of the various outputs during power-up and power-down with typical V_{CC} rise and fall times.

RESET Output

A µP's reset input starts the µP in a known state. The MAX817/MAX818/MAX819 µP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. $\overline{RESET}$ is guaranteed to be a logic low for 0V < V_{CC} < V_{RST} if V_{BATT} is greater than 1V. Without a backup battery (V_{BATT} = GND) $\overline{RESET}$ is guaranteed valid for V_{CC} ≥ 1V. Once V_{CC} exceeds the reset threshold an internal timer keeps $\overline{RESET}$ low for the reset timeout period, t_{RP}. After this interval $\overline{RESET}$ returns high (Figure 2).

If a brownout condition occurs (V_{CC} drops below the reset threshold), $\overline{RESET}$ goes low. Each time $\overline{RESET}$ is asserted it stays low for at least the reset timeout period. Any time V_{CC} goes below the reset threshold the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold. $\overline{RESET}$ both sources and sinks current.

Manual Reset Input (MAX819)

Many µP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX819, a logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{RP} (200ms) after it returns high.

During the reset timeout period (t_{RP}), $\overline{MR}$'s state is ignored if the battery freshness seal is enabled. $\overline{MR}$ has an internal 63kΩ pull-up resistor, so it can be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity.

Note that $\overline{MR}$ must be high or open to enable the battery freshness seal. Once the battery freshness seal is enabled its operation is unaffected by $\overline{MR}$.

Battery Freshness Seal

The MAX817/MAX818/MAX819 battery freshness seal disconnects the backup battery from internal circuitry and OUT until it is needed. This allows an OEM to ensure that the backup battery connected to BATT will be fresh when the final product is put to use. To enable the freshness seal on the MAX817 and MAX819:

1) Connect a battery to BATT.
2) Ground $\overline{PFO}$.
3) Bring V_{CC} above the reset threshold and hold it there until reset is deasserted following the reset timeout period.
4) Bring V_{CC} down again (Figure 3).

Use the same procedure for the MAX818, but ground $\overline{CE}$ OUT instead of $\overline{PFO}$. Once the battery freshness seal is enabled (disconnecting the backup battery from internal circuitry and anything connected to OUT), it remains enabled until V_{CC} is brought above V_{RST}.

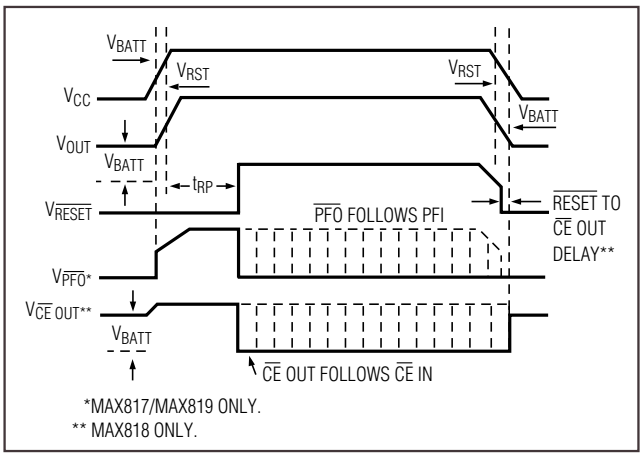


Figure 2. Power-Up and Power-Down Timing

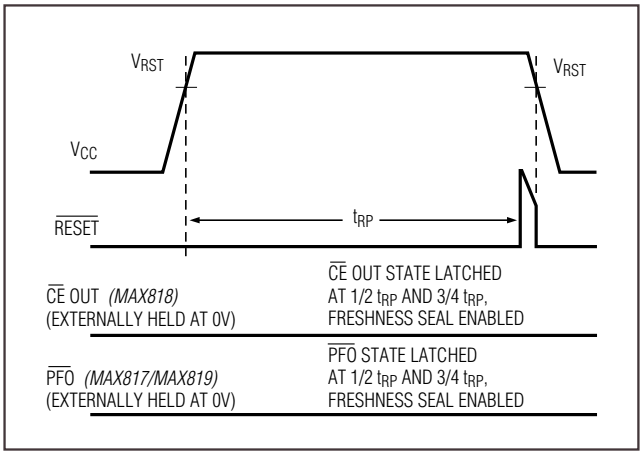


Figure 3. Battery Freshness Seal Timing

On the MAX819, $\overline{MR}$ must be high or open to enable the battery freshness seal. Once the battery freshness seal is enabled its operation is unaffected by $\overline{MR}$.

Watchdog Input (MAX817/MAX818)

In the MAX817/MAX818, the watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within t_{WD} (1.6sec), reset asserts. The internal 1.6sec timer is cleared by either a reset pulse or by toggling WDI, which can detect pulses as short as 50ns. The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting (Figure 4).

To disable the watchdog function, leave WDI unconnected or three-state the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period, then momentarily pulses high, resetting the watchdog counter. When WDI is left open-circuited, this internal driver clears the 1.6sec timer every 1.4sec. When WDI is three-stated or left unconnected, the maximum allowable leakage current is 10µA and the maximum allowable load capacitance is 200pF.

Chip-Enable Gating (MAX818)

Internal gating of the chip-enable (CE) signal prevents erroneous data from corrupting CMOS RAM in the event of an undervoltage condition. The MAX818 uses a series transmission gate from $\overline{CE}$ IN to $\overline{CE}$ OUT (Figure 5). During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the MAX818 to be used with most µPs. If $\overline{CE}$ IN is low when reset asserts, $\overline{CE}$ OUT remains low for typically 15µs to permit the current write cycle to complete.

Chip-Enable Input (MAX818)

The CE transmission gate is disabled and $\overline{CE}$ IN is high impedance (disabled mode) while reset is asserted. During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables and $\overline{CE}$ IN immediately becomes high impedance if the voltage at $\overline{CE}$ IN is high. If $\overline{CE}$ IN is low when reset asserts, the CE transmission gate will disable 15µs after reset asserts (Figure 6). This permits the current write cycle to complete during power-down.

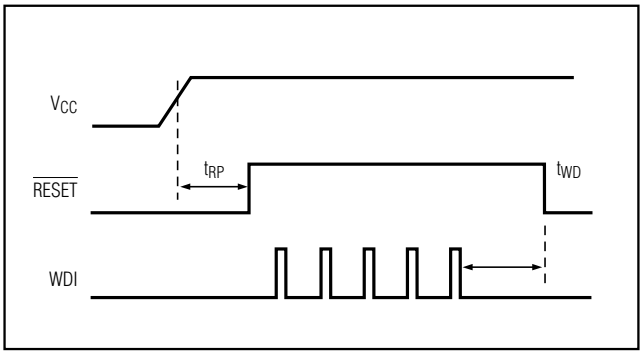


Figure 4. Watchdog Timing

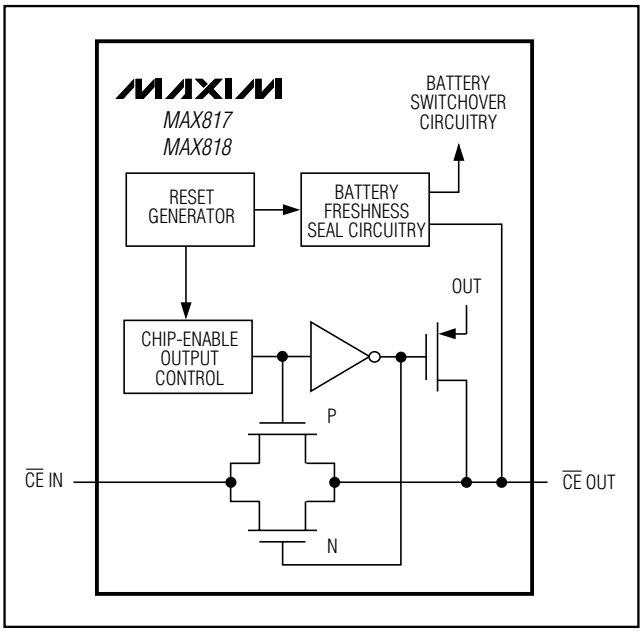


Figure 5. Chip-Enable Transmission Gate

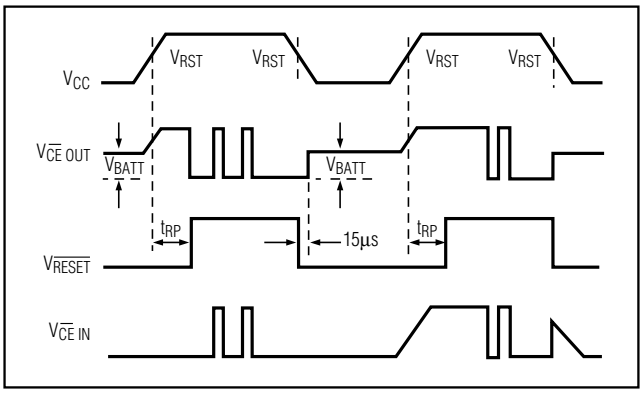


Figure 6. Chip-Enable Timing

Any time a reset is generated, the CE transmission gate remains disabled and $\overline{CE}$ IN remains high impedance (regardless of $\overline{CE}$ IN activity) for the reset timeout period. When the CE transmission gate is enabled, the impedance of $\overline{CE}$ IN appears as a 40Ω resistor in series with the load at $\overline{CE}$ OUT. The propagation delay through the CE transmission gate depends on V_{CC}, the source impedance of the drive connected to $\overline{CE}$ IN, and the loading on $\overline{CE}$ OUT (see *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and a 50pF load capacitance (Figure 7). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT and use a low-output-impedance driver.

Chip-Enable Output (MAX818)

When the CE transmission gate is enabled, the impedance of $\overline{CE}$ OUT is equivalent to a 40Ω resistor in series with the source driving $\overline{CE}$ IN. In the disabled mode, the transmission gate is off and an active pull-up connects $\overline{CE}$ OUT to OUT (Figure 5). This pull-up turns off when the transmission gate is enabled.

Power-Fail Comparator (MAX817/MAX819)

The MAX817/MAX819 PFI input is compared to an internal reference. If PFI is less than the power-fail threshold (V_{PFT}), $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply (Figure 8). However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

The power-fail comparator turns off and $\overline{PFO}$ goes low when V_{CC} falls below V_{BATT}. During the reset timeout period (t_{RP}), $\overline{PFO}$ is forced high, regardless of the state of V_{PFI} (see *Battery Freshness Seal* section). If the comparator is unused, connect PFI to ground and leave $\overline{PFO}$ unconnected. $\overline{PFO}$ can be connected to $\overline{MR}$ on the MAX819 so that a low voltage on PFI will generate a reset (Figure 9). In this configuration, when the monitored voltage causes PFI to fall below V_{PFT}, $\overline{PFO}$ pulls $\overline{MR}$ low, causing a reset to be asserted. Reset remains asserted as long as $\overline{PFO}$ holds $\overline{MR}$ low, and for t_{RP} (200ms) after $\overline{PFO}$ pulls $\overline{MR}$ high when the monitored supply is above the programmed threshold. When $\overline{PFO}$ is connected to $\overline{MR}$, it is not possible to enable the battery freshness seal. Enabling the battery freshness seal requires $\overline{MR}$ to be high or open. Once the battery freshness seal is enabled, it is no longer affected by $\overline{PFO}$'s connection to $\overline{MR}$.

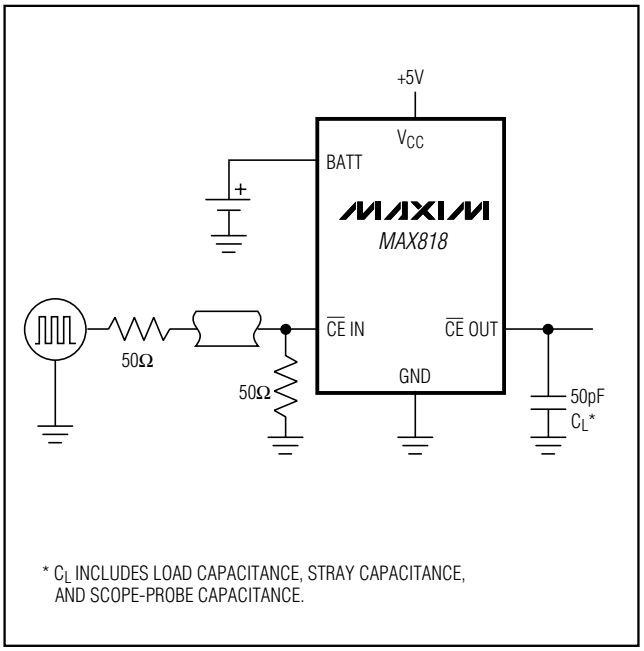


Figure 7. CE Propagation Delay Test Circuit

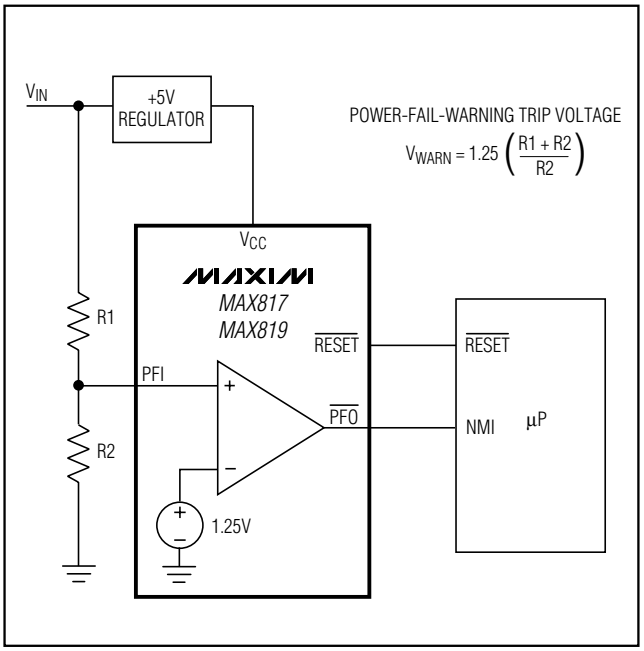


Figure 8. Using the Power-Fail Comparator to Generate a Power-Fail Warning

Backup-Battery Switchover

In a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at BATT, the MAX817/MAX818/MAX819 automatically switch RAM to backup power when V_{CC} falls. These devices require two conditions before switching to battery-backup mode: 1) V_{CC} must be below the reset threshold, and 2) V_{CC} must be below V_{BATT}. Table 1 lists the status of the inputs and outputs in battery-backup mode.

As long as V_{CC} exceeds the reset threshold, OUT connects to V_{CC} through a 5Ω PMOS power switch. Once V_{CC} falls below the reset threshold, V_{CC} or V_{BATT} (whichever is higher) switches to OUT. When V_{CC} falls below V_{RST} and V_{BATT}, BATT switches to OUT through an 80Ω switch.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}.
V_{OUT}	Connected to V_{BATT} through an internal 80Ω PMOS switch.
V_{BATT}	Connected to V_{OUT}. Current drawn from the battery is less than 1µA, as long as $V_{CC} < V_{BATT} - 0.2V$.
$V_{\overline{RESET}}$	Logic low
V_{WDI}	Watchdog timer is disabled.
$V_{\overline{CE}OUT}$	Logic high. The open-circuit voltage is equal to V_{OUT}.
$V_{\overline{CE}IN}$	High impedance

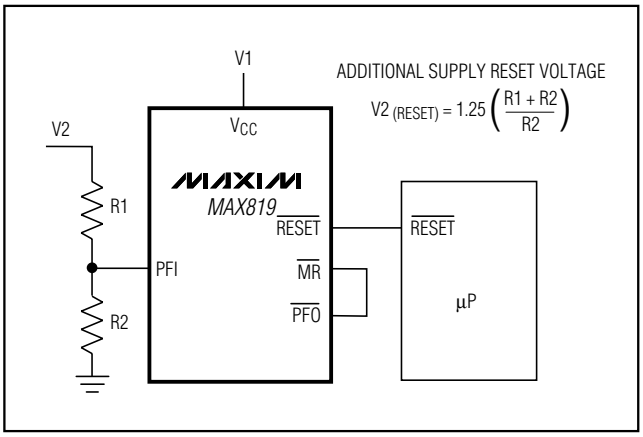
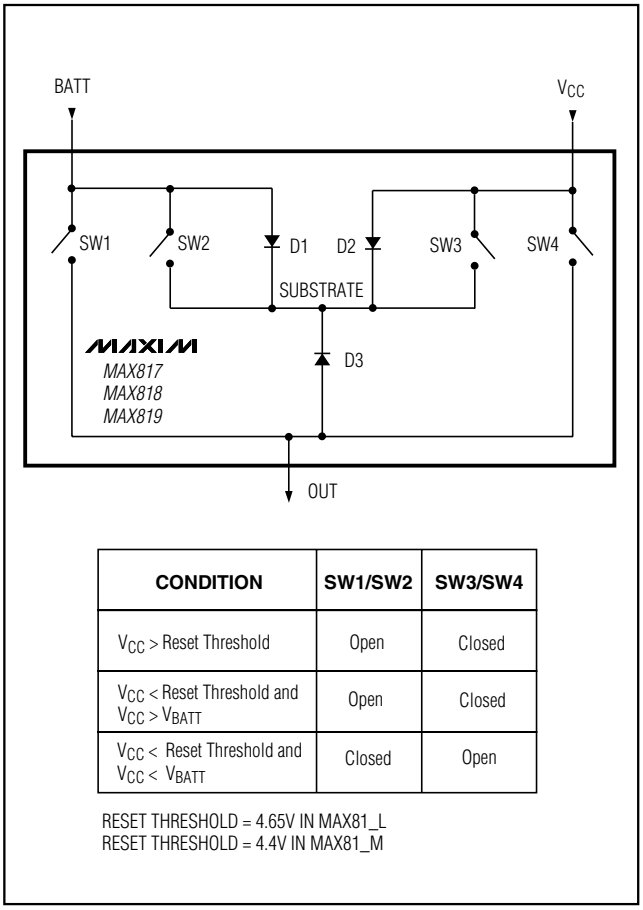


Figure 9. Monitoring an Additional Supply by Connecting $\overline{PFO}$ to $\overline{MR}$.

When V_{CC} exceeds the reset threshold, it is connected to the substrate, regardless of the voltage applied to BATT (Figure 10). During this time, the diode (D1) between BATT and the substrate will conduct current from BATT to V_{CC} if V_{BATT} is 0.6V greater than V_{CC}. When BATT connects to OUT, backup mode is activated and the internal circuitry is powered from the battery (Table 1). When V_{CC} is just below V_{BATT}, the current draw from BATT is typically 6µA. When V_{CC} drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Applications Information

The MAX817/MAX818/MAX819 are protected for typical short-circuit conditions of 10sec or less. Shorting OUT to ground for longer than 10sec destroys the device. Decouple V_{CC}, OUT, and BATT to ground by placing 0.1µF capacitors as close to the device as possible.



CONDITION	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and $V_{CC} > V_{BATT}$	Open	Closed
V_{CC} < Reset Threshold and $V_{CC} < V_{BATT}$	Closed	Open

RESET THRESHOLD = 4.65V IN MAX81_L
RESET THRESHOLD = 4.4V IN MAX81_M

Figure 10. Backup-Battery-Switchover Block Diagram

Watchdog Input Current

The MAX817/MAX818 WDI inputs are internally driven through a buffer and series resistor from the watchdog counter (Figure 1). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within 7/8 of the watchdog timeout period to reset the watchdog timer. If instead WDI is externally driven high for the majority of the timeout period, up to 150µA can flow into WDI.

Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values (on the order of 0.47F) for their size. Since BATT has the same operating voltage range as V_{CC}, and the battery switchover threshold voltages are typically ±30mV centered at V_{BATT}, a SuperCap and simple charging circuit can be used as a backup power source. Figure 11 shows a SuperCap used as a backup source.

If V_{CC} is above the reset threshold and V_{BATT} is 0.5V above V_{CC}, current flows to OUT and V_{CC} from BATT until the voltage at BATT is less than 0.5V above V_{CC}. For example, if a SuperCap is connected to BATT through a diode to V_{CC}, and V_{CC} quickly changes from 5.4V to 4.9V, the capacitor discharges through OUT and V_{CC} until V_{BATT} reaches 5.1V typical. Leakage current through the SuperCap charging diode and the internal power diode eventually discharges the SuperCap to V_{CC}. Also, if V_{CC} and V_{BATT} start from 0.1V above the reset threshold and power is lost at V_{CC}, the SuperCap on BATT discharges through V_{CC} until V_{BATT} reaches the reset threshold. Battery-backup mode is then initiated and the current through V_{CC} goes to zero.

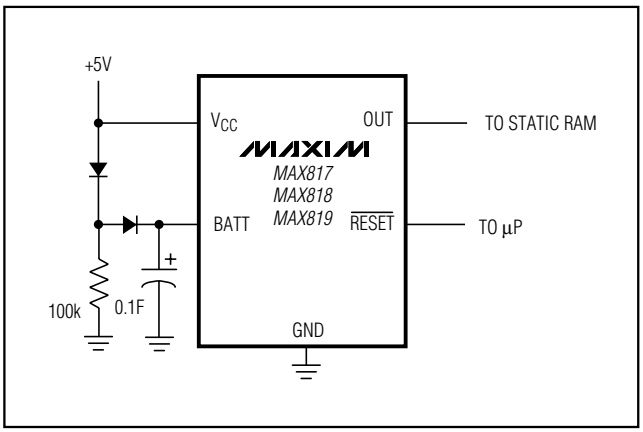


Figure 11. Using a SuperCap™ as a Backup Power Source with a +5V ±10% Supply

SuperCap is a trademark of Baknor Industries.

Operation Without a Backup Power Source

The MAX817/MAX818/MAX819 were designed for battery-backed applications. If a backup battery is not used, connect V_{CC} to OUT, and connect BATT to ground.

Replacing the Backup Battery

The backup power source can be removed while V_{CC} remains valid, without danger of triggering a reset pulse, if BATT is decoupled with a 0.1µF capacitor to ground. As long as V_{CC} stays above the reset threshold, battery-backup mode cannot be entered.

Adding Hysteresis to the Power-Fail Comparator (MAX817/MAX819)

The power-fail comparator has a typical input hysteresis of 4mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see *Monitoring an Additional Supply*).

For additional noise margin, connect a resistor between $\overline{PFO}$ and PFI, as shown in Figure 12. Select the ratio of R1 and R2 such that PFI sees V_{PFT} when V_{IN} falls to the

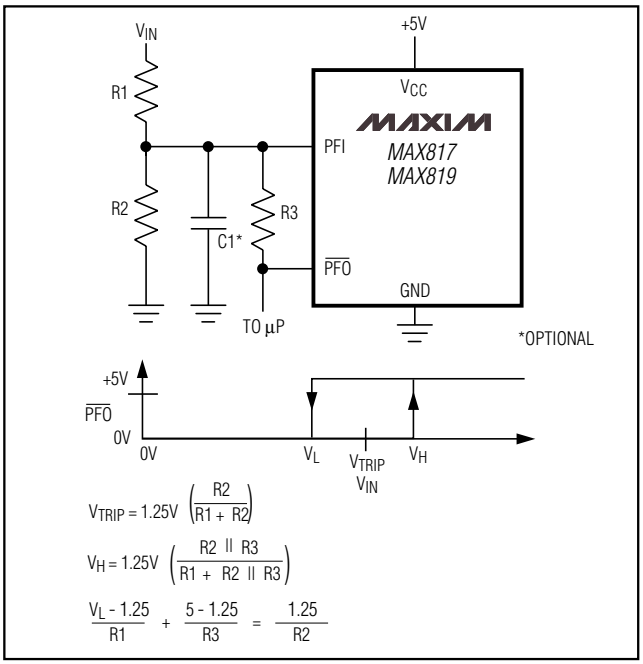


Figure 12. Adding Hysteresis to the Power-Fail Comparator

desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. It will typically be an order of magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input leakage current does not shift the trip point. R3 should be larger than 200kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring an Additional Supply (MAX817/MAX819)

The MAX817/MAX819 µP supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI. $\overline{PFO}$ can be used to generate an interrupt to the µP or to trigger a reset (Figures 9 and 13).

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX817/MAX818/MAX819 $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as in Figure 14. Buffer the $\overline{RESET}$ output to other system components.

Negative-Going V_{CC} Transients

These supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches) while issuing a reset to the µP during power-up, power-down, and brownout conditions. Therefore, resetting the µP when V_{CC} experiences only small glitches is usually not desirable.

The *Typical Operating Characteristics* show a graph of Maximum Transient Duration vs. Reset Threshold Overdrive for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 135µs will not trigger a reset pulse.

A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

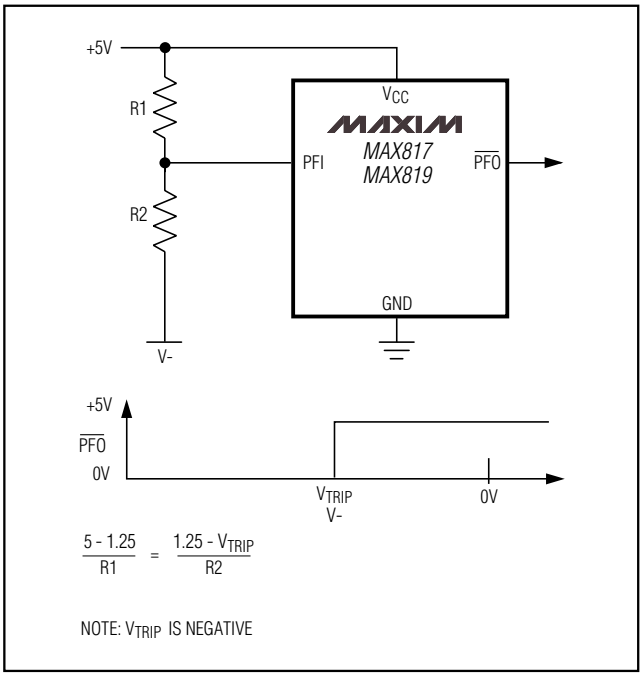


Figure 13. Monitoring a Negative Voltage

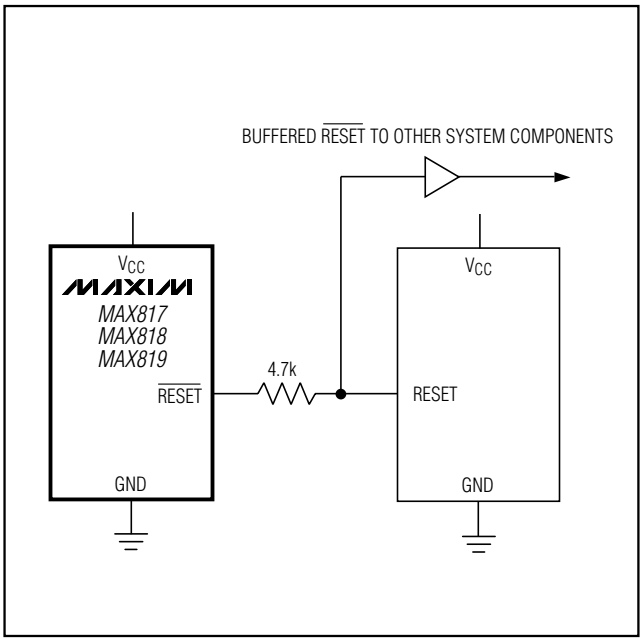


Figure 14. Interfacing to µPs with Bidirectional Reset I/O

Watchdog Software Considerations (MAX817/MAX818)

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop, in which the watchdog timer would continue to be reset within the loop, keeping the watchdog from timing out. Figure 15 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, triggering a reset or an interrupt. As described in the *Watchdog Input Current* section, this scheme results in higher average WDI input current than does the method of leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

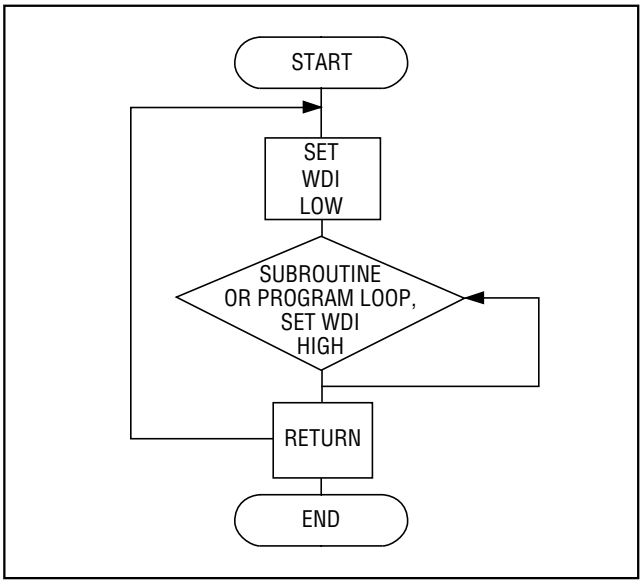
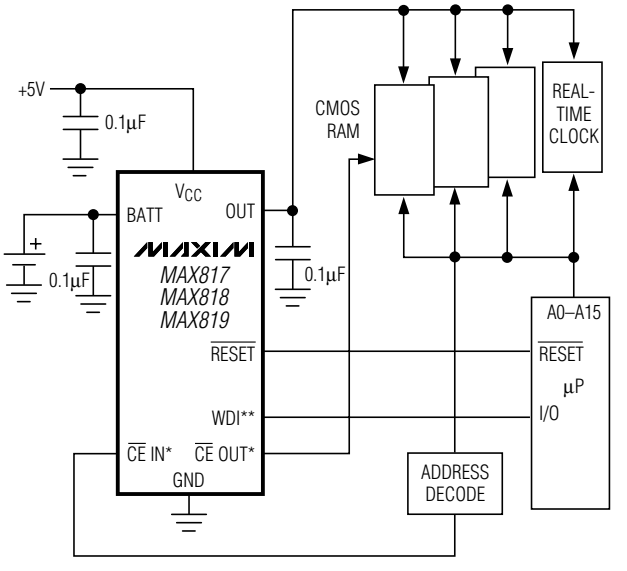


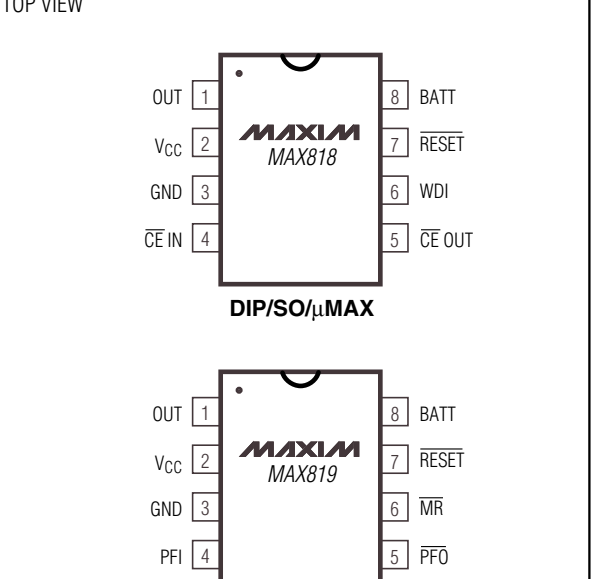
Figure 15. Watchdog Flow Diagram

Typical Operating Circuit



*CE IN AND CE OUT APPLY TO MAX818 ONLY.
**WDI APPLIES TO MAX817/MAX818 ONLY.

Pin Configurations (continued)



+5V Microprocessor Supervisory Circuits

Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE
MAX817_EPA	-40°C to +85°C	8 Plastic DIP
MAX817_ESA	-40°C to +85°C	8 SO
MAX818_CPA	0°C to +70°C	8 Plastic DIP
MAX818_CSA	0°C to +70°C	8 SO
MAX818_CUA	0°C to +70°C	8 µMAX
MAX818_EPA	-40°C to +85°C	8 Plastic DIP
MAX818_ESA	-40°C to +85°C	8 SO
MAX819_CPA	0°C to +70°C	8 Plastic DIP
MAX819_CSA	0°C to +70°C	8 SO
MAX819_CUA	0°C to +70°C	8 µMAX
MAX819_EPA	-40°C to +85°C	8 Plastic DIP
MAX819_ESA	-40°C to +85°C	8 SO

†*These parts offer a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.*

Devices are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering.

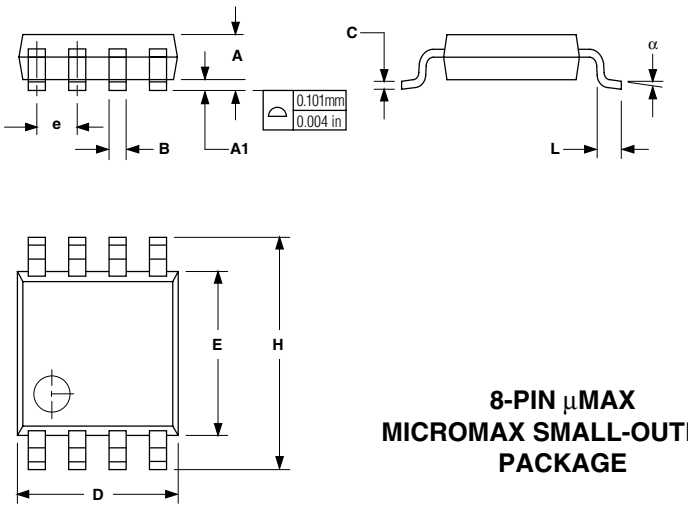
SUFFIX	RESET THRESHOLD (V)
L	4.65
M	4.40

Chip Information

TRANSISTOR COUNT: 719

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

21-0036D

8-PIN µMAX
MICROMAX SMALL-OUTLINE
PACKAGE

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