Hi-Speed USB 2.0 Switches with ±15kV ESD

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_{CC}, COM_, NO_, NC_, EN, $\overline{EN}$, CB ..... -0.3V to +6.0V
Continuous Current into Any Terminal ..... ±30mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin UTQFN (derate 6.9mW/°C above +70°C)..... 559mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
10-Pin UTQFN .....20.1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
10-Pin UTQFN ..... 143.1°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature Range ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.8V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Power-Supply Range	V_{CC}			2.8		5.5	V
Supply Current	I_{CC}	V_{CB} = 0V or V_{CC}, $V_{\overline{EN}}$ = 0V or V_{EN} = V_{CC}	V_{CC} = 3.0V		0.6	1.5	µA
			V_{CC} = 5.5V		3	6.5	
Shutdown Supply Current	I_{SHDN}	Switch disabled ($V_{\overline{EN}}$ = V_{CC} or V_{EN} = 0V)			0.1		µA
Increase in Supply Current with V_{CB}, V_{EN} Voltage		0 ≤ V_{CB} ≤ V_{IL} or V_{IH} ≤ V_{CB} ≤ V_{CC} or 0 ≤ V_{EN} ≤ V_{IL} or V_{IH} ≤ V_{EN} ≤ V_{CC}				2	µA
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}	V_{EN} = V_{CC} or $V_{\overline{EN}}$ = 0V (Note 3)		0		V_{CC}	V
Fault-Protection Trip Threshold	V_{FP}	COM_ only, T_A = +25°C		V_{CC} + 0.6	V_{CC} + 0.8	V_{CC} + 1	V
On-Resistance	R_{ON}	V_{COM} = 0V to V_{CC}			5	10	Ω
		V_{COM} = 3.6V, V_{CC} = 3.0V			5.5		
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = 3.0V, V_{COM} = 2V (Note 4)			0.1	1	Ω
On-Resistance Flatness	R_{FLAT}	V_{CC} = 3.0V, V_{COM} = 0V to V_{CC} (Note 5)			0.1		Ω
Off-Leakage Current	$I_{COM(OFF)}$	V_{CC} = 4.5V, V_{COM} = 0V or 4.5V, V_{NO}, V_{NC} = 4.5V or 0V		-250		+250	nA
		V_{CC} = 5.5V, V_{COM} = 0V or 5.5V, V_{NO}, V_{NC} with 50µA sink current to GND				180	µA
On-Leakage Current	$I_{COM(ON)}$	V_{CC} = 5.5V, V_{COM} = 0V or 5.5V, V_{NO}, V_{NC} = unconnected		-250		+250	nA
AC PERFORMANCE							
On-Channel -3dB Bandwidth	BW	R_L = R_S = 50Ω, signal = 0dBm			950		MHz
Off-Isolation	V_{ISO}	V_{NO}, V_{NC} = 0dBm, R_L = R_S = 50Ω (Figure 1)	f = 10MHz		-48		dB
			f = 250MHz		-20		
			f = 500MHz		-17		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.8V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk (Note 6)	V_{CT}	V_{NO}, V_{NC} = 0dBm, R_L = R_S = 50Ω, Figure 1	f = 10MHz		-73		dB
			f = 250MHz		-54		
			f = 500MHz		-33		
LOGIC INPUT							
Input Logic-High	V_{IH}			1.4			V
Input Logic-Low	V_{IL}					0.5	V
Input Leakage Current	I_{IN}			-250		+250	nA
DYNAMIC							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, $V_{\overline{EN}}$ = V_{CC} to 0V or V_{EN} = 0V to V_{CC} (Figure 2)			20	100	µs
Turn-Off Time	t_{OFF}	V_{NO} or V_{NC} = 1.5V, R_L = 300Ω, C_L = 35pF, V_{EN} = V_{CC} to 0V or $V_{\overline{EN}}$ = 0V to V_{CC} (Figure 2)			1	5	µs
Propagation Delay	t_{PLH}, t_{PHL}	R_L = R_S = 50Ω, Figure 3			100		ps
Fault Protection Response Time	t_{FP}	V_{COM} = 0V to 5V step, R_L = R_S = 50Ω, V_{CC} = 3.3V (Figure 4)		0.5		5.0	µs
Fault Protection Recovery Time	t_{FPR}	V_{COM} = 5V to 0V step, R_L = R_S = 50Ω, V_{CC} = 3.3V (Figure 4)				100	µs
Output Skew Between Switches	t_{SK}	Skew between switch 1 and 2, R_L = R_S = 50Ω, (Figure 3, Note 7)			40		ps
NO_ or NC_ Off-Capacitance	$C_{NO(OFF)}$ or $C_{NC(OFF)}$	f = 1MHz (Figure 5, Note 7)			2		pF
COM Off-Capacitance (Figure 5, Note 7)	$C_{COM(OFF)}$	f = 1MHz			5.5		pF
		f = 240MHz			4.8		
COM On-Capacitance (Figure 5, Note 7)	$C_{COM(ON)}$	f = 1MHz			6.5		pF
		f = 240MHz			5.5		
Total Harmonic Distortion Plus Noise	THD+N	V_{COM} = 1V_{P-P}, V_{BIAS} = 1V, R_L = R_S = 50Ω, f = 20Hz to 20kHz			0.03		%
ESD PROTECTION							
COM1, COM2		Human Body Model			±15		kV
		IEC 61000-4-2 Air-Gap Discharge			±15		
		IEC 61000-4-2 Contact Discharge			±8		
All Pins		Human Body Model			±2		

Note 2: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: The switch turns off for voltages above V_{FP}, protecting downstream circuits in case of a fault condition.
Note 4: $\Delta R_{ON(MAX)} = ABS(R_{ON(CH1)} - R_{ON(CH2)})$.
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.
Note 6: Between any two switches.
Note 7: Switch off-capacitance, switch on-capacitance, and output skew between switches are not production tested; guaranteed by design.

Hi-Speed USB 2.0 Switches with ±15kV ESD

Test Circuits/Timing Diagrams

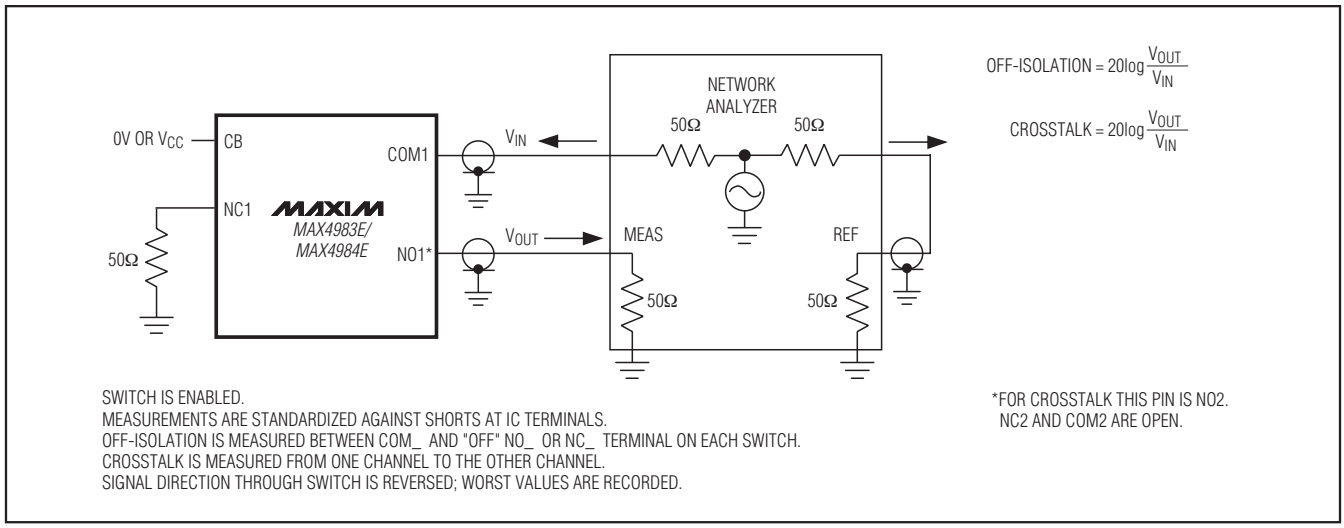


Figure 1. Off-Isolation and Crosstalk

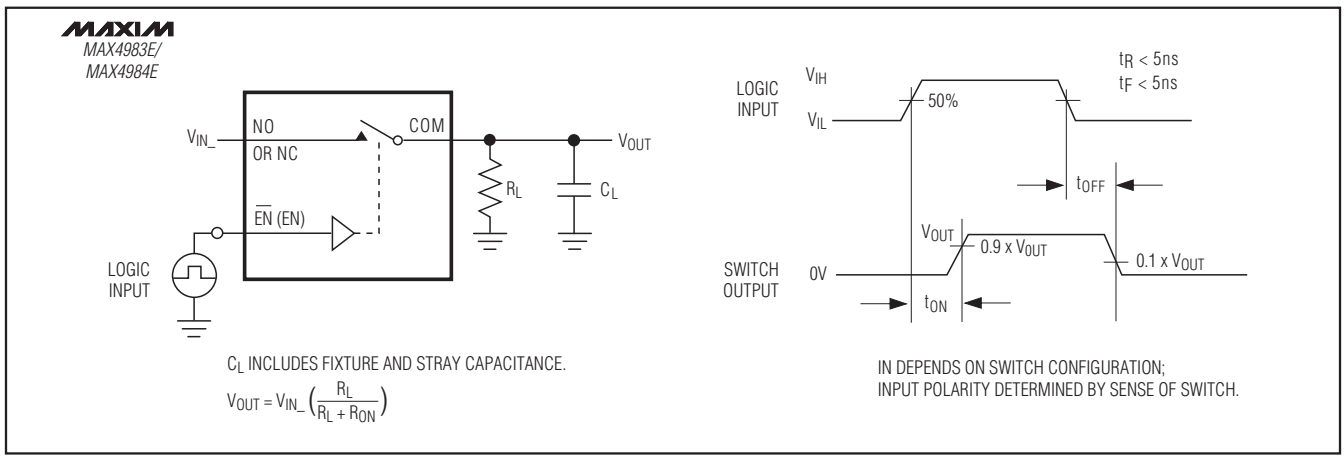


Figure 2. Switching Time

Test Circuits/Timing Diagrams (continued)

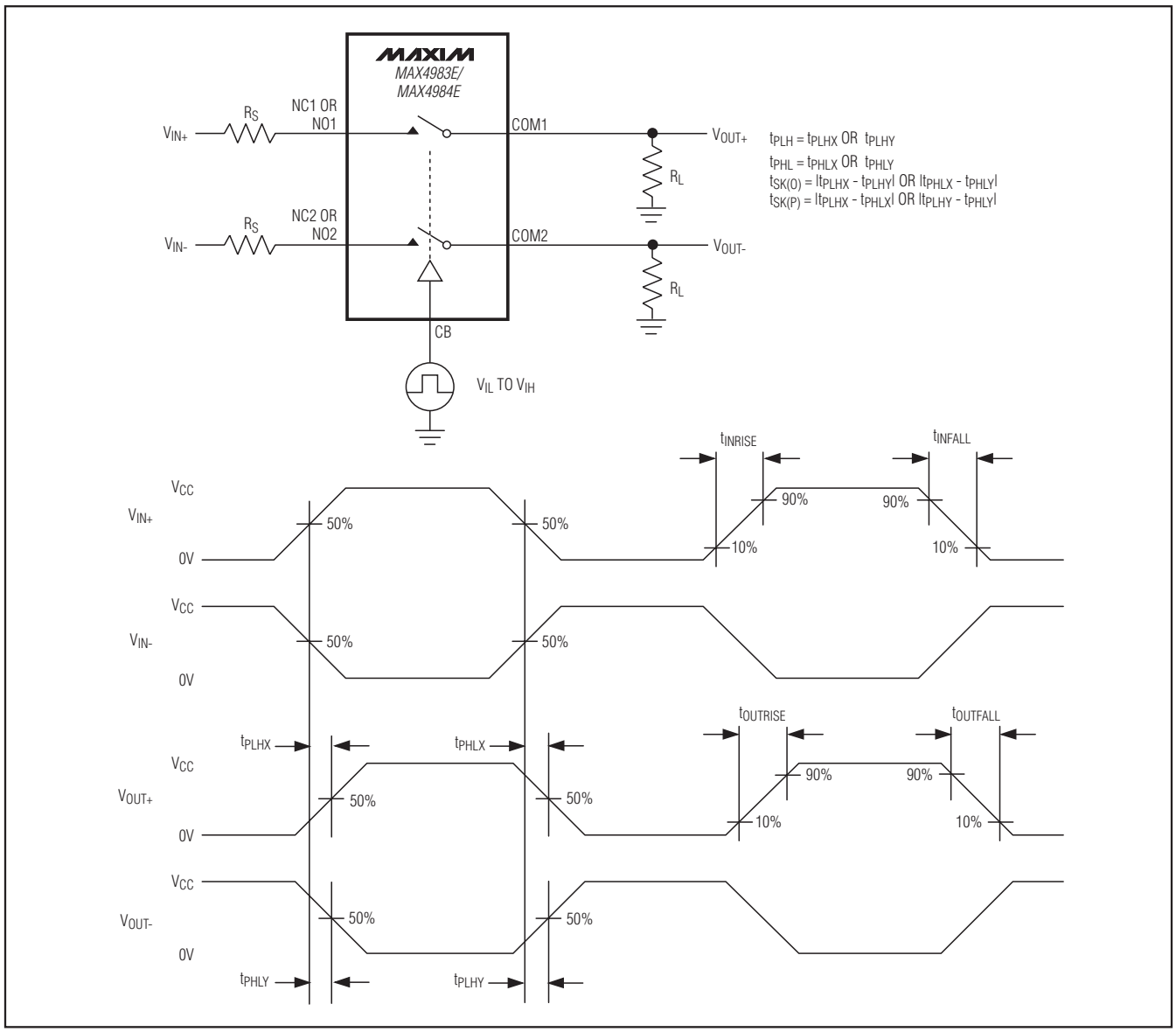


Figure 3. Output Signal Skew, Rise/Fall Time, Propagation Delay

Hi-Speed USB 2.0 Switches with ±15kV ESD

Test Circuits/Timing Diagrams (continued)

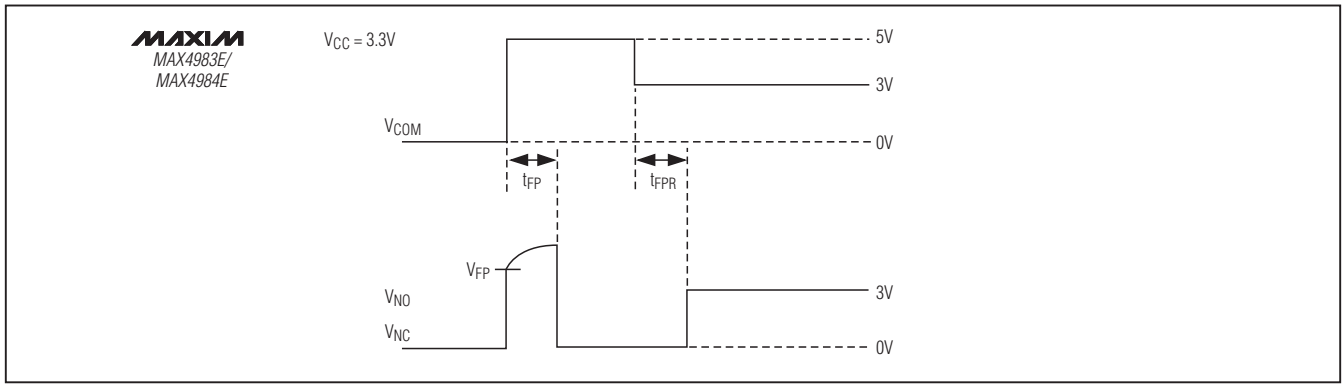


Figure 4. Fault-Protection Response/Recovery Time

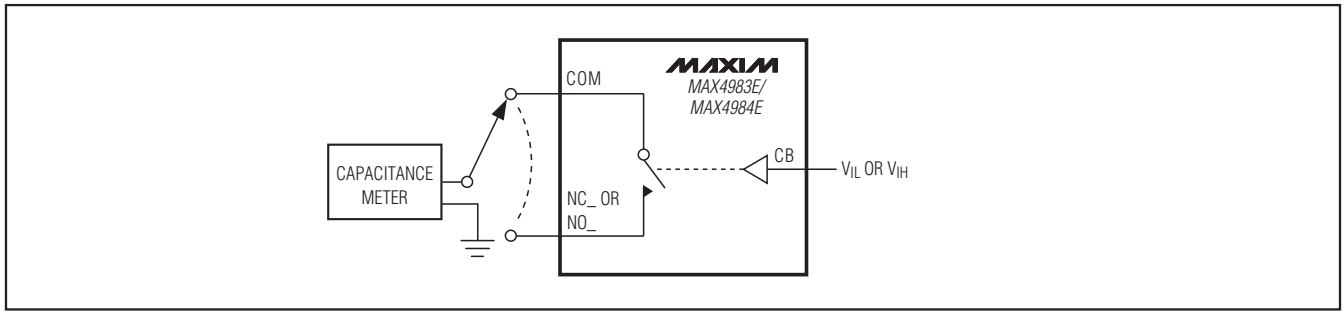
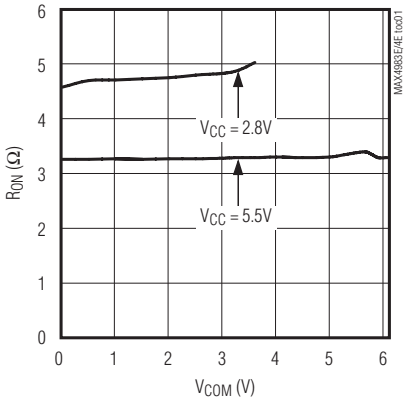


Figure 5. Channel Off-/On-Capacitance

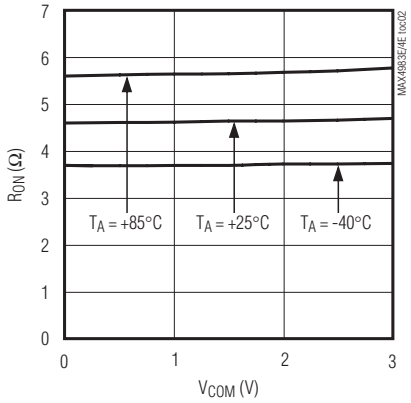
Typical Operating Characteristics

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

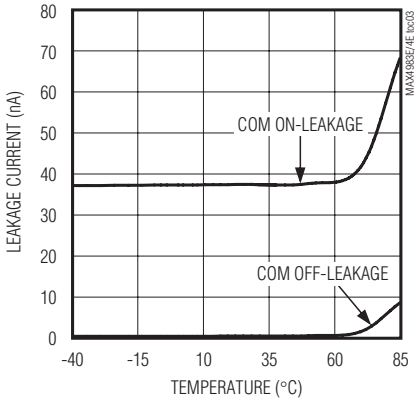
ON-RESISTANCE vs. V_{COM}



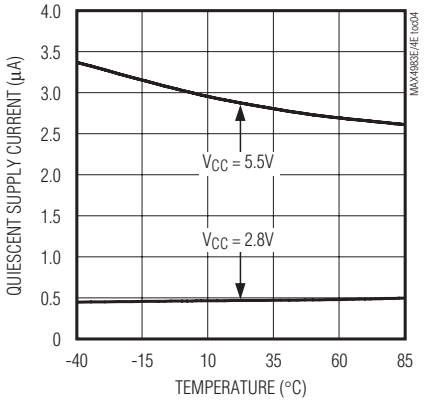
ON-RESISTANCE vs. V_{COM}



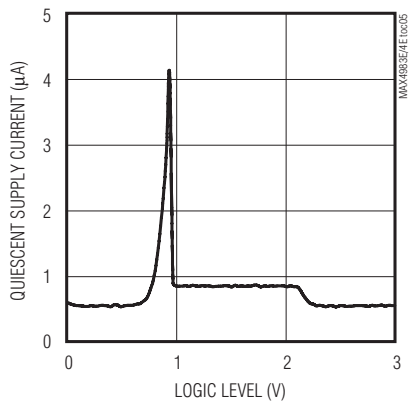
COM LEAKAGE CURRENT vs. TEMPERATURE



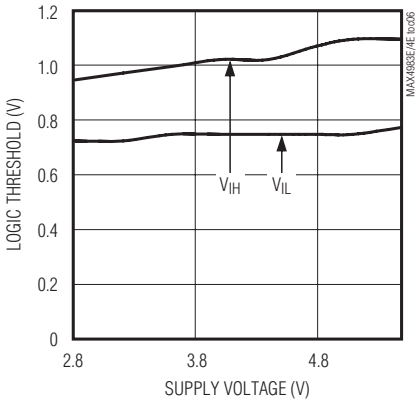
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



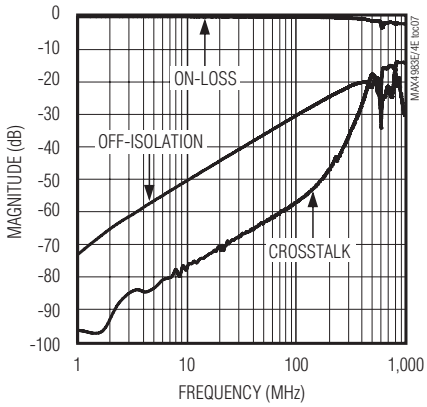
QUIESCENT SUPPLY CURRENT vs. LOGIC LEVEL



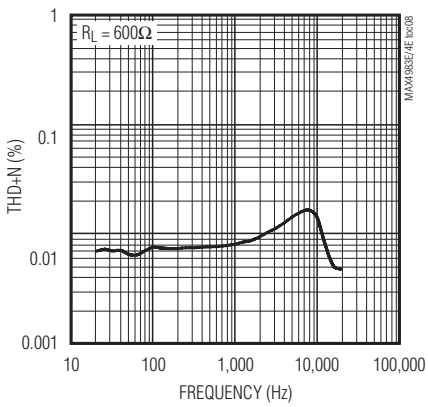
LOGIC-INPUT THRESHOLD vs. SUPPLY VOLTAGE



FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



Hi-Speed USB 2.0 Switches with ±15kV ESD

Pin Description

PIN		NAME	FUNCTION
MAX4983E	MAX4984E		
1	1	NC1	Normally Closed Terminal for Switch 1
2	2	NO1	Normally Open Terminal for Switch 1
3	3	COM1	Common Terminal for Switch 1
4	4	GND	Ground
5	5	COM2	Common Terminal for Switch 2
6	6	NO2	Normally Open Terminal for Switch 2
7	7	NC2	Normally Closed Terminal for Switch 2
8	—	$\overline{EN}$	Active-Low Enable Input. Drive $\overline{EN}$ high to put switches in high impedance. Drive $\overline{EN}$ low for normal operation.
—	8	EN	Active-High Enable Input. Drive EN low to put switches in high impedance. Drive EN high for normal operation.
9	9	V_{CC}	Positive Supply Voltage Input. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor as close as possible to the device.
10	10	CB	Digital Control Input. Drive CB low to connect COM_ to NC_. Drive CB high to connect COM_ to NO_.

Detailed Description

The MAX4983E/MAX4984E are ±15kV ESD-protected DPDT analog switches. The devices are ideal for USB 2.0 Hi-Speed (480Mbps) switching applications and also meet USB low- and full-speed requirements.

The MAX4983E/MAX4984E are fully specified to operate from a single +2.8V to +5.5V supply. The low V_{IH} threshold of the devices permits them to be used with logic levels as low as 1.4V. The MAX4983E/MAX4984E are based on a charge-pump-assisted n-channel architecture. The devices feature a shutdown mode to reduce the quiescent current to less than 0.1µA (typ).

Digital Control Input

The MAX4983E/MAX4984E provide a single-bit control logic input, CB. CB controls the position of the switches as shown in the *Functional Diagram/Truth Table*. Driving CB rail-to-rail minimizes power consumption. With a +2.8V to +5.5V supply voltage range, the device is +1.4V logic compatible.

Analog Signal Levels

The on-resistance of the MAX4983E/MAX4984E is very low and stable as the analog input signals are swept from ground to V_{CC} (see the *Typical Operating Characteristics*). These switches are bidirectional, allowing NO_, NC_, and COM_ to be configured as either inputs or outputs. The charge-pump-assisted n-channel architecture allows the switch to pass analog signals that exceed V_{CC} up to the overvoltage fault protection threshold. This allows USB signals that exceed V_{CC} to pass, allowing compliance with USB requirements for voltage levels.

Overvoltage Fault Protection

The MAX4983E/MAX4984E feature overvoltage fault protection on COM_. Fault protection protects the switch and USB transceiver from damaging voltage levels. When voltages on COM exceed the fault protection threshold, (V_{FP}), COM_, NC_ and NO_ are high impedance.

Enable Input

The MAX4983E/MAX4984E feature a shutdown mode that reduces the supply current to less than 0.1µA and places COM_ in high impedance. Drive $\overline{EN}$ high for the MAX4983E or EN low for the MAX4984E to place the devices in shutdown mode. When $\overline{EN}$ is driven low or EN is driven high, the devices are in normal operation.

Applications Information

USB Switching

The MAX4983E/MAX4984E analog switches are fully compliant with the USB 2.0 specification. The low on-resistance and low on-capacitance of these switches make them ideal for high-performance switching applications.

The MAX4983E/MAX4984E are ideal for routing USB data lines (see Figure 6) and for applications that require switching between multiple USB hosts (see Figure 7). The MAX4983E/MAX4984E also feature overvoltage fault protection to guard systems against shorts to the USB VBUS voltage that is required for all USB applications.

Extended ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. COM1 and COM2 are further protected against static electricity. The ESD structures withstand high ESD in normal operation and when the device is powered down. After an ESD event, the MAX4983E/MAX4984E continue to function without latchup.

The MAX4983E and MAX4984E are characterized for protection to the following limits:

- ±15kV using Human Body Model
- ±8kV using IEC 61000-4-2 Contact Discharge method
- ±15kV using IEC 61000-4-2 Air-Gap Discharge method

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 8a shows the Human Body Model and Figure 8b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 61000-4-2

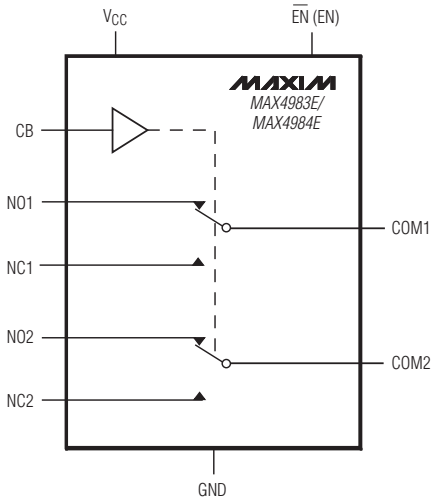
The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 9a), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 9b shows the current waveform for the ±8kV IEC 61000-4-2 Level 4 ESD Contact Discharge test.

The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Layout

USB Hi-Speed requires careful PCB layout with 45Ω controlled-impedance matched traces of equal lengths.

Functional Diagram/Truth Table



MAX4983E				
$\overline{EN}$	CB	NO_	NC_	COM_
0	0	OFF	ON	—
0	1	ON	OFF	—
1	X	OFF	OFF	HI-Z

X = DON'T CARE.

MAX4984E				
EN	CB	NO_	NC_	COM_
1	0	OFF	ON	—
1	1	ON	OFF	—
0	X	OFF	OFF	HI-Z

X = DON'T CARE.

Ensure that bypass capacitors are as close as possible to the device. Use large ground planes where possible.

Power-Supply Sequencing

Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the device.

Proper power-supply sequencing is recommended for all devices. Always apply V_{CC} before applying analog signals, especially if the analog signal is not current limited.

Chip Information

PROCESS: BiCMOS

Hi-Speed USB 2.0 Switches with ±15kV ESD

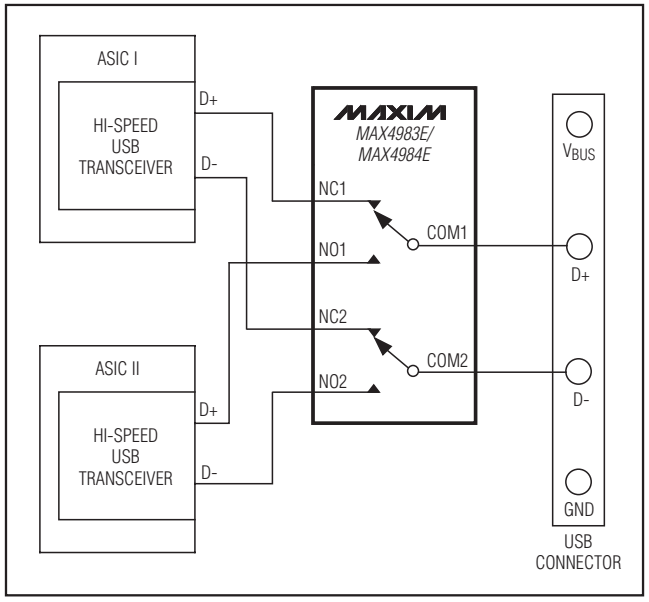


Figure 6. USB Data Routing/Typical Application Circuit

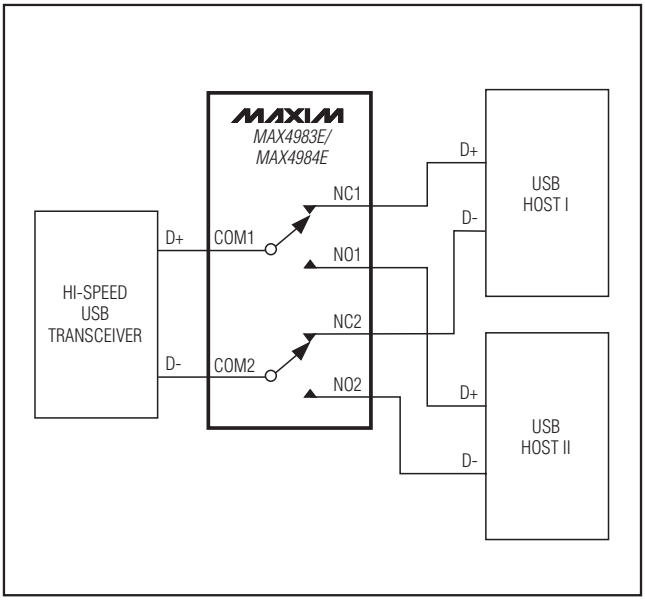


Figure 7. Switching Between Multiple USB Hosts

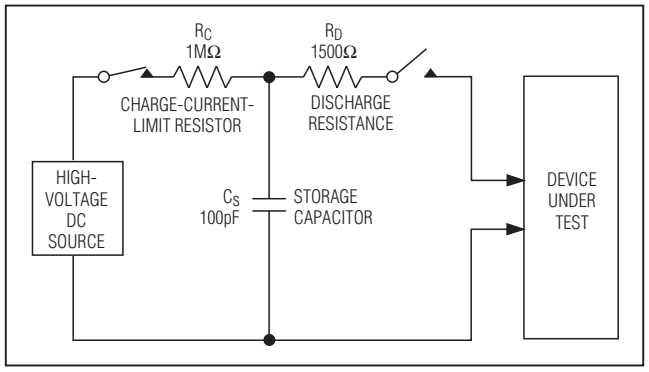


Figure 8a. Human Body ESD Test Model

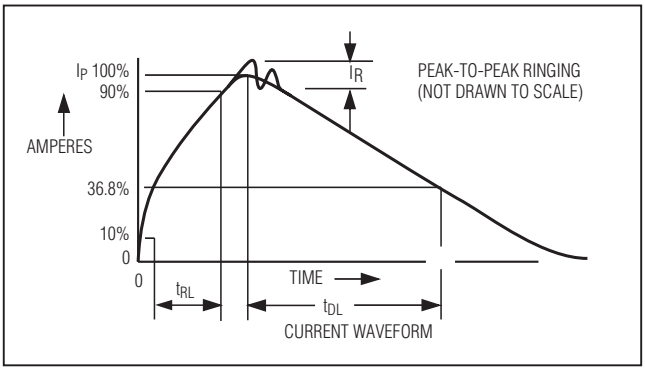


Figure 8b. Human Body Current Waveform

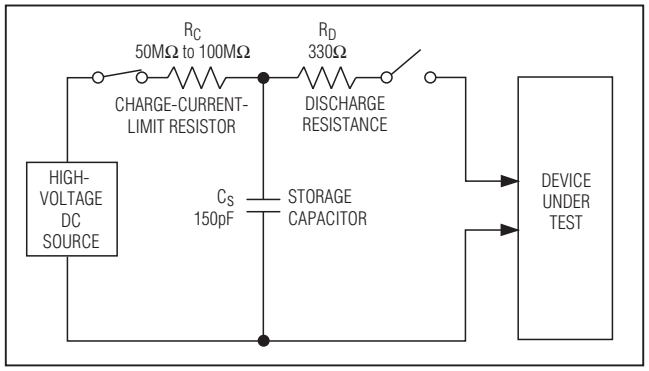


Figure 9a. IEC 61000-4-2 ESD Test Model

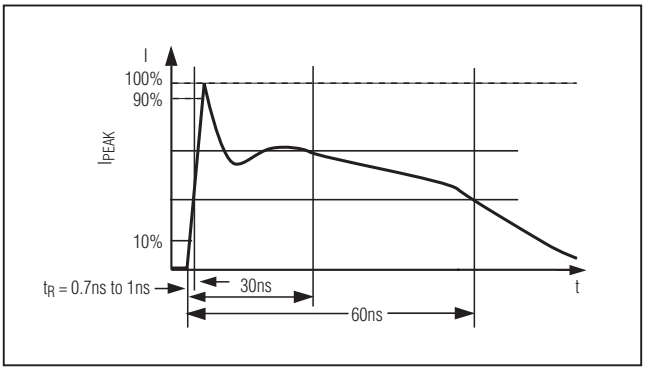


Figure 9b. IEC 61000-4-2 ESD Generator Current Waveform

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10 Ultra-Thin QFN	V101A1CN-1	**21-0028**

Hi-Speed USB 2.0 Switches with ±15kV ESD

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/08	Initial release	—
1	5/08	Removal of future product asterisks, global change to Hi-Speed	1, 8, 9, 10
2	9/08	Changes to EC table	3