Absolute Maximum Ratings

(All voltages referenced to GND.)
V_{CC}, CB_ .....-0.3V to +6.0V
X, X_, Y, Y_ .....(V_{CC} - 6V) to (V_{CC} + 0.3V)
Continuous Current X, X_, Y, Y_.....±300mA
Peak Current X, X_, Y, Y_ (pulsed at 1ms,
50% Duty Cycle).....±400mA
Peak Current X, X_, Y, Y_ (pulsed at 1ms,
10% Duty Cycle).....±500mA

Continuous Power Dissipation (T_A = +70°C)
12-Bump WLP (derate 8.5mW/°C above +70°C).....678mW
14-Pin TDFN, Single-Layer Board
(derate 18.5mW/°C above +70°C) 1482mW
14-Pin TDFN, Multilayer Board
(derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{CC}			1.8		5.5	V
Supply Current	I_{CC}	V_{CC} = +5.5V, $V_{CB\_}$ = 0V or V_{CC}			0.05	2	µA
		V_{CC} = +2.7V, $V_{CB\_}$ = +0.5V or +1.4V				4	
		V_{CC} = +5.5V, $V_{CB\_}$ = +0.5V or +1.4V				8	
ANALOG SWITCH							
Analog Signal Range (Note 2)	$V_{X\_}$, $V_{Y\_}$, V_X, V_Y			V_{CC} - 5.5V		V_{CC}	V
On-Resistance (Note 3)	R_{ON}	V_{CC} = +2.7V; $V_{X\_}$ = $V_{Y\_}$ = V_{CC} - 5.5V; -1V, 0V, +1V, +2V, V_{CC}; $I_{X\_}$ = $I_{Y\_}$ = 100mA	T_A = +25°C		0.38	0.75	Ω
			T_A = T_{MIN} to T_{MAX}			0.8	
On-Resistance Match Between Channels (Notes 3 and 4)	ΔR_{ON}	Between X0 and Y0, X1 and Y1, X2 and Y2; V_{CC} = +2.7V; $V_{X\_}$ or $V_{Y\_}$ = 0V; $I_{X\_}$ = $I_{Y\_}$ = 100mA				0.1	Ω
On-Resistance Flatness (Notes 3 and 5)	R_{FLAT}	V_{CC} = +2.7V; $V_{X\_}$ = $V_{Y\_}$ = V_{CC} - 5.5V, -1V, 0, +1V, +2V, V_{CC}; $I_{X\_}$ = $I_{Y\_}$ = 100mA				0.35	Ω
Shunt Switch Resistance	R_{SH}			2	3.8	6	kΩ
X0, Y0 Off-Leakage Current (MAX4909/MAX4930/MAX4932)	$I_{L(OFF)}$	V_{CC} = +2.7V, switch open, V_{X0} or V_{Y0} = -2.5V or +2.5V, V_X or V_Y = +2.5V or -2.5V	T_A = +25°C	-50		+50	nA
			T_A = T_{MIN} to T_{MAX}	-200		+200	
X1, Y1 Off-Leakage Current (MAX4930/MAX4932)		V_{CC} = +2.7V, switch open, V_{X1} or V_{Y1} = -2.5V or +2.5V, V_X or V_Y = +2.5V or -2.5V	T_A = +25°C	-50		+50	
			T_A = T_{MIN} to T_{MAX}	-200		+200	
X2, Y2 Off-Leakage Current (MAX4932)		V_{CC} = +2.7V, switch open, V_{X2} or V_{Y2} = -2.5V or +2.5V, V_X or V_Y = +2.5V or -2.5V	T_A = +25°C	-50		+50	
			T_A = T_{MIN} to T_{MAX}	-200		+200	
X, Y On-Leakage Current	$I_{L(ON)}$	V_{CC} = +2.7V, switch closed, V_{X0} or V_{Y0} = -2.5V or +2.5V or unconnected, V_X = V_Y = -2.5V or +2.5V or floating	T_A = +25°C	-100		+100	nA
			T_A = T_{MIN} to T_{MAX}	-300		+300	

Electrical Characteristics (continued)

(V_{CC} = +2.7V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.0V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-On Time	t_{ON}	V_{CC} = +2.7V, CB_ = low to high, R_L = 50Ω, C_L = 5pF, Figure 2		1.0		µs
Turn-Off Time	t_{OFF}	V_{CC} = +2.7V, CB_ = high to low, R_L = 50Ω, C_L = 5pF, Figure 2		1.0		µs
Break-Before-Make Delay Time	t_D	V_{CC} = +2.7V, CB_ = low to high or high to low, R_L = 50Ω, C_L = 5pF, Figure 3	1.0	15		ns
Charge Injection	Q	V_X = V_Y = 0V, R_{GEN} = 0Ω, C_L = 1nF, Figure 4		300		pC
Power-Supply Rejection Ratio	PSRR	f_{SW} = 20kHz, V_X or V_Y = $1V_{RMS}$, R_L = 50Ω, C_L = 5pF		60		dB
Off-Isolation	V_{ISO}	f_{SW} = 20kHz, V_X = V_Y = $1V_{RMS}$, R_L = 50Ω, Figure 5 (Note 6)		-80		dB
Crosstalk	V_{CT}	f_{SW} = 20kHz, V_X or V_Y = $1V_{RMS}$, R_L = 50Ω, Figure 5		-70		dB
Total Harmonic Distortion	THD	f_{SW} = 20Hz to 20kHz, V_X or V_Y = $0.5V_{P-P}$, R_L = 50Ω, DC bias = 0		0.02		%
X_, Y_ Off-Capacitance	$C_{X\_(OFF)}$ $C_{Y\_(OFF)}$	f_{SW} = 1MHz, V_X or V_Y = $0.5V_{P-P}$, DC bias = 0, Figure 6		200		pF
X, Y On-Capacitance	$C_{X(ON)}$ $C_{Y(ON)}$	f_{SW} = 1MHz, V_X or V_Y = $0.5V_{P-P}$, DC bias = 0, Figure 6		450		pF
DIGITAL INPUTS (CB_)						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.5	V
Input Leakage Current	I_{CB}	$V_{CB\_}$ = 0V or V_{CC}	-1		+1	µA

Note 1: All parameters are production tested at T_A = +25°C and guaranteed by design over the specified temperature range.

Note 2: Signals on X, Y, X_, or Y_ exceeding V_{CC} are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Note 3: Guaranteed by design; not production tested.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

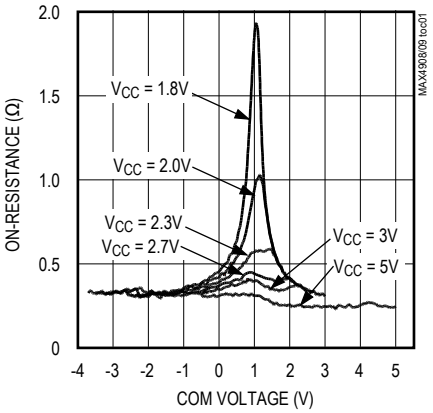
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Note 6: X Off-Isolation = $20\log_{10}$ [V_X / $V_{X\_}$], V_X = output, $V_{X\_}$ = input to off switch. Y Off-Isolation = $20\log_{10}$ [V_Y / $V_{Y\_}$], V_Y = output, $V_{Y\_}$ = input to off switch.

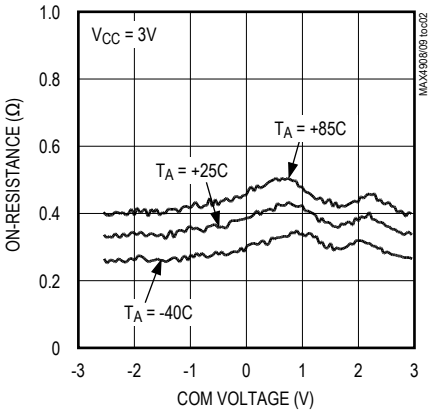
Typical Operating Characteristics

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

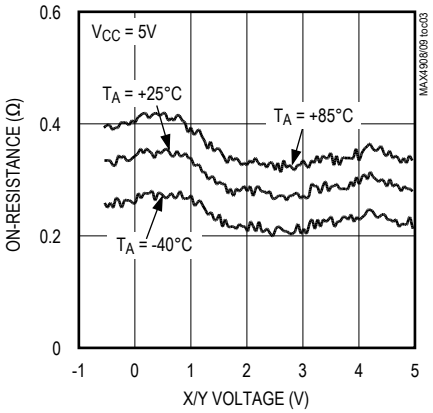
CHANNEL ON-RESISTANCE vs. COM VOLTAGE



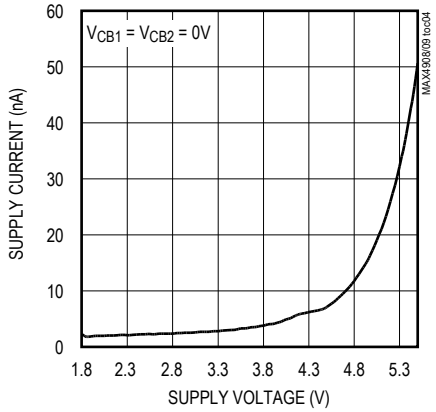
CHANNEL ON-RESISTANCE vs. COM VOLTAGE



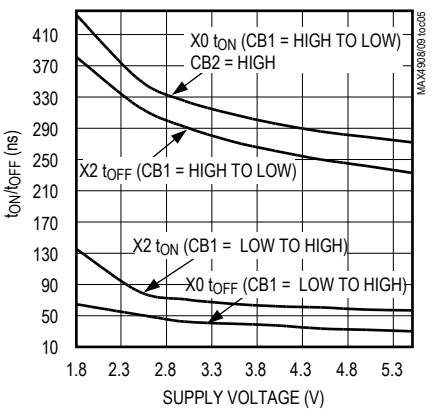
CHANNEL ON-RESISTANCE vs. X/Y VOLTAGE



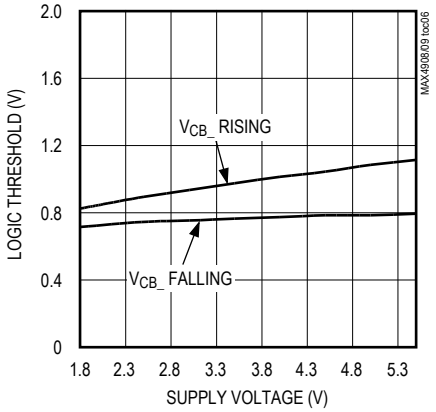
SUPPLY CURRENT vs. SUPPLY VOLTAGE



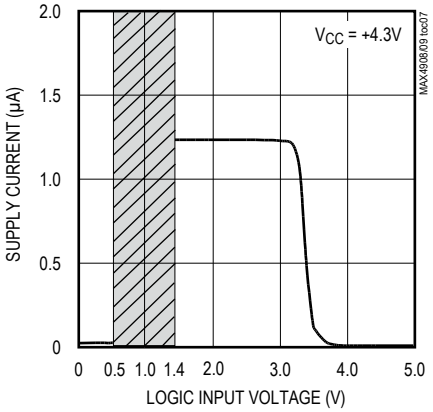
TURN-OFF/TURN-ON TIME vs. SUPPLY VOLTAGE



LOGIC THRESHOLD vs. SUPPLY VOLTAGE



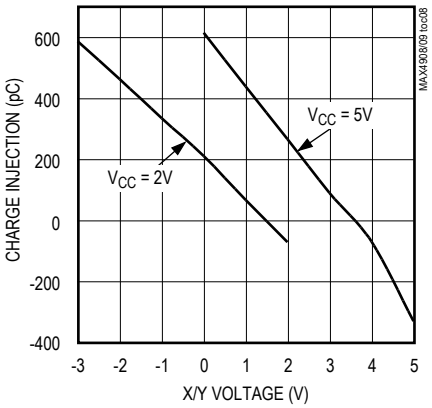
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



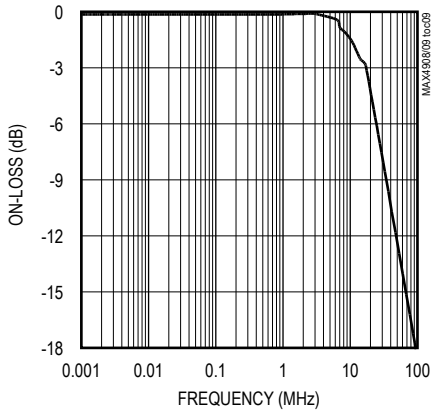
Typical Operating Characteristics (continued)

(V_{CC} = 3.0V, T_A = +25°C, unless otherwise noted.)

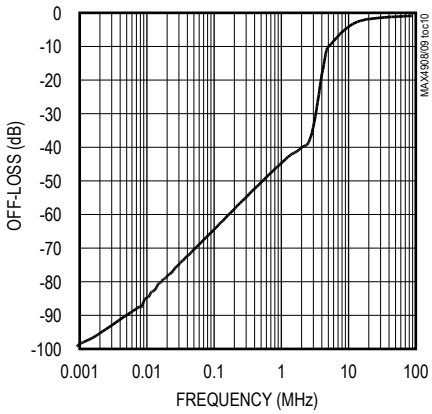
CHARGE INJECTION vs. X/Y COMMON VOLTAGE



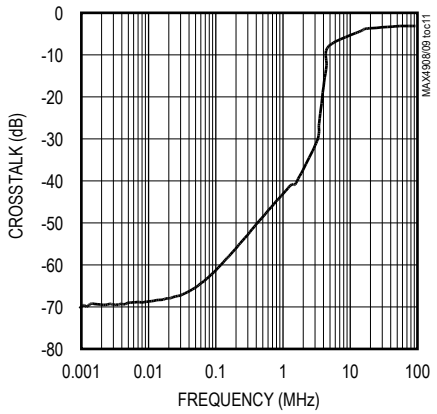
FREQUENCY RESPONSE



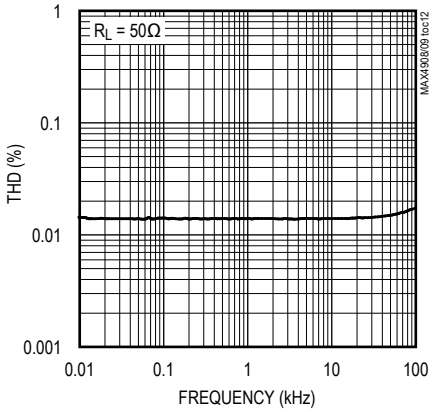
OFF-ISOLATION vs. FREQUENCY



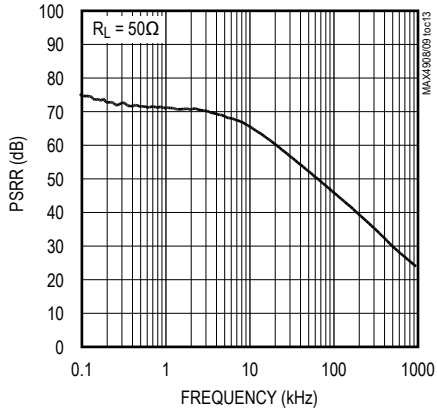
CROSSTALK vs. FREQUENCY



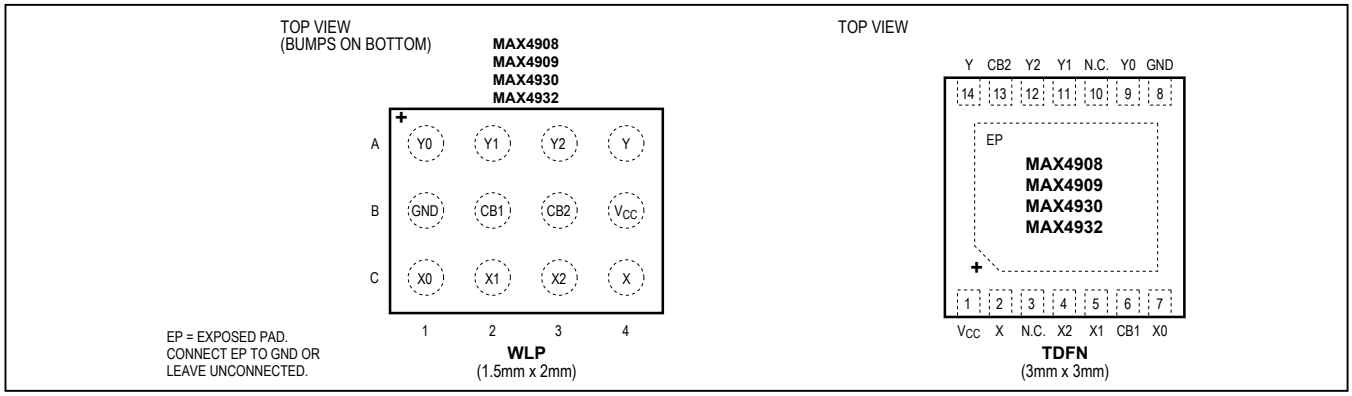
TOTAL HARMONIC DISTORTION vs. FREQUENCY



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



Bump Configurations



Bump Descriptions

PIN		NAME	FUNCTION
TDFN-EP	WLP		
1	B4	V_{CC}	Positive Supply Voltage Input
2	C4	X	Analog Output X Common Terminal
3,10	—	N.C.	No Connection. Not internally connected.
4	C3	X2	Analog Input X2
5	C2	X1	Analog Input X1
6	B2	CB1	Digital Control Input 1
7	C1	X0	Analog Input X0
8	B1	GND	Ground
9	A1	Y0	Analog Input Y0
11	A2	Y1	Analog Input Y1
12	A3	Y2	Analog Input Y2
13	B3	CB2	Digital Control Input 2
14	A4	Y	Analog Output Y Common Terminal
—	—	EP	Exposed Pad. Connect to ground or leave unconnected.

Detailed Description

The MAX4908/MAX4909/MAX4930/MAX4932 dual 3:1 clickless audio multiplexers are low 0.38Ω (typ) on-resistance, low 150nA (typ) supply current, high power-supply rejection ratio (PSRR) devices that operate from a +1.8V to +5.5V single supply. These devices feature a negative signal capability that allows signals below GND to pass through without distortion and break-before-make switching.

The MAX4908/MAX4909/MAX4930/MAX4932 use two digital control bits CB1 and CB2 to switch between signals (see Table 1). The MAX4908 has shunt resistors on all the unselected terminals to suppress click-and-pop sounds that may occur from switching to a precharged terminal. The MAX4909 does not have click-and-pop suppression resistors on X0 and Y0 terminals for applications that do not require predischarge switching. The MAX4930 only has shunt resistors on X2 and Y2 terminals. The MAX4932 has no shunt resistors on all terminals.

Table 1. Truth Table

CB1	CB2	COMMON X	COMMON Y
0	0	High Impedance	High Impedance
0	1	Connected to X0	Connected to Y0
1	0	Connected to X1	Connected to Y1
1	1	Connected to X2	Connected to Y2

Applications Information

Digital Control Inputs

The MAX4908/MAX4909/MAX4930/MAX4932 logic inputs accept up to +5.5V regardless of supply voltage. For example, with a +3.3V supply, CB_ can be driven low to GND and high to +5.5V, allowing for mixing of logic levels in a system. Driving CB_ rail-to-rail minimizes power consumption. For a +3.3V supply voltage, the logic thresholds are +0.5V (low) and +1.4V (high).

Analog Signal Levels

These devices have a low on-resistance of 0.38Ω (typ) and the on-resistance flatness is guaranteed over temperature and will show minimal variation over the entire voltage supply range (see the *Typical Operating Characteristics*). The on-resistance flatness and low-leakage features make it ideal for bidirectional operation. The switches are bidirectional, so X_, Y_, and common terminals X and Y pins can be either inputs or outputs.

These devices pass signals as low as V_{CC} - 5.5V, including signals below ground with minimal distortion.

Click-Pop Suppression

The MAX4908 has a 3.8kΩ (typ) shunt resistor on all of its input terminals to automatically discharge any capacitance when they are not connected to common terminal X and Y. The MAX4909 has shunt resistors on all terminals except X0 and Y0. The MAX4930 only has shunt resistors on X2 and Y2. The shunt resistors reduce audible click-and-pop sounds that occur when switching between audio sources.

Audible clicks and pops are caused when a step DC voltage is switched into the speaker. The DC step transients can be reduced by automatically discharging the side that is not connected to the common terminal, thus reducing any residual DC voltage and clicks and pops.

Break-Before-Make Switching

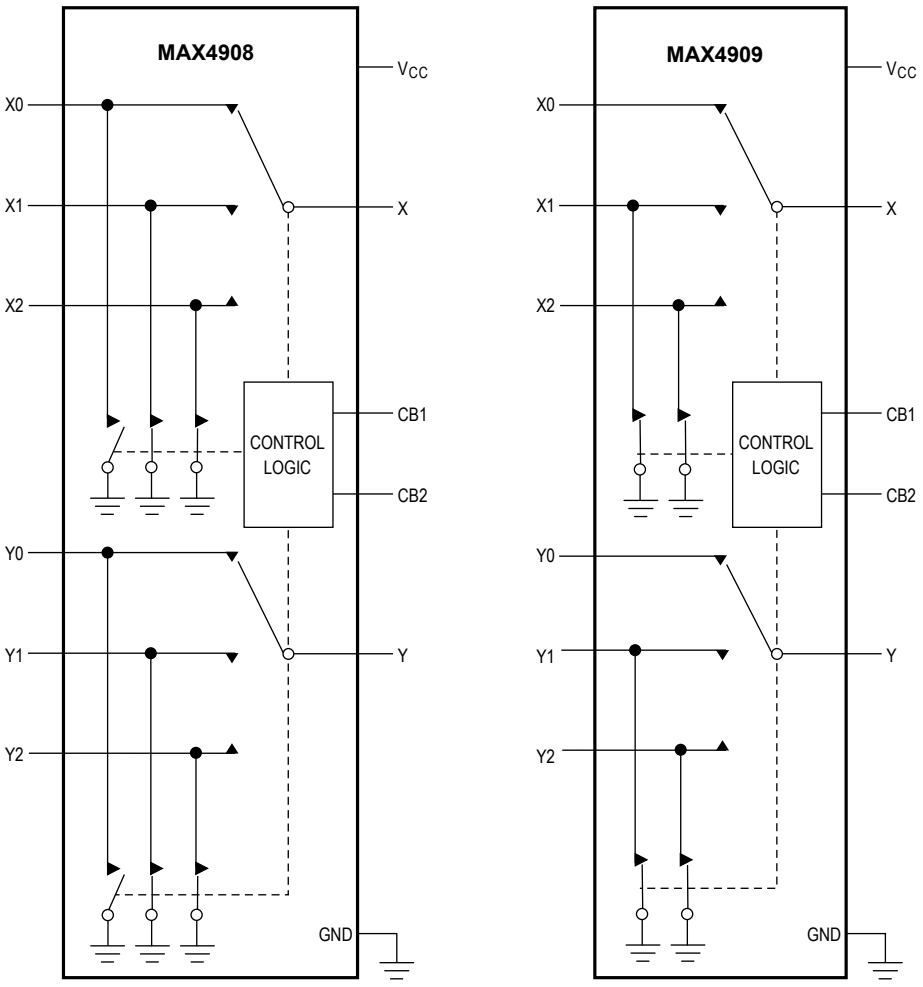
The MAX4908/MAX4909/MAX4930/MAX4932 feature break-before-make switching, which is configured to break (open) the first set of contacts before engaging (closing) the new contacts. This prevents the momentary connection of the old and new signal paths to the output, further reducing click-and-pop sounds.

Power-Supply Sequencing and Overvoltage Protection

Caution: Do not exceed the Absolute Maximum Ratings since stresses beyond the listed ratings may cause permanent damage to the device.

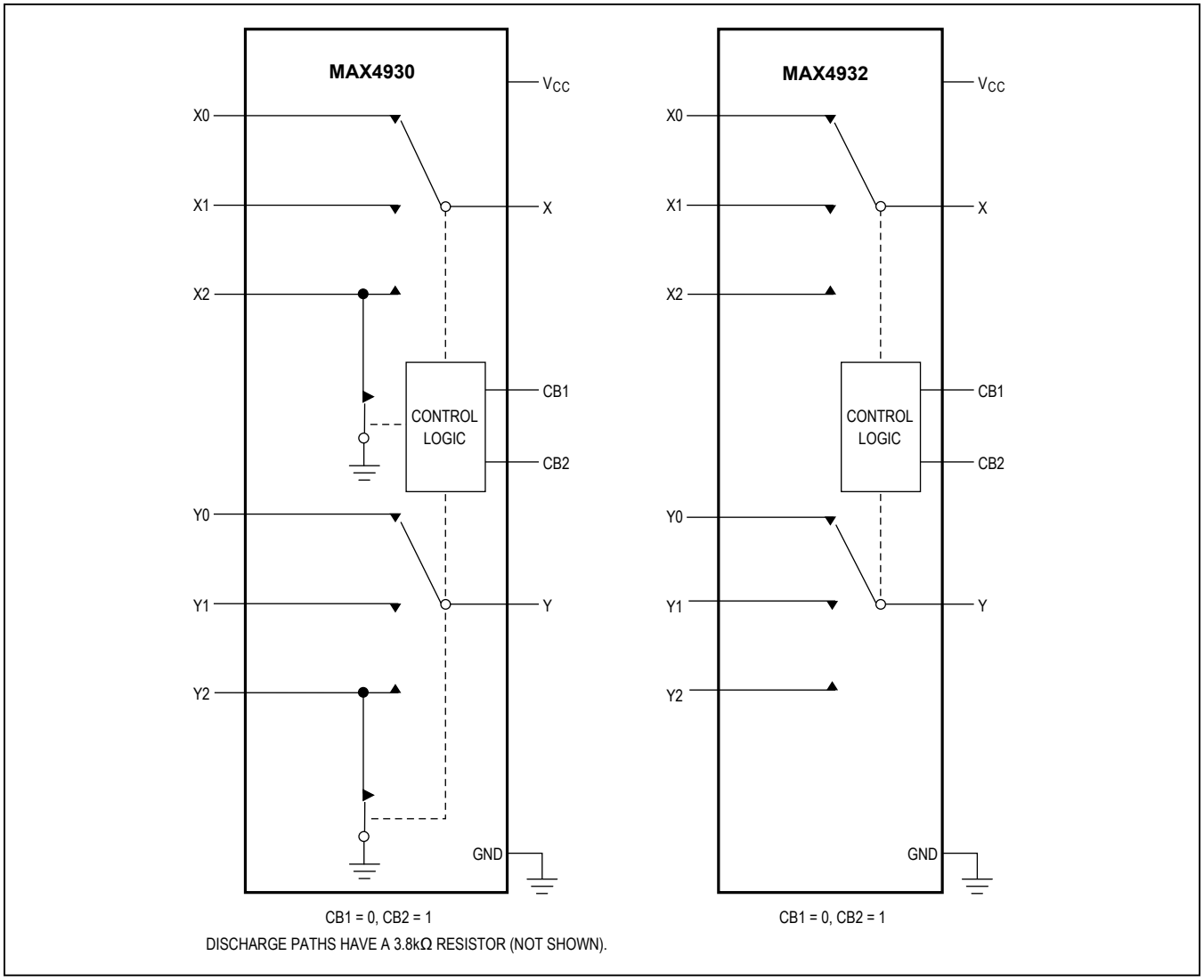
Proper power-supply sequencing is recommended for all CMOS devices. Improper supply sequencing can force the switch into latchup, causing it to draw excessive supply current. The only way out of latchup is to recycle the power and reapply properly. Connect all ground pins first, apply power to V_{CC} , and finally apply signals to X_, Y_, and common terminals. Follow the reverse order upon power-down.

Functional Diagram



DISCHARGE PATHS HAVE A 3.8kΩ RESISTOR (NOT SHOWN).

Functional Diagram (continued)



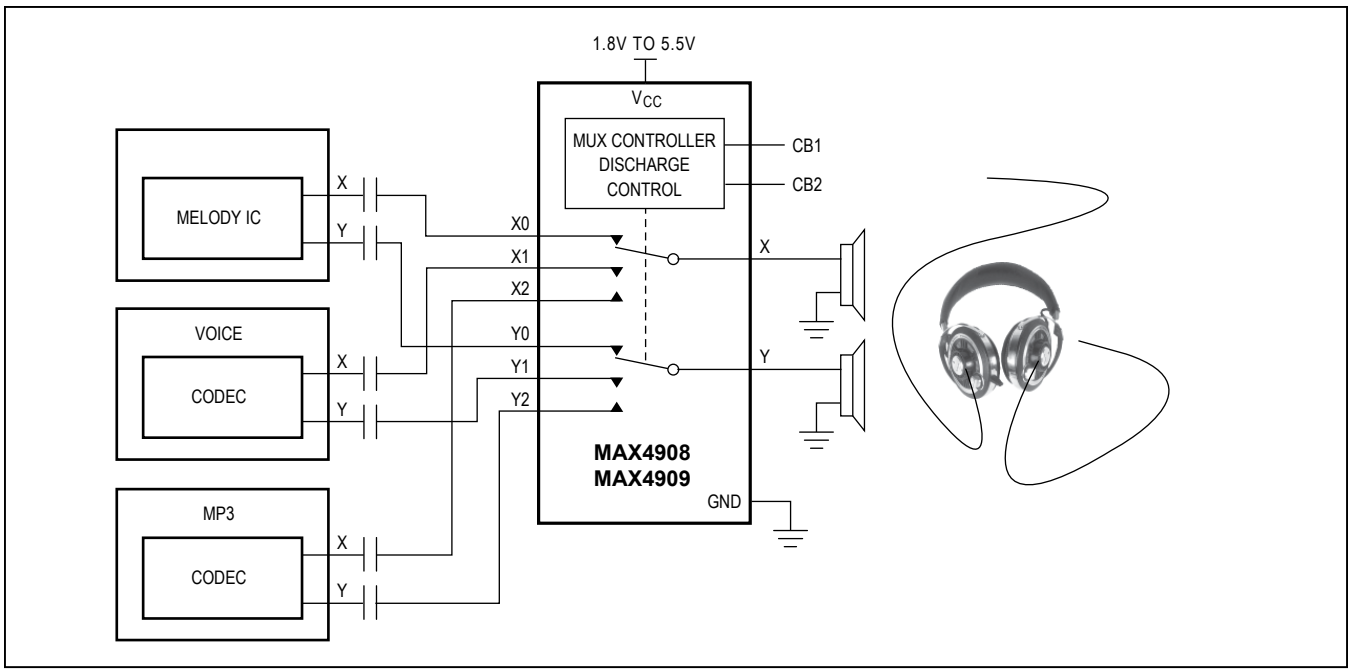


Figure 1. Typical Application Circuit

Test Circuits/Timing Diagrams

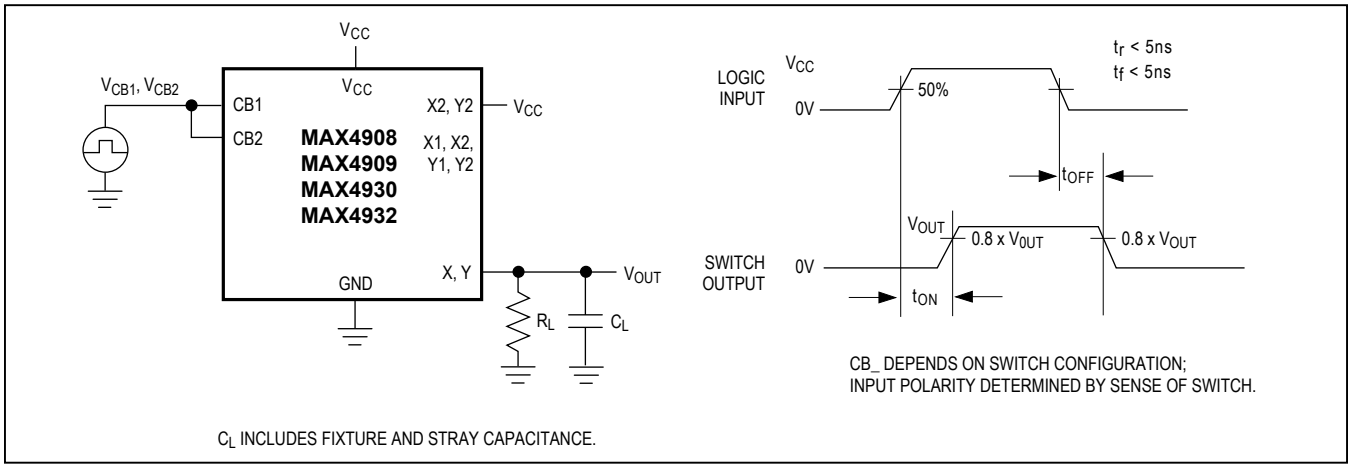


Figure 2. Switching Time

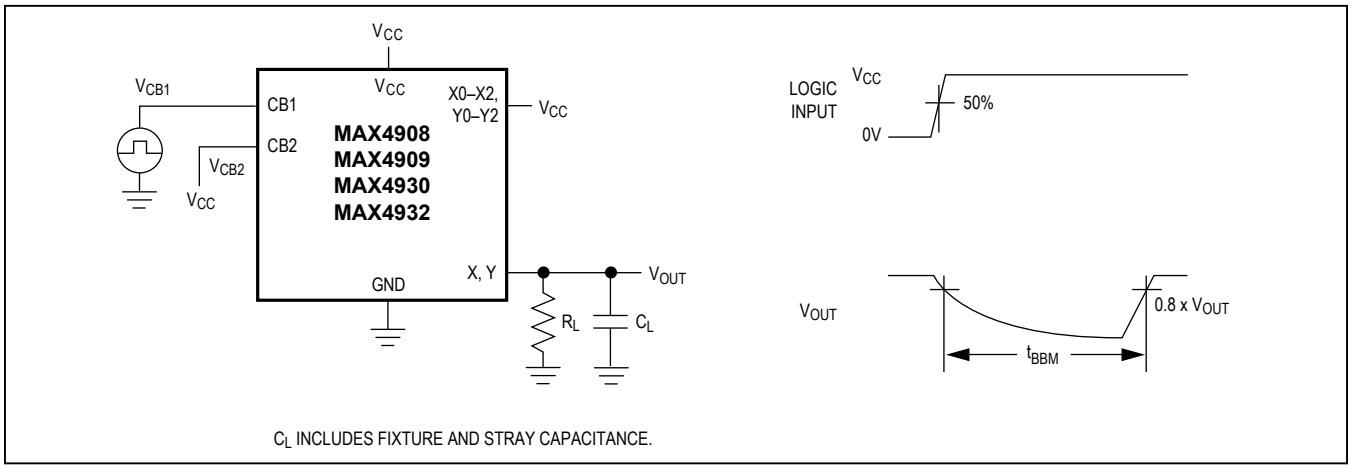


Figure 3. Break-Before-Make Interval

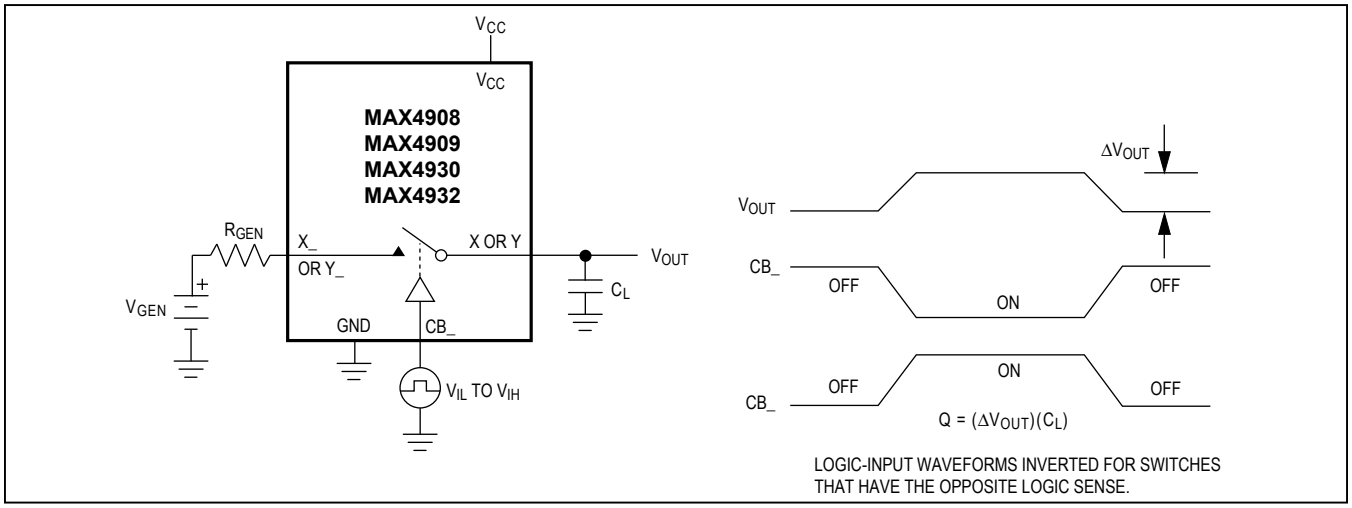


Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

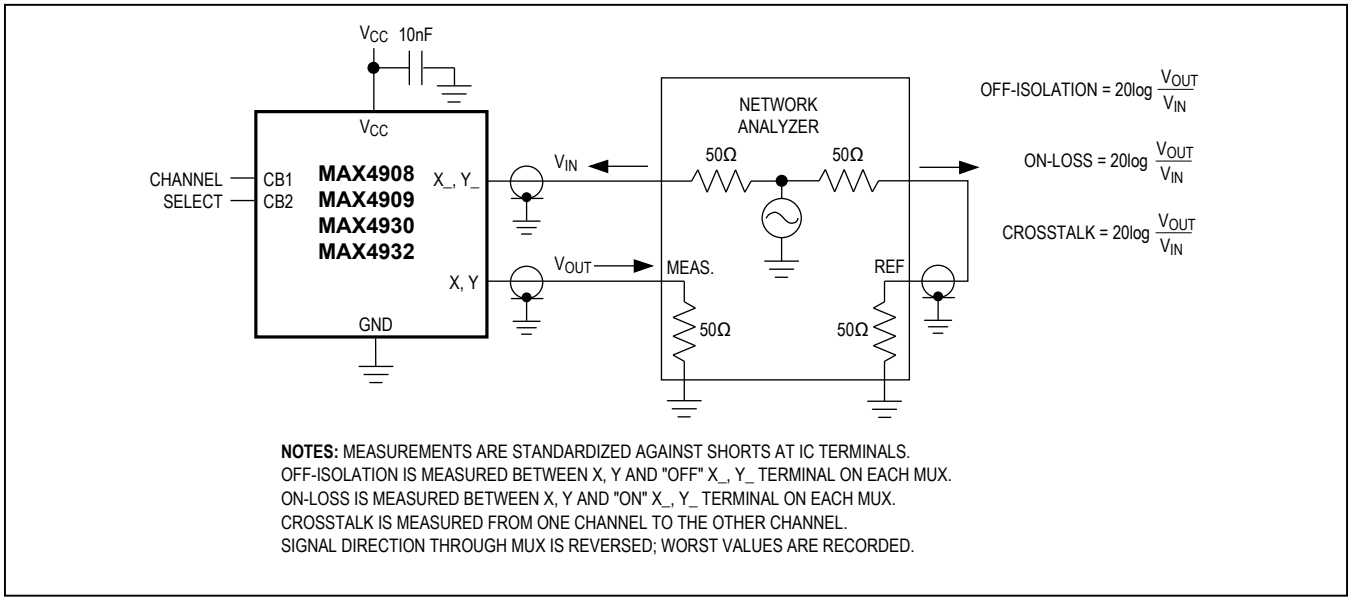


Figure 5. On-Loss, Off-Isolation, and Crosstalk

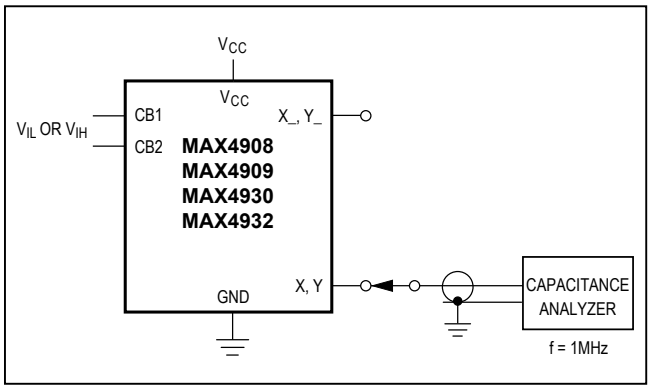


Figure 6. Channel Off/On-Capacitance

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4908ETD+T	-40°C to +85°C	14 TDFN-EP**	ABI
MAX4908EWC+T	-40°C to +85°C	12 WLP	AAF
MAX4909ETD+T	-40°C to +85°C	14 TDFN-EP**	ABJ
MAX4909EWC+T*	-40°C to +85°C	12 WLP	AAG
MAX4930ETD+T	-40°C to +85°C	14 TDFN-EP**	ADM
MAX4930EWC+T*	-40°C to +85°C	12 WLP	ADY
MAX4932ETD+T	-40°C to +85°C	14 TDFN-EP**	ADN
MAX4932EWC+T*	-40°C to +85°C	12 WLP	AAN

+Denotes a lead-free/RoHS-compliant package.
T = Tape and reel.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
14 TDFN	T1433+2	**21-0137**
12 WLP	W121B2+1	**21-100112**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	7/07	Adding of the MAX4930/MAX4932	1-13
2	6/08	Changing UCSP to WLP packaging	1,2,6,8,11
3	1/16	Removed future product asterisk from MAX4908EWC+T	12
4	3/16	Updated package codes and package outline drawing in *Package Information* table	13