Up to 8.0Gbps Dual Passive Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{CC} .... -0.3V to +4V
SEL, SELB, AIN+, AIN-, BIN+, BIN-, AOUTA+, AOUTA-, AOUTB+, AOUTB-, BOUTA+, BOUTA-, BOUTB+, BOUTB- (Note 1) .. -0.3V to (V_{CC} + 0.3V)
Continuous Current (AIN_ to AOUTA_/AOUTB_, BIN_ to BOUTA_/BOUTB_) .... ±15mA
Peak Current (AIN_ to AOUTA_/AOUTB_, BIN_ to BOUTA_/BOUTB_) (pulsed at 1ms, 10% duty cycle) .... ±70mA
Continuous Current (SEL, SELB) .... ±10mA
Peak Current (SEL, SELB) (pulsed at 1ms, 10% duty cycle) .... ±10mA
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 28.6mW/°C above +70°C) 2286mW
Operating Temperature Range .... -40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Note 1: Signals on SEL, SELB, AIN_, BIN _, AOUTA_, AOUTB_, BOUTA_, and BOUTB_ exceeding V_{CC} or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 35°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 2°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V ±10%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE						
Analog-Signal Range	V_{INPUT}	AIN_, BIN_, AOUTA_, BOUTA_, AOUTB_, BOUTB_	-0.3		V_{CC} - 1.8	V
On-Resistance	R_{ON}	V_{CC} = +3.0V, $I_{AIN\_}$ = $I_{BIN\_}$ = 15mA, $V_{\_OUTA\_}$ = $V_{\_OUTB\_}$ = 0V, 1.2V		6.4	8.4	Ω
On-Resistance Match Between Channels	ΔR_{ON}	V_{CC} = +3.0V, $I_{AIN\_}$ = $I_{BIN\_}$ = 15mA, $V_{\_OUTA\_}$ = $V_{\_OUTB\_}$ = 0V (Note 4)		0.2	1.5	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	V_{CC} = +3.0V, $I_{AIN\_}$ = $I_{BIN\_}$ = 15mA, $V_{\_OUTA\_}$ = $V_{\_OUTB\_}$ = 0V, 1.2V (Note 5)		0.3	1	Ω
OUTA or _OUTB_ Off-Leakage Current	$I_{\_OUTA\_(OFF)}$, $I_{\_OUTB\_(OFF)}$	V_{CC} = +3.6V, $V_{AIN\_}$ = $V_{BIN\_}$ = 0V, 1.2V; $V_{\_OUTA\_}$ or $V_{\_OUTB\_}$ = 1.2V, 0V (MAX4888B)	-1		+1	µA
AIN_, BIN_ On-Leakage Current	$I_{AIN\_(ON)}$, $I_{BIN\_(ON)}$	V_{CC} = +3.6V , $V_{AIN\_}$ = $V_{BIN\_}$ = 0V, 1.2V; $V_{\_OUTA\_}$ or $V_{\_OUTB\_}$ = $V_{AIN\_}$ = $V_{BIN\_}$ or unconnected (MAX4888B)	-1		+1	µA
Output Short-Circuit Current		All other ports are unconnected (MAX4888C)	5		15	µA
Output Open-Circuit Voltage		All other ports are unconnected (MAX4888C)	0.2	0.6	0.9	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3.3V ±10%, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Switch Turn-On Time	t_{ON_SEL}	$Z_S = Z_L = 50\Omega$		65		ns
Switch Turn-Off Time	t_{OFF_SEL}	$Z_S = Z_L = 50\Omega$, Figure 1, measured at 500MHz		7		ns
Propagation Delay	t_{PD}	$Z_S = Z_L = 50\Omega$, Figure 2, measured at 500MHz		43		ps
Output Skew Between Pairs	t_{SK1}	$Z_S = Z_L = 50\Omega$, Figure 2, measured at 500MHz		8		ps
Output Skew Between Same Pair	t_{SK2}	$Z_S = Z_L = 50\Omega$, Figure2		10		ps
Differential Return Loss (Note 6)	S_{DD11}	0Hz < f ≤ 2.8GHz	-14			dB
		2.8GHz < f ≤ 5.0GHz	-8			
		5.0GHz < f ≤ 8.0GHz	-5			
		f > 8.0GHz	-1			
Differential Insertion Loss	S_{DD21}	Table 1				dB
Bandwidth	S_{DD12}/S_{DD21}			8		GHz
Differential Crosstalk (Note 6)	S_{DDCTK}	0Hz < f ≤ 2.5GHz		-30		dB
		2.5GHz < f ≤ 5.0GHz		-25		
		5.0GHz < f ≤ 8.0GHz		-35		
		f > 8.0GHz		-35		
Differential Off-Isolation (Note 6)	S_{DD21_OFF}	0Hz < f ≤ 2.5GHz		-15		dB
		2.5GHz < f ≤ 5.0GHz		-12		
		5.0GHz < f ≤ 8.0GHz		-12		
		f > 8.0GHz		-12		
CONTROL INPUT						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.6	V
Input Logic Hysteresis	V_{HYST}			130		mV
POWER SUPPLY						
Power-Supply Range	V_{CC}		3.0		3.6	V
V_{CC} Supply Current	I_{CC}				1	mA

Note 3: All units are 100% production tested at T_A = +85°C. Limits over the operating temperature range are guaranteed by design and characterization and are not production tested.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog-signal range.

Note 6: Guaranteed by design; not production tested.

Up to 8.0Gbps Dual Passive Switches

Test Circuits/Timing Diagrams

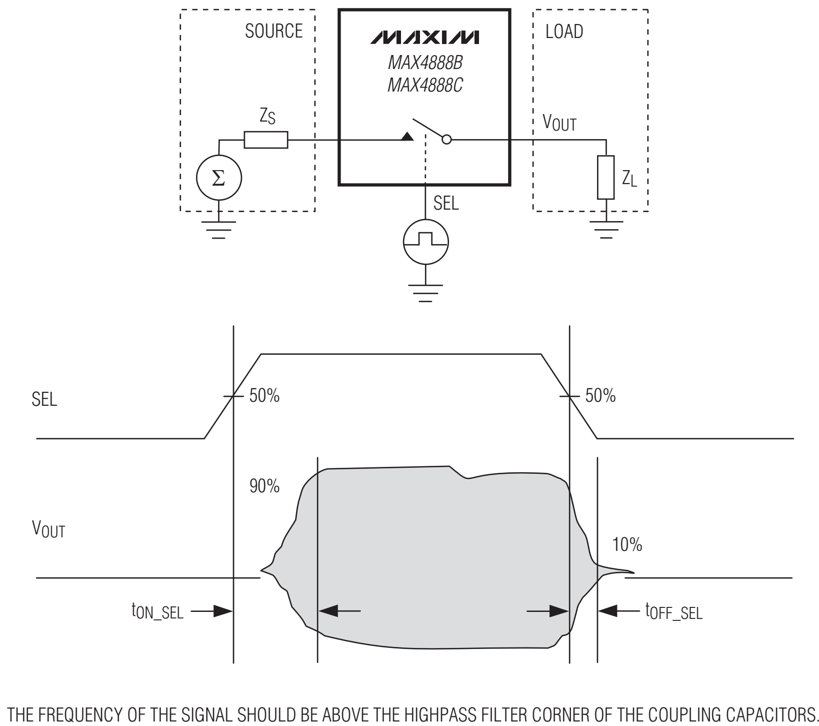


Figure 1. Switching Time

Table 1. Insertion Loss Mask

FREQUENCY RANGE (GHz)	MAXIMUM INSERTION LOSS (dB)
0 to 2.5	1/3 x f_{GHZ} + 17/30
2.5 to 5	2/5 x f_{GHZ} - 2/5
5 to 8	18/5 x f_{GHZ} - 4/15
Greater than 8	2 x f_{GHZ} - 12

Test Circuits/Timing Diagrams (continued)

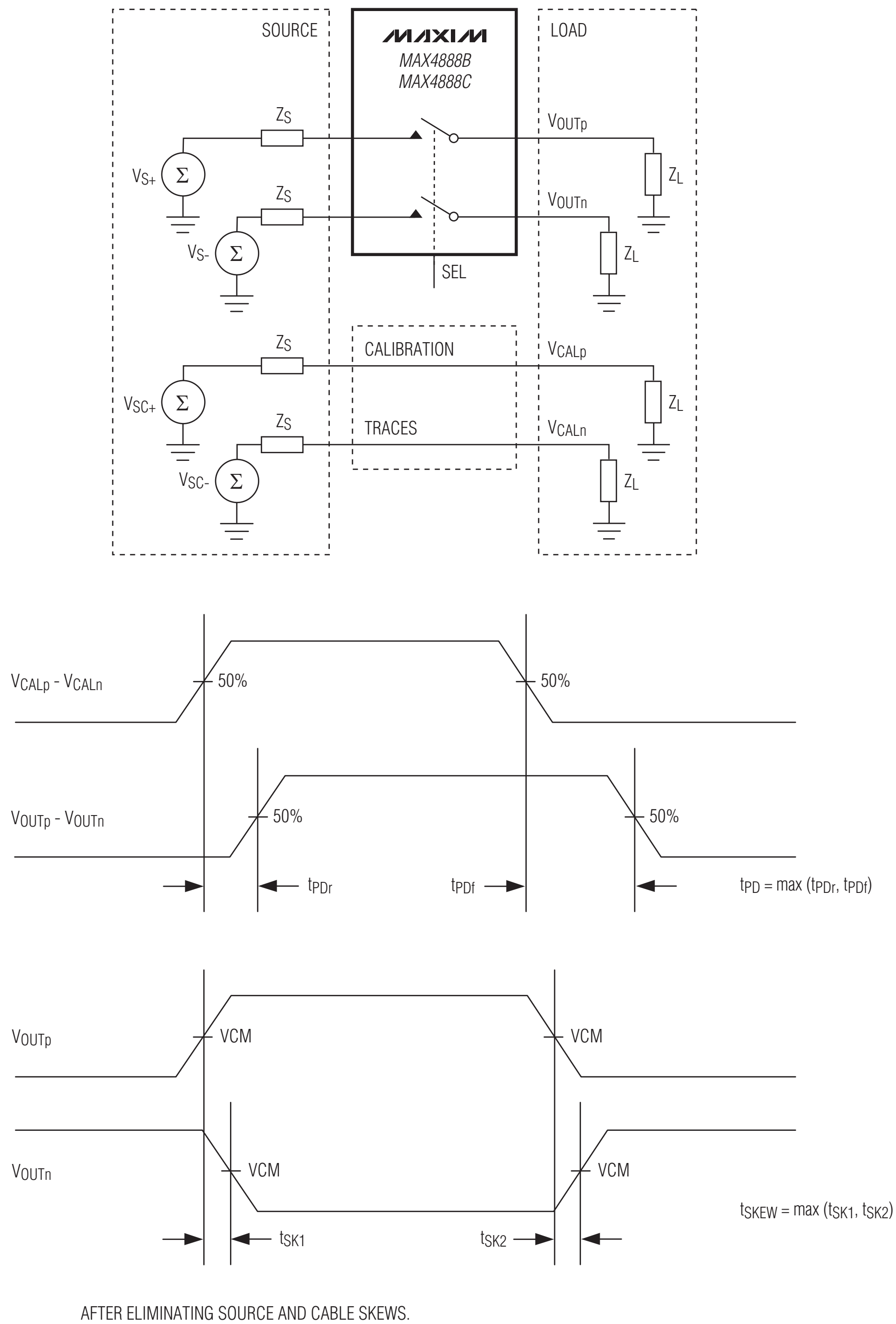


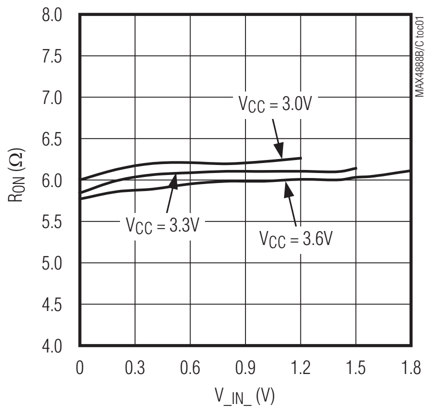
Figure 2. Propagation Delay and Output Skew

Up to 8.0Gbps Dual Passive Switches

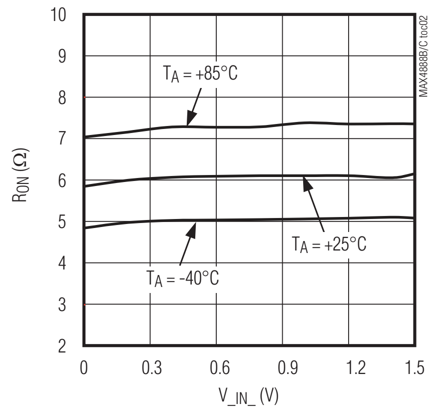
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

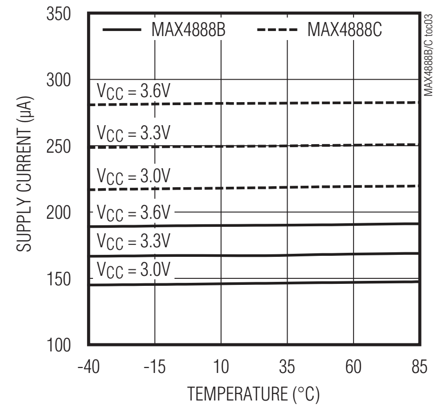
ON-RESISTANCE vs. V_IN_



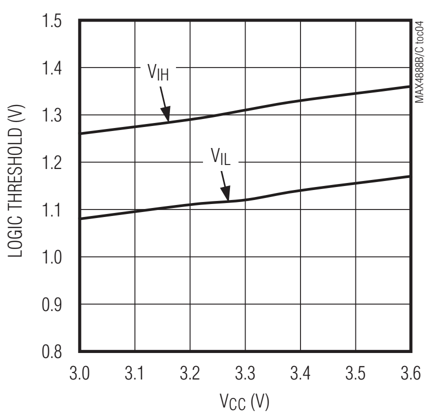
ON-RESISTANCE vs. V_IN_



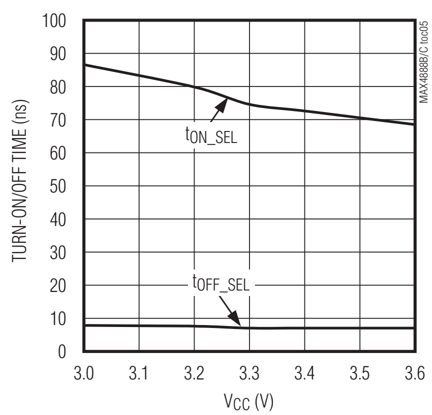
SUPPLY CURRENT vs. TEMPERATURE



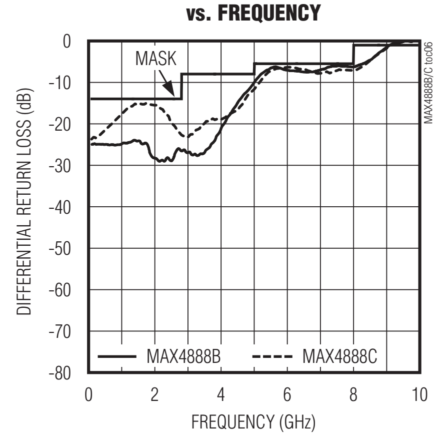
LOGIC THRESHOLD vs. SUPPLY VOLTAGE



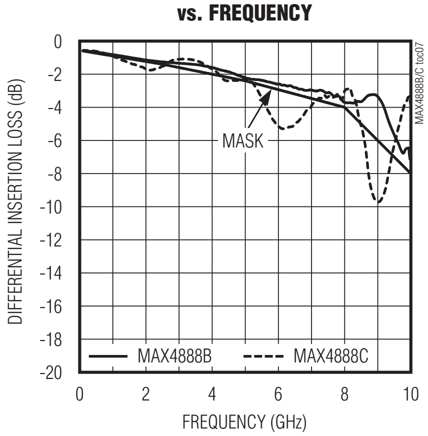
TURN-ON/OFF TIME vs. SUPPLY VOLTAGE



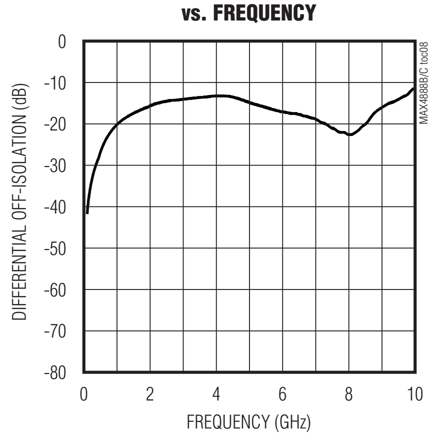
DIFFERENTIAL RETURN LOSS vs. FREQUENCY



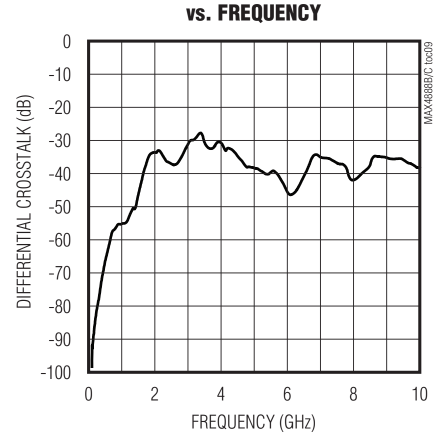
DIFFERENTIAL INSERTION LOSS vs. FREQUENCY



DIFFERENTIAL OFF-ISOLATION vs. FREQUENCY



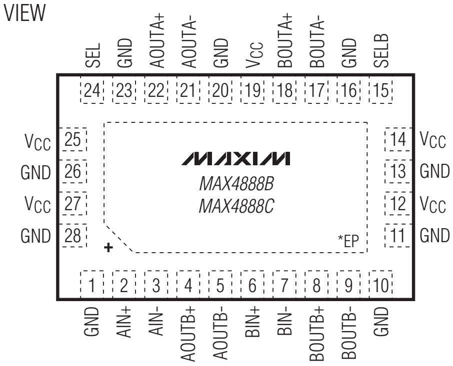
DIFFERENTIAL CROSSTALK vs. FREQUENCY



MAXIM

Pin Configuration

TOP VIEW



TQFN

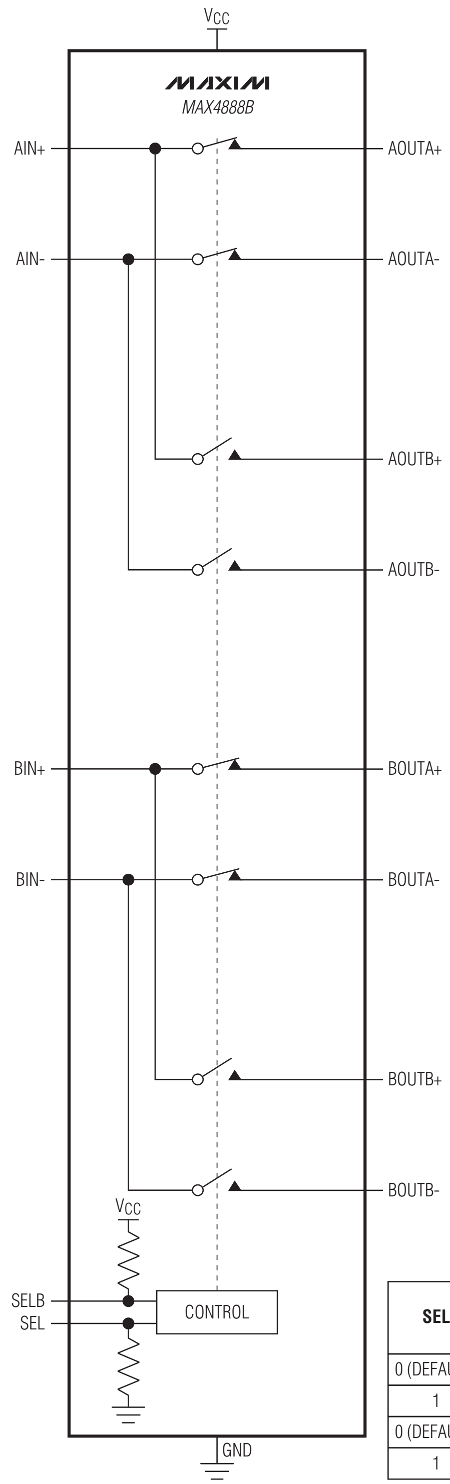
*CONNECT EXPOSED PAD TO GND.

Pin Description

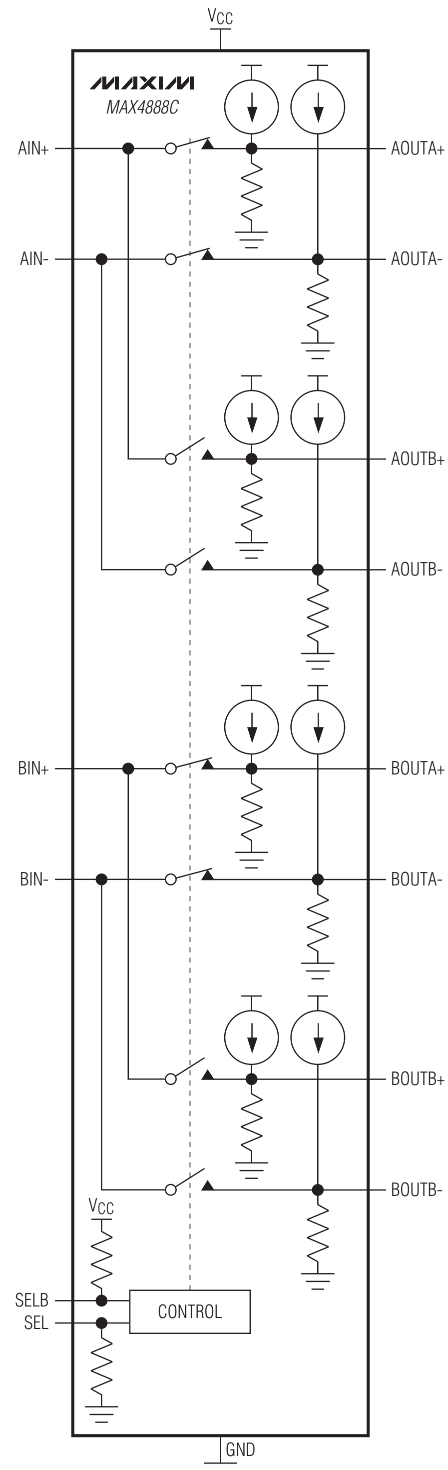
PIN	NAME	FUNCTION
1, 10, 11, 13, 16, 20, 23, 26, 28	GND	Ground
2	AIN+	Analog Switch 1, Common Positive Terminal
3	AIN-	Analog Switch 1, Common Negative Terminal
4	AOUTB+	Analog Switch 1, Normally Open Positive Terminal
5	AOUTB-	Analog Switch 1, Normally Open Negative Terminal
6	BIN+	Analog Switch 2, Common Positive Terminal
7	BIN-	Analog Switch 2, Common Negative Terminal
8	BOUTB+	Analog Switch 2, Normally Open Positive Terminal
9	BOUTB-	Analog Switch 2, Normally Open Negative Terminal
12, 14, 19, 25, 27	V_{CC}	Positive Supply-Voltage Input. Connect V_{CC} to a 3.0V to 3.6V supply voltage. Bypass V_{CC} to GND with a 0.1µF ceramic capacitor placed as close as possible to the device. See the *Board Layout* section.
15	SELB	Control Signal Input. SELB has a 70kΩ (typ) pullup resistor to V_{CC}. If SELB is not in use, leave unconnected.
17	BOUTA-	Analog Switch 2, Normally Closed Negative Terminal
18	BOUTA+	Analog Switch 2, Normally Closed Positive Terminal
21	AOUTA-	Analog Switch 1, Normally Closed Negative Terminal
22	AOUTA+	Analog Switch 1, Normally Closed Positive Terminal
24	SEL	Control Signal Input. SEL has a 70kΩ (typ) pulldown resistor to GND.
—	EP	Exposed Pad. Connect EP to GND.

Up to 8.0Gbps Dual Passive Switches

Functional Diagram/Truth Table



SEL	SELB	AIN_, BIN_ TO AOUTA_, BOUTA_	AIN_, BIN_ TO AOUTB_, BOUTB_
0 (DEFAULT)	0	OFF	ON
1	0	OFF	ON
0 (DEFAULT)	1 (DEFAULT)	ON	OFF
1	1 (DEFAULT)	OFF	ON



Detailed Description

The MAX4888B high-speed passive switch routes high-speed differential signals such as PCIe, SAS, SATA, and XAUI from one source to two possible destinations or vice versa. The MAX4888B is ideal for routing PCIe signals to change the system configuration. The MAX4888C features a 10µA (typ) source current and a 60kΩ (typ) internal biasing resistor to GND at the AOUTA_, BOUTA_, AOUTB_, and BOUTB_ terminals. The MAX4888C is ideal for circuits that are capacitively coupled at both the output and input. These devices are protocol independent and can be used to switch two different protocol signals over the same physical lane. They feature dual digital control inputs (SEL, SELB) to switch signal paths. SEL has a 70kΩ (typ) pulldown resistor to GND and SELB has a 70kΩ (typ) pullup resistor to V_{CC}.

These devices are fully specified to operate from a single 3.0V to 3.6V power supply.

Digital Control Input (SEL, SELB)

The devices provide dual digital control inputs (SEL, SELB) to select the signal path between the AIN_, BIN_ and AOUTA_, BOUTA_ or AOUTB_, BOUTB_ channels. In most cases SEL is chosen and SELB is unconnected. The truth table for the devices is depicted in the *Functional Diagram/Truth Table*. SEL has a 70kΩ (typ) pulldown resistor to GND and SELB has a 70kΩ (typ) pullup resistor to V_{CC}.

Analog-Signal Levels

The devices accept signals from -0.3V to (V_{CC} - 1.8V). Signals on the AIN+ and BIN+ channels are routed to either the AOUTA+, BOUTA+ or AOUTB+, BOUTB+ channels. Signals on the AIN- and BIN- channels are routed to either the AOUTA-, BOUTA- or AOUTB-, BOUTB- channels. The devices are bidirectional switches, allowing AIN_, BIN_ and AOUTA_, BOUTA_, AOUTB_, and BOUTB_ to be used as either inputs or outputs.

Applications Information

High-Speed Switching

The devices' primary applications are aimed at sharing resources. For example, a single lane of PCIe or SAS can be shared between a single host and two devices. This could be used for redundancy or to share resources such as a physical lane or route a lane between one host and two devices or two hosts and one device.

Board Layout

High-speed switches require proper layout and design procedures for optimum performance. Keep controlled impedance PCB traces as short as possible or follow impedance layouts per the PCIe specification. Ensure that power-supply bypass capacitors are placed as close as possible to the device. Multiple bypass capacitors are recommended. Connect all grounds and the exposed pad to a large ground plane.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T283555+1	**21-0184**	**90-0123**

Up to 8.0Gbps Dual Passive Switches

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—