# 1Ω, Low-Voltage, Single-Supply SPDT Analog Switches

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+, IN .....-0.3V to +6V
COM, NC, NO (Note 1).....-0.3V to (V+ + 0.3V)
Continuous Current NO, NC to COM.....±200mA
Peak Current NO, NC to COM
(pulsed at 1ms, 10% duty cycle max) ..... ±400mA

Continuous Power Dissipation
6-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW
6-Pin Thin SOT23 (derate 6.25mW/°C above +70°C)...500mW
Operating Temperature Range
MAX462_E_T .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C

**Note 1:** Signals on NC, NO, and COM exceeding V+ or GND are clamped by internal diodes.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, GND = 0, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 4.5V, $V_{NO}$ or $V_{NC}$ = 3.5V, $I_{COM}$ = 100mA | $T_A$ = +25°C | | 0.65 | 1 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 1.2 | |
| On-Resistance Match Between Channels (Note 4) | $\Delta R_{ON}$ | V+ = 4.5V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 3.5V | $T_A$ = +25°C | | 0.06 | 0.12 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 0.15 | |
| On-Resistance Flatness (Note 5) | $R_{FLAT(ON)}$ | V+ = 4.5V; $I_{COM}$ = 100mA; $V_{NO}$ or $V_{NC}$ = 0, 1V, 2V | $T_A$ = +25°C | | 0.08 | 0.12 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 0.15 | |
| NO or NC Off-Leakage Current | $I_{NO(OFF)}$, $I_{NC(OFF)}$ | V+ = 5.5V; $V_{COM}$ = 1V, 4.5V; $V_{NO}$ or $V_{NC}$ = 4.5V, 1V | $T_A$ = +25°C | -2 | 0.01 | 2 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -20 | | 20 | |
| COM On-Leakage Current | $I_{COM(ON)}$ | V+ = 5.5V; $V_{COM}$ = 1V, 4.5V; $V_{NO}$ or $V_{NC}$ = 1V, 4.5V, or floating | $T_A$ = +25°C | -4 | 0.3 | 4 | nA |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | -40 | | 40 | |
| Overcurrent-Protection Current Threshold | | $T_A$ = +25°C | | | 1.2 | | A |
| **DYNAMIC** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 3V, Figure 2 | $T_A$ = +25°C | | 40 | 50 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 60 | |
| Turn-Off Time | $t_{OFF}$ | $V_{NO}$ or $V_{NC}$ = 3V, Figure 2 | $T_A$ = +25°C | | 40 | 50 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 60 | |
| Break-Before-Make Delay (Note 6) | $t_{BBM}$ | MAX4624 only, Figure 3a | $T_A$ = +25°C | 1 | 20 | | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 1 | | | |
| Make-Before-Break Delay (Note 6) | $t_{MBB}$ | MAX4625 only, Figure 3b | $T_A$ = +25°C | 1 | 6 | | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | 1 | | | |

## ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, GND = 0, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Charge Injection | Q | $C_L$ = 1.0nF, $V_{GEN}$ = 0, $R_{GEN}$ = 0, $T_A$ = +25°C, Figure 4 | | 65 | | pC |
| Off-Isolation (Note 7) | OIRR | $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz, $T_A$ = +25°C, Figure 5 | | -57 | | dB |
| Crosstalk (Note 8) | | $R_L$ = 50Ω, $C_L$ = 5pF, f = 1MHz, $T_A$ = +25°C, Figure 5 | | -57 | | dB |
| NC or NO Off-Capacitance | $C_{OFF}$ | f = 1MHz, $T_A$ = +25°C, Figure 6 | | 32 | | pF |
| COM On-Capacitance | $C_{COM(ON)}$ | f = 1MHz, $T_A$ = +25°C, Figure 6 | | 100 | | pF |
| **LOGIC INPUT** | | | | | | |
| Input Voltage Low | $V_{INL}$ | | | | 0.8 | V |
| Input Voltage High | $V_{INH}$ | | 2.4 | | | V |
| Logic Input Current | $I_{IN}$ | | -1 | | 1 | µA |
| **SUPPLY** | | | | | | |
| Power-Supply Range | V+ | | 1.8 | | 5.5 | V |
| Positive Supply Current | I+ | V+ = 5.5V, $V_{IN}$ = 0 or V+ | | | 10 | µA |

## ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, GND = 0, $V_{INH}$ = 2.0V, $V_{INL}$ = 0.6V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| Analog Signal Range | $V_{COM}$, $V_{NO}$, $V_{NC}$ | | | 0 | | V+ | V |
| On-Resistance | $R_{ON}$ | V+ = 2.7V, $V_{NO}$ or $V_{NC}$ = 1.5V, $I_{COM}$ = 100mA | $T_A$ = +25°C | | 1.2 | 2.0 | Ω |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 2.5 | |
| On-Resistance Flatness (Note 6) | $R_{FLAT(ON)}$ | V+ = 2.7V; $I_{COM}$ = 100mA; $V_{NO}$ or $V_{NC}$ = 0, 0.75V, 1.5V; $T_A$ = +25°C | | | 0.25 | | Ω |
| **DYNAMIC** | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{NO}$ or $V_{NC}$ = 1.5V, Figure 2 | $T_A$ = +25°C | | 65 | 80 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 100 | |
| Turn-Off Time | $t_{OFF}$ | $V_{NO}$ or $V_{NC}$ = 1.5V, Figure 2 | $T_A$ = +25°C | | 62 | 80 | ns |
| | | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 100 | |
| Break-Before-Make Time Delay (Note 4) | $t_{BBM}$ | MAX4624 only, Figure 3a | | 1 | 40 | | ns |
| Make-Before-Break Time Delay (Note 4) | $t_{MBB}$ | MAX4625 only, Figure 3b | | 1 | 8 | | ns |
| Charge Injection | Q | $C_L$ = 1.0nF, Figure 4, $V_{GEN}$ = 0, $R_{GEN}$ = 0, $T_A$ = +25°C | | | 40 | | pC |

# 1Ω, Low-Voltage, Single-Supply SPDT Analog Switches

## ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +2.7V to +3.6V, GND = 0, $V_{INH}$ = 2.0V, $V_{INL}$ = 0.6V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.) (Notes 2, 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **LOGIC INPUT** | | | | | | |
| Input Voltage Low | $V_{INL}$ | | | | 0.6 | V |
| Input Voltage High | $V_{INH}$ | | 2.0 | | | V |
| Logic Input Current | $I_{IN}$ | | -1 | | 1 | µA |
| **SUPPLY** | | | | | | |
| Positive Supply Current | I+ | V+ = 3.6V, $V_{IN}$ = 0 or V+ | | | 10 | µA |

**Note 2:** The algebraic convention, where the most negative value is a minimum and the most positive value is a maximum, is used in this data sheet.

**Note 3:** SOT-packaged parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.

**Note 4:** $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.

**Note 5:** Flatness is defined as the difference between the maximum and minimum values of on-resistance as measured over the specified analog signal range.

**Note 6:** Guaranteed by design.

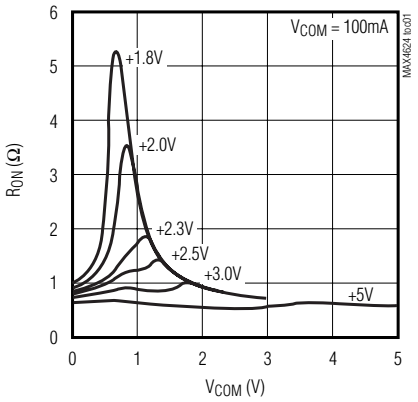
**Note 7:** Off-Isolation = $20\log_{10}$ [$V_{COM}$ / ($V_{NC}$ or $V_{NO}$)], $V_{COM}$ = output, $V_{NC}$ or $V_{NO}$ = input to off switch.

**Note 8:** Between the two switches.

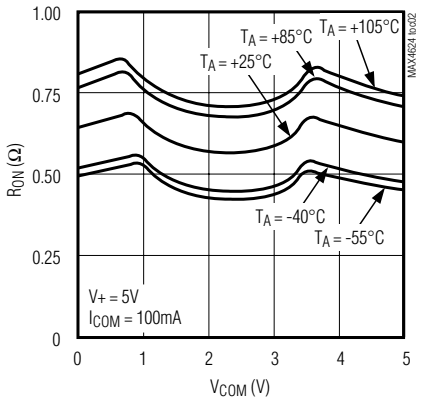
## Typical Operating Characteristics

($T_A$ = +25°C, unless otherwise noted.)

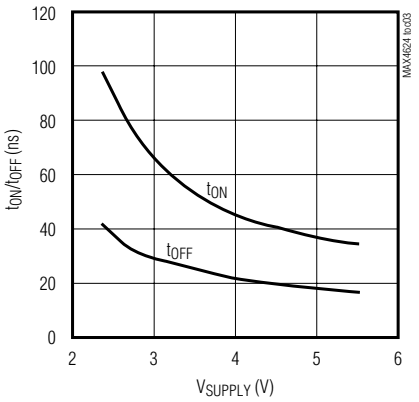
**ON-RESISTANCE vs. COM VOLTAGE OVER SUPPLY VOLTAGE**




**ON-RESISTANCE vs. COM VOLTAGE OVER TEMPERATURE**



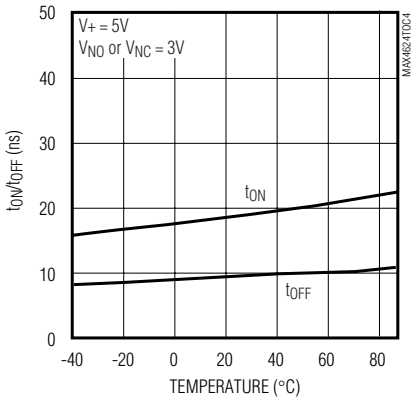

**TURN-ON/OFF TIMES vs. SUPPLY VOLTAGE**



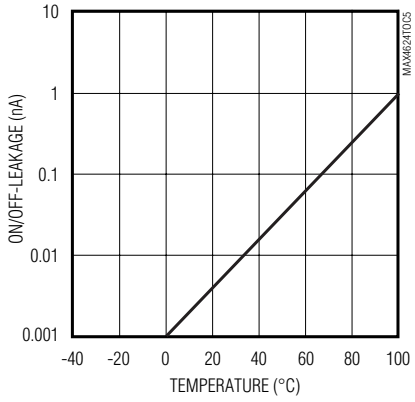
## Typical Operating Characteristics (continued)

($T_A$ = +25°C, unless otherwise noted.)

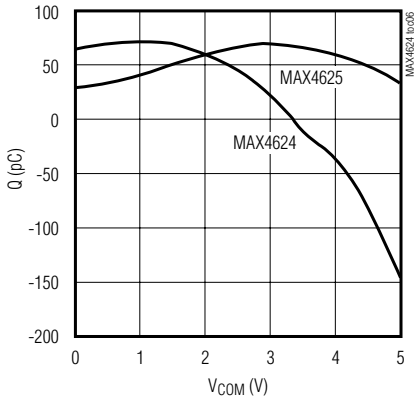
**TURN-ON/OFF TIMES vs. TEMPERATURE**



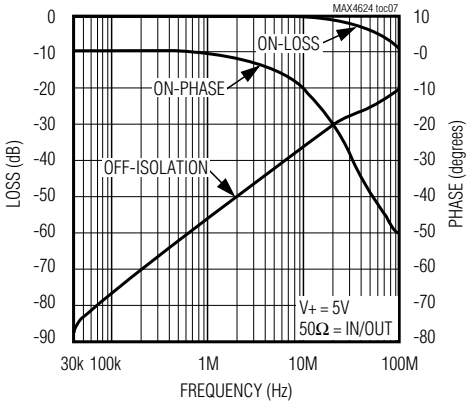

**ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE**



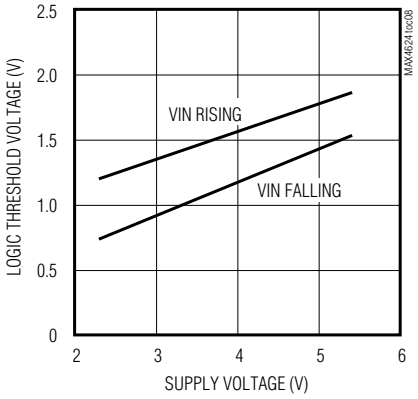

**CHARGE INJECTION vs. COM VOLTAGE**



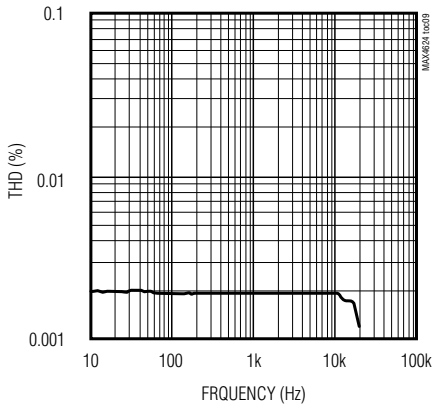

**FREQUENCY RESPONSE**



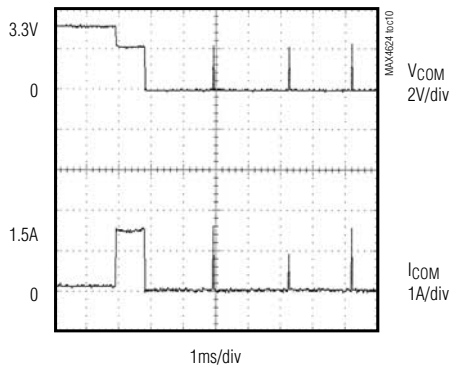

**LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE**




**TOTAL HARMONIC DISTORTION vs. FREQUENCY**




**OVERCURRENT RESPONSE**



# 1Ω, Low-Voltage, Single-Supply SPDT Analog Switches

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | IN | Digital Control Input |
| 2 | V+ | Positive Supply Voltage Input |
| 3 | GND | Ground |
| 4 | NC | Analog Switch—Normally Closed |
| 5 | COM | Analog Switch—Common |
| 6 | NO | Analog Switch—Normally Open |

## Detailed Description

The MAX4624/MAX4625 are low-on-resistance ($R_{ON}$), low-voltage, single-pole/double-throw (SPDT) analog switches that operate from a +1.8V to +5.5V supply. The MAX4624 has break-before-make switching, and the MAX4625 has make-before-break switching. These devices also have fast switching speeds ($t_{ON}$ = 50ns max, $t_{OFF}$ = 50ns max).

When powered from a +5V supply, their 1Ω max $R_{ON}$ allows high continuous currents to be switched in a variety of applications. In an overcurrent condition, these switches provide both current-limit and thermal-shutdown protection.

### Current-Limit Protection

The MAX4624/MAX4625 feature current-limit protection circuitry. When the voltage drop across the on switch reaches 0.6V typ, the internal circuitry activates. The current limit is not instantaneous, but rather integrates over time, so current limiting will not activate when the switch output charges a small 0.1µF capacitor. For sustained overload conditions, the switch turns off (opens). The switch turns on after 5ms. If the overload persists, the switch cycles off and on to produce a pulsed output. A direct short circuit will be detected immediately, and the switch will pulse on for 1µs, then remain off for 5ms.

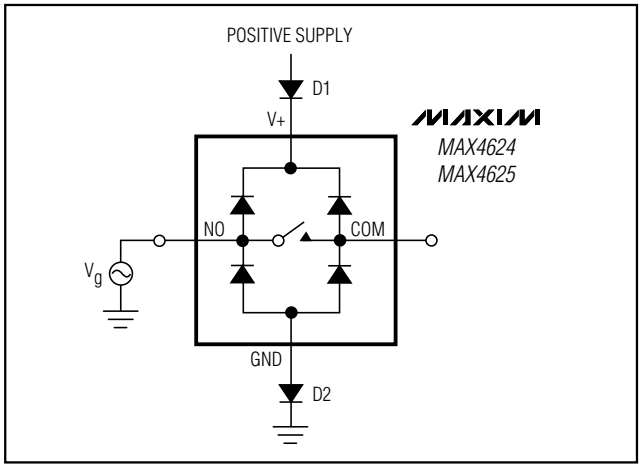



*Figure 1. Overvoltage Protection Using Two External Blocking Diodes*

## Applications Information

### Logic Inputs

The MAX4624/MAX4625 logic inputs can be driven up to +5.5V regardless of the supply voltage. For example, with a +3.3V supply, IN may be driven low to 0V and high to 5.5V. Driving IN Rail-to-Rail® minimizes power consumption.

### Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) can be passed with very little change in on-resistance (see *Typical Operating Characteristics*). The switches are bidirectional, so the NO, NC, and COM pins can be used as either inputs or outputs.

### Power-Supply Sequencing and Overvoltage Protection

**Caution: Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices.**

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals, especially if the analog signal is not current limited. If this sequencing is not possible, and if the analog inputs are not current limited to <20mA, add

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.*

a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog range to a diode drop (about 0.7V) below V+ (for D1), and a diode drop above ground (for D2). On-resistance increases slightly at low supply voltages. Maximum supply voltage (V+) must not exceed +6V.

Adding protection diode D2 causes the logic threshold to be shifted relative to GND. TTL compatibility is not guaranteed when D2 is added.

Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

## Test Circuits/Timing Diagrams

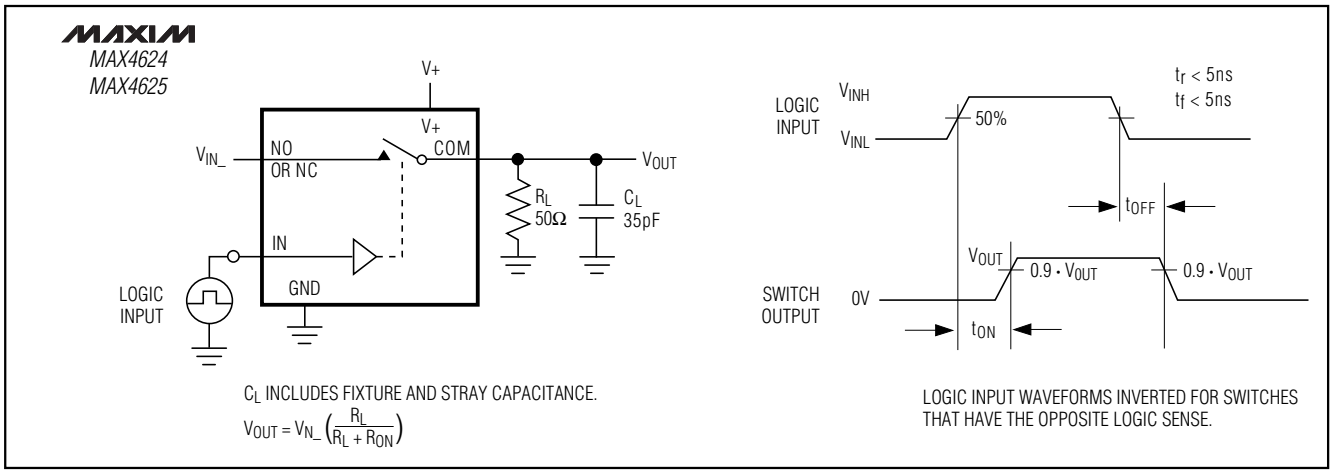



*Figure 2. Switching Time*

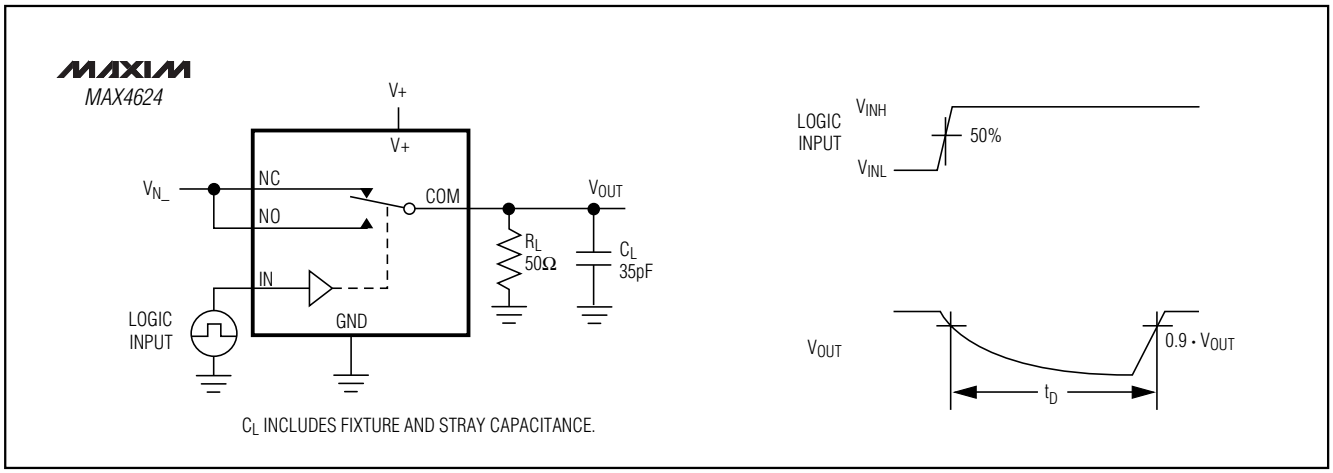



*Figure 3a. Break-Before-Make Interval (MAX4624 only)*

# 1Ω, Low-Voltage, Single-Supply SPDT Analog Switches

## Test Circuits/Timing Diagrams (continued)

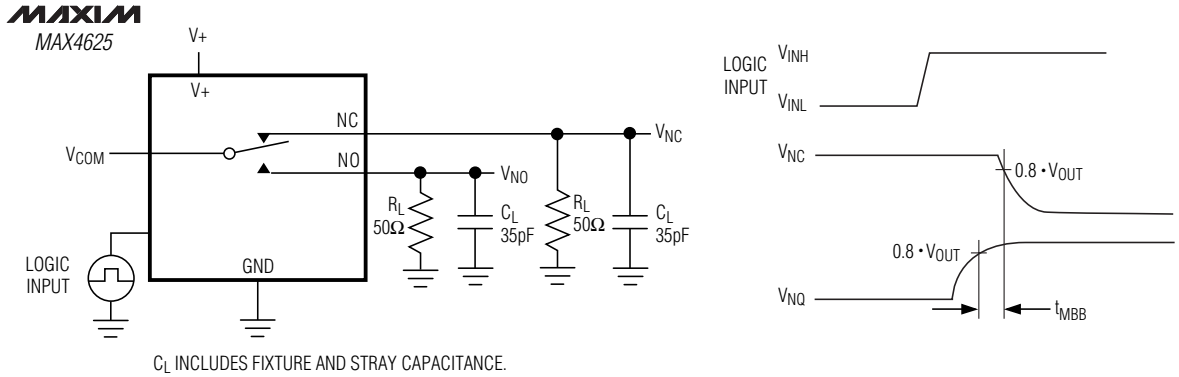



*Figure 3b. Make-Before-Break Interval (MAX4625 only)*

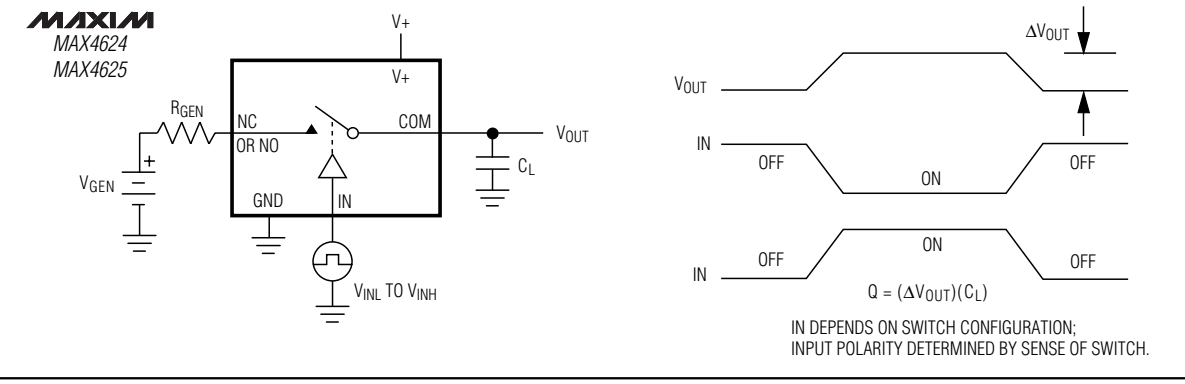



*Figure 4. Charge Injection*

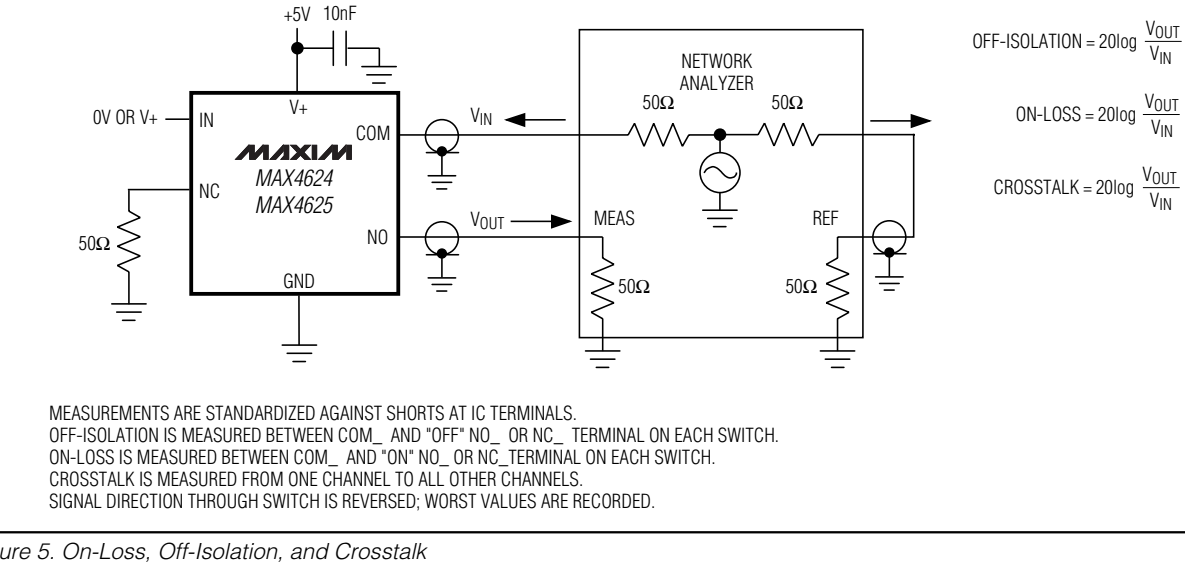



*Figure 5. On-Loss, Off-Isolation, and Crosstalk*

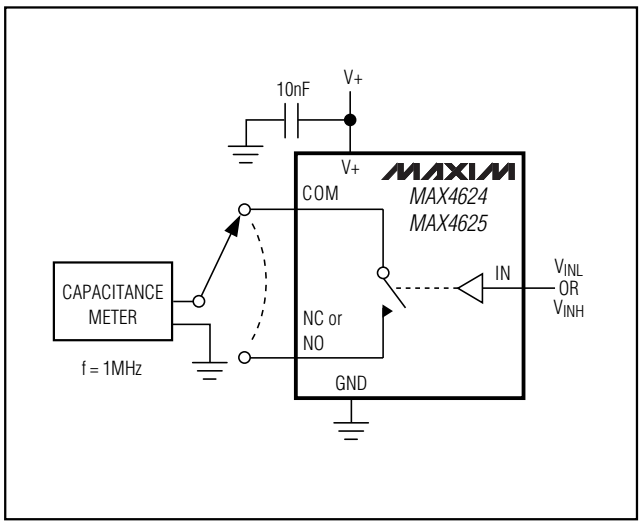


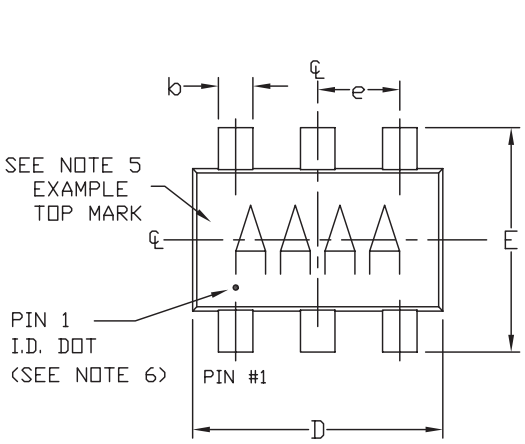

*Figure 6. Channel Off/On-Capacitance*

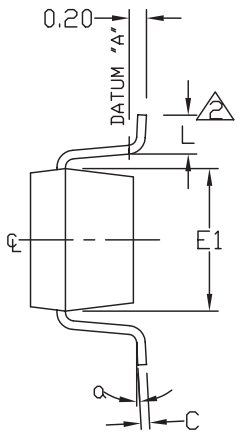
## Chip Information

TRANSISTOR COUNT: 186

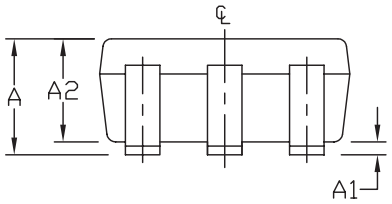
# 1Ω, Low-Voltage, Single-Supply SPDT Analog Switches

## Package Information




| SYMBOL | MIN | MAX |
|---|---|---|
| A | 0.90 | 1.45 |
| A1 | 0.00 | 0.15 |
| A2 | 0.90 | 1.30 |
| b | 0.35 | 0.50 |
| C | 0.08 | 0.20 |
| D | 2.80 | 3.00 |
| E | 2.60 | 3.00 |
| E1 | 1.50 | 1.75 |
| L | 0.35 | 0.55 |
| e | 0.95 REF | |
| a | 0° | 10° |




NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178.

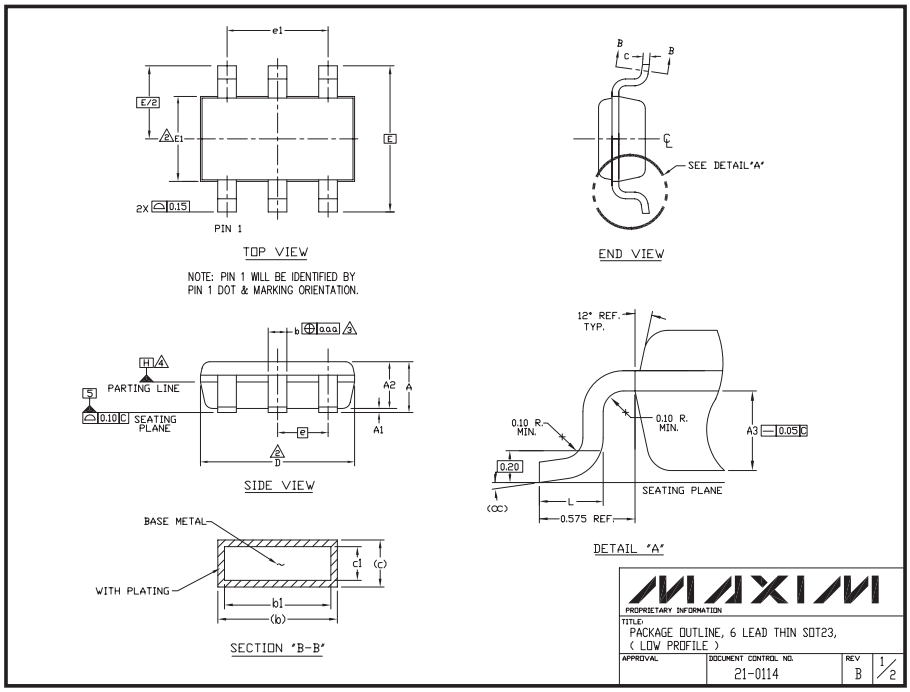
6LSOT.EPS

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SOT-23, 6L

| APPROVAL | DOCUMENT CONTROL NO. | REV | |
|---|---|---|---|
| | 21-0058 | E | 1/1 |

## Package Information (continued)




NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.

3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.

4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.

5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.

6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.

| SYMBOLS | | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.10 |
| A1 | 0.05 | 0.075 | 0.10 |
| A2 | 0.85 | 0.88 | 0.90 |
| A3 | | 0.50 BSC | |
| b | 0.30 | - | 0.45 |
| b1 | 0.25 | 0.35 | 0.40 |
| c | 0.15 | - | 0.20 |
| c1 | 0.12 | 0.127 | 0.15 |
| D | 2.80 | 2.90 | 3.00 |
| E | | 2.75 BSC | |
| E1 | 1.55 | 1.60 | 1.65 |
| L | 0.30 | 0.40 | 0.50 |
| e1 | | 1.90 BSC | |
| e | | 0.95 BSC | |
| OC | 0° | 4° | 8° |
| aaa | | 0.20 | |


MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 6 LEAD THIN SOT23, ( LOW PROFILE )
APPROVAL
DOCUMENT CONTROL NO. 21-0114
REV B
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