

Absolute Maximum Ratings

Supply Voltage -0.5V to +4.2V
 Current Into IN +100mA
 Voltage at OUT+, OUT- $V_{CC} - 1.2V$ to $V_{CC} + 0.5V$
 Voltage at CCAP -0.3V to 1.2V
 Continuous Power Dissipation ($T_A = +85^\circ\text{C}$,
 derate 24.4mW/ $^\circ\text{C}$ above $+85^\circ\text{C}$.) 1904.8mW

Operating Temperature Range -40°C to $+85^\circ\text{C}$
 Operating Junction Temperature Range (die) .. -40°C to $+150^\circ\text{C}$
 Storage Temperature Range -55°C to $+150^\circ\text{C}$
 Soldering Temperature (reflow) $+260^\circ\text{C}$
 Die Attach Temperature $+400^\circ\text{C}$
 ESD HBM Rating at IN $\pm 150V$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



CAUTION! ESD SENSITIVE DEVICE

The MAX40658/MAX40659 amplifiers can be damaged by electrostatic discharge (ESD). They must be handled with appropriate precautions. Failure to observe proper handling can cause damage. ESD damage can range from small performance shifts to product failure.

Package Information

8-TDFN

PACKAGE CODE	T833+1F
Outline Number	21-0137
Land Pattern Number	90-0059
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	55
Junction to Case (θ_{JC})	8
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	42
Junction to Case (θ_{JC})	8

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

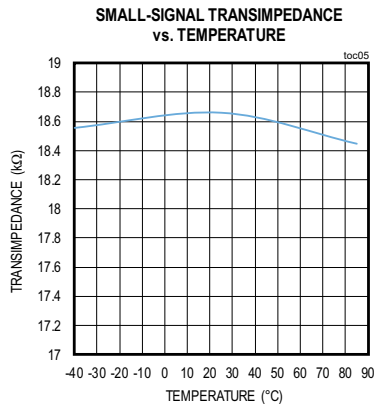
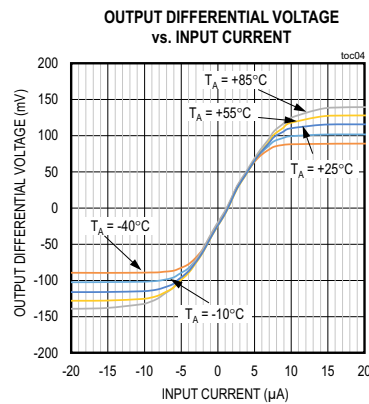
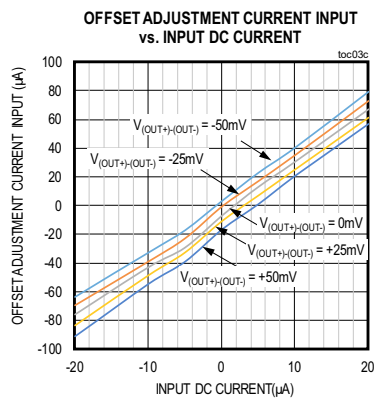
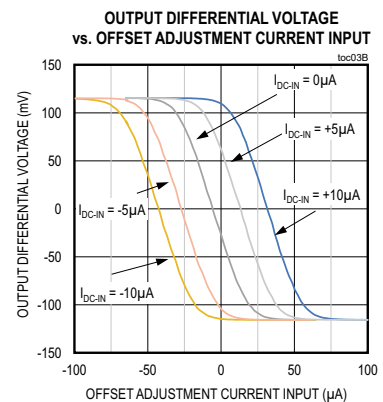
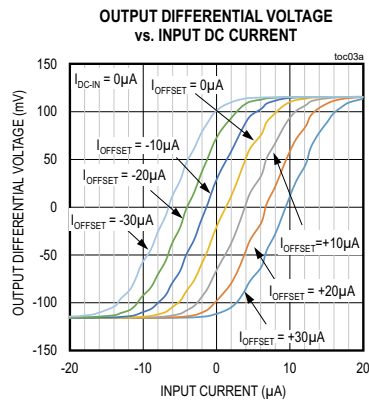
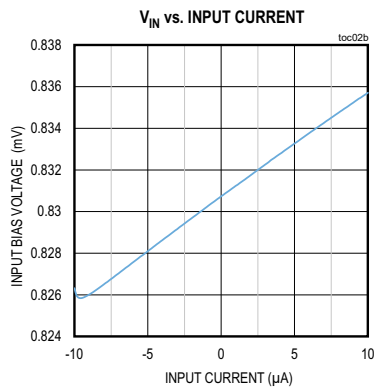
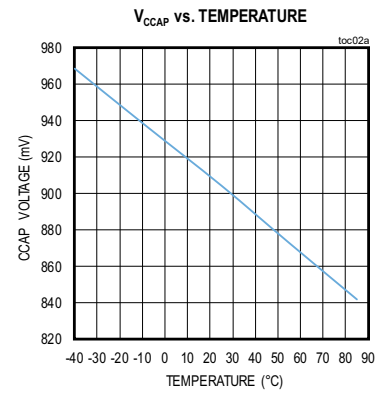
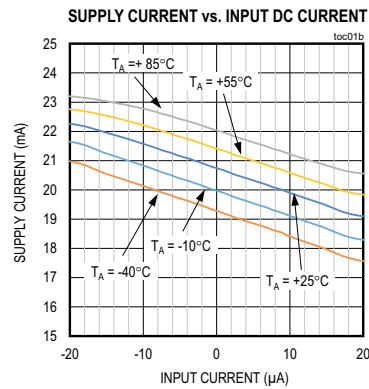
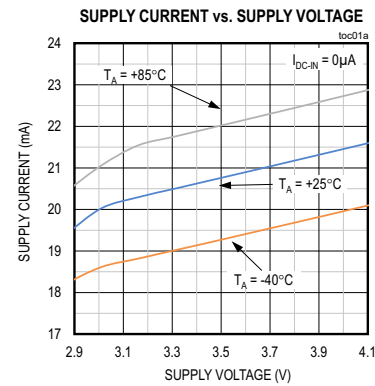
Electrical Characteristics

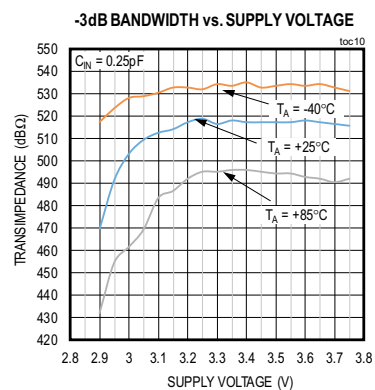
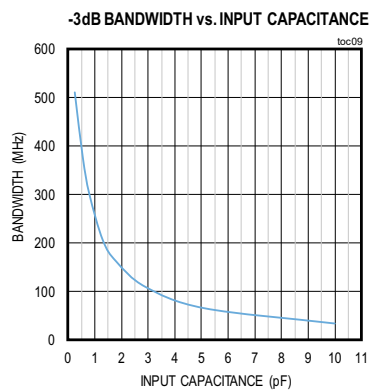
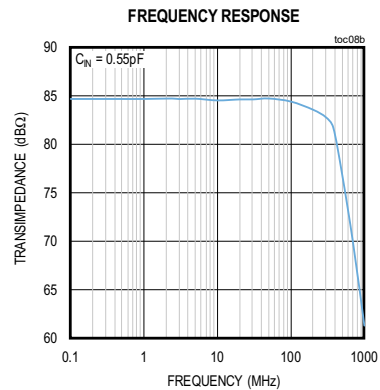
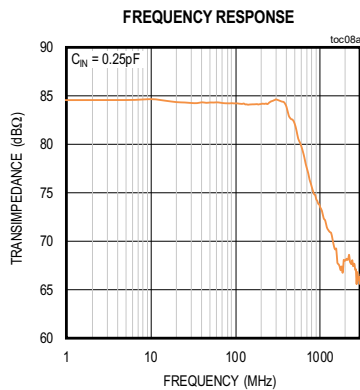
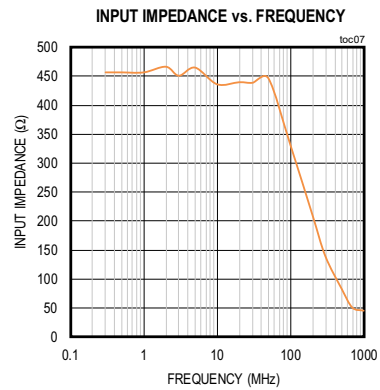
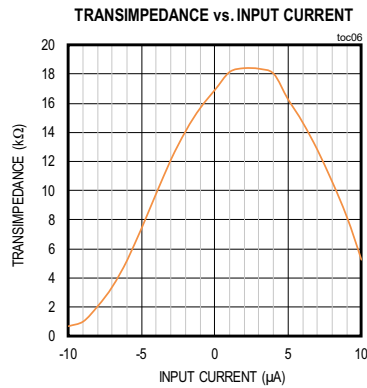
(V_{CC} = +2.97V to +3.63V, 150Ω AC-coupled load between OUT+ and OUT-, T_A = -40°C to +85°C, C_{IN} = 0.25pF (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I _{CC}			21	30	mA
Input Bias Voltage	V _{IN}	I _{IN} = 1μA		0.78	1.0	V
Transimpedance Linearity		MAX40658 I _{IN} = I _{INCENTER} ±2μA, I _{OFFSET} = 0, Note 2			6	%
Small-Signal Transimpedance (Note 2)	Z ₂₁	MAX40658, I _{IN} < 2μA _{P-P}	15.7	18.3	20.9	kΩ
Small-Signal Transimpedance	Z ₂₁	MAX40659, I _{IN} < 1μA _{P-P}		36.4		kΩ
OFFSET Input Transimpedance		MAX40658		4.7		kΩ
		MAX40659		9.4		
Input Clamping Current				100		mA
Output Common-Mode Voltage		MAX40658		V _{CC} - 0.125		V
		MAX40659		V _{CC} - 0.25		
Differential Output Offset	ΔV _{OUT}	I _{IN} = 0mA		-27		mV
Output Impedance	Z _{OUT}	Single ended	60	75	90	Ω
Maximum Differential Output Voltage	V _{OUT(MAX)}	MAX40658, I _{IN} = ±1mA _{P-P} . V _{OUT} = V _{OUT + P-P} - V _{OUT - P-P}	150	240	400	mV _{P-P}
		MAX40659, I _{IN} = ±1mA _{P-P} . V _{OUT} = V _{OUT + P-P} - V _{OUT - P-P}		480		
Input Resistance	R _{IN}			450		Ω
Bandwidth	BW	MAX40658, V _{CC} = 3.3V, Note 3	360	520		MHz
		MAX40659, V _{CC} = 3.3V		520		
Input-Referred Noise	i _n	BW = 267MHz		45		nA _{RMS}
Input Noise Density		f = 267MHz		2.1		pA/Hz ^{1/2}

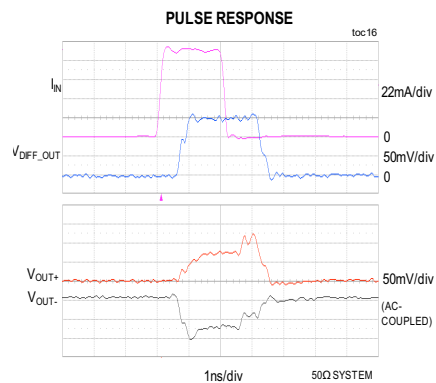
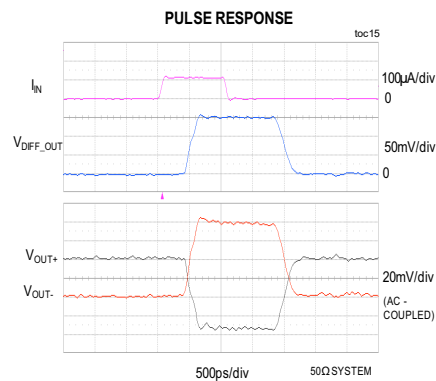
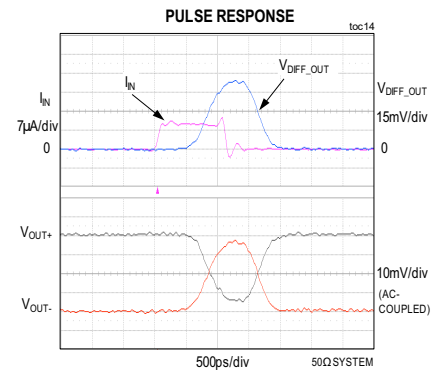
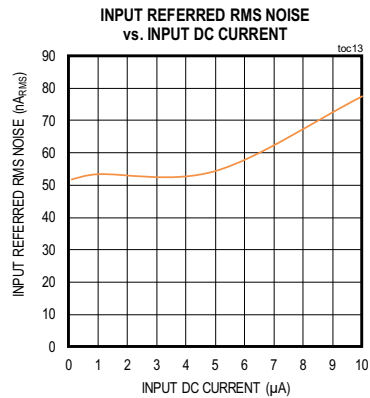
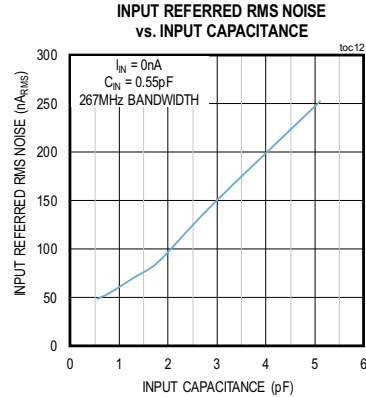
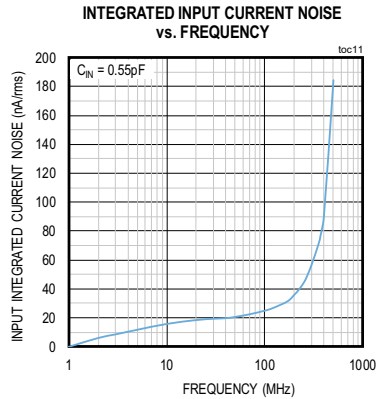
Note 1: Limits are 100% production tested at T_A = +25°C.**Note 2:** I_{INCENTER} is the input current that results in a differential output voltage of 0V.**Note 3:** Not production tested, guaranteed by design and characterization.

Typical Operating Characteristics

(V_{CC} = +3.3V, C_{IN} = 0.5pF, T_A = +25°C, unless otherwise noted.)

Typical Operating Characteristics (continued)(V_{CC} = +3.3V, C_{IN} = 0.5pF, T_A = +25°C, unless otherwise noted.)

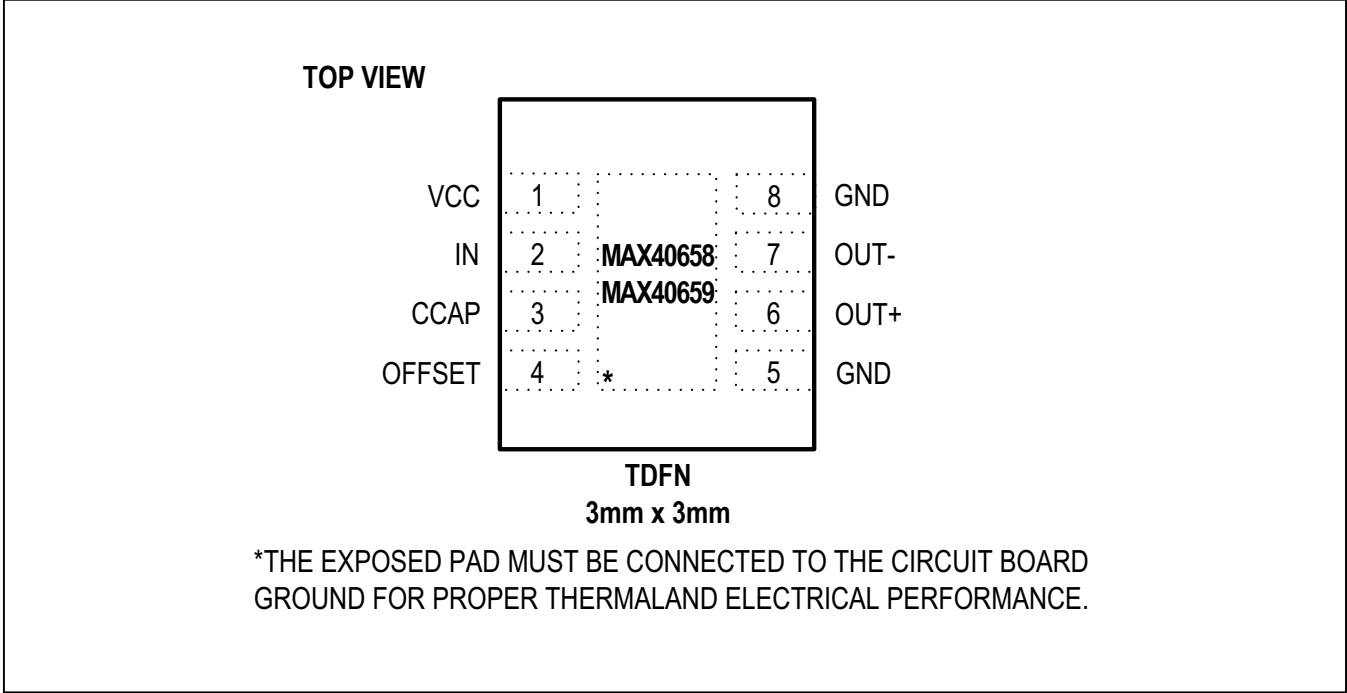
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C_{IN} = 0.5pF, T_A = +25°C, unless otherwise noted.)

MAX40658/MAX40659

Transimpedance Amplifier with 100mA Input
Current Clamp for LiDAR Applications

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	VCC	+3.3V Supply Voltage
2	IN	Signal Input. Connect to photodiode anode.
3	CCAP	Capacitor connection for clamp bias.
4	OFFSET	Offset adjustment current input. Apply a current to this input to adjust the effective input offset current. A positive current into the pin produces a negative offset voltage at OUT+ pin.
6	OUT+	Positive 75Ω Output. Increasing input current causes OUT+ to increase.
7	OUT-	Negative 75Ω Output. Increasing input current causes OUT- to decrease.
5, 8, EP	GND	Circuit Ground

Detailed Description

The MAX40658 and MAX40659 transimpedance amplifiers are designed for optical distance measurement applications and are comprised of a transimpedance amplifier and a voltage amplifier/output buffer.

Gain Stage 1

The signal current at the input flows into the summing node of a high-gain transimpedance amplifier. Shunt feedback through the feedback resistor converts this current into a voltage. An internal Schottky diode clamps input currents up to 100mA (see the [Typical Application Circuits](#)). Bypass CCAP (internally connected to the cathode of the internal Schottky diode) with a 1 μ F capacitor. An external Schottky diode may be added for increased clamping current capability.

Gain Stage 2

The second gain stage provides additional gain and converts the transimpedance amplifier single-ended output into a differential signal. Two different versions are available (MAX40658 and MAX40659), each with a different voltage amplifier gain.

This stage is designed to drive a 150 Ω differential load between OUT+ and OUT-. For optimum supply noise rejection, the outputs should be terminated with a differential load. The single-ended outputs do not drive a DC-coupled grounded load. The outputs should be AC-coupled or terminated to V_{CC}. If a single-ended output is required, both the used and unused outputs should be terminated in a similar manner.

Offset Adjustment

The OFFSET input accepts an input current that may be used to adjust the input offset current of the TIA. Current flowing into the pin yields a negative offset equivalent to $I_{OSIN}/4$, where I_{OSIN} is the current flowing into the OFFSET pin. The OFFSET pin is biased to the same voltage as the IN pin.

Applications Information

Photodiode

Noise performance and bandwidth are adversely affected by capacitance on the TIA input node. Select a low-capacitance photodiode to minimize the total input capacitance on this pin. The TIA is optimized for 0.5pF of capacitance on the input. Assembling the TIA in die form using chip and wire technology provides the lowest capacitance input and the best possible performance.

Supply Filter

Sensitive optical receivers require wide-band power supply decoupling. Power supply bypassing should provide low impedance between V_{CC} and ground for frequencies between 10kHz and 700MHz. Isolate the amplifier from noise sources with LC supply filters and shielding. Place a supply filter as close to the amplifier as possible.

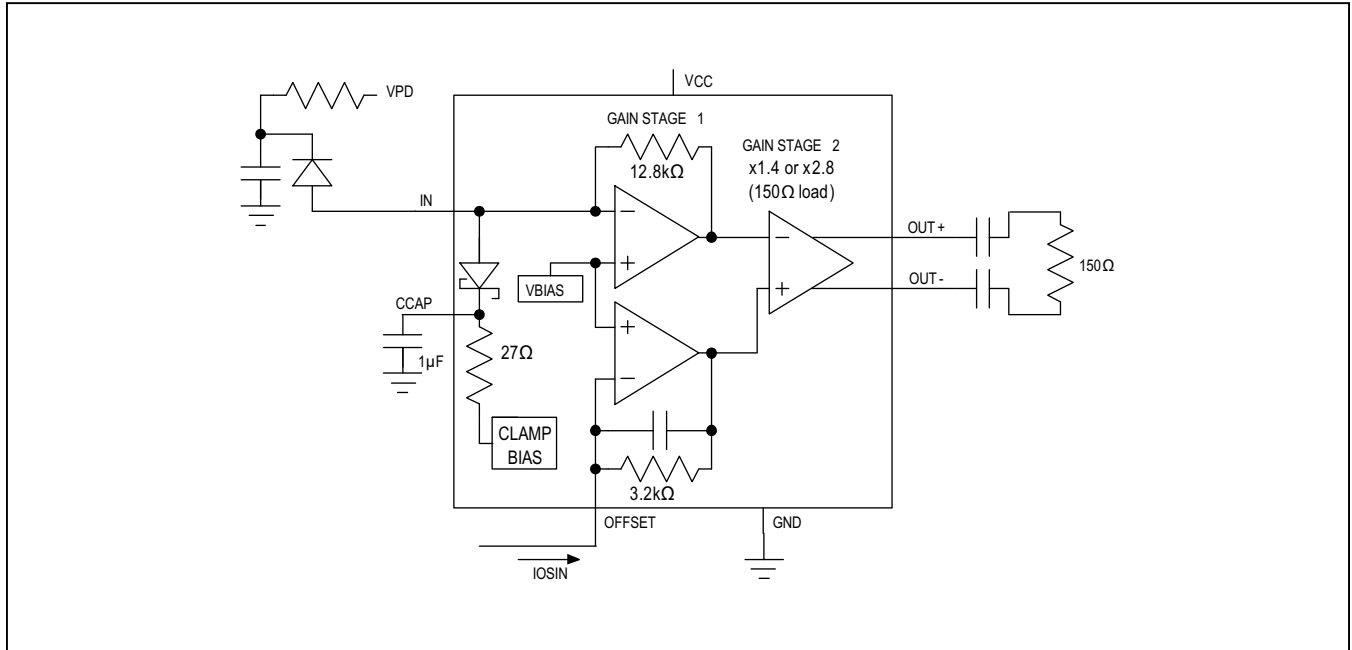
ESD Protection

The MAX40658/MAX40659 TIAs do not contain ESD protection diodes on the analog input (IN). This is to ensure maximum bandwidth and dynamic performance. Care must be taken when handling the package to ensure proper operation.

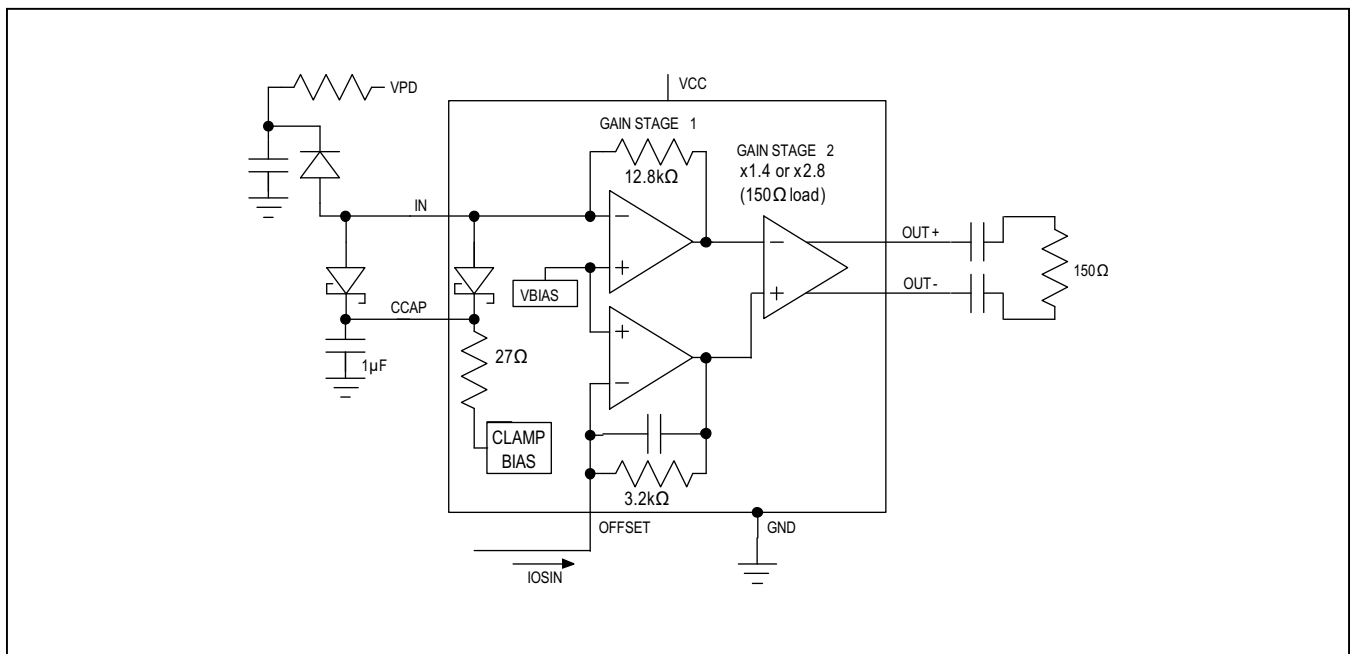
Refer to Maxim [Application Note 639](#) and [Application Note 651](#) for more details.

Typical Application Circuits

DC-Coupled APD Receiver TIA Using 100mA Internal Clamp



DC-Coupled APD Receiver TIA Using External Schottky Clamp For Higher Input Current Handling



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING	TRANSIMPEDANCE
MAX40658ETA+	-40°C to +85°C	8-TDFN	BSE	18.3kΩ
MAX40659ETA+**	-40°C to +85°C	8-TDFN	BSF	36.6kΩ
MAX40658E/D**	-	Dice*	—	18.3kΩ
MAX40659E/D**	-	Dice*	—	36.6kΩ

*Dice are designed to operate over a -40°C to +100°C junction temperature (T_J) range, but are tested and guaranteed at $T_A = +25^\circ\text{C}$.

+Denotes a lead(Pb)-free/RoHS-compliant package

T Denotes tape-and-reel.

**Future product—Contact Maxim for availability.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	6/18	Added ESD warning and added <i>ESD Protection</i> section	2, 8

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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