

Absolute Maximum Ratings

V_{CC} to GND -0.3V to +6.0V
 RF Signals: LO+, LO-, OSCIN +10dBm
 I+ to I-, Q+ to Q- 2V
 LO+, LO-, I+, I-, Q+, Q-, BUFEN, TXEN, CLK, DATA,
 \overline{EN} , SYNEN, OSCIN, OSCOUT, BUFOUT, CHP,
 \overline{SHDN} , LOCK, V_{CC_CP} to GND -0.3V to ($V_{CC} + 0.3V$)
 Digital Input Current $\pm 10mA$
 Short-Circuit Duration RFOUT, BUFOUT, OSCOUT,
 Lock, CHP 10s

Continuous Power Dissipation
 28-Pin TQFN ($T_A = +70^\circ C$) 2W
 (derate 28.5mW/ $^\circ C$ above $+70^\circ C$)
 Operating Temperature Range $-40^\circ C$ to $+85^\circ C$
 Junction Temperature Range $+150^\circ C$
 Storage Temperature $-65^\circ C$ to $+150^\circ C$
 Lead Temperature (soldering 10s) $+300^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



CAUTION! ESD SENSITIVE DEVICE

DC Electrical Characteristics

(MAX2150 EV kit. $V_{CC} = +2.7V$ to $+3.6V$, GND = 0V, $\overline{SHDN} = \overline{PLEN} = TXEN = \text{high}$, BUFEN = low. No AC input signals. RFOUT and BUFOUT output ports are terminated in 50 Ω . $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $V_{CC} = +3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
Supply Voltage		2.7	3	3.6	V
Supply Current	TX mode, $\overline{\text{SHDN}}$ = $\overline{\text{PLEN}}$ = TXEN = high BUFEN = low		72	107	mA
	SYNTH mode, $\overline{\text{SHDN}}$ = $\overline{\text{PLEN}}$ = high, TXEN = BUFEN = low		25	38	
	MOD mode, $\overline{\text{SHDN}}$ = TXEN = high, SYNEN = BUFEN = low		46	69	
LO Buffer Supply Current	Additional current in all modes for BUFEN = high		3.3	5.5	mA
Shutdown Supply Current	HW_SHDN mode, $\overline{\text{SHDN}}$ = low		0.3	600	μA
	SW_SHDN mode, $\overline{\text{PWDN}}$ bit at logic low		35	600	
CONTROL INPUT/OUTPUTS ($\overline{\text{SHDN}}$, TXEN, SYNEN, BUFEN)					
Input Logic High		2			V
Input Logic Low				0.5	V
Input Logic High Current				1	μA
Input Logic Low Current		-1			μA
Lock Detect High (Locked)		2			V
Lock Detect Low (Unlocked)				0.5	V
Power-Up Time	MOD mode		25		μs
Power-Down Time	MOD mode		1		μs
3-WIRE CONTROL INPUT (CLK, DATA, $\overline{\text{EN}}$)					
Input Logic High		$V_{\text{CC}} - 0.5$			V
Input Logic Low				0.5	V
Input Logic High Current				1	μA
Input Logic Low Current		-1			μA

AC Electrical Characteristics

(MAX2150 EV kit. $V_{CC} = +2.7V$ to $+3.6V$, $\overline{SHDN} = \overline{PLEN} = TXEN = \text{high}$, $BUFEN = \text{low}$. Input I/Q signals: $F_{I/Q} = 500kHz$, $V_{I/Q} = 1V_{P-P}$. I+, Q+ single-ended input, driven from AC-coupled source. I-, Q- single-ended inputs are AC-coupled to GND. RFOUT and BUFOUT output ports are terminated in 50Ω loads. $f_{LO} = 1750MHz$, $P_{LO} = -10dBm$, typical values are at $V_{CC} = +3V$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MODULATION INPUT					
I/Q Input Bandwidth	BW (-1dB)		26		MHz
	BW (-3dB)		75		
I/Q Differential Input Level	Assumes a sine-wave input to achieve the RFOUT output power specified below		1		V_{P-P}
I/Q DC Input Resistance			200		k Ω
I/Q Common-Mode Input Range	(Note 2)	1.5	1.6	1.7	V
RF OUTPUT					
Frequency Range		700		2300	MHz
Output Power	$TXEN = \text{high}$, $f_{RF} = 1750MHz$	-7	-1		dBm
	$TXEN = \text{low}$, $f_{RF} = 1750MHz$		-60		
Output 1dB Compression Point			1		dBm
Output IP3			14		dBm
Carrier Suppression	$f_{RF} = 1750MHz$		34		dBc
Sideband Suppression	$f_{LO} - f_{I/Q}$, $f_{RF} = 1750MHz$	25	34		dBc
RF Output Noise Floor	$f_{OFFSET} > 40MHz$ (Note 2)		-148	-143	dBm/Hz
Output Return Loss	(Note 3)		-9		dB
LO INPUT/OUTPUT					
Frequency Range		700		2300	MHz
LO Input Power	(Note 2)	-12	-10	-7	dBm
LO Input Return Loss	$f_{LO} = 1750MHz$		-15		dB
LO Buffer Output Level	$BUFEN = \text{high}$ (Note 2)	-14	-9.5		dBm
SIGMA-DELTA FRACTIONAL-N SYNTHESIZER					
SYSTEM REQUIREMENTS					
Frequency Range	(Note 2)	700		2300	MHz
Phase-Detector Input-Referred Phase Noise Floor	$f_{COMP} = f_{REF} = 20MHz$, $CP0 = CP1 = CPX = 1$ (Note 4)		-138		dBc/Hz
In-Loop Spurious Emissions	$f_{LO} = 1740.005MHz$, $f_{COMP} = f_{REF} = 20MHz$, $CP0 = CP1 = CPX = 1$ (Note 5)		-40		dBc
MAIN DIVIDER AND PHASE DETECTOR					
Minimum Fractional-N Step Size		$f_{COMP}/2^{28}$			
Phase-Detector Comparison Frequency			20	30	MHz
Maximum N Division			251		
Minimum N Division			35		

AC Electrical Characteristics (continued)

(MAX2150 EV kit. $V_{CC} = +2.7V$ to $+3.6V$, $\overline{SHDN} = \overline{PLEN} = \overline{TXEN} = \text{high}$, $\overline{BUFEN} = \text{low}$. Input I/Q signals: $F_{I/Q} = 500\text{kHz}$, $V_{I/Q} = 1V_{P-P}$. I+, Q+ single-ended input, driven from AC-coupled source. I-, Q- single-ended inputs are AC-coupled to GND. RFOUT and BUFOUT output ports are terminated in 50Ω loads. $f_{LO} = 1750\text{MHz}$, $P_{LO} = -10\text{dBm}$, typical values are at $V_{CC} = +3V$, $T_A = +25^\circ\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE OSCILLATOR AND DIVIDER						
Input Frequency Range			10		50	MHz
AC-Coupled Input Sensitivity	AC-coupled, single ended (Note 2)		0.4		2.3	V _{P-P}
Reference Division Ratio	(Notes 2, 6)		1		4	
CHARGE-PUMP OUTPUT						
Charge-Pump Current (Note 7)	CP1, CP0 = 00	CPX = 0	0.12	0.17	0.22	mA
		CPX = 1	0.23	0.34	0.44	
	CP1, CP0 = 01	CPX = 0	0.23	0.35	0.46	
		CPX = 1	0.47	0.67	0.88	
	CP1, CP0 = 10	CPX = 0	0.36	0.52	0.68	
		CPX = 1	0.70	1.00	1.30	
	CP1, CP0 = 11	CPX = 0	0.48	0.69	0.90	
		CPX = 1	0.91	1.31	1.70	
Charge-Pump Voltage Compliance	Sink/source currents match within ±5%		0.5		V _{CC} - 0.5	V

Note 1: Parameters are guaranteed by production testing at $+25^\circ\text{C}$ and $+85^\circ\text{C}$. Minimum and maximum values over the temperature and supply voltage range are guaranteed by design and characterization.

Note 2: Guaranteed by design and characterization.

Note 3: Measured with MAX2150 EV kit.

Note 4: Measured with an on-chip crystal oscillator.

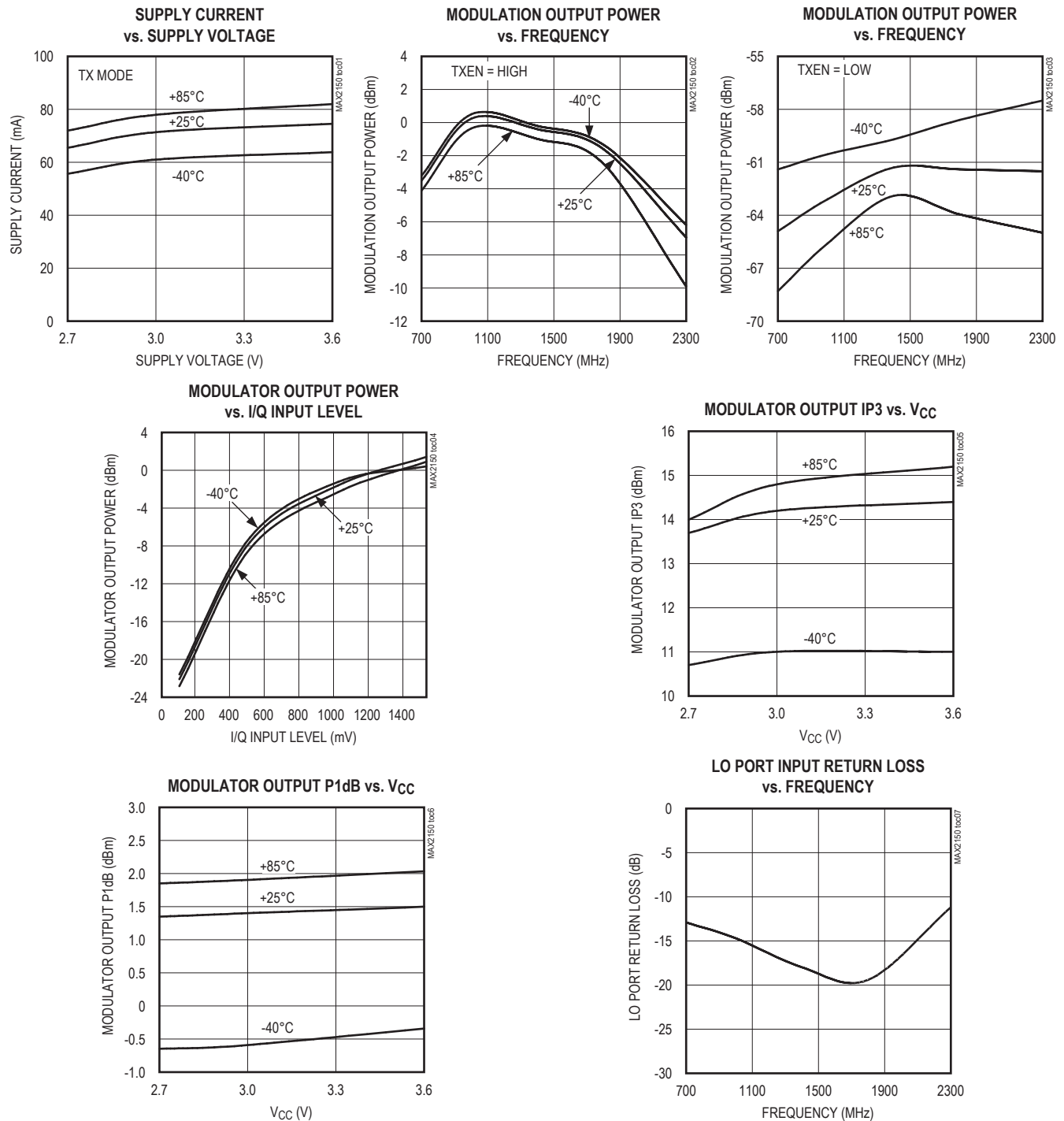
Note 5: In-loop spurious emissions occur when synthesizing a frequency at an integer multiple of the comparison frequency with fractional offset within the PLL loop BW.

Note 6: If an on-chip oscillator is used, a fundamental tone crystal is needed.

Note 7: Minimum and maximum values at CPX = 1 are guaranteed by production testing. Values at CPX = 0 are guaranteed by design and characterization.

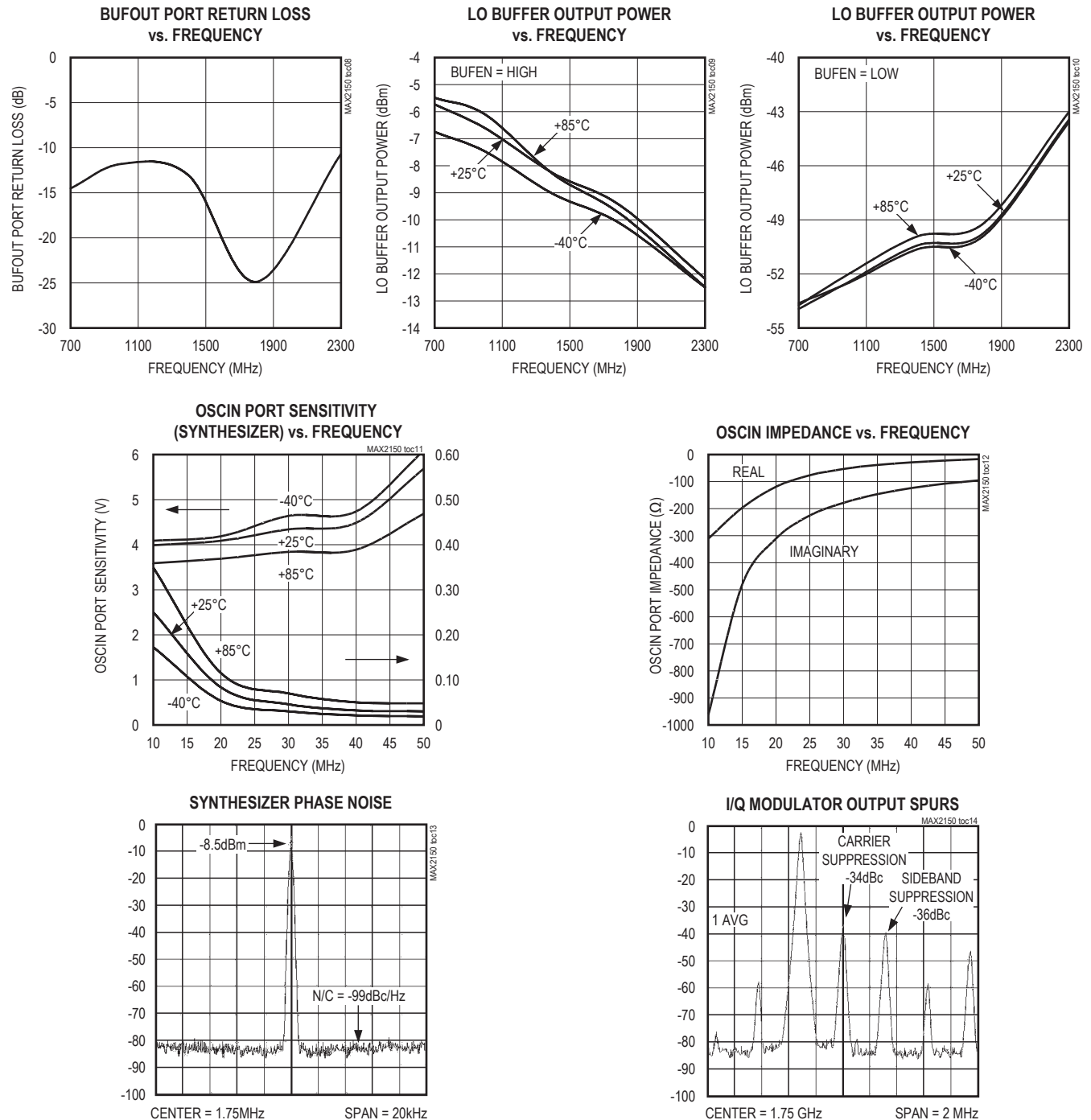
Typical Operating Characteristics

(MAX2150 EV kit. $V_{CC} = +3V$, $\overline{SHDN} = \overline{PLEN} = TXEN = \text{high}$, $BUFEN = \text{low}$. Input I/Q signals: $F_{I/Q} = 500\text{kHz}$, $V_{I/Q} = 1V_{P-P}$. I+, Q+ single-ended input, driven from AC-coupled source. I-, Q- single-ended inputs are AC-coupled to GND. RFOUT and BUFOUT output ports are terminated in 50Ω loads. $f_{LO} = 1750\text{MHz}$, $P_{LO} = -10\text{dBm}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Typical Operating Characteristics (continued)

(MAX2150 EV kit. $V_{CC} = +3V$, $\overline{SHDN} = \overline{PLEN} = TXEN = \text{high}$, $BUFEN = \text{low}$. Input I/Q signals: $F_{I/Q} = 500\text{kHz}$, $V_{I/Q} = 1V_{P-P}$. I+, Q+ single-ended input, driven from AC-coupled source. I-, Q- single-ended inputs are AC-coupled to GND. RFOUT and BUFOUT output ports are terminated in 50Ω loads. $f_{LO} = 1750\text{MHz}$, $P_{LO} = -10\text{dBm}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	TXEN	Modulator Enable Input. Set TXEN low to inhibit the RF and modulator circuits. This mode can be used for quiet frequency synthesis.
2	VCC_PA	Supply Voltage Input for RFOUT Output Driver Circuits. Bypass as close to the pin as possible. The bypass capacitor should not share ground vias with other branches.
3	RFOUT	Modulator RF Output. This is a wideband, internally matched 50Ω output. A DC-blocking capacitor is required.
4, 5	N.C.	Do Not Connect. (These pins must be left floating.)
6	LOCK	Lock Status of the PLL. A static logic-level high indicates that the PLL is in the locked condition.
7	VCC_SD	Supply Voltage Input for Sigma-Delta Modulator Circuits. Bypass as close to the pin as possible. The bypass capacitor should not share ground vias with other branches.
8, 9, 10	CLK, DATA, EN	Input Pins from 3-Wire Serial Bus. An RC lowpass filter on each of these pins can be used to reduce digital noise.
11	$\overline{\text{SHDN}}$	Shutdown Control. Set $\overline{\text{SHDN}}$ low to disable all internal circuits for lowest power consumption. An RC lowpass filter can be used to reduce digital noise.
12	SYNEN	Synthesizer Enable Input. Set SYNTH low to disable the internal frequency synthesizer. An RC lowpass filter can be used to reduce digital noise.
13	OSCIN	Reference Oscillator Input. Connect a parallel, resonant, fundamental-tone crystal between this pin and ground to facilitate a crystal oscillator circuit. For applications with an external reference oscillator, the OSCIN input can be driven through a large-value series capacitor.
14	VCC_XTAL	Supply Voltage Input for Crystal Oscillator. Bypass as close to the pin as possible. The bypass capacitor should not share ground vias with other branches.
15	VCC_CHP	Supply Voltage Input for Charge Pump. Bypass as close to the pin as possible. The bypass capacitor should not share ground vias with other branches.
16	CHP	High-Impedance Charge-Pump Output. Connect to the tune input of the VCO through the PLL loop filter. Keep the line from this pin to the tune input as short as possible to prevent spurious pickup, and connect the loop filter as close to the tune input as possible.
17	VCC_A	Supply Voltage Input for PLL. Bypass as close to the pin as possible. The bypass capacitor should not share ground vias with other branches.
18	VCC_D	Supply Voltage Input for PLL. Bypass as close to the pin as possible. The bypass capacitor should not share ground vias with other branches.
19	VCC_LO	Supply Voltage Input for Internal LO Circuits. Bypass as close to the pin as possible. The bypass capacitor should not share ground vias with other branches.
20, 21	LO-, LO+	Differential Local-Oscillator Input. These inputs require DC-blocking capacitors. The LO can be applied with a single-ended input to the LO+/LO- pin. In this mode, the other pin should be AC-grounded.
22	BUFOUT	Buffered LO Output. Internally matched to 50Ω, requires a DC-blocking capacitor.
23	BUFEN	LO Output Buffer Amplifier Enable. Set BUFEN high to enable the on-chip output LO buffer for driving external circuits. An RC lowpass filter can be used to reduce digital noise.
24, 25	Q-, Q+	Differential Q-Channel Baseband Inputs to the Modulator. These pins connect directly to the bases of a differential pair and require an external common-mode bias voltage of 1.6V.

Pin Description (continued)

PIN	NAME	FUNCTION
26, 27	I-, I+	Differential I-Channel Baseband Inputs to the Modulator. These pins connect directly to the bases of a differential pair and require an external common-mode bias voltage of 1.6V.
28	VCC_RF	Supply Voltage Input for RF Circuits. Bypass as close to pin as possible. The bypass capacitor should not share ground vias with other branches.
—	Exposed pad	Ground

Detailed Description

Internally, the MAX2150 includes a broadband I/Q modulator, internally matched broadband output driver amplifier, fine-resolution fractional-N frequency synthesizer, an LO buffer amplifier, and an on-chip low-noise crystal oscillator circuit.

A simple 3-wire interface is provided for synthesizer programming and device configuration and control. Independent hardware and software power-down control of the I/Q modulator, frequency synthesizer, and LO buffer amplifier is provided, as well as the ability to shut down the entire chip.

I/Q Modulator

The MAX2150 modulator is composed of a pair of matched double-balanced mixers, a broadband passive LO quadrature generator, and a summing amplifier. The mixers accept differential I/Q baseband signals that directly modulate the internal 0° and 90° LO signals applied to the I/Q mixers. An external LO source drives an internal LO quadrature generator that shifts the phase of the LO signal applied to the Q mixer by 90° relative to the LO signal applied to the I-channel mixer. The modulated output of the I/Q mixers is summed together, and the undesired sideband is suppressed.

The I+, I-, Q+, and Q- input ports feature high-linearity buffer amplifiers with a typical -3dB bandwidth of 75MHz and accept differential input voltages up to 1V_{P-P}. The ports require external biasing and have an input common-mode requirement of 1.6V. For single-ended operation, bypass the I and Q ports to ground. See the *Typical Application Circuit* for recommended component values.

The broadband output driver amplifier is matched on chip across the entire operating frequency range and requires an output DC-blocking capacitor. For optimum performance, the output match can be improved with simple L-section and/or PI-section matching networks. Always ensure that DC blocking is provided, because internal bias voltages are present at this output.

The modulator can be shut down with both hardware (pin 1) and software (TE bit). This mode is useful for quiet synthesizer programming or to mute the RF output signal. The hardware pin and software bits must be set to logic-1 to enable the modulator. If the hardware pin or software bit is set to logic-0, or if both are set to logic-0, the modulator is disabled.

LO Buffer Amplifier

The broadband buffer amplifier output is internally matched and requires a DC-blocking capacitor to isolate on-chip bias voltages. Power-down of the LO buffer can be controlled by both BUFEN (pin 23), as well as BUFEN by software by setting the BUFEN (BE) bit through the 3-wire interface. The hardware pin and the software bit must be a logic-1 to enable the buffer. If the hardware or software bit is set to logic-0, the LO buffer is disabled.

Frequency Synthesizer

The MAX2150 features an internal 28-bit sigma-delta frequency synthesizer. This architecture enables the use of very high (30MHz) comparison frequencies, which significantly reduces the in-loop phase noise as a result of reduced division ratios. The high comparison frequency also allows significantly increased PLL bandwidths for very fast switching speed applications.

Divider Programming

The MAX2150 frequency programming is determined as follows. The overall division ratio (D) has an integer value (N), as well as a fractional component (F):

$$D = N.F = N + F / 2^{28}$$

The N and F values are encoded as straight binary numbers. Determination of these values is illustrated by the following example:

$$F_{LO} = 1721.125\text{MHz}, F_{COMP} = 20\text{MHz}$$

Then:

$$D = 1721.125 / 20 = 86.05625$$

Therefore:

$$N = 86 \text{ and } F = 0.05625 \times 2^{28} = 15,099,494$$

Converting each to binary representation results in the following:

N register = 86 = 0101,0110

F register value =
0000,1110,0110,0110,0110,0110

The F-register value is then split between an upper 14 bits and a lower 14 bits as follows:

Upper 14 bits + address 00 = 0000,1110,0110,0100

Lower 14 bits + address 01 = 1001,1001,1001,1001

Synthesizer Shutdown

The synthesizer can be disabled by setting SYNEN (pin 12) to a logic low. This mode is useful when an external frequency synthesizer is employed.

Applications Information

Serial Interface and Register Definition

3-Wire Interface and Registers

The MAX2150 is programmed through a simple 3-wire (CLK, DATA, $\overline{\text{EN}}$) interface. The programming data is contained within 16-bit words loaded into four unique address locations. Each location contains programming information for setting operational modes and device configuration. Two words (address 00, 01) control the fractional divide number in the sigma-delta synthesizer. The third word (address 10) sets the integer divide value, reference divide value, charge-pump current, and charge-pump compensation DAC settings. The fourth and final word (address 11) contains various device configuration registers and test registers, as well as additional charge-pump compensation registers. See Tables 1 through 11 for details.

3-Wire Interface Timing Diagram

Figure 1 shows the programming logic. The 16-bit shift register is programmed by clocking in data at the rising edge of CLK. Pulling enable low allows data to be clocked

into the shift register; pulling enable high loads the register addressed.

Fractional Spurs

When synthesizing a frequency that is an integer multiple of the reference divider and having a fractional offset with a value less than the PLL filter bandwidth, fractional spurs can be observed at a typical level of -40dBc. For example, to synthesize 1640.005MHz when using a 20MHz reference and a PLL bandwidth of 25kHz, spurious products offset from the LO by 5kHz can be observed. The 1640MHz is an integer multiple of 20MHz, and the fractional offset of 5kHz is within the PLL bandwidth.

It is possible to avoid the above-mentioned spurious products by using two reference oscillators with slightly offset frequencies or by using a higher reference frequency and changing the comparison frequency of the reference divider.

Crystal Oscillator

The MAX2150 includes a simple-to-use on-chip low-noise reference oscillator circuit. The oscillator is formed by connecting a fundamental mode parallel resonant crystal from OSCIN to ground. The oscillator circuit is useful from 10MHz to 50MHz.

The phase noise of the MAX2150 can be improved by using a precision high-frequency external reference oscillator (TCXO). The external oscillator is connected through a DC-blocking capacitor directly to the OSCIN pin.

Layout Considerations

A properly designed PC board is an essential part of any RF circuit. A ground plane is essential. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. The exposed pad on the underside of the MAX2150 must be adequately grounded by ensuring that the exposed paddle of the device package is soldered evenly to the board ground plane. Use multiple, low-inductance vias to ground the exposed paddle.

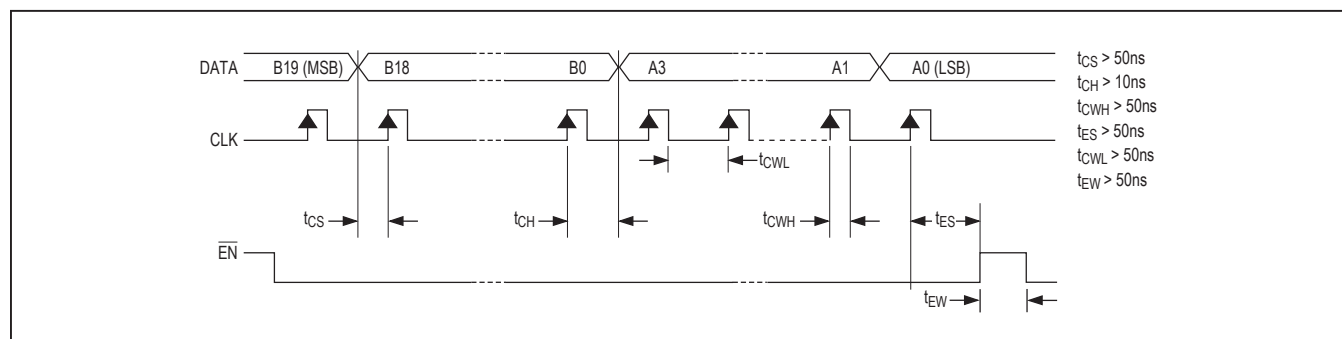


Figure 1. 3-Wire Interface Timing Diagram

Table 1. Register Tables

MSB		SHIFT REGISTER DATA												LSB	ADDRESS	
Upper (MSBs) Fractional Divider Value (F) 14 Bits (Default = 8192, 10000000000000)														Address		
27	26	25	24	23	22	21	20	19	18	17	16	15	14	0	0	
Lower (LSBs) Fractional Divider Value (F)14 Bits (Default 0 DEC, 00000000000000)														Address		
13	12	11	10	9	8	7	6	5	4	3	2	1	0	0	1	
R Divider Default = 00		CP Bleed Default = 00		CP Current Default = 11		Integer Divide Value (N) 8 Bits Defvault = 177 DEC								Address		
R1	R0	LIN1	LIN0	CP1	CP0	7	6	5	4	3	2	1	0	1	0	
Reset Delay Default = 00		Test Registers 6 Bits Default = 0 DEC						Control Register 6 Bits Default = 15 DEC						Address		
BL1	BL0	T5	T4	T3	T2	T1	T0	INT	PD	TE	BE	XX	CPX	1	1	

Table 2. Reference Divider

R1	R0	REFERENCE DIVIDE VALUE
0	0	1
0	1	2
1	0	3
1	1	4

Table 3. Integer Divider-N*

N7	N6	N5	N4	N3	N2	N1	N0	INTEGER DIVIDE VALUE
0	0	1	0	0	0	1	1	35
0	0	1	0	0	1	0	0	36
—	—	—	—	—	—	—	—	—
1	1	1	1	1	0	1	0	250
1	1	1	1	1	0	1	1	251

*N divider is limited to $35 < N < 251$.

Table 4. Fractional Divider-F (Upper 14 Bits)

F27	F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
—	—	—	—	—	—	—	—	—	—	—	—	—	—
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 5. Fractional Divider-F (Lower 14 Bits)

F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0	INTEGER DIVIDE VALUE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	2
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
1	1	1	1	1	1	1	1	1	1	1	1	1	0	268435454
1	1	1	1	1	1	1	1	1	1	1	1	1	1	268435455

Table 6. Control Register

BIT ID	BIT NAME	PWR-UP STATE	BIT LOCATION 0 = LSB	FUNCTION
CPX	CP_MULT	1	0	A logic high doubles the charge pump current selected through registers CP1 and CP0. Logic low sets the charge-pump current to the value selected by registers CP1 and CP0.
XX	XX	XX	1	Unused.
BE	BUFEN	1	2	High enables the VCO buffer. Low disables this output.
TE	TXEN	1	3	Low enables SW_MUTE mode, which shuts down the RF circuits while leaving the 3-wire interface, register, and PLL circuits active.
PD	PWDN	0	4	Low enables register-based shutdown. This mode shuts down all circuits except the 3-wire interface and internal registers.
INT	INT_MODE	0	5	Logic high disables the sigma-delta modulator. Logic low enables the sigma-delta modulator for normal operation.

Table 7. Device Modes

MODE	HW PINS				SOFTWARE CONTROL BITS			DESCRIPTION
	SHDN	TXEN	SYNEN	BUFEN	PWDN	TXEN	BUFEN	
TX	H	H	H	H/L	H	H	H/L	All circuits active.
MOD	H	H	L	H/L	H	H	H/L	Modulator circuits active. Synthesizer blocks disabled. Mode is used with external PLL circuit.
SYNTH	H	L	H	H/L	H	X	H/L	Serial interface and synthesizer blocks active. RF and modulator blocks disabled. Mode is used to gate RF ON/OFF with external logic control.
SW_MUTE	H	H	H	H/L	H	L	H/L	Serial interface and synthesizer blocks all active. Modulator blocks disabled. Mode is used to gate RF ON/OFF with software control.
HW_SHDN	L	X	X	X	X	X	X	All circuits disabled. Lowest current mode of operation.
SW_SHDN	H	X	X	X	L	X	X	Serial interface and registers active, all other circuits inactive regardless of the state of the HW pins with the exception of HW_SHDN.

Power-Supply (V_{CC}) Bypassing

Proper voltage-supply bypassing is essential to reduce the spurious emissions mentioned above. It is recommended that each V_{CC} pin be bypassed independently

and share no common vias with any other ground connection. See the *Typical Operating Circuit* for suggested bypass component values.

Table 8. TXEN Pin and Software Bit Definitions

TXEN		TX MODE
PIN	BIT	
0	0	TX off
0	1	TX off
1	0	TX off
1	1	TX enabled

Table 9. Charge-Pump Registers

CPX	CP1	CP0	I _{CP} (μA)
0	0	0	170
0	0	1	350
0	1	0	520
0	1	1	690
1	0	0	340
1	0	1	670
1	1	0	1000
1	1	1	1310

**Table 10. Test Register Definition
(Default 0 Dec)***

TEST MODE	T5	T4	T3	T2	T1	T0	TEST PIN
Normal Operating Mode	0	0	0	0	0	0	—
Charge Pump Forced to Source I _{cp}	0	0	0	0	0	1	CP
Charge Pump Forced to Sink I _{cp}	0	0	0	0	1	0	CP
Reference Divider Output	0	1	0	0	0	0	Lock
Main Divider Output	0	1	1	0	0	0	Lock

*All other logic states are undefined.

Table 11. BUFEN Pin and Software Bit Definitions

BUFEN		BUF MODE
PIN	BIT	
0	0	Buffer off
0	1	Buffer off
1	0	Buffer off
1	1	Buffer on

Chip Information

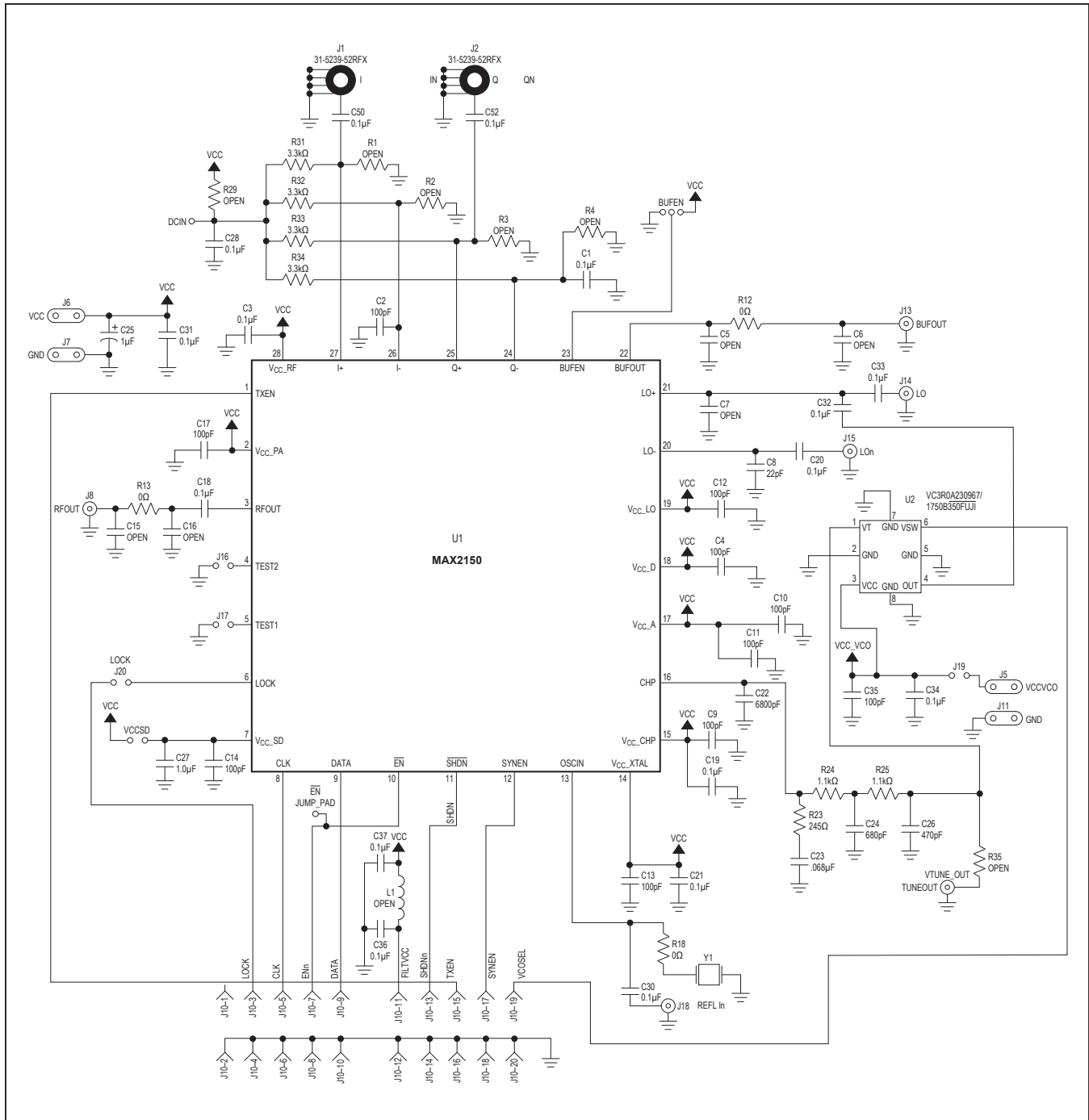
TRANSISTOR COUNT: 16,321

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2855-3	21-0140

Typical Operating Circuit



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	6/08	Updated table in <i>Package Information</i>	13
5	6/21	Updated <i>Typical Operating Characteristics</i>	5, 6

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